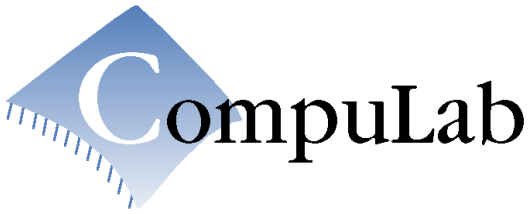


# EM-X270
# Embedded Mobile Device

# Reference Guide

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# 1. Revision Notes

| Date | Description |
|---|---|
| 01-Sep-2007 | ▪ First release |
| 26-Nov-2007 | ▪ Updated weight data (p. 7)<br>▪ Added battery charger and power modes description (section 3.10)<br>▪ Updated sleep mode power consumption data<br>▪ Fixed battery connector (P4) pin-out<br>▪ Fixed audio jack (P6) pin-out<br>▪ Added LED functionality for DS1 and DS2 (section 4.13)<br>▪ Updated keypad interface note (section 4.9)<br>▪ Added NOR flash mapping note (section 6) |
| 18-Mar-2008 | ▪ US and Canada GSM bands support note (section 3.5)<br>▪ Corrected WLAN encryption support |
| 25-Jun-2008 | ▪ Added changes for rev1.3<br>▪ Added secondary USB host port (section 4.2)<br>▪ Added USB host port on the extender connector<br>▪ Telit GE864 module replaced with Telit 864 global form factor connector (section 3.5)<br>▪ BGW200 WLAN replaced with W2SW0001 WLAN module (section 3.6)<br>▪ Touch-screen signal lines routed to the extender connector<br>▪ Charging indication LED connection changed in order to support depleted battery charging indication. |
| 10-Sep-2008 | ▪ Configuration options updated. |
| 28-Jan-2010 | ▪ Added absolute maximum ratings and operating conditions sections |

Please check for a newer revision of this manual in CompuLab's website - http://www.compulab.co.il, following [Products] >> [Developer] >> [EM-X270] links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

# 2. Overview

## 2.1. Highlights

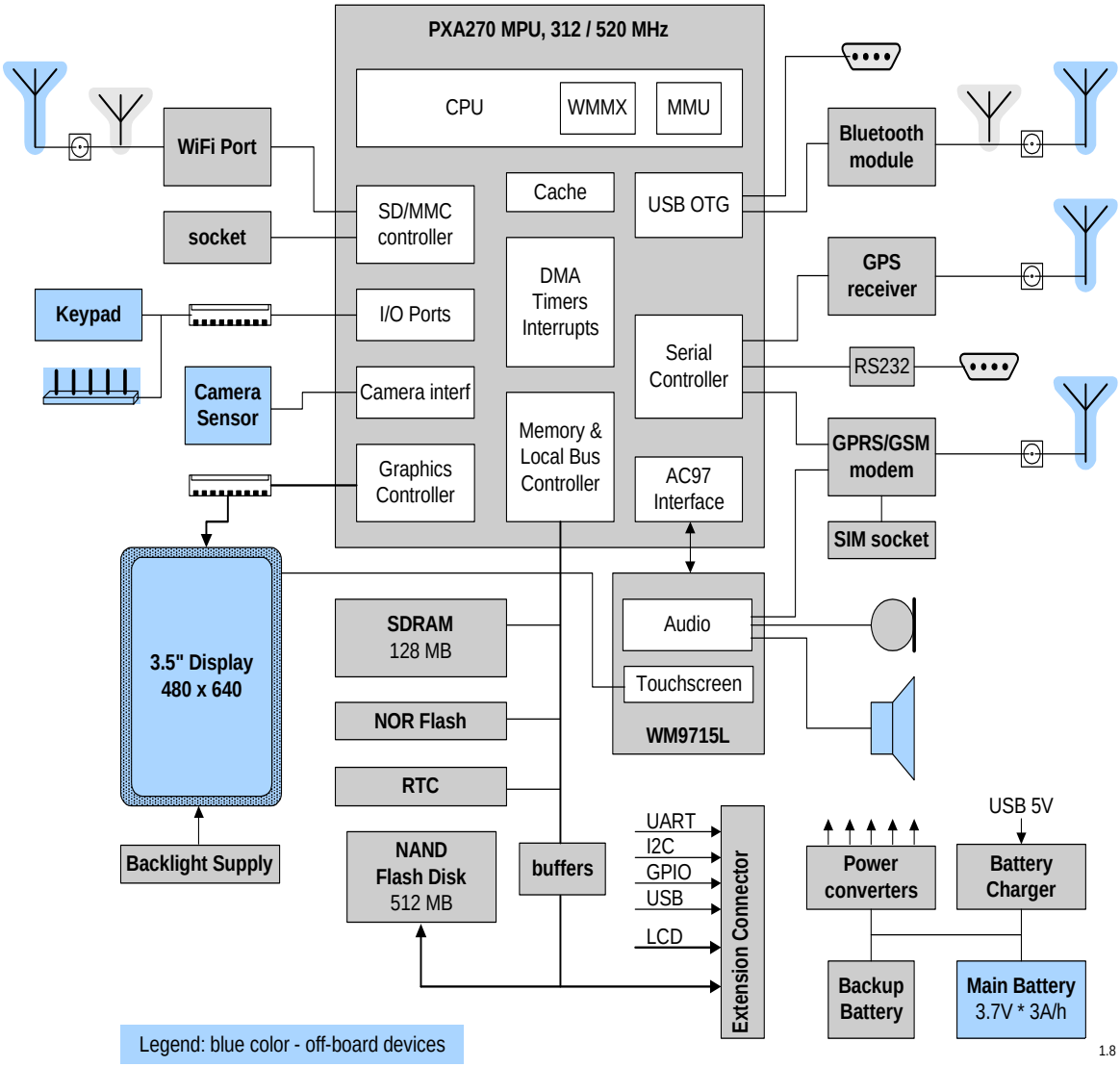
- **Full-featured handheld computer board for embedded applications**
- **Intel's XScale PXA270 CPU, up to 520 MHz, 32+32 KB cache, WMMX**
- **128 Mbyte SDRAM**
- **512 Mbyte Flash Disk**
- **Cellular voice and GPRS modem**
- **Integrated 3.5" 480 x 640 VGA display with touchscreen** (optional)
- **Graphics controller supporting STN and TFT panels with 800x 600 max resolution**
- **WiFi 802.11b interface**
- **Bluetooth interface**
- **GPS receiver, Sirf-III chipset**
- **Expansion connector**
- **Camera Interface**
- **SD / SDIO / MMC socket**
- **Sound codec with integrated speaker and microphone**
- **Slave and host USB port, serial port, GPIO's**
- **Main and backup batteries, and battery charger**
- **Very low standby and active power consumption**
- **Size - 97 x 66 mm**

**EM-X270** is a full-featured computer board, designed specifically for handheld / mobile implementations. Its functional contents are similar to the latest generation of Pocket PC's and smartphones, including all types of wireless, satellite and cellular connectivity found in today's state-off-the-art mobile devices. Yet, it is designed to serve custom implementations, retaining the flexibility expected from an embedded computer board. Available with an optional display, battery with charger and keypad, the EM-X270 offers a self-contained solution requiring just an enclosure for implementing the final custom product.

The feature set of the EM-X270 board combines a 32-bit CPU, SDRAM, Flash Disk and vital computing peripherals. On-board wireless interfaces include WiFi, Bluetooth, GPS and cellular Voice/GPRS modem. The last interface enables the device to act essentially as a customized cellular phone.

EM-X270 has several connectors and slots as used in PDA's and also an internal extension connector for application-specific add-on's. Ready-to-run Windows CE and Linux packages are available from CompuLab.

## 2.2. Block Diagram



## 2.3. Features

"Option" (last) column specifies the configuration code required to have the particular feature. "+" means that the feature is available always.

**CPU, Memory and Busses**

| | | |
|---|---|---|
| CPU | Intel XScale PXA270, 312 / 520 MHz, WMMX<br>32 KB I-cache and 32 KB D-cache, WB, 128 MB address space. DMA and Interrupt controllers, Timers | C |
| RAM | 64 / 128 MB, SDRAM, 100 MHz, 32-bit | D |
| NAND Flash Disk | 128 / 512 Mbytes, more in future. | N |
| External local bus | 32-bit data, 26-bit address, variable rate up to 100 MHz | Y |

**Peripherals**

| | | |
|---|---|---|
| GPRS / GSM module | Telit GC864 module. GSM 850, 900, DCS 1800 or PCS 1900 network communication services. GPRS Class 10, Voice, Circuit Switched Data transfer, Fax, Phone-book and SMS. On-board SIM card socket. Connector for external antenna | K |
| Bluetooth | Bluetooth V2.0+EDR system. CSR BlueCore4-ROM chipset, 2.4GHz band, up to 3Mbps. On-board ceramic chip antenna and connector for external antenna | J |
| WiFi Interface | Implements 802.11b wireless connectivity standard.<br>Wi2Wi W2SW0001 chipset, 11 Mbps, 2.4 GHz band.<br>On-board antenna and connector for external antenna | W |
| GPS | NAVMAN Jupiter32 receiver module, Sirf-III chipset.<br>Supports the NMEA data messages protocol. Connector for external antenna | H |
| Graphics Controller | 4/8/16 bit color, TFT / STN, resolution up to 800 x 600 x 16 | + |
| Camera Interface | Direct camera sensor support, max resolution 2048 x 2048.<br>30 fps @ 320x240, 15 fps @640x480 | + |
| USB | USB Host/Slave port, 12 Mbps, 24-endpoints, OHCI v1.1<br>Additional Host port, 12 Mbps, OHCI v1.0 compliant | + |
| Serial Port (UART) | 16550 compatible, max 921 kbps, RS232, full modem | + |
| General Purpose I/O | Up to 16 dedicated lines. Can also be used as interrupt inputs. Shared with keypad interface | + |
| Audio codec | Wolfson WM9715L, AC97 interface. On-board microphone and speaker connectors, and external audio jack | AT |
| Touchscreen ctrl. | A part of the Wolfson WM9715L chip. Supports resistive | AT |

| | | |
|---|---|---|
| | touch panels | |
| SD / MMC socket | Supports Multimedia Card, Secure Digital and Secure Digital I/O communications protocols. Data-transfer rates up to 19.5 Mbps for MMC and 1-bit SD/SDIO, and up to 78 Mbps for 4-bit SD/SDIO transfers | + |
| RTC | Real Time Clock, uninterrupted power supply | R |

**Electrical, Mechanical and Environmental Specifications**

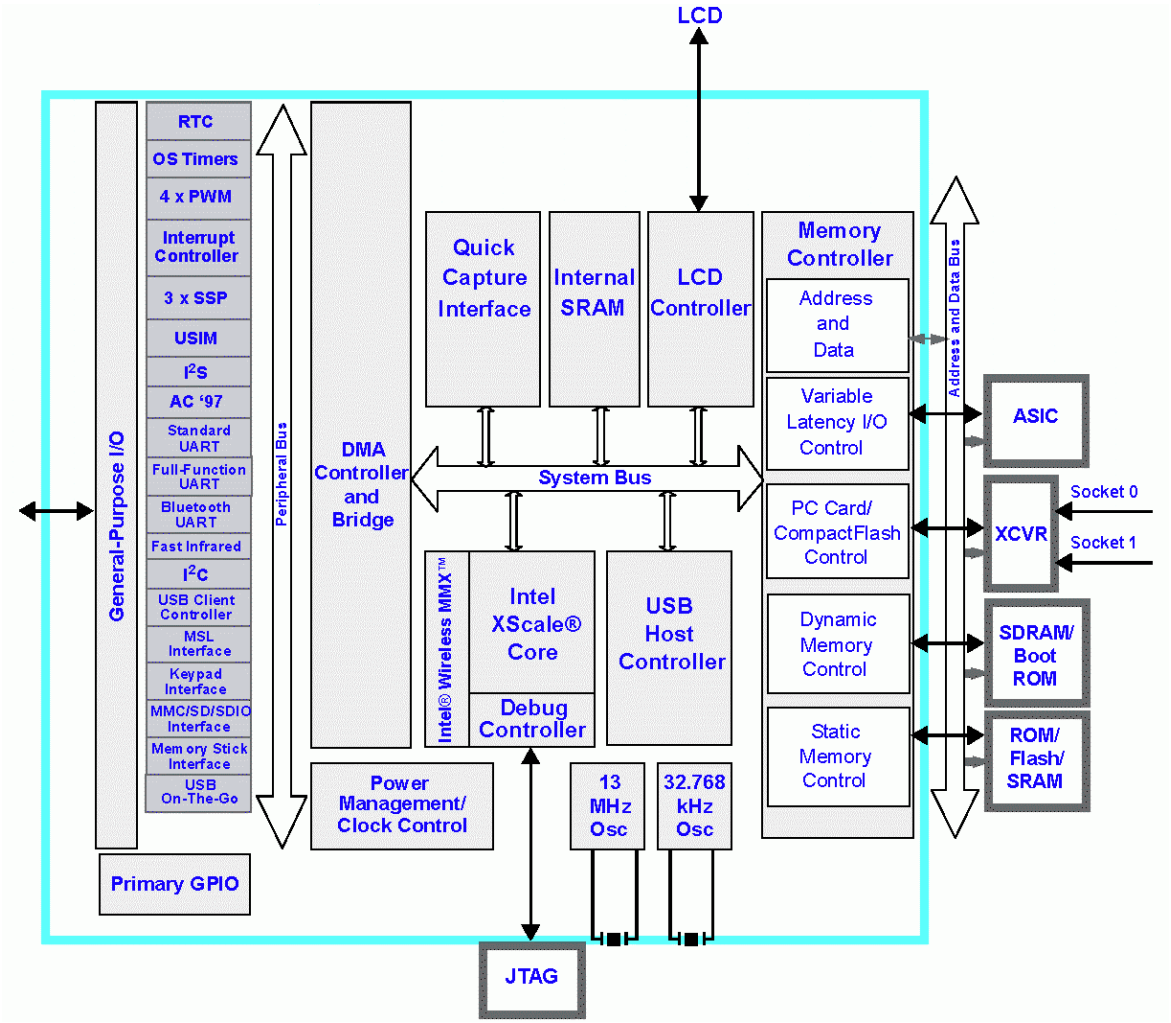
| | |
|---|---|
| Battery charger | Charger for board's lithium polymer battery. The power is supplied from a 5V source via the USB connector. |
| Active consumption | All contents, excluding GPRS: 0.2 - 2 W. GPRS: 1-2 W |
| Sleep consumption | 10 - 50 mW, depending on configuration and mode |
| Dimensions | 97 x 66 mm. Height: board - 6 mm, LCD - 5 mm, battery - 6 mm |
| Weight | Board - 40 gram, LCD - 45 gram, battery - 60 gram |
| MTBF | > 100,000 hours |
| Operation temperature | Commercial: $0^o$ to $70^o$ C<br>Extended: $-20^o$ to $70^o$ C<br>Industrial: $-40^o$ to $85^o$ C<br>* specified for board only, on component case |
| Storage temperature | $-40^o$ to $85^o$ C |
| Relative humidity | 10% to 90% (operation)<br>05% to 95% (storage) |
| Shock | 50G / 20 ms |
| Vibration | 20G / 0 - 600 Hz |

**Off-board Devices**

| | |
|---|---|
| LCD Panel | TPO/Philips TD035STEE1 - 3.5" TFT, 480 x 640 VGA, 16-bit parallel RGB interface, transflective, LED backlight, integrated touch-screen, below 1W consumption |
| Battery | Lithium polymer, 97 x 55 x 6 mm, 10 W/h. Designed for 8-10 hours of continuous operation under normal conditions |
| Keypad | 9 key keypad |

# 3. System Components

## 3.1. PXA270 Processor




**XScale PXA270 Block Diagram**

The PXA270 processor is an integrated system-on-a-chip microprocessor for high-performance, low-power, portable handheld and handset devices. It incorporates Intel's XScale micro-architecture with on-the-fly frequency scaling and sophisticated power management to provide excellent MIPs/mW performance. The PXA270 processor is ARM Architecture Version 5TE instruction set compliant (excluding floating point instructions) and follows the ARM programmer's model.

An integrated LCD display controller provides support for displays up to 800 x 600 pixels, and permits 1-, 2-, 4-, and 8-bit grayscale and 8-, or 16-bit color pixels. A 256 entry/512

byte palette RAM provides flexibility in color mapping.

A set of serial devices and general system resources provide computation and connectivity capabilities for a variety of applications. Intel XScale micro-architecture provides the following features:

- ARM Architecture Version 5TE ISA compliant
  - ARM Thumb Instruction Support
  - ARM DSP Enhanced Instructions
- Low power consumption and high performance
- Media Processing Technology
  - Enhanced 16-bit Multiply
  - 40-bit Accumulator
- 32-KByte Instruction Cache
- 32-KByte Data Cache
- Instruction and Data Memory Management Units
- Branch Target Buffer

The processor integrates XScale micro-architecture with the following peripheral set:

- Clock and Power Controllers
- DMA Controller
- LCD Controller
- Interrupt Controller
- AC97
- Universal Serial Bus (USB) Client
- I2C
- MultiMediaCard
- Synchronous Serial Protocol (SSP) Port
- General Purpose I/O pins
- UART's
- Real-Time Clock
- OS Timers
- USB Host and Slave controller
- Camera Interface

The PXA270 has and integrated coprocessor to accelerate multimedia applications. This coprocessor is characterized by a 64-bit single-instruction multiple-data (SIMD) architecture and compatibility with the integer functionality of the Intel's Wireless MMX™ technology and streaming SIMD extensions (SSE) instruction sets. Key features of this coprocessor include:

- 30 media-processing instructions
- 64-bit architecture up to eight-way SIMD
- 16 x 64-bit register file
- SIMD PSR flags with group-conditional execution support

- SIMD instruction support for sum of absolute differences (SAD) and multiply-accumulate (MAC) operations
- Instruction support for alignment and video operations
- Intel's MMX and SSE integer instruction compatibility
- Superset of existing media-processing instructions in the Intel XScale® core
- PXA270 processor has 256 Kbytes on-chip memory.

## 3.2. Memory

**DRAM**

The EM-X270 board is assembled with 128 Mbytes of Synchronous DRAM. The SDRAM interface is 32-bits wide and runs with a 100 MHz clock.

**NOR Flash**

The EM-X270 is assembled with 1 Mbyte of linear (NOR) Flash ROM. This memory space is used for the boot-loader and system setup data storage. The setup block contains vital production information including boot-loader configuration, PCB revision, manufacturing stamp and MAC addresses for Ethernet and WLAN.

**NAND Flash**

The EM-X270 features 512 Mbytes of NAND Flash.
The NAND Flash is a block device – optimized for block read and write operations rather than for random access. It is used for implementation of a Flash Disk, regarded by the operating system as a regular disk drive.

## 3.3. Graphics System

The EM-X270 graphics system is based on the LCD controller integrated in the PXA270 chip. The LCD controller provides an interface between the PXA270 processor and a flat-panel display module. The flat-panel display module can be either passive (DSTN) or active (TFT), or an LCD panel with internal frame buffering.

The EM-X270 board features an LCD panel connector (P11) that is designed for connecting the TD035STEE1 LCD module. The TD035STEE1 is a 3.5" transflective active matrix color 480x640 TFT LCD module that includes a touch panel, backlight and TFT LCD panel. All the signals necessary for graphics output, touch-screen support and backlight control are routed to the LCD panel connector.

The LCD controller signals are also routed to the expansion connector. The EM-X270 may be integrated with other types of LCD panels either through LCD connector (P11) or through expansion connector. See section 4.5 for details about the LCD connector.

**LCD Controller Features**

The following list describes features supported by the PXA270 processor LCD controller:

- Display modes
  - Support for single- or dual-scan display modules
  - Passive monochrome mode supports up to 256 gray-scale levels (8 bits)
  - Support for up to 16-bit per pixel single-scan color displays without an internal frame buffer
- Support for display sizes from 1x1 to 800 x 600 pixels
- Supports pixel depths of 2, 4, 8 and 16 bits per pixel (bpp) in RGB format
- Supports a hardware cursor for single-scan displays (see Section 7.4.11 in PXA270 manual for cursor modes and sizes)
- Programmable toggle of AC bias pin output (toggled by line count)
- Programmable pixel clock from 52.0 MHz down to 25.4 kHz (104.0 MHz/2 to 13 MHz/512)
- Backward compatible with the Intel's PXA255 graphics controller

## 3.4. Audio System

The audio system of the EM-X270 is implemented with the Wolfson WM9715L codec chip connected to the AC97 port of the PXA270.

**AC'97 Controller Unit Overview**

The AC'97 Controller Unit (ACUNIT) of the PXA270 processor supports AC'97 revision 2.0 features. The ACUNIT also supports the audio controller link (AC-link). The AC-link is a serial interface for transferring digital audio, modem, mic-in, CODEC register control and status information.

The AC'97 CODEC sends the digitized audio samples that the ACUNIT stores in memory. For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the CODEC through the AC-link. The external digital-to-analog converter (DAC) in the CODEC then converts the audio samples to an analog audio waveform.

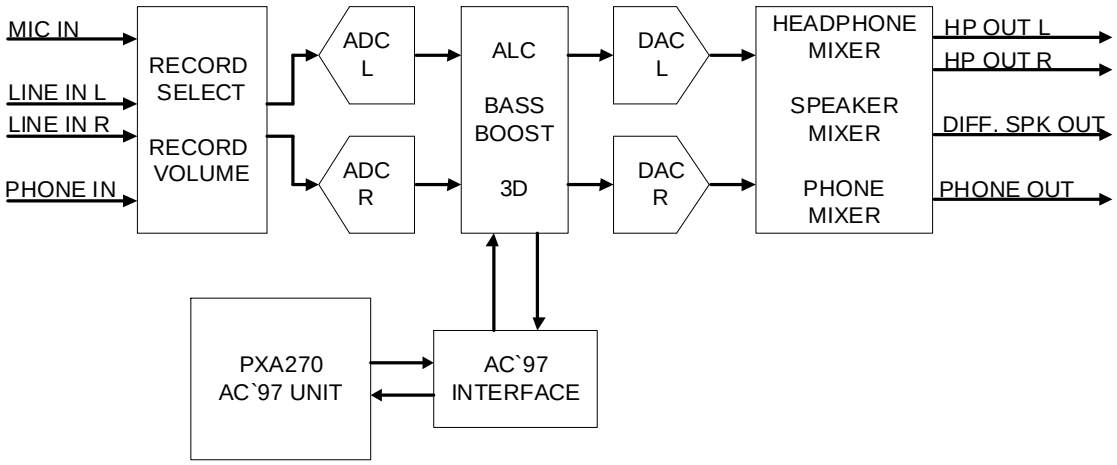
**WM9715L**

The WM9715L is a highly integrated device supporting audio and touchscreen functions. The device can connect directly to a 4-wire touch panel, mono or stereo microphones, stereo headphones and a mono speaker. Additionally, phone input and output pins are provided for seamless integration with wireless communication devices.

The WM9715L contains a universal touch screen interface for a 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. The touch screen interface is connected to the system's LCD panel connector.

**Audio Interconnection**

The following block diagram describes the EM-X270's audio interconnection path.




- The headphone stereo output connects to the on-board audio jack (P6). This output is designed to drive a 16Ω or 32Ω headphone or a line output.
- The audio mic input is directly connected to the on-board ECM microphone.
- The phone output and input are internally connected to the cellular module audio signals.

- The WM9715L audio amplifier differential output is routed to the system speaker connector (P15). This output is designed to differentially drive an 8Ω mono speaker.
- The line-in inputs are routed to the extender board connector (P3).

Each of the audio inputs may be multiplexed to each of the audio outputs or into the AC`97 interface for digital recording. The AC`97 interface output may also be multiplexed into any of the analog audio outputs for digital playback.

Audio multiplexing and gain control is supported through Linux and Win CE packages provided for the EM-X270.

**Audio Specifications**

| PARAMETER | SYMBOL | TYP | UNIT |
|---|---|---|---|
| **Headphone Output** | | | |
| Output Power per Channel | Po | 20 | mW |
| Signal to Noise Ratio | SNR | 95 | dB |
| **Speaker Output with 8Ω bridge tied load** | | | |
| Output Power at 1% TDH | Po | 400 | mW |
| Abs. Max Output Power | Po_max | 500 | mW |
| Signal to Noise Ratio | SNR | 97 | dB |
| **On-board Microphone at F=1kHz, Vs=2.0V,** | | | |
| Sensitivity | | -40 +/-3 | dB |
| S/N Ratio (A) | SNR | 58 | dB |
| Directivity | | Omni Directional | |
| **Line Input** | | | |
| Full Scale Input Signal Level | Vinfs | 1.0 | V rms |
| Input Resistance | Rin | 17 | Kohm |

## 3.5. Cellular Module

NOTE: The following section refers to EM-X270 - revisions 1.3 and higher. For previous revisions of EM-X270 please refer to the shaded section below.

The EM-X270 cellular connectivity feature is based on the Telit 864 series of cellular modules. The cellular module connector (P37) is conformant with the Telit global form factor interface and can accommodate the following modules:

- GC864 – quad-band EGSM 850 / 900 / 1800 / 1900 MHz
- UC864-E – UMTS/HSDPA 2100 MHz, quad-band EGSM 850 / 900 / 1800 / 1900 MHz
- CC864 – dual-band CDMA 800 / 1900 MHz

The cellular module is interfaced to the PXA270 processor via the BT_UART.
The SIM interface is connected to the on-board SIM card socket (see 4.11 for a detailed SIM card socket description).

**Audio Path Connection**

The cellular module audio signals are connected to the EM-X270 audio system, providing the audio functionality of a standard cellular phone. See section 3.4 for more details about the audio path.

**Antenna**

The antenna should fulfill the following requirements:

| | |
|---|---|
| Frequency range | Depending on frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| Bandwidth | 70MHz in GSM850, 80MHz in GSM900, 170 MHz in DCS, 140 MHz in PCS, 250 MHz in WCDMA2100 |
| Gain | > 1.5 dBi |
| Impedance | 50 ohm |
| Input power | > 2 W peak power |
| VSWR absolute max | 10:1 |
| VSWR recommended | < 2:1 |

Please refer to Telit's specific module documentation for more details.
The antenna is connected to a standard UFL connector present on the cellular module.

NOTE: For some modules, the default configuration is set to the European (GSM-900 GSM-1800) band frequencies. Users in the US and Canada need to re-configure the modem to the GSM-850 GSM-1900 bands. Use the "AT#BND=3" command to set the proper band settings. Please see page 300 in the “Telit AT Commands Reference Guide” for detailed info about the band configurations.

**RF Specifications**

Please refer to Telit’s specific module documentation for RF specifications.

**LED Indication**

The on-board LED DS4 shows information regarding network service availability and call status.

| LED status | Cellular module status |
|---|---|
| Permanently off | Cellular module off |
| Fast blinking (period 1s, Ton 0,5s) | Net search / Not registered / turning off |
| Slow blinking (period 3s, Ton 0,3s) | Registered full service |
| Permanently on | A call is active |

NOTE: The following section refers to EM-X270 - revisions 1.2 and older.

The cellular GSM/GPRS connectivity feature is based on the Telit GE864 module.
The GE864 module allows digital communication services wherever a GSM 850, 900, DCS 1800 or PCS 1900 network is present.
The GE864 includes features like GPRS Class 10, Voice, Circuit Switched Data transfer, Fax, Phone book, SMS support and ‘EASY GPRS’ embedded TCP/IP stack.
The module also provides SIM card interface with auto-detection and hot insertion.
The interface supports phase 2 GSM11.14 - SIM 3V.

The GE864 module is interfaced to the PXA270 processor via the BT_UART.
The SIM interface is connected to the on-board SIM card socket (see 4.11 for a detailed SIM card socket description).

**Audio Path Connection**

The GE864 audio signals are connected to the EM-X270 audio system, providing the audio functionality of a standard cellular phone. See section 3.4 for more details about the audio path.

**Antenna**

The antenna should fulfill the following requirements:

| | |
|---|---|
| Frequency range | Depending on frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| Bandwidth | 136 MHz in GSM 850/900, 170 MHz in DCS, 140 MHz PCS |
| Gain | > 1.5 dBi |
| Impedance | 50 ohm |
| Input power | > 2 W peak power |
| VSWR absolute max | 10:1 |
| VSWR recommended | < 2:1 |

The module RF signal is routed to a standard UFL connector for off-board antenna connection. See section 4.12 for a detailed connector description.

NOTE: The modem default configuration is set to the European (GSM-900 GSM-1800) band frequencies. Users in the US and Canada need to re-configure the modem to the GSM-850 GSM-1900 bands. Use the "AT#BND=3" command to set the proper band settings. Please see page 300 in the “Telit AT Commands Reference Guide” for detailed info about the band configurations.

**RF Specifications**

| **Operating Frequency** | | | | |
|---|---|---|---|---|
| Mode | Freq. TX (MHz) | Freq. RX (MHz) | Channels (ARFC) | TX - RX offset |
| E-GSM-850 | 824.2÷848.8 | 869.2÷893.8 | 0 – 124 | 45 MHz |
| E-GSM-900 | 890.0 - 914.8 | 935.0 - 959.8 | 0 – 124 | 45 MHz |
| | 880.2 - 889.8 | 925.2 - 934.8 | 975 - 1023 | 45 MHz |
| DCS-1800 | 1710.2 - 1784.8 | 1805.2 - 1879.8 | 512 – 885 | 95 MHz |
| PCS-1900 | 1850.2 - 1909.8 | 1930.2 - 1989.8 | 512 – 810 | 80 MHz |

| **Output Power** | | |
|---|---|---|
| Mode | Device class | Nominal Peak Power |
| GSM–850/900 | class 4 | +33dBm |
| DCS–1800/PCS–1900 | class 1 | +30dBm |

| **Reference sensitivity** | | |
|---|---|---|
| Mode | Device class | Nominal Peak Power |
| GSM–850/900 | class 4 | -107dBm |
| DCS–1800/PCS–1900 | class 1 | -106dBm |

**LED Indication**

The onboard LED DS4 shows information regarding network service availability and call status.

| LED status | GSM module status |
|---|---|
| Permanently off | GSM module off |
| Fast blinking (period 1s, Ton 0,5s) | Net search / Not registered / turning off |
| Slow blinking (period 3s, Ton 0,3s) | Registered full service |
| Permanently on | A call is active |

## 3.6. WLAN Module

NOTE: The following section refers to EM-X270 - revisions 1.3 and higher. For previous revisions of EM-X270 please refer to the shaded section below.

The EM-X270 incorporates full-featured 802.11 b/g capabilities, implemented with the Wi2Wi W2SW0001 WLAN controller module. The W2SW0001 is a complete IEEE 802.11b/g solution based on the Marvell's 88W8686 chipset.

Security features:

- WEP encryption (64 bit/128 bit)
- WPA TKIP security
- WPA2

The W2SW0001 is connected to the PXA-270 CPU using the SPI #2 interface.

**Antenna Connection**

The EM-X270 features a small on-board ceramic patch antenna dedicated to WLAN connectivity. Alternatively, an external antenna may be connected via the on-board high frequency connector. Any type of 2.45GHz WLAN antenna can be used. See section 4.12 for a detailed connector description.
Note: An external antenna cannot operate together with the on-board patch antenna. In order to use an external WLAN antenna, the on-board antenna must be disconnected.

**RF Specifications**

| **802.11b RF system specifications** | | | |
|---|---|---|---|
| Transmit Power Output | | 15 | dBm |
| Receive Sensitivity | 1 Mbps, 8% PER | -87 | dBm |
| | 2 Mbps, 8% PER | -87 | dBm |
| | 5.5 Mbps, 8% PER | -87 | dBm |
| | 11 Mbps, 8% PER | -85 | dBm |
| Maximum Receive Level | PER < 8% | IEEE Compliant | |
| Transmit Frequency Offset | Low, Middle, High channels | +/-10 | PPM |
| Spectral Mask | Max. TX power | -40@fc+/-11MHz | dBc |
| | | -60@fc+/-22MHz | |
| Error Vector Magnitude | Max. TX power @ 11Mbps | -36 | dB |
| Carrier Suppression | Max. TX power | -25 | dBc |
| Adjacent channel rejection | Desired channel is 3dB above sensitivity, 11Mbps, PER < 8% | 48 | dBc |
| **802.11g RF system specifications** | | | |
| Transmit Power Output | | 15 | dBm |
| Receive Sensitivity | 6 Mbps, 10% PER | -86 | dBm |
| | 9 Mbps, 10% PER | -85 | dBm |
| | 12 Mbps, 10% PER | -85 | dBm |
| | 18 Mbps, 10% PER | -84 | dBm |
| | 24 Mbps, 10% PER | -80 | dBm |
| | 36 Mbps, 10% PER | -77 | dBm |
| | 48 Mbps, 10% PER | -73 | dBm |
| | 54 Mbps, 10% PER | -72 | dBm |
| Maximum Receive Level | PER < 8% | IEEE Compliant | |
| Transmit Frequency Offset | Low, Middle, High channels | +/-10 | PPM |
| Spectral Mask | Max. TX power | -30@fc+/-11MHz | dBc |
| | | -40@fc+/-20MHz | |
| | | -50@fc+/-30MHz | |
| Error Vector Magnitude | Max. TX power @ 54Mbps | -29 | dB |
| Carrier Suppression | Max. TX power | -25 | dBc |
| Adjacent channel rejection | Desired channel is 3dB above sensitivity, 54Mbps, PER < 8% | 15 | dBc |

NOTE: The following section refers to EM-X270 - revisions 1.2 and older.

The EM-X270 incorporates full-featured 802.11b capability implemented using a Phillips BGW200 WLAN controller. The implementation contains a baseband MAC subsystem, RF transceiver and high-power RF front-end, thus incorporating all the components required to provide high-quality WLAN capability.
The BGW200 is based on an internal controller sub-system with dedicated CPU, ROM and RAM. The sub-system executes firmware, responsible for all low-level WLAN networking functionality, thus considerably reducing the load on the main CPU.
The RF interface supports antenna diversity for improved stability. It provides +16dBm transmitter output power - the standard level for 802.11 NIC's.
BGW200 firmware supports both infrastructure (access point managed) and independent (without access point) network topologies. On the other hand, firmware does not support BGW200 acting as an access point.

Security features:

• WEP64
• WEP128

Other firmware features:

• Extended rate protection
• Regulatory domain
• Power save protocol
• Fragmentation & De-fragmentation
• Antenna diversity

Infrastructure/Ad-hoc modes:

• BSS
• IBSS

The BGW200 is connected to the PXA-270 CPU using the SPI #2 interface.

**Antenna Connection**

The EM-X270 features a small on-board ceramic patch antenna dedicated to WLAN connectivity. Alternatively, an external antenna may be connected via the on-board high frequency connector. Any type of 2.45GHz WLAN antenna can be used. See section 4.12 for a detailed connector description.
Note: An external antenna cannot operate together with the on-board patch antenna. In order to use an external WLAN antenna, the on-board antenna must be disconnected.

**NVM Data**

During the EM-X270 manufacturing process, WLAN sub-system configuration and RF calibration data is stored in the NOR flash. RF calibration data allows the BGW200 to provide its best RF performance throughout a wide range of temperatures while still staying compliant with FCC regulations. The WLAN MAC address is also stored in the NOR flash.

**RF Specifications**

| Symbol Parameter | Conditions | Typ. value | Unit |
|---|---|---|---|
| **Receiver sensitivity** | | | |
| 1 Mbps sensitivity | PER < 8%<br>PSDU = 1024 bytes | -91 | dBm |
| 2 Mbps sensitivity | | -87 | dBm |
| 5.5 Mbps sensitivity | | -83 | dBm |
| 11Mbps sensitivity | | -83 | dBm |
| **Maximum input level** | | | |
| Max input level for 2 Mbps | PER < 8%<br>PSDU = 1024 bytes | -0.4 | dBm |
| Max input level for 11 Mbps | | 0.6 | dBm |
| **Linear output power** | | | |
| 1 Mbps and 2 Mbps output power | meets FCC restricted band specifications | 15.5 | dBm |
| 5.5 Mbps and 11 Mbps output power | | 16 | dBm |

* All values at nominal supply voltage, 25°C and channel 6

## 3.7. Bluetooth Module

The EM-X270 Bluetooth system is based on the CSR BlueCore 4-ROM component. The BlueCore 4-ROM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.
With the on-chip CSR Bluetooth software stack, it provides a fully-compliant Bluetooth system to v2.0 of the specification for data and voice communications.

**Features:**

- Fully Compliant Bluetooth v2.0+EDR system
- Enhanced Data Rate (EDR) compliant with v2.0 of specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support

The BlueCore 4-ROM is connected to the PXA270 processor USB host port through the USB hub.

**Antenna Connection**

The EM-X270 features a small on-board ceramic patch antenna dedicated to Bluetooth connectivity. Alternatively, an external antenna may be connected via the on-board UFL high frequency connector. See section 4.12 for a detailed connector description.
Note: The external antenna cannot operate together with the on-board patch antenna. In order to use an external Bluetooth antenna, the on-board antenna must be disabled.

**RF Specification**

| | |
|---|---|
| Standards | IEEE 802.15.1 |
| BlueTooth Class | Class II device |
| Wireless Signal Rates | 2.1Mbps (Bluetooth 2.0) |
| Wireless Transmit Power* | 4dBm |
| Wireless Operating Range* | Up to 10m |
| Receiver Sensitivity* | -84dBm |

* Preliminary data

**LED Indication**

The onboard LED DS5 indicates BlueTooth transceiver activity.

## 3.8. GPS Receiver

The EM-X270 GPS function is implemented with the NAVMAN Jupiter32 module based on the SiRF GSC3f chip-set. The GSC3f chip integrates baseband, RF sections and Flash memory, thereby reducing power consumption and size. Integrated 4 Megabit flash memory gives the user the ability to store configurations permanently.
The protocol supported is NMEA (National Marine Electronics Association) data messages.
The Jupiter32 module is interfaced with the PXA270 processor via the STD_UART.

**Antenna**

The RF input is routed to a standard UFL connector for off-board antenna connection. See section 4.12 for a detailed connector description.
The following table summarizes the recommendations for the EM-X270 GPS antenna:

| Characteristic | Passive Antenna | Active Antenna |
|---|---|---|
| Polarization | Right-hand circular polarized | Right-hand circular polarized |
| Receive frequency L1 | 1.57542 GHz +/- 1.023 MHz | 1.57542 GHz +/- 1.023 MHz |
| Power supply | - | 3V |
| DC current | - | <10mA at 3V |
| Antenna gain | 2 to 5 dBi with 1 dB loss (max) in connections | - |
| Total gain | - | < 18dBi |
| Axial ratio: | < 3 dB | < 3 dB |
| Output VSWR | - | < 2.5 |

The active ceramic patch antenna available from Compulab (part name ANTGPS) meets the requirements above and may be used for evaluation and pilot production.

**Performance Specifications**

The table below shows the corresponding TTFF times for each of the acquisition modes.

| Mode | @ –125 dBm | | @ –140 dBm | |
|---|---|---|---|---|
| | Typ | 90% | Typ | 90% |
| Hot start TTFF | 500 ms | <1 s | <1 s | <1 s |
| Warm start TTFF | 32 s | 38 s | 49 s | 59 s |
| Cold start TTFF | 34 s | 42 s | 52 s | 66 s |
| Re-acquisition (<10s obstruction) | 1 s | | 1 s | |

The position and velocity accuracy are shown in the following table, assuming full accuracy C/A code.

| Parameter | Value |
|---|---|
| Horizontal CEP | 2.2 m |
| Horizontal (2 dRMS) | 5.5 m |
| Vertical VEP | 2.0 m |

## 3.9. RTC

V3020 chip provides RTC functionality on the EM-X270. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year and century information. A time/date programmable polled ALARM is included. The end-of-the-month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either 24hr or 12hr format with an AM/PM indicator.

Setting the time and date of V3020 RTC is supported through Linux and Win CE packages provided for the EM-X270.

**Interface**

The V3020 RTC uses a single line serial I/O interface, implemented using standard R/W operations and an MD[0] local bus data line at physical address 0x10000000 in the PXA-270 CPU memory space.

The RTC chip's power supply is connected both to the main battery and to the onboard back-up coin cell battery. Thus, the RTC data is preserved even when the main battery is detached from EM_X270. See section 3.10 for a more detailed explanation.

## 3.10. Power System and Power Consumption

**EM-X270 Power Management Concepts**

The EM-X270 system is designed as a handheld device, providing minimized power consumption operation, very low power sleep mode, on-line battery replacement capability and long battery life.
The main power supply source is a rechargeable lithium battery. A regulated DC power source of 3.7V – 4V may also be used, but this will require software adaptation.
An on-board rechargeable coin cell battery provides back-up power in standby and off modes.

The DA9030 PMIC manages most of the EM-X270's power system, providing regulated voltages for the PXA270 processor, memories and peripheral devices.
Certain units of the EM-X270 are powered by discrete voltage regulators connected directly to the main battery and controlled by PXA270 GPIO's.
Battery charging and supervision are also managed by the DA9030.

**EM-X270 Batteries**

The EM-X270 system is designed to operate with a rechargeable lithium battery.
The battery pack must include an NTC thermistor for temperature measurement during battery charging.
The EM-X270 power management software was designed to operate with the 10W/h Li-Polymer battery available from Compulab. Custom batteries may also be integrated with the EM-X270, but this will require software adaptation. The following battery chemistries are supported by EM-X270:

- Single-Cell Li-Ion at 4.1V
- Li-Polymer Pack

Please see the "Battery charger control" section in the DA9030 datasheet for more details.

An on-board 14mAh rechargeable coin cell lithium battery is the back-up power supply for RTC timekeeping. This battery is constantly being charged whenever the main battery is present.

### Battery Charging and Supervision

Battery charging is managed by the DA9030 that supports constant current / constant voltage charging, PWM and trickle charge modes, external DC detection, pre-charge, over voltage and current lock out, battery removal and charge watchdog functions.
The charge DC signal is applied to the USB OTG connector. Thus, the battery may be charged from a DC charger device with a mini USB connector or from a standard USB host with a 5V power supply. External charger voltage must be between 4.5V and 5.5V. The charging current is set in the power management software and may vary between 100mA and 1000mA.

During charging, battery temperature, voltage and charge current must be supervised, in order to prevent battery over-heating or overcharge. These measurements are performed with the DA9030 internal ADCs. Please see the “Battery charger control” section in the DA9030 datasheet and the “Power Management” section in the O/S package documentation for more details.

### Power Modes

#### Active Mode

The active mode is entered after a successful start-up or pre-charge mode. During this operating mode the PXA270 processor controls the system power management and is able to respond to any faults that have been detected. Status information is passed to PXA270 via the I2C interface. The DA9030 can flag interrupt requests to the processor via a dedicated interrupt pin.

#### Sleep Mode

The sleep mode may be entered from active mode only. The PXA270 processor is in deep sleep mode and the DA9030 is in sleep mode. All power sources except for SDRAM deep sleep self-refresh and RTC timekeeping power are shut down. The EM-X270 will wake-up when one of the following events is detected: sleep/resume button (SW2) is pressed; an external charger device is connected.

#### Pre-charge Mode

The pre-charge power mode is entered when the EM-X270 is powered up with a heavily discharged battery (voltage below 3.45V) and an external DC charger is connected to the device. The system will enable battery charging and wait until the battery voltage reaches the 3.45V threshold. Only then, the EM-X270 will proceed with the standard boot sequence. If the battery voltage is below 3.45V and there is no charger connected, the system will go into shutdown.

**Absolute Maximum Ratings**

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Input voltage VCC_BAT | -0.3 | | 5.5 | V |

**Operating Conditions**

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Input voltage VCC_BAT | 3.45 | | 4.3 | V |

**Power Consumption**

| | Max Activity | Idle | Sleep | Units |
|---|---|---|---|---|
| EM-X270 basic system with minimum peripherals | 500 | 170 | 5.5 | mA |

**On-board optional functions**

| Peripheral System | Test Condition | Max Consumption | Typical Consumption |
|---|---|---|---|
| WLAN module | Receive mode | 220mA | 210mA |
| | Transmit mode | 240mA | 230mA |
| GSM/GPRS module* | Stand-by (GSM idle) | 8mA | 4mA |
| | Voice channel mode | 200mA | 170mA |
| | GPRS class 10 mode | 500mA | 250mA |
| Audio | Idle mode | TBD | 2mA |
| | Everything on | TBD | 25mA |
| GPS receiver | | 100mA | 30mA |
| Bluetooth | | 40mA | TBD |

* GC864 power consumption only. For other cellular modules, refer to specific module documentation.

**Off-board peripherals**

| Peripheral System | Test Condition | Max Consumption | Typical Consumption |
|---|---|---|---|
| Ethernet on EB-X270 | | TBD | 70mA |
| TD035STEE 1 LCD panel | No backlight | 30mA | 30mA |
| | Backlight at half intensity | 150mA | 150mA |
| | Backlight at full intensity | 260mA | 260mA |

All power consumption tests were performed at 25°C with the Lithium Polymer battery pack at a nominal 3.7V.

# 4. Peripheral Interfaces & Connectors

## 4.1. Main USB Interface (P1)

The EM-X270 main USB interface complies with the USB OTG standard. The PXA270 USB controller is a USB Revision 1.1-compliant, full-speed device that operates half-duplex at a baud rate of 12 Mbps. Refer to chapter 12 of the PXA270 Reference Guide for a more detailed description of the USB controller.

When operating in USB host mode, the EM-X270 power supply system provides 5V/100mA DC (in compliance with USB OTG standard) on the VCC pin of connector P1. When operating in USB slave mode, voltage output is disabled, and the VCC pin of connector P1 is used as an input voltage pin of an external battery charger. Refer to section 3.10 for more details about the USB power system.

Connector P1, mini USB type AB:

| Pin | Signal Name |
|---|---|
| 1 | USV_VCC |
| 2 | USB_N |
| 3 | USB_P |
| 4 | USB_ID |
| 5 | GND |

Reference connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Astron | 22-2601-5G-1T-R | Standard USB mini-B plug.<br>Standard USB mini-A plug. |

## 4.2. Secondary USB Interface (P10)

NOTE: The secondary USB interface is available only on EM-X270 - rev1.3 and higher.

The EM-X270 provides an additional USB host interface on connector P10. This USB port is connected to the PXA270 host port through a USB hub. Refer to chapter 20 of the PXA270 Reference Guide for a more detailed description of the USB host controller.

The EM-X270 power supply system provides 5V/100mA DC (in compliance with USB OTG standard) on the VCC pin of connector P10.

Connector P10, mini USB type AB:

| Pin | Signal Name |
|---|---|
| 1 | USV_VCC |
| 2 | USB_N |
| 3 | USB_P |
| 4 | NC |
| 5 | GND |

Reference connector data:

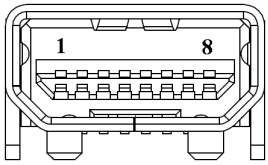
| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Astron | 22-2601-5G-1T-R | Standard USB mini-B plug. |

## 4.3. RS232 (P2)

The FF-UART of the PXA270 is connected to the on-board RS232 driver and to the extender board connector (see section 4.15 for details).
The RS232 driver signals are routed to the RS232 ultra-mini connector (P2).

Connector P2, ultra-mini serial, RS232 levels:

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | RS232_TXD | 5 | RS232_DTR |
| 2 | RS232_RTS | 6 | RS232_DSR |
| 3 | RS232_RXD | 7 | RS232_DCD |
| 4 | RS232_CTS | 8 | GND |




Note: the Ring Indicator signal is not available.

Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Wieson | G3169-500001 | Wieson, P/N: 4306-5000 |

The connector is compatible with the "DB9-F to Ultra Mini Plug" cable available from CompuLab.

## 4.4. MMC/SDIO/SD (P5)

The EM-X270's MMC/SDIO/SD interface is based on the MMC controller of the PXA270 processor. The controller acts as a link between the software that accesses the PXA270 processor and the MMC stack (a set of memory cards) and supports Multimedia Card, Secure Digital, and Secure Digital I/O communications protocols. The MMC controller in the PXA270 processor is based on the standards outlined in the "Multimedia Card System Specification Version 3.2". The SD controller supports one SD or SDIO card based on the standards outlined in the "SD Memory Card Specification Version 1.01" and "SDIO Card Specification Version 1.0 (Draft 4)".

The MMC controller signals are routed to the on-board SD socket (P5).

Connector P5, standard MMC/SDIO socket:

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | MMCDAT3 | 9 | MMCDAT2 |
| 2 | MMCCMD | 10 | GND |
| 3 | GND | 11 | MMC_CD |
| 4 | VCC_SDIO | 12 | MMC_WP |
| 5 | MMCLK | 13 | GND |
| 6 | GND | 14 | GND |
| 7 | MMDAT0 | 15 | GND |
| 8 | MMCDAT1 | | |

## 4.5. LCD Connector (P11)

The EM-X270 LCD panel connector allows seamless integration with the TD035STEE1 LCD module. LCD interface signals, LCD control signals, LCD power and touch-screen interface signals are routed to this connector.

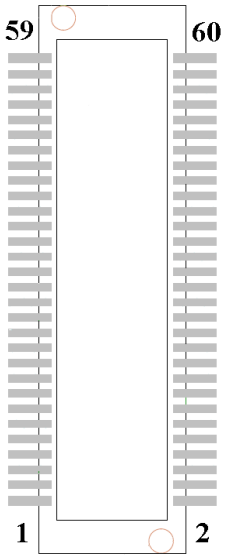
**LCD Controller Signals**

| EM-X270 Name | PXA270 Name | Description |
|---|---|---|
| LCD_B[5-1] | LDD[4-0] | LCD bus data lines |
| LCD_G[5-0] | LDD[5-10] | LCD bus data lines |
| LCD_R[5-1] | LDD[11-15] | LCD bus data lines |
| LCD_PCLK | L_PCLK_WR | LCD bus pixel clock |
| LCD_FCLK | L_FCLK_RD | LCD bus frame clock |
| LCD_LCLK | L_LCLK_A0 | LCD bus line clock |
| LCD_DE_M | L_BIAS | LCD bus output enable |

All above signals are outputs, 3V level.
For more information, please see chapter 7: “LCD Controller” in the PXA270 Reference Guide.

Connector P11, 2x30 board-to-board socket connector:

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|
| 1 | GND | 21 | GND | 41 | LCD_R5 |
| 2 | LCD_TSPY | 22 | GND | 42 | GND |
| 3 | LCD_TSPX | 23 | LCD_B1 | 43 | VCC_LCD |
| 4 | LCD_TSMY | 24 | LCD_B2 | 44 | NC |
| 5 | LCD_TSMX | 25 | LCD_B3 | 45 | GND |
| 6 | GND | 26 | LCD_B4 | 46 | LCD_PCLK |
| 7 | NC | 27 | LCD_B5 | 47 | GND |
| 8 | NC | 28 | GND | 48 | LCD_DE_M |
| 9 | GND | 29 | LCD_G0 | 49 | SSP1_RXD |
| 10 | NC | 30 | LCD_G1 | 50 | SSP1_FRM |
| 11 | NC | 31 | LCD_G2 | 51 | SSP1_TXD |
| 12 | NC | 32 | LCD_G3 | 52 | NC |
| 13 | NC | 33 | LCD_G4 | 53 | SSP1_CLK |
| 14 | NC | 34 | LCD_G5 | 54 | LCD_FCLK |
| 15 | GND | 35 | GND | 55 | LCD_LCLK |
| 16 | NC | 36 | GND | 56 | NC |
| 17 | LCD_RST# | 37 | LCD_R1 | 57 | NC |
| 18 | NC | 38 | LCD_R2 | 58 | LCD_WLED_N |
| 19 | NC | 39 | LCD_R3 | 59 | LCD_WLED_P |
| 20 | VCC_LCD | 40 | LCD_R4 | 60 | GND |




- SSP1_RXD, SSP1_FRM, SSP1_TXD, SSP1_CLK signals are SSP interface lines used for LCD setup. The SSP interface is described in section 4.15 – SSP.
- LCD_TS[PX/PY/MX/MY] signals are input lines of the onboard touch screen controller.
- VCC_LCD is the LCD module power supply line at 3V / 60mA.
- GND is the EM-X270 general ground plane.
- LCD_RST# is a PXA270 GPIO_87 line used as LCD module reset.
- LCD_WLED_P and LCD_WLED_N are positive and negative terminals of the 20V / 20mA white LED driver that supplies the LCD backlight.

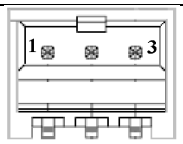
Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Matsushita | AXK5F60547YG | Matsushita, P/N: AXK6F60547YG |

The connector is compatible with the TD035STEE1 LCD panel available from CompuLab.

## 4.6. Main Battery Connector (P4)

Connector P4, 3pin wire-to-board:

| Pin | Signal Name | |
|---|---|---|
| 1 | GND |  |
| 2 | NTC_BAT | |
| 3 | VCC_BAT | |



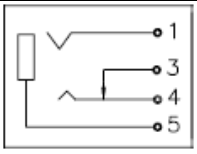
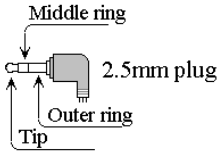
Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Molex | 87438-0343 | Molex, P/N: 87439-0300 |

The connector is compatible with the Li Polymer battery available from CompuLab.

## 4.7. Audio Jack (P6)

Connector P6, 2.5mm jack, headphone output:

| Pin | Signal Name | Mating plug pin | Jack pin-out | Mating plug |
|---|---|---|---|---|
| 1 | LOUT_R | Middle ring |  |  |
| 3 | NC | - | | |
| 4 | LOUT_L | Tip | | |
| 5 | LOUT_C | Outer ring | | |



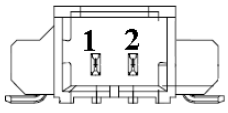


Reference connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Wieson | G7273-050001 | Standard 2.5mm stereo plug. |

## 4.8. Speaker Connector (P15)

Connector P7, 2-pin wire-to-board:

| Pin | Name | |
|---|---|---|
| 1 | SPK_OUT_P |  |
| 2 | SPK_OUT_N | |

Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Molex | 53261-0271 | Molex, P/N: 51021-0200 |

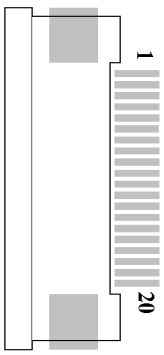
The connector is compatible with the speaker available from CompuLab.

## 4.9. Keypad and General Purpose I/O (P8)

The PXA270 keypad interface is used to provide external matrix keypad connectivity. Matrix keypads of up to 64 keys are supported. The 16 signal lines that control the keypad interface are routed to the keypad FPC connector (P8).
Alternatively, if the keypad interface is not required, or if not all the signal lines are utilized for keypad control, the remaining signals may be used as general purpose I/O.

Additionally, the suspend/resume signal (SUS/RES) is also routed to the keypad connector. This allows placing the suspend/resume button on the keypad of the device.
Connector P8, 20-contacts. FPC 0.5mm:

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | MKIN0_GPIO_100 | 11 | MKOUT0_GPIO_103 |
| 2 | MKIN1_GPIO_101 | 12 | MKOUT1_GPIO_104 |
| 3 | MKIN2_GPIO_102 | 13 | MKOUT2_GPIO_105 |
| 4 | MKIN3_GPIO_34 | 14 | MKOUT3_GPIO_106 |
| 5 | SUS/RES | 15 | RESERVED |
| 6 | MKIN4_GPIO_39 | 16 | MKOUT4_GPIO_107 |
| 7 | MKIN5_GPIO_99 | 17 | MKOUT5_GPIO_108 |
| 8 | MKIN6_GPIO_91 | 18 | MKOUT6_GPIO_96 |
| 9 | MKIN7_GPIO_36 | 19 | MKOUT7_GPIO_22 |
| 10 | RESERVED | 20 | GND |




Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| CVILux | CF20-201D0R0 | FFC, 20 cont, 0.5mm |

## 4.10. Camera Module Connector (P36)

The "quick capture interface" of the PXA270 processor provides a connection between the processor and a camera image sensor. The quick capture interface was designed to work primarily with CMOS-type image sensors. However, it may be possible to connect some

CCD-type image sensors to the PXA270 processor, depending on a specific CCD sensor's interface requirements.
The quick capture interface acquires data and control signals from the image sensor and performs the appropriate data formatting prior to routing the data to memory using direct memory access (DMA). A broad range of interface and signaling options provides direct connection. The image sensor can provide raw data through a variety of parallel and serial formats. For sensors that provide pre-processing capabilities, the quick capture interface supports several formats for RGB and YCbCr color space. The interface supports the "International Telecommunication Union Recommendation ITU-R BT.656-4*"* *(www.itu.int)* Start-of-Active-Video (SAV) and End-of-Active-Video (EAV) embedded synchronization sequences for four- and eight-bit configurations.

For additional information, see Chapter 27: "Quick Capture Interface" in the PXA270 Reference Guide.

The quick capture interface signals are routed to the camera module connector (P36). The camera module connector is designed to operate directly with the OPCOM CM1314YMH-MO02 camera.

Connector P36, 24cont. FPC 0.5mm:

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | CIF_DD0 | 13 | NC |
| 2 | CIF_DD1 | 14 | CIF_VDD_3V |
| 3 | CIF_DD4 | 15 | CIF_VDD_1V8 |
| 4 | CIF_DD3 | 16 | CIF_LV |
| 5 | CIF_DD5 | 17 | GND |
| 6 | CIF_DD2 | 18 | CIF_FV |
| 7 | CIF_DD6 | 19 | CAM_RST |
| 8 | CIF_PCLK | 20 | I2C_SCL |
| 9 | CIF_DD7 | 21 | CIF_VDD_3V |
| 10 | GND | 22 | I2C_SDA |
| 11 | NC | 23 | GND |
| 12 | CIF_MCLK | 24 | GND |

Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| CVILux | CF20-241D0R0 | FFC, 24 cont, 0.5mm |

## 4.11. SIM Card Socket (P7)

Connector P7, standard SIM card socket:

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | GPRS_SIMVCC | 7 | GPRS_SIMIO |
| 2 | GPRS_SIMRST | 8 | GND |
| 3 | GPRS_SIMCLK | 9 | GND |
| 4 | - | 10 | GND |
| 5 | GND | 11 | GND |
| 6 | NC | | |

Reference connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Astron | 5190006-006-R | Standard SIM card. |

## 4.12. Antenna Connectors (J3, J4, J6, J7)

The table below summarizes all the RF antennas' connectivity of the EM-X270.

| Interface | Antenna Connector |
|---|---|
| GPRS | J4* |
| GPS | J7 |
| WLAN | J3 |
| BlueTooth | J6 |

*Only present on EM-X270 – rev1.2 and older.

Connector data:

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| Hirose | U.FL-R-MT(10) | Hirose U.FL-LP-040 |

## 4.13. LED's and Push Buttons

**EM-X270 push-buttons**

The EM-X270 features two user accessible push buttons:

- SW2 is connected to GPIO_1 of the PXA270 processor and is used as a system suspend-resume button.
- SW3 is the main system hardware reset button.

**EM-X270 LED's**

The following table describes EM-X270 LED's.

| LED | Color | System | LED activity |
|---|---|---|---|
| DS1 | Green | General purpose | The LED is on when the system is in active mode. LED function may be redefined in software |
| DS2 | Orange | Battery charger | The LED is on when the main battery is being charged. |
| DS4 | Orange | GSM/GPRS module | See section 3.5 |
| DS5 | Green | Bluetooth module | |

## 4.14. Cellular Module Connector (P37)

The EM-X270 cellular module connector (P37) is conformant with the Telit global form factor interface and can accommodate the Telit 864 series cellular modules. Refer to section 3.5 for more details.

## 4.15. Extender Connector (P3): Local Bus, LCD, UART, SSP, I2C

The EM-X270 extender connector outputs the most significant internal interfaces of the system. This allows for custom hardware boards to be interfaced with the EM-X270.

**PXA270 Local Bus**

The EM-X270's Local Bus is derived from PXA270 processor's memory interface bus. Local Bus implements the access to various types of devices sharing the same interface lines. Interface lines' functioning changes dynamically per-cycle, according to the type of addressed device.

The external memory bus interface supports:

- RAM / ROM memories
- Variable Latency I/O
- PCMCIA / Compact Flash cards
- 16-bit (only) aligned access

Use the memory interface configuration registers of the PXA270 processor to program the device types. Refer to the PXA270 Processors Design Guide, "Processor Block Diagram" for the block diagram of the Memory Controller configuration. Refer to the "Memory Address Map" for the processor memory map. Refer to "Normal Mode Memory Address Mapping" for alternate mode address mapping.

**Local Bus Signals**

| EM-X270 Name | PXA270 Name | Voltage Level | Type | Description |
|---|---|---|---|---|
| LB_D[15-0] | MD[15-0] | 3V | I/O | Local bus data, lower 16 bit |
| P_MB_D[31-16] | MD[31-16] | 1.8V | I/O | Local bus data, upper 16 bit |
| LB_A[9-0] | MA[9-0] | 3V | Output | Local bus address, lower 10 bit |
| P_MB_A[25-10] | MA[25-10] | 1.8V | Output | Local bus address, upper 16 bit |
| LB_WE# | nWE | 3V | Output | Local Bus Write Control |
| LB_OE# | nOE | 3V | Output | Local Bus Read Control |
| LB_PWE# | nPWE | 3V | Output | Local Bus VLIO Write Control |
| LB_RDY | RDY | 3V | Input | Local Bus I/O Ready input |
| P_MB_RD_WR# | RDnWR | 1.8V | Output | Data direction signal |
| LB_CS2# | nCS<2> | 3V | Output | Chip select for static memory range 0x08000000-0x0C000000 |

| | | | | |
|---|---|---|---|---|
| | | | | This range is dedicated to extender board devices. |
| LB_DATA_EN | - | 3V | | Data enable signal. Derived from chip select signals. Should be connected to output enable on the data buffers. |

**Local Bus Buffering**

The internal local bus of the EM-X270 operates at 1.8V voltage levels. A part of the bus is level shifted to 3V on the EM-X270 board. The signals available on the extender connector are partially at the 3V level and partially at the 1.8V level. Voltage level shifting buffering is needed when the 1.8V signals are used.
The local bus must be used very carefully, as bad routing, overloading or contention created by off-board circuitry will affect functionality of on-board components as well. As a general rule, the local bus should be buffered before any further routing or connections on the baseboard. Buffers should be located near the module's connectors. Buffer reference design is available in the schematics of the EB-X270.

**LCD Controller Bus**

The PXA270 LCD controller signals are routed to the extender board connector to allow custom LCD panels to be interfaced with the EM-X270 board.
The LCD Controller signals are described in section 4.5.
For more information, please see chapter 7 – “LCD Controller” in the PXA270 Reference Guide. Reference design for LCD bus connection is available in the schematics of the EB-X270.

**Touch Screen Interface**

NOTE: only available on EM-X270 – rev1.3 and higher.
The four input signals of the on-board touch screen controller are routed to the extender board connecter.

| EM-X270 Name | Type | Description |
|---|---|---|
| LCD_TSPX | Analogue input | Touch-panel input: X+ (Right) for 4-wire |
| LCD_TSMX | Analogue input | Touch-panel input: X- (Left) for 4-wire |
| LCD_TSPY | Analogue input | Touch-panel input: Y+ (Top) for 4-wire |
| LCD_TSMY | Analogue input | Touch-panel input: Y- (Bottom) for 4-wire |

**USB**

NOTE: only available on EM-X270 – rev1.3 and higher.
The PXA270 USB host port is routed to the extender board connector through the on-board USB hub.

| EM-X270 Name | Type | Description |
|---|---|---|
| EXT_USB_DP | I/O | USB differential data plus. |
| EXT_USB_DM | I/O | USB differential data minus. |

**UART**

The PXA270 FF-UART signals are routed to the extender board connector.
NOTE: The signals are at 3V levels.

| EM-X270 Name | PXA270 Name | Type | Description |
|---|---|---|---|
| FFUART_TXD | FF_TXD | Output | Serial data output |
| FFUART_RXD | FF_RXD | Input | Serial data input |
| FFUART_RTS | FF_nRTS | Output | Request to send signal |
| FFUART_DTR | FF_nDTR | Output | Data terminal ready signal |
| FFUART_DSR | FF_nDSR | Input | Data set ready signal |
| FFUART_CTS | FF_nCTS | Input | Clear to send signal |
| FFUART_DCD | FF_nDCD | Input | Data carrier detect signal |

**SSP - Synchronous Serial Protocol**

The SSP is a synchronous serial interface that connects to a variety of external analog-to-digital (A/D) converters, telecommunication CODEC's and other devices that use serial protocols for data transfer. The SSP provides support for the following protocols:

- Texas Instruments (TI) Synchronous Serial Protocol
- Motorola Serial Peripheral Interface (SPI) protocol
- National Semiconductor Microwire
- Programmable Serial Protocol (PSP)

The SSP operates as a full-duplex device for the TI Synchronous Serial Protocol, SPI, and PSP protocols and as a half-duplex device for the Microwire protocol. The FIFO's can be loaded or emptied by the CPU using programmed I/O or DMA burst transfers.

SSP port #1 of the PXA270 is routed to the extender board connector.

NOTE: SSP port #1 is also routed to the onboard LCD panel connector in order to control the TD035STEE1 LCD module. Thus, this port may only be used when the TD035STEE1 LCD module is not required.

| EM-X270 Name | PXA270 Name | Type | Description |
|---|---|---|---|
| SSP1_TXD | SSP1_TXD_GPIO_57 | Output | Transmit data serialized data line |
| SSP1_RXD | SSP1_RXD_GPIO_26 | Input | Receive data serialized data line |
| SSP1_CLK | SSP1_CLK_GPIO_23 | I/O | Serial bit-clock to control the timing of a transfer |
| SSP1_FRM | SSP1_FRM_GPIO_24 | I/O | Serial frame signal |

All signals have 3V levels

**I2C**

The I2C is a serial bus with a two-pin interface. The data pin is used for input and output functions and the clock pin is used to control and reference the I2C bus. The I2C unit allows the processor to serve as a master and slave device that resides on the I2C bus. The PXA270 standard I2C bus is routed to the extender board connector. All signals have 3V levels.

| EM-X270 Name | PXA270 Name | Type | Description |
|---|---|---|---|
| SDA | SDA_GPIO_118 | I/O | I2C serial data/address signal |
| SCL | SCL_GPIO_117 | I/O | I2C serial clock line signal |

**Power Signals**

The DC_VBAT line is connected directly to the EM-X270 main battery positive terminal. Thus, two power supply options exist:

1) The device is supplied from the main battery pack and the extender board circuit is supplied through the DC_VBAT lines.
2) The EM-X270 battery is not used. The extender board features a power supply circuit that provides regulated 3.7V – 4V on the DC_VBAT lines and supplies the EM-X270 through the extender board connector. A reference design for such a power supply system is available in the schematics of the EB-X270.

IMPORTANT NOTE: The EM-X270 does not feature protection circuitry on the DC_VBAT line. It is connected directly to the positive terminal of the battery. Simultaneous connection of a battery and an extender board with a power supply circuit is unsafe and will cause irreversible damage to the battery and EM-X270's electronic circuits.

The GND line is connected to the general ground plane of the EM-X270. Connect these signals to the extender board ground. All GND pins should be connected.

**Miscellaneous Signals**

| EM-X270 Name | PXA270 Name | Voltage Level | Type | Description |
|---|---|---|---|---|
| EXT_PWR_EN | GPIO_97 | 3V | I/O | PXA270 GPIO line. Used in the EB-X270 reference design as a power enable line for the extender board circuitry. |
| EXT_IRQ1# | GPIO_114 | 3V | I/O | PXA270 GPIO line. Pulled up on the EM-X270 board. Used in the EB-X270 reference design as an interrupt input line for the extender board circuitry. |
| EXT_IRQ2 | GPIO_41 | 3V | I/O | PXA270 GPIO line. Pulled down on the EM-X270 board. Used in the EB-X270 reference design as an interrupt input line for the extender board circuitry. |
| EXT_RST# | GPIO_38 | 3V | Output | External board reset output. Active low. |
| LIN_L, LIN_R | - | Analog | Input | Audio line inputs. See chapter 3.4 for details. |

**Extender Connector Pin-out**

Connector P3, 2x70 pin board-to-board:

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|
| 1 | GND | 48 | LB_D10 | 95 | P_MB_A10 |
| 2 | SSP1_TXD | 49 | GND | 96 | P_MB_A18 |
| 3 | SSP1_RXD | 50 | DC_VBAT | 97 | GND |
| 4 | SSP1_CLK | 51 | LB_D8 | 98 | P_MB_A20 |
| 5 | SSP1_FRM | 52 | LB_D12 | 99 | P_MB_A12 |
| 6 | LCD_BUF_FRM | 53 | LB_D11 | 100 | P_MB_A22 |
| 7 | DC_VBAT | 54 | LB_D14 | 101 | P_MB_A13 |
| 8 | GND | 55 | LB_D13 | 102 | LCD_TSPY* |
| 9 | LCD_DE_M | 56 | GND | 103 | P_MB_A15 |
| 10 | LCD_PCLK | 57 | LB_D15 | 104 | GND |
| 11 | LCD_BUF_LP | 58 | P_MB_D17 | 105 | P_MB_A17 |
| 12 | LCD_B2 | 59 | P_MB_D16 | 106 | LB_PWE# |
| 13 | GND | 60 | P_MB_D19 | 107 | P_MB_A19 |
| 14 | DC_VBAT | 61 | GND | 108 | DC_VBAT |
| 15 | LCD_B1 | 62 | P_MB_D20 | 109 | GND |
| 16 | LCD_B4 | 63 | P_MB_D18 | 110 | EXT_USB_DP* |
| 17 | LCD_B3 | 64 | P_MB_D22 | 111 | P_MB_A21 |
| 18 | LCD_G0 | 65 | P_MB_D21 | 112 | EXT_USB_DN* |
| 19 | LCD_B5 | 66 | P_MB_D24 | 113 | LCD_TSPX* |
| 20 | GND | 67 | DC_VBAT | 114 | RESERVED |
| 21 | LCD_G3 | 68 | GND | 115 | LCD_TSMX* |
| 22 | LCD_G1 | 69 | P_MB_D23 | 116 | GND |
| 23 | LCD_G5 | 70 | P_MB_D27 | 117 | LB_DATA_EN |
| 24 | LCD_G2 | 71 | P_MB_D25 | 118 | FFUART_TXD |
| 25 | GND | 72 | P_MB_D29 | 119 | P_MB_RD_WR# |
| 26 | LCD_G4 | 73 | GND | 120 | FFUART_RXD |
| 27 | LCD_R2 | 74 | P_MB_D30 | 121 | GND |
| 28 | LCD_R1 | 75 | P_MB_D26 | 122 | FFUART_RTS |
| 29 | LCD_R4 | 76 | LB_RDY | 123 | EXT_PWR_EN |
| 30 | LCD_R3 | 77 | P_MB_D28 | 124 | FFUART_DTR |
| 31 | DC_VBAT | 78 | LB_A1 | 125 | EXT_IRQ1# |
| 32 | GND | 79 | P_MB_D31 | 126 | FFUART_DSR |
| 33 | LCD_R5 | 80 | GND | 127 | EXT_IRQ2 |
| 34 | LB_OE# | 81 | LB_A0 | 128 | GND |
| 35 | LB_CS2# | 82 | LB_A4 | 129 | LCD_TSMY* |
| 36 | LB_D0 | 83 | LB_A2 | 130 | FFUART_CTS |
| 37 | GND | 84 | LB_A6 | 131 | GND |

| | | | | | |
|---|---|---|---|---|---|
| 38 | LB_D2 | 85 | GND | 132 | SCL |
| 39 | LB_WE# | 86 | LB_A8 | 133 | FFUART_DCD |
| 40 | LB_D4 | 87 | LB_A3 | 134 | EXT_RST# |
| 41 | LB_D1 | 88 | P_MB_A11 | 135 | RESERVED |
| 42 | LB_D7 | 89 | LB_A5 | 136 | SDA |
| 43 | LB_D3 | 90 | P_MB_A14 | 137 | LIN_L |
| 44 | GND | 91 | LB_A7 | 138 | RESERVED |
| 45 | LB_D5 | 92 | GND | 139 | LIN_R |
| 46 | LB_D9 | 93 | LB_A9 | 140 | GND |
| 47 | LB_D6 | 94 | P_MB_A16 | | |

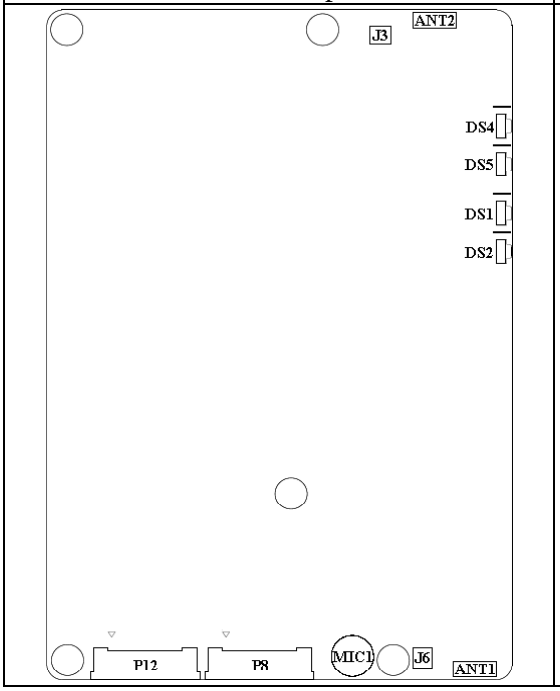
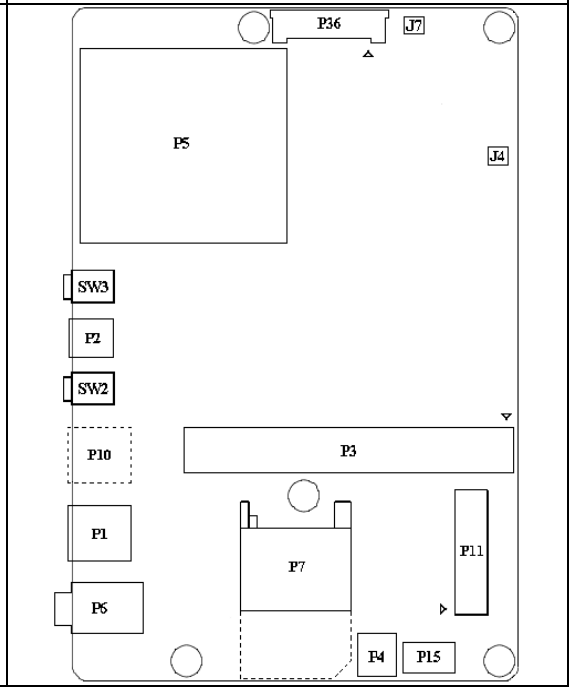
*These signals are available only on EM-X270 - rev1.3 and higher.

**Connector:**

| Manufacturer | Mfg. P/N | Mating connector |
|---|---|---|
| AMP | 8-5353183-0 | 1-5353190-0 or CON140 |

Mating connectors and standoffs are available from CompuLab,
see [prices] >> [accessories] links in CompuLab's website.
CompuLab's p/n name for AMP/Tyco 1-5353190-0 connector is "CON140".

# 5. Connector Location

| EM-X270 Top Side | EM-X270 Bottom Side, bottom view |
|---|---|
|  |  |

# 6. Address Range Mapping

| Memory Address | PXA270 Function | Usage in EM-X270 |
|---|---|---|
| 0x60000000<br>:<br>0x4C000000 | Reserved Address Space | |
| 0x48000000 | Memory Mapped Registers | Memory Ctrl |
| 0x44000000 | Memory Mapped Registers | LCD controller |
| 0x40000000 | Memory Mapped Registers | PXA270 on-chip peripherals |
| 0x30000000 | PCMCIA/CF | Not used |
| 0x20000000 | PCMCIA/CF | Not used |
| 0x1C000000 | Reserved Address Space | |
| 0x18000000 | Reserved Address Space | |
| 0x14000000 | Static Chip Select 5 | Not used |
| 0x10000000 | Static Chip Select 4 | Miscellaneous onboard peripherals |
| 0x0C000000 | Static Chip Select 3 | Reserved for onboard peripherals |
| 0x08000000 | Static Chip Select 2 | Extender board peripherals |
| 0x04000000 | Static Chip Select 1 | NAND flash |
| 0x00000000 | Static Chip Select 0 | NOR Flash |

**NOR flash block mapping**

Please refer to section 7 of the “U-Boot for EM-X270 Reference Guide” for NOR flash memory map.

# 7. Mechanical Considerations

The 3D solidworks model and “dxf” assembly files of the EM-X270 board may be downloaded following [Developer] >> [EM-X270] >> [EM-X270 Dimensions] links in CompuLab's web-site.

# 8. Operating Temperature Ranges

The information in this section refers to the EM-X270 board only. For temperature ranges of off-board components such as the LCD panel or battery pack, please refer to the component's datasheet.

The EM-X270 is available with three options of operating temperature range:

| Range | Temp. | Description |
|---|---|---|
| Commercial | $0^o$ to $70^o$ C | Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested. |
| Extended | $-20^o$ to $70^o$ C | Every card undergoes a short test for the lower limit ($-20^o$ C) qualification. |
| Industrial | $-40^o$ to $85^o$ C | Every card is extensively tested for both lower and upper limits and at several midpoints. |