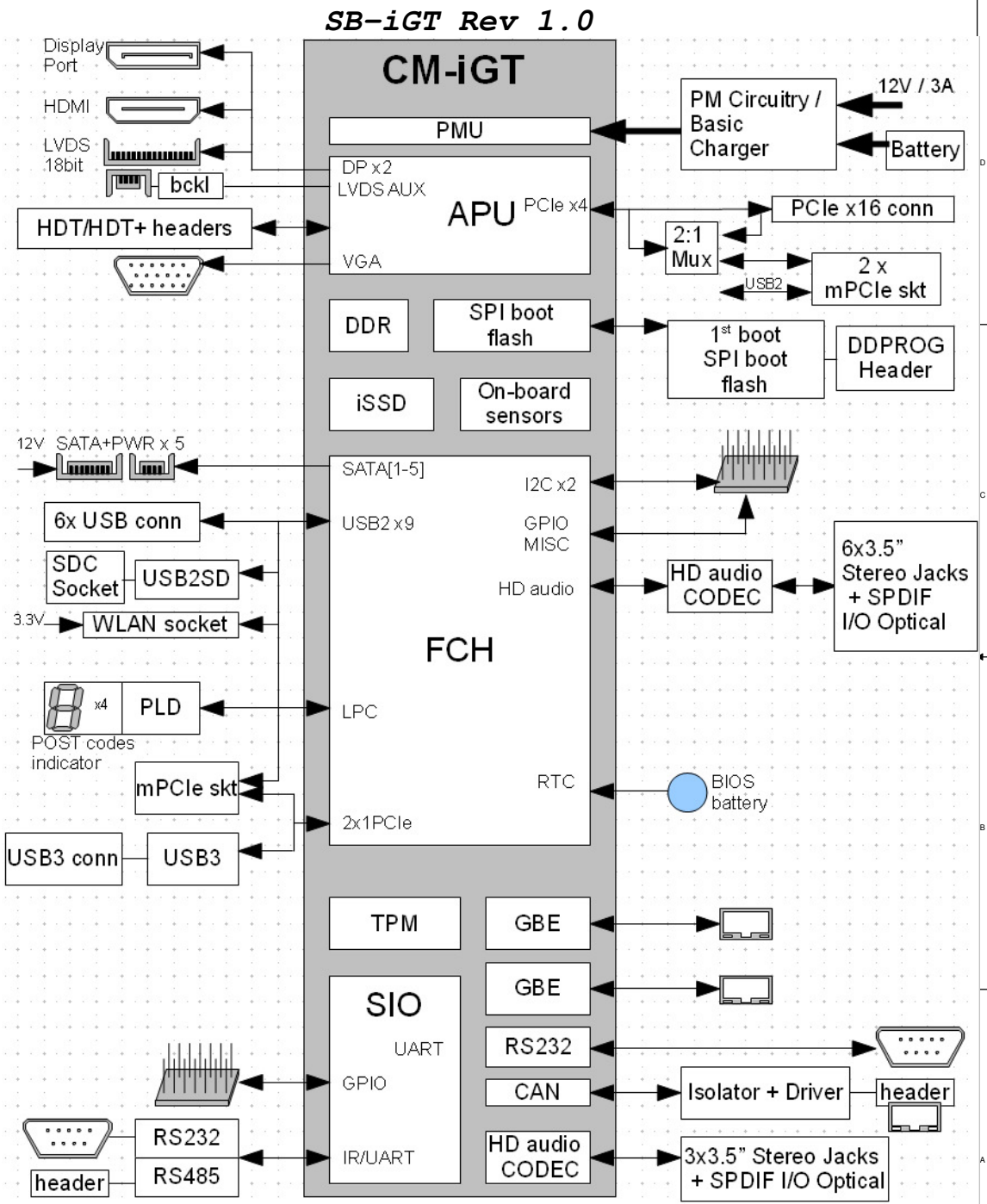
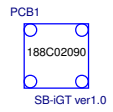
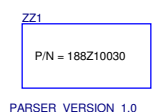
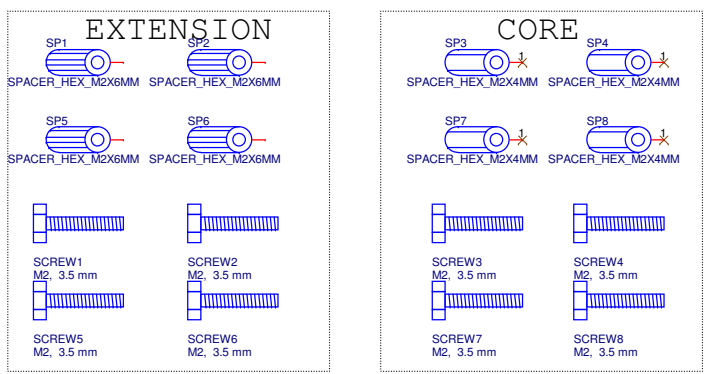
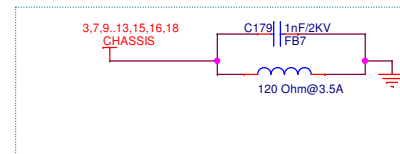
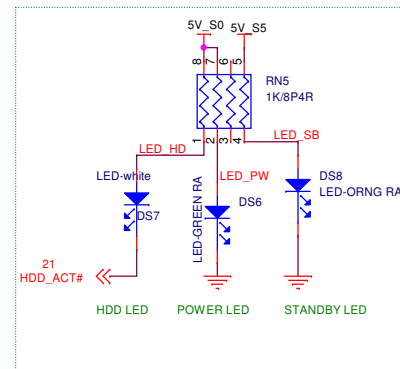
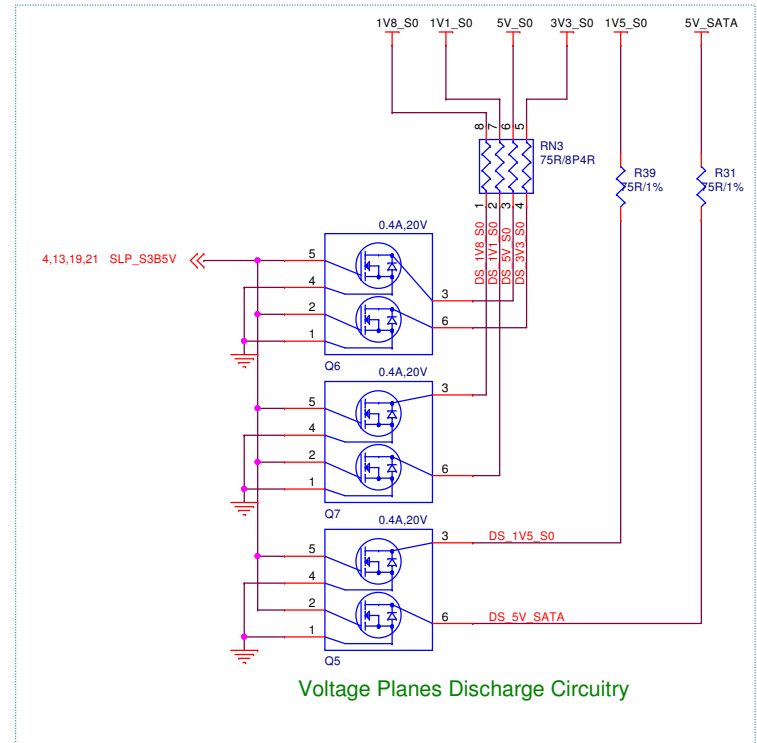
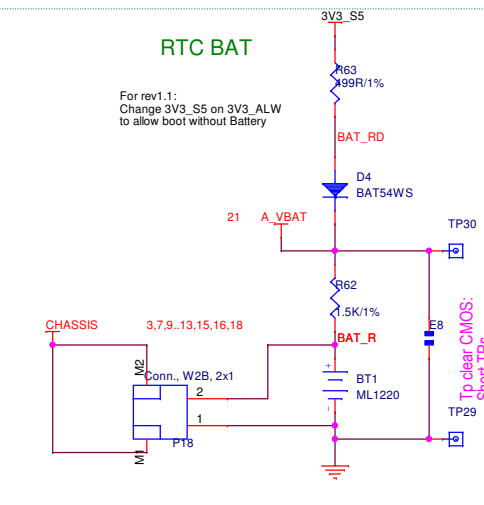
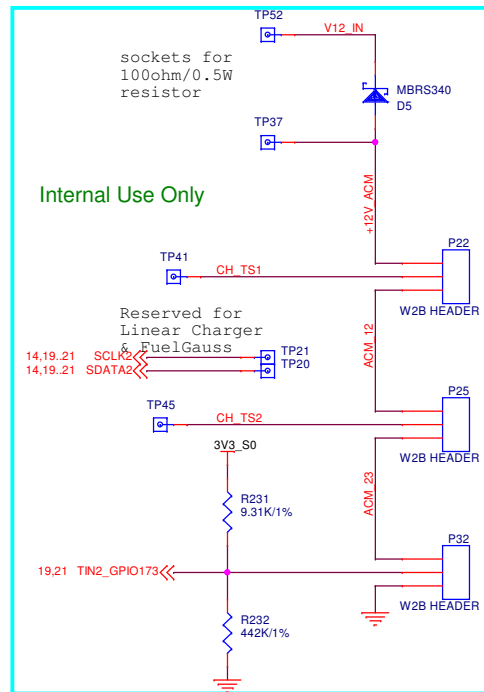
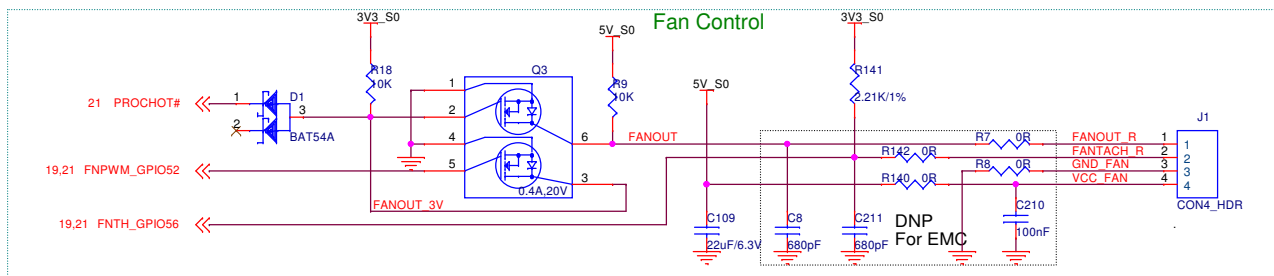
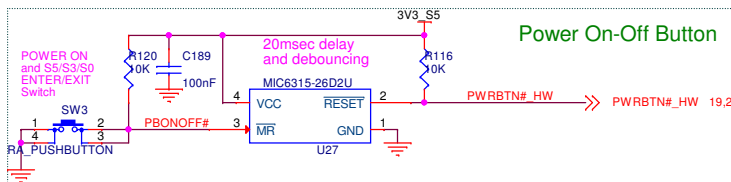
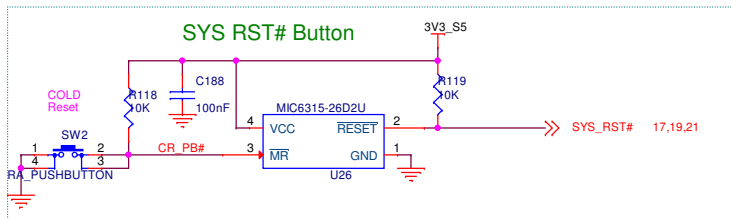
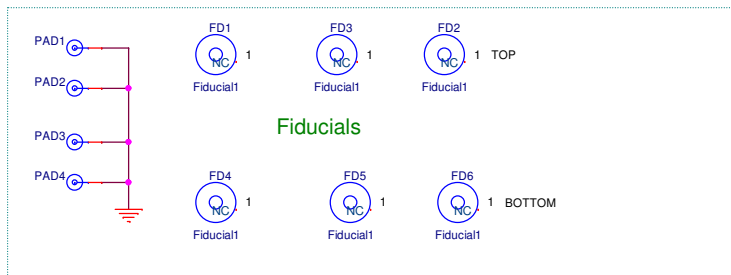
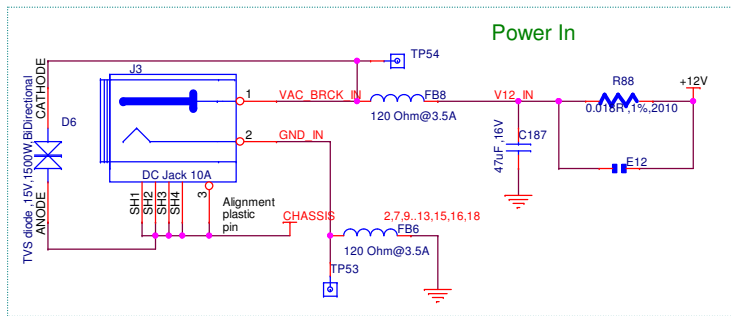
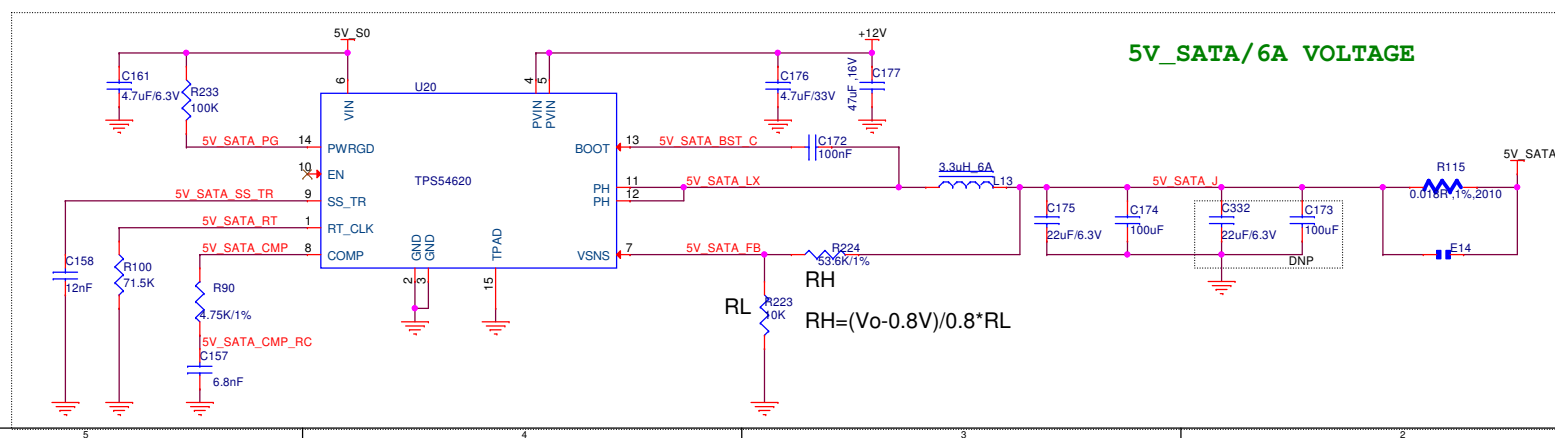
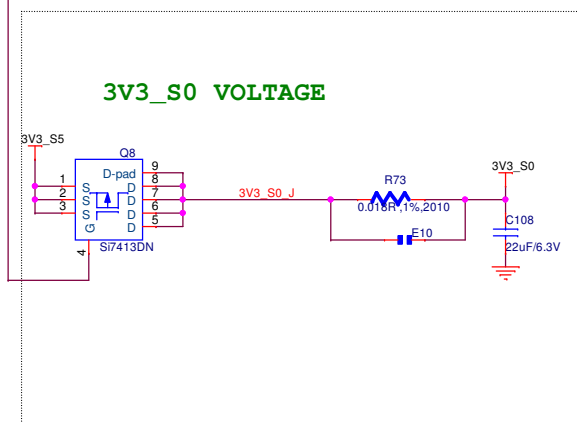
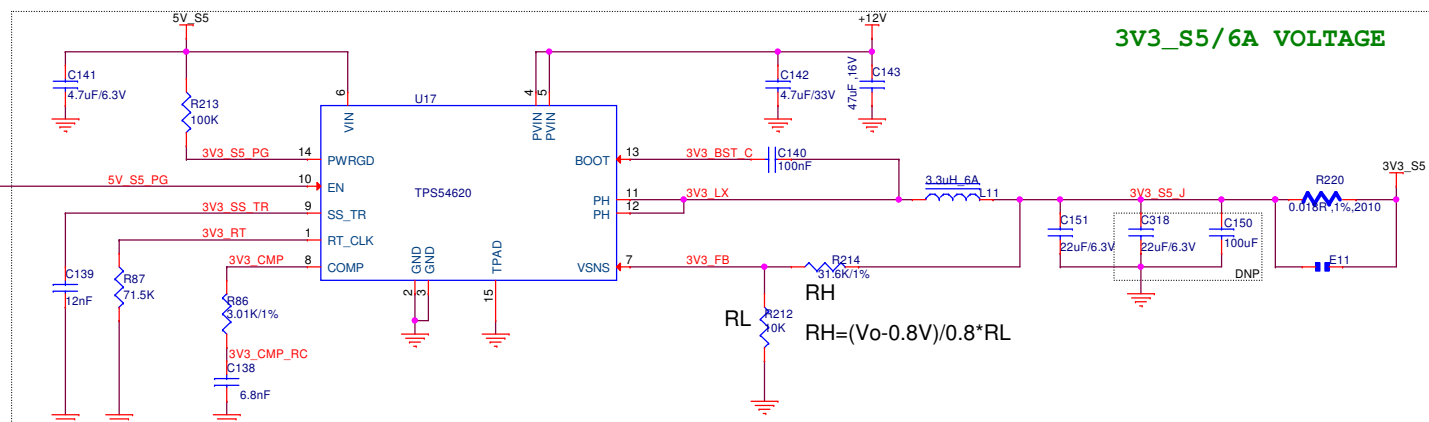
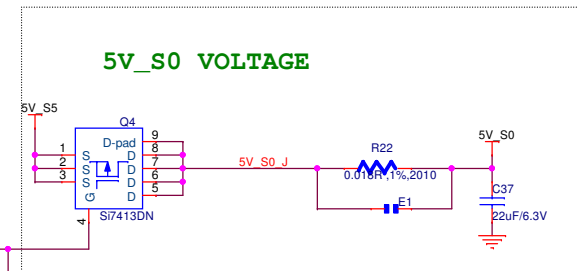
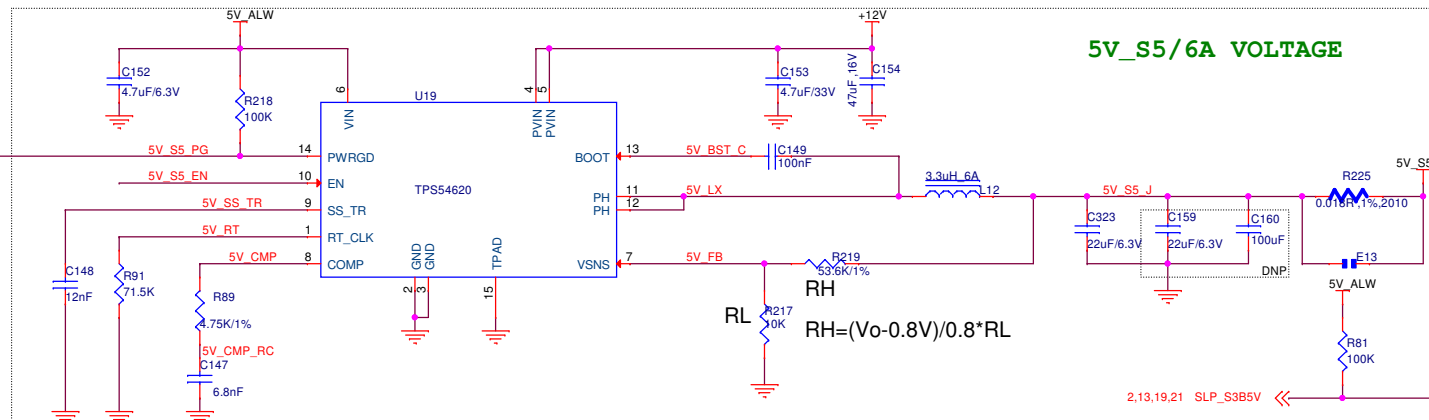
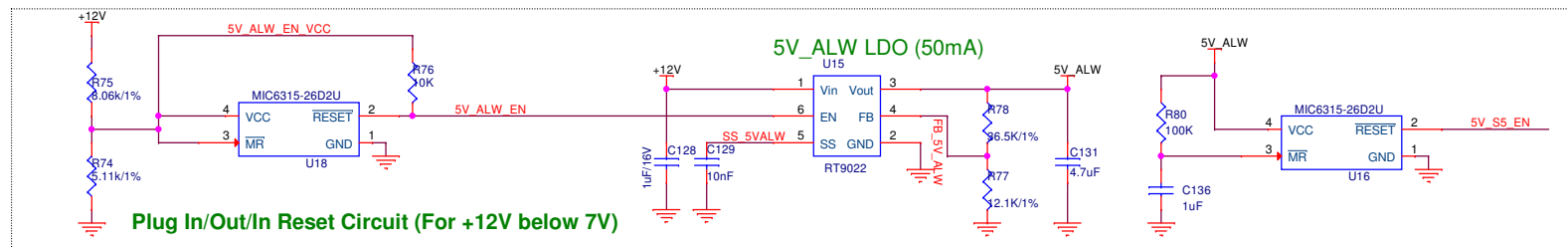


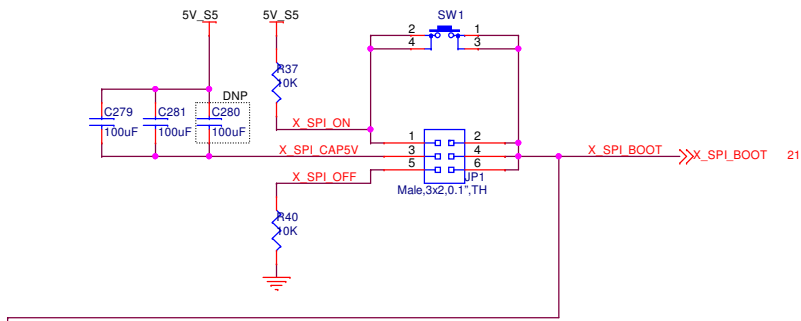
PAGE	FUNCTION
01	INDEX
02	Power In, Init, Reset & Fan
03	SWR: 6A Voltages
04	SWR: 2A Voltages
05	BOOT-FLASH-DDPRG-HDT
06	DP & HDMI / LVDS18bit
07	VGA & COM
08	GBE x 2, USB2 x 2
09	USB0/F1
10	USB2uSD
11	USB3 x 2
12	PCIEx4 - mux - mPCIE
13	Audio- Bases Board
14	Audio- CM
15	PLD+7SEG - Internal Use
16	RS232/485 & CAN
17	Misc Signals, PCB Decoupling
18	SATAx5 & PCIE-CLK-Buf & mPCIE-FCH
19	CAMI connectors







BOOT Selection



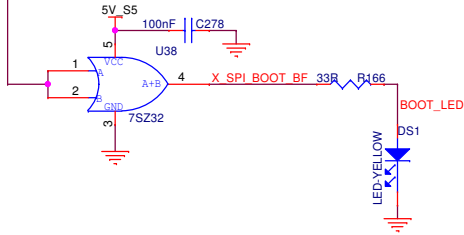
BOOT FLASH Selection

=====

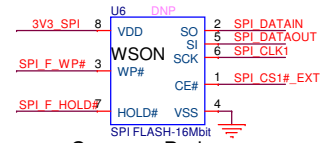
Jumper JP1:

I) Power On:

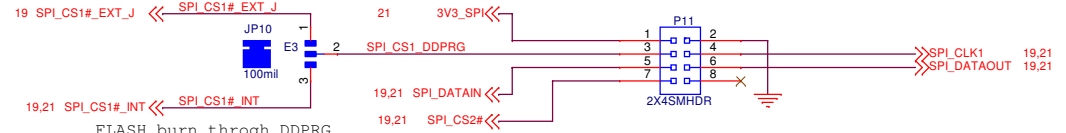
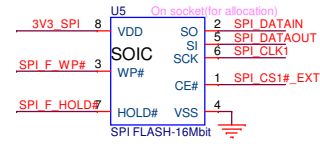
- a) 1-2: BASE FLASH
- b) 3-4: BASE - delay - CORE FLASH
- c) 5-6: CORE FLASH



BIOS FLASH in Socket



Common Pads



FLASH burn throught DDRPG

=====

Jumper Exxx:

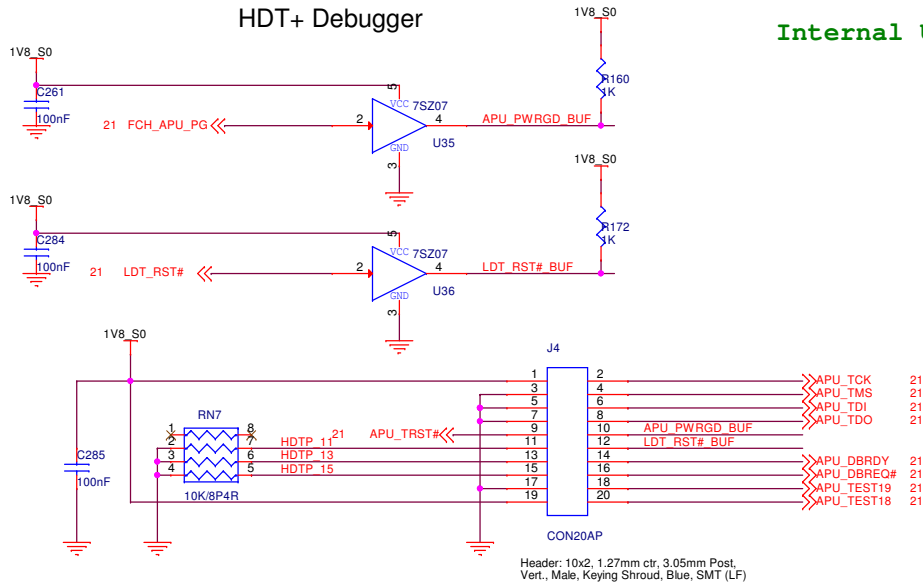
I) Power Off:

- a) 1-2: BASE FLASH
- b) 2-3: CORE FLASH

II) Power On:

- a) Jumper Off
- b) FLASH Selection by JP1

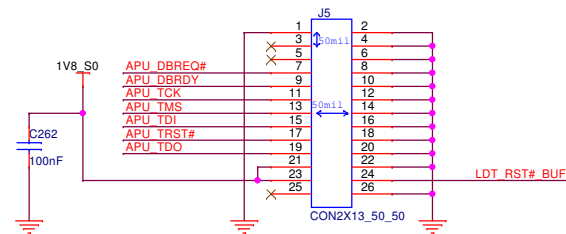
HDT+ Debugger



Header: 10x2, 1.27mm ctr, 3.05mm Post, Vert., Male, Keying Shroud, Blue, SMT (LF)

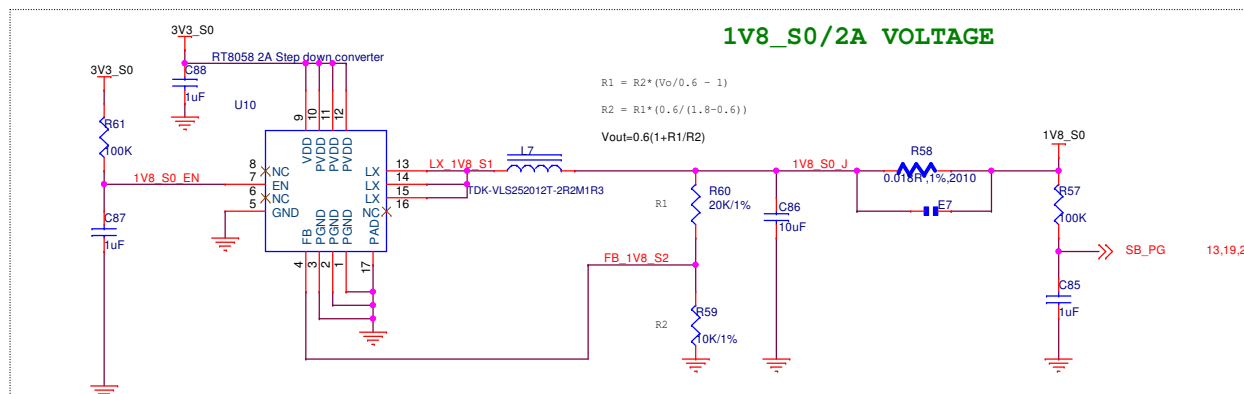
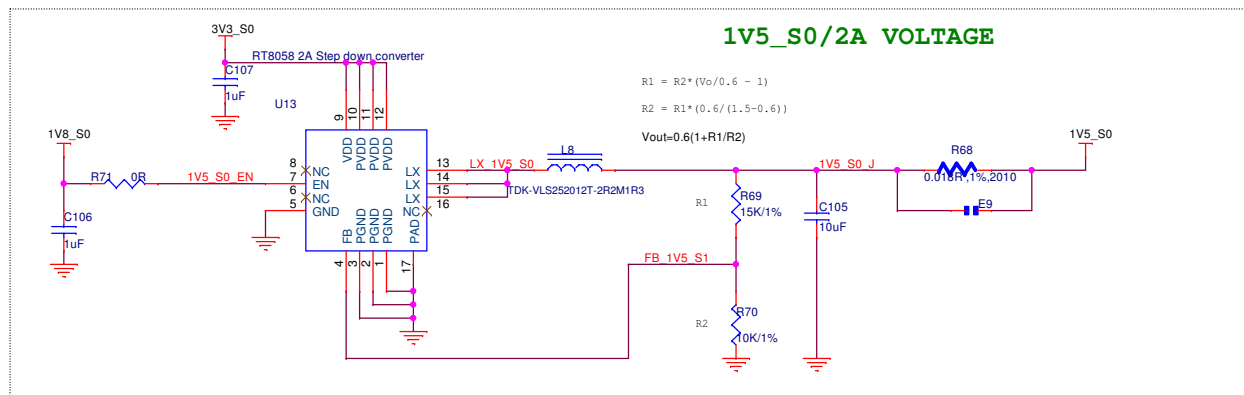
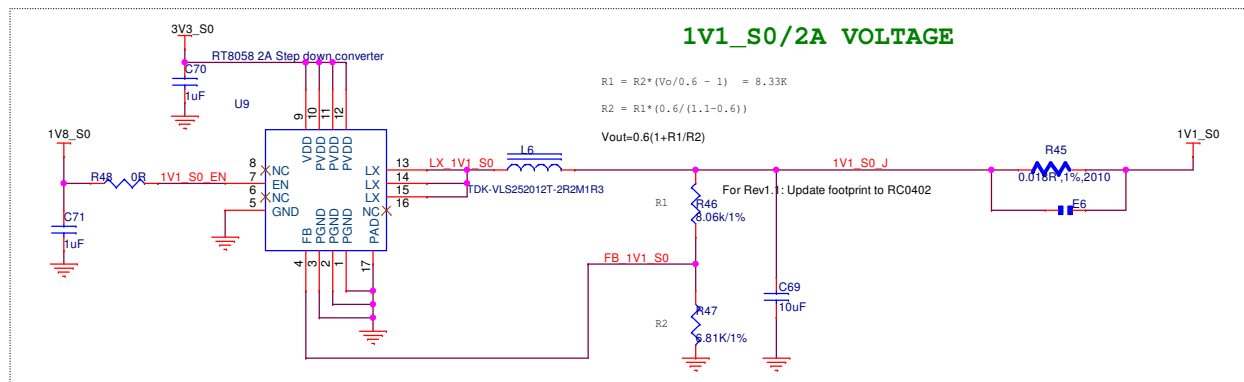
Internal Use Only

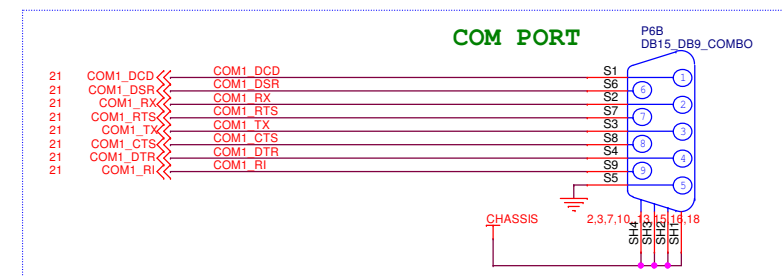
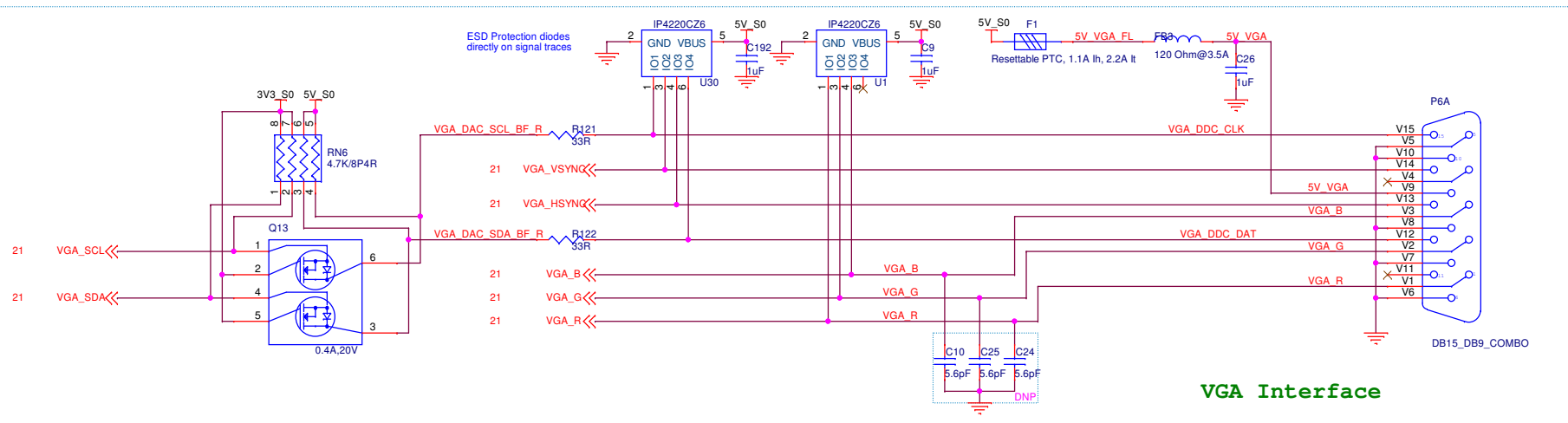
HDT Debugger Option

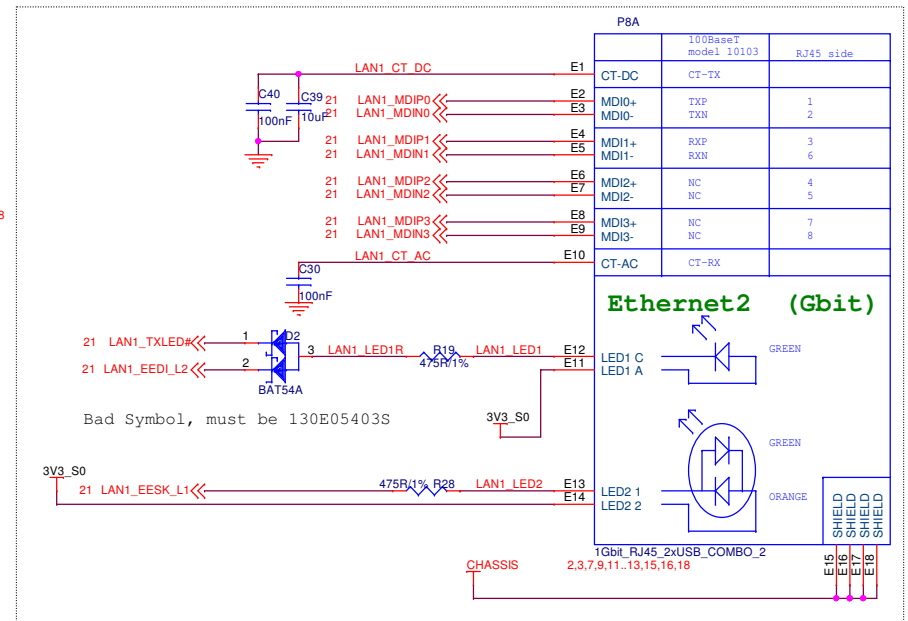
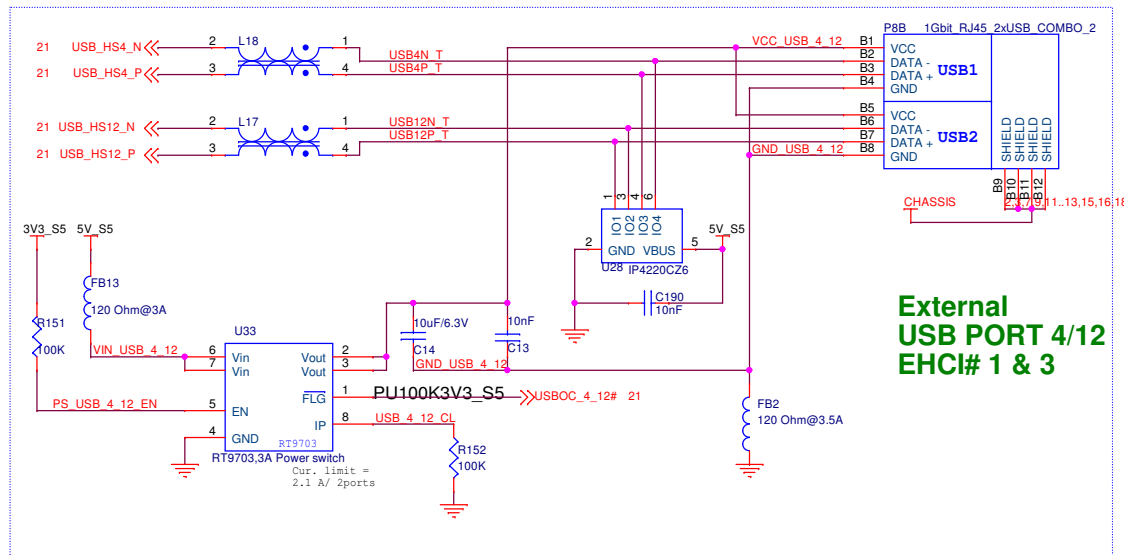
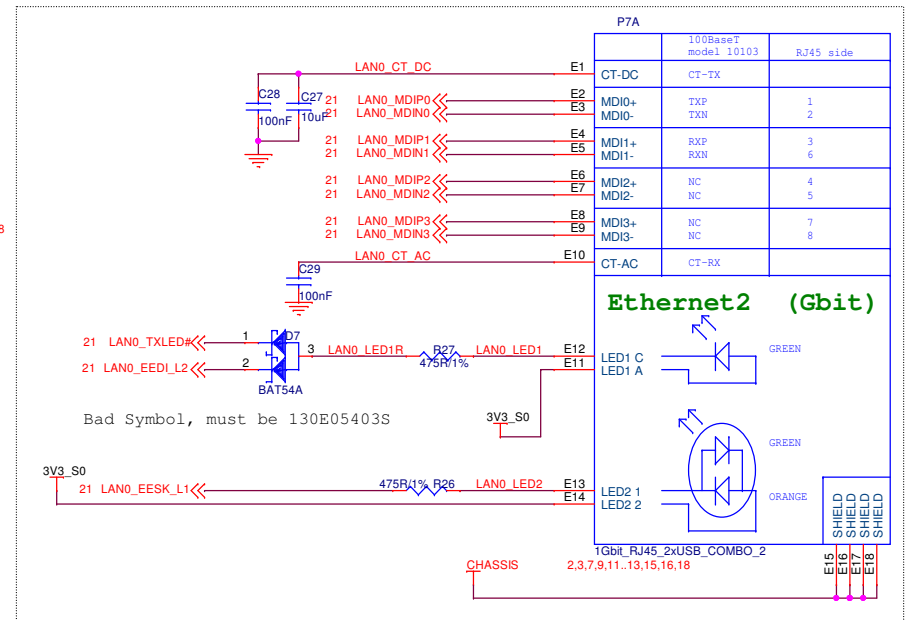
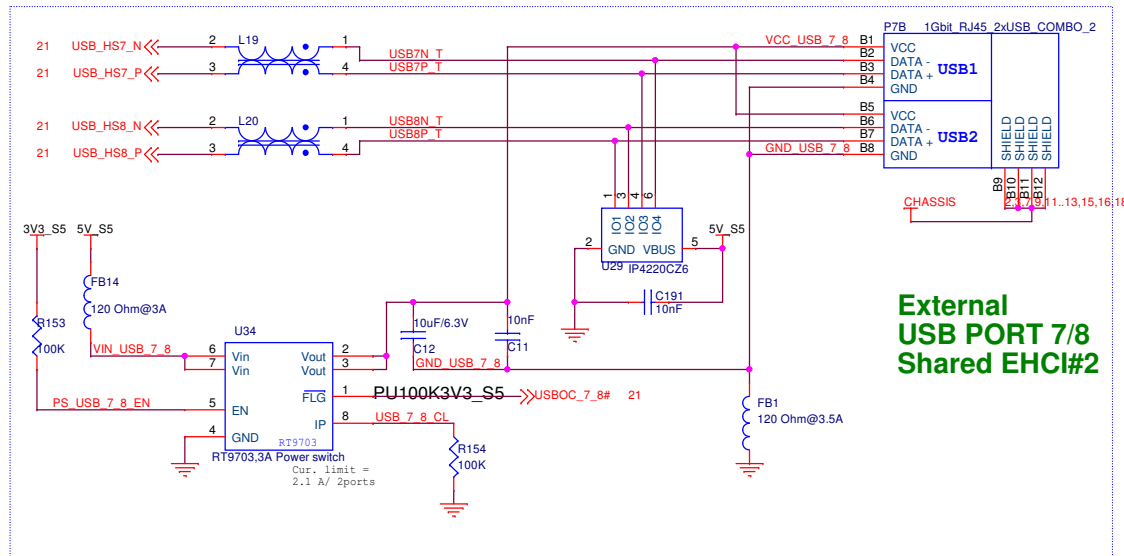


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P.O.Box 66
Nasher 36770, Israel
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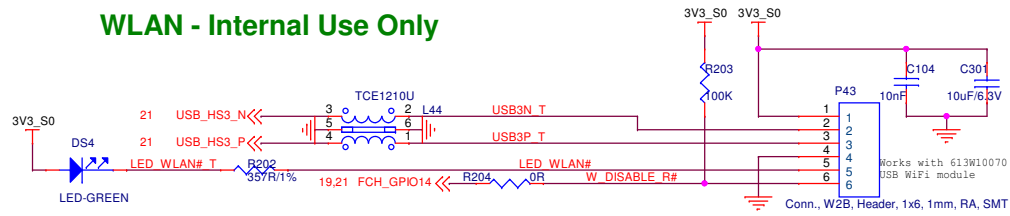
Size	A3	Title	05-SB-IGT: BOOT & HDT Debugger	Rev	1.0
Document Number:	800008000				
Date:	Tuesday, February 26, 2013				
Sheet	5	of	19		



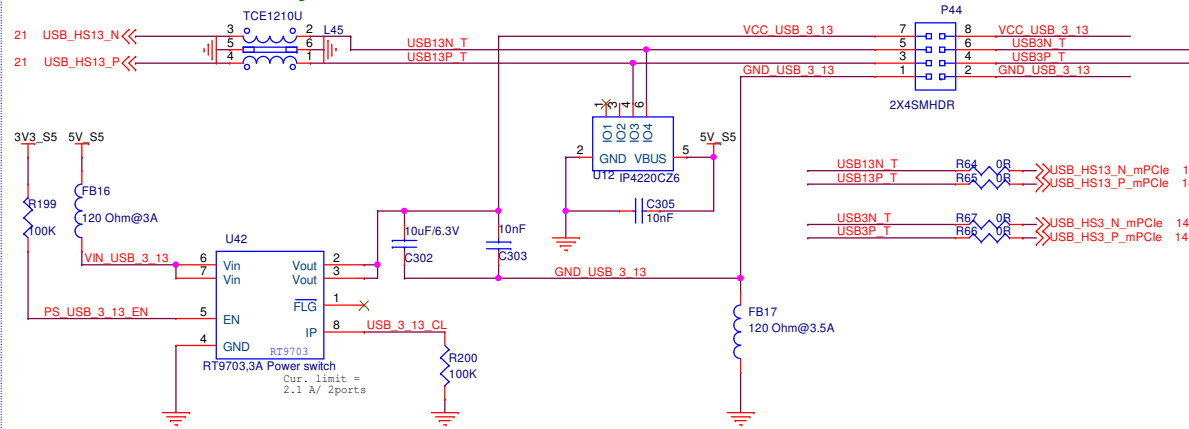




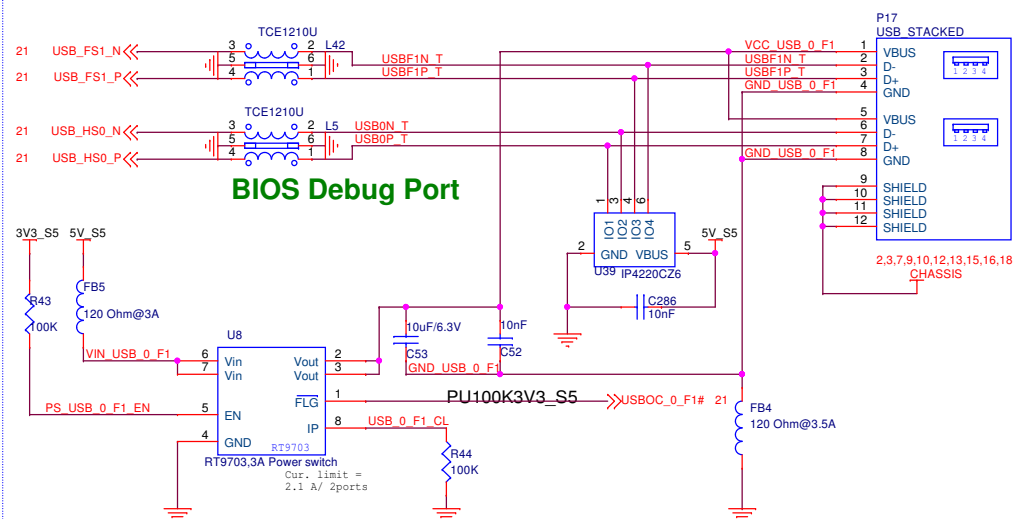
WLAN - Internal Use Only



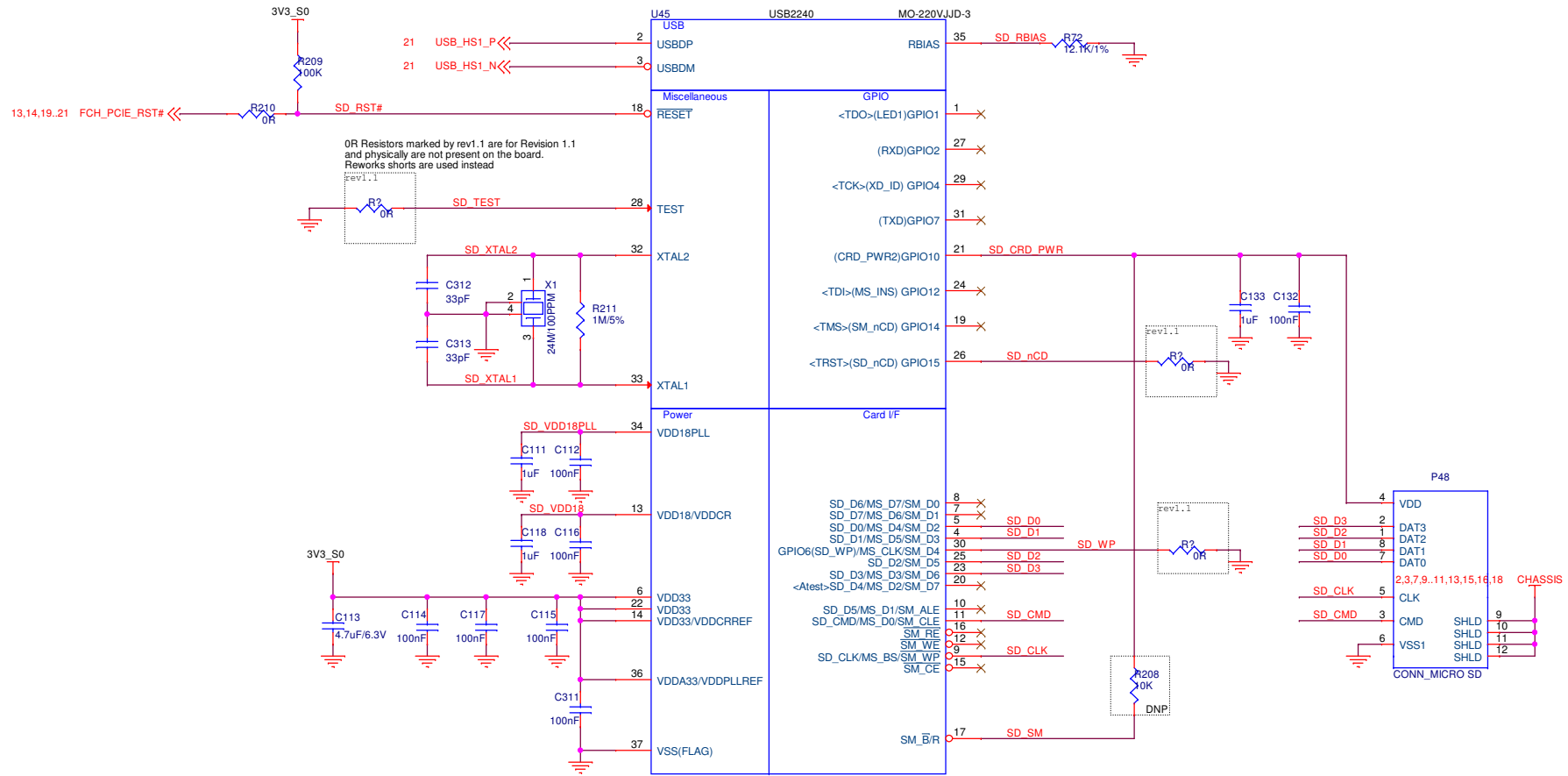
Internal Use Only



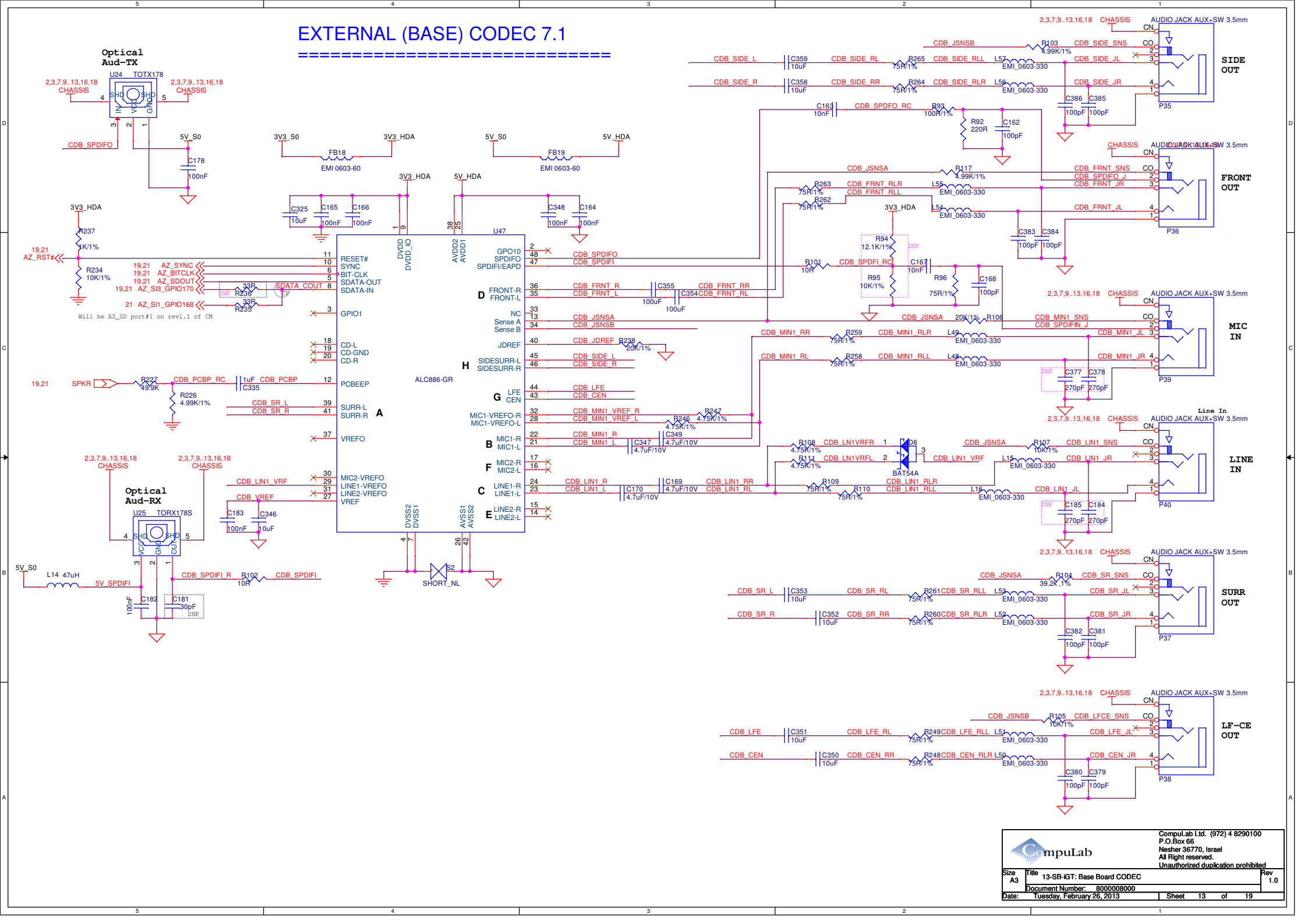
BIOS Debug Port



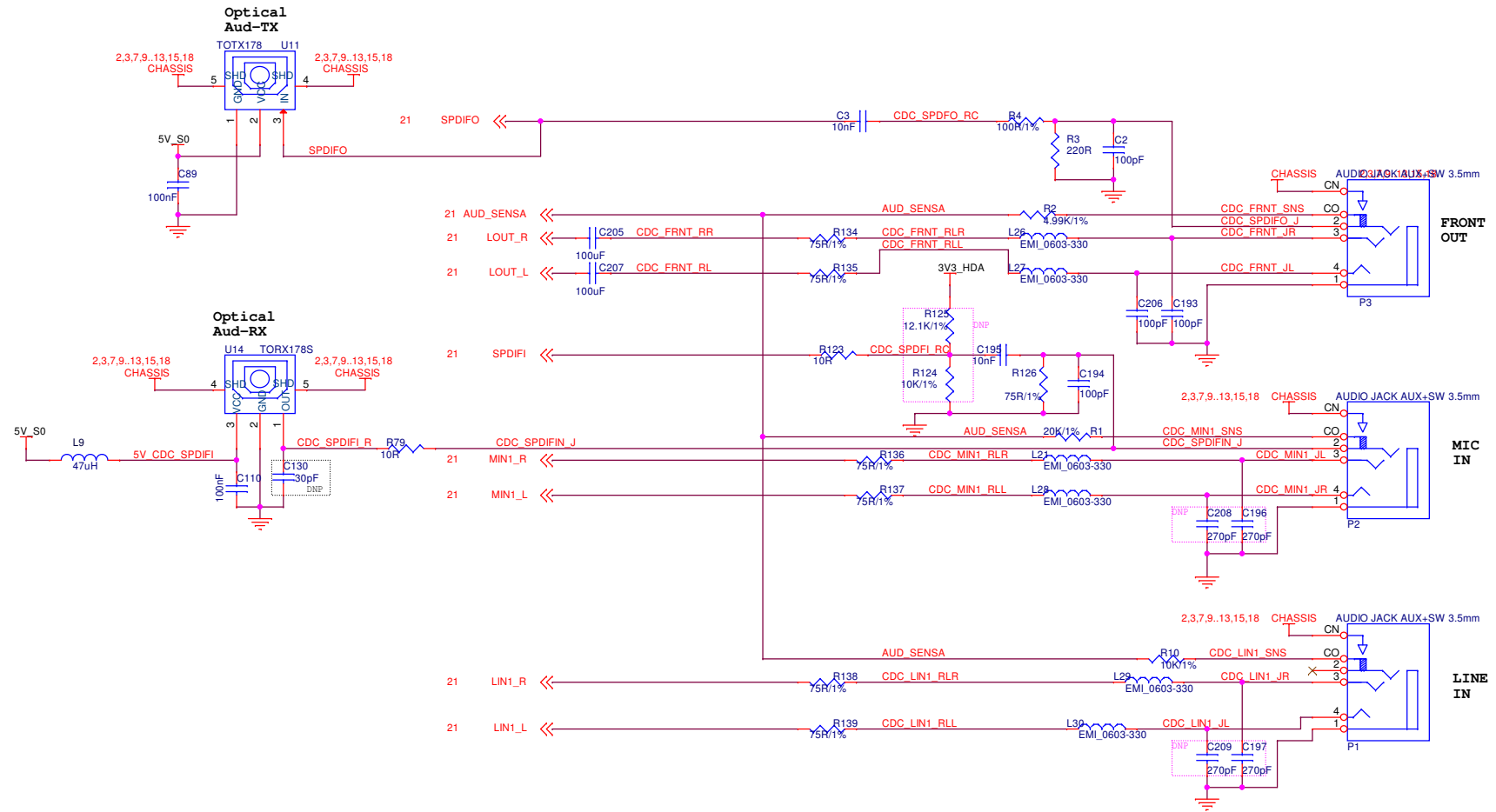
USB to micro-SD



EXTERNAL (BASE) CODEC 7.1



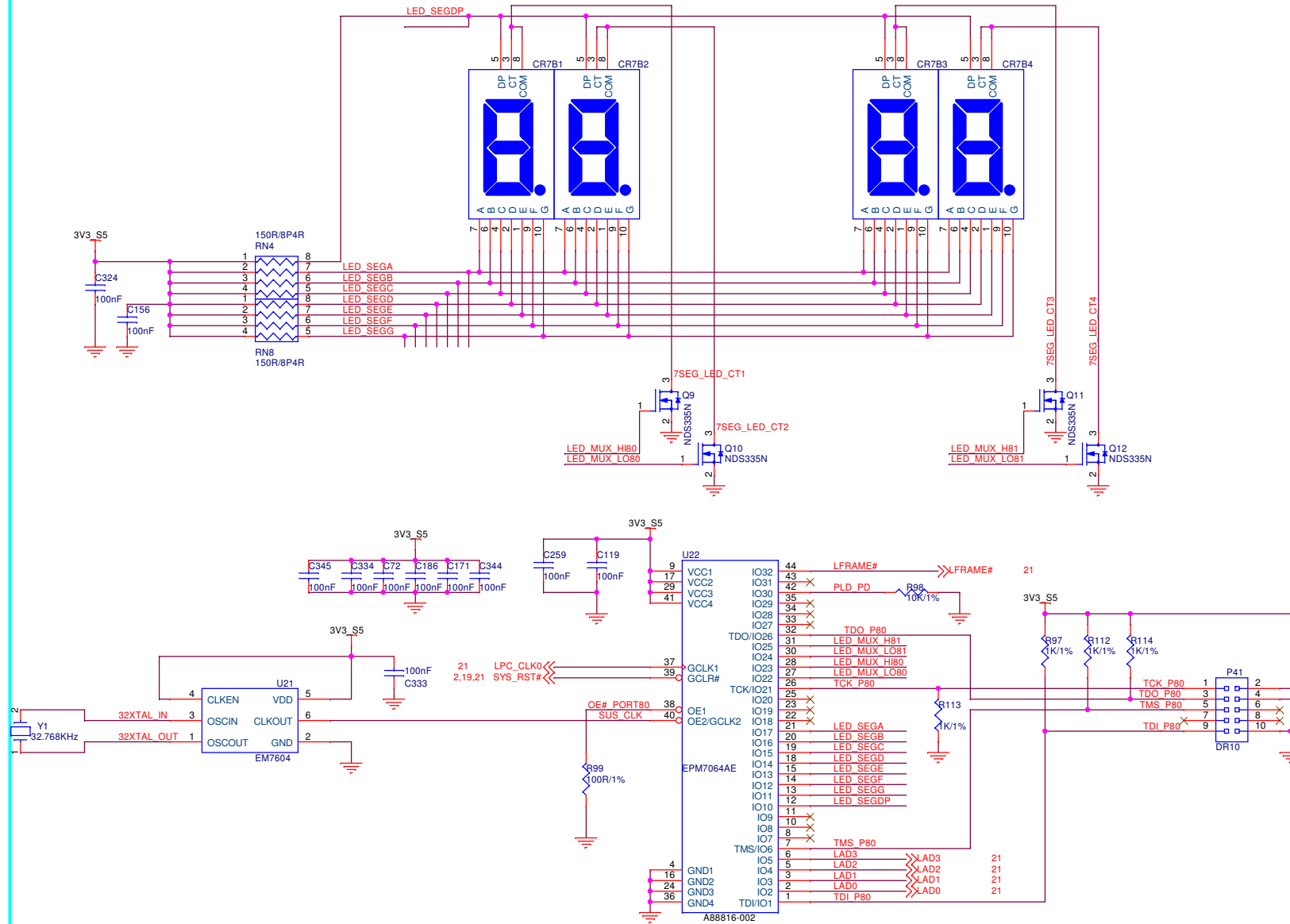
INTERNAL (CORE) CODEC 7.1



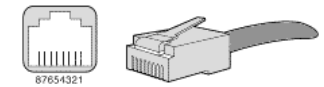
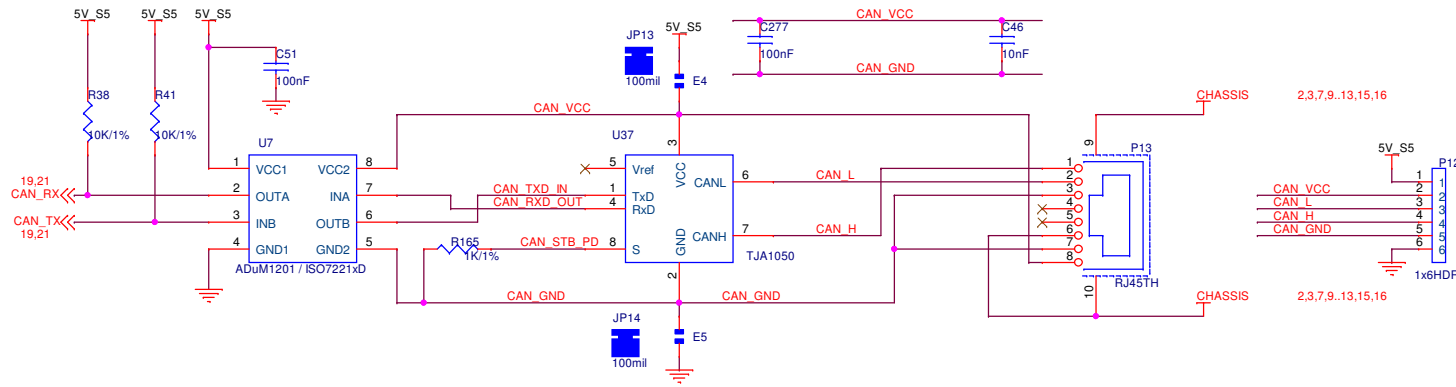
Internal Use Only

BITS: 0-7

BITS: 8-15



CAN INTERFACE + ISOLATOR + TRANSCEIVER



RJ-45 connector
RJ10, RJ45 CAN Bus PinOut

RJ45 Pin #	RJ10 Pin #	Signal Name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional

COM2

