CM-T54 CoM

Reference Guide

CompuLab

CompuLab Ltd.
P.O. Box 687 Yokneam Elite
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.co.il
Fax: +972 (4) 8325251

Table of Contents

Table 1 Revision Notes

Date	Description
Mar 2014	First release
May 2014	Fixed PMIC_PWRON pin# to 165 instead of 162 in table 44. Fixed Table 22 heading to "USB 3.0 OTG interface signals"
June 2014	Table 51: CM-T54 connector implementation revised to "2-sides PCB based SODIMM-204 edge connector"

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CM-T54 Computer-on-Module.

1.2 CM-T54 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CM-T54 part number: http://compulab.co.il/products/computer-on-modules/CM-T54/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-T54 Developer Resources	http://www.compulab.com/
OMAP5432 Reference Manual	http://www.ti.com/product/omap5432
OMAP5432 Datasheet	http://www.ti.com/product/omap5432

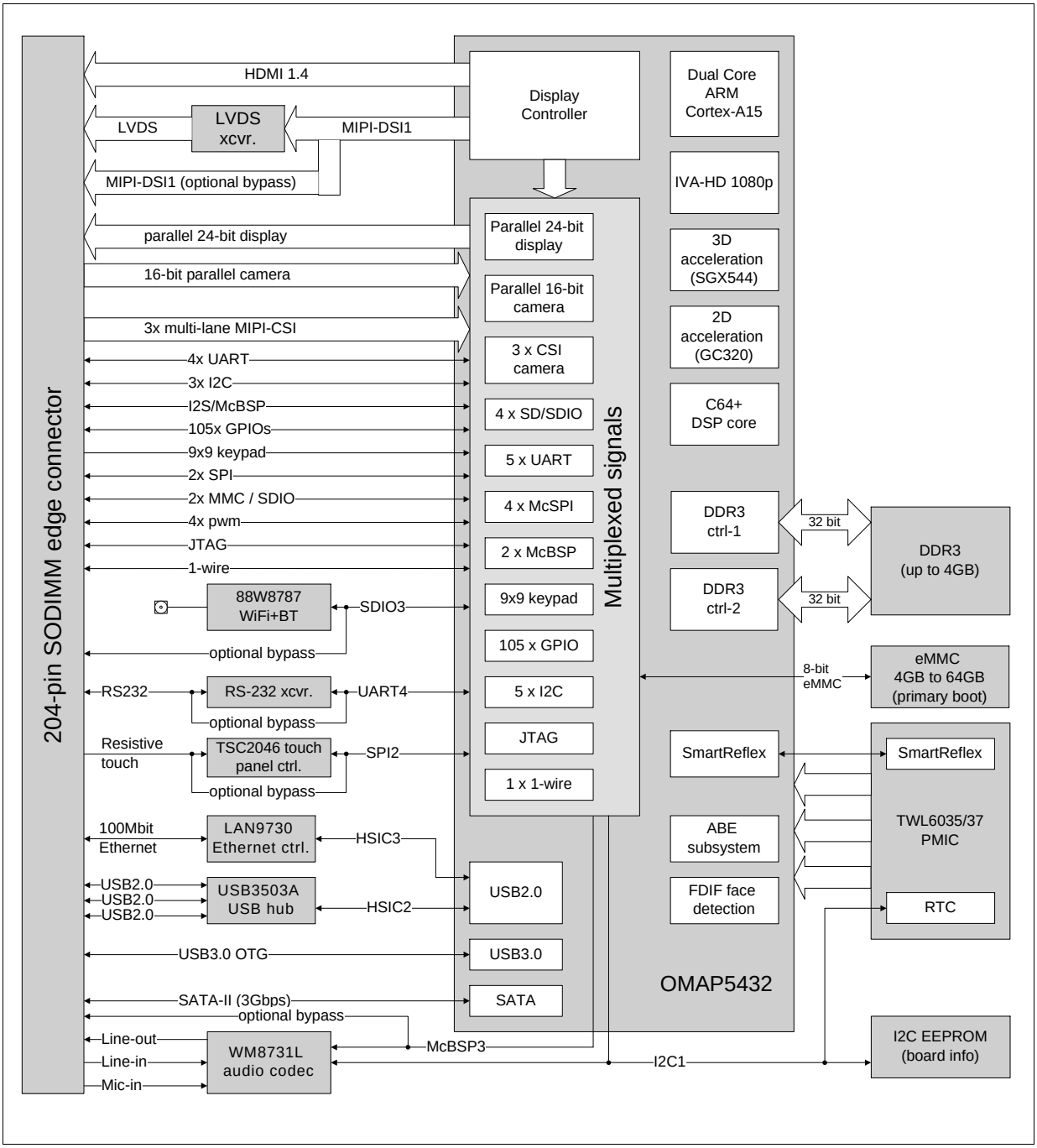
2 OVERVIEW

2.1 Highlights

- Texas Instruments OMAP5 Dual core ARM Cortex-A15 MPCore processor capable of speeds up to 1.5 GHz
- ARM Cortex-M4 processors for low-power offload and real-time responsiveness.
- Up to 4GB Dual Channel DDR3
- Up to 32GB on-board eMMC storage
- Multi-core POWERVR™ SGX544-MPx graphics accelerators
- Dedicated TI 2D BitBlt graphics accelerator
- IVA-HD hardware accelerators enable full HD, multi-standard video encode/decode as well as stereoscopic 3D (S3D)
- HDMI 1.4, LVDS, SATAII (3Gbps), USB3.0 Host + OTG x 1, USB2.0 Host x3, UART x4, SDIO x3, ADC, Onboard WiFi 802.11b/g/n (2.4GHz), Bluetooth 3.0.
- Miniature size: 72 x 68 x 5 mm
- SB-T54 carrier board turns the CM-T54 module into SBC-T54 - a single board computer

2.2 Block Diagram

Figure 1 CM-T54 Block Diagram



2.3 CM-T54 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available. Strikethrough option means that the option must not be chosen for the feature to be available.

Table 3 System and Graphics

Feature	Specifications	Option
CPU	Texas Instruments OMAP5432 (dual-core ARM Cortex-A15 @ 1.5GHz) with: NEON™ SIMD Coprocessor with VFPv4 per ARM core TMS320DM64 32-bit DSP,	C1500
RAM	512MB - 4GB, Dual Channel DDR3-1066 with 32-bit bus width.	D
Storage	On-board eMMC flash, 4GB to 32GB	N
Video Processing Unit	Dedicated IVA-HD audio/video codecs with MPEG1/2/4, H264, H263, DivX, RealVideo and more codecs support.	+
Graphics Acceleration Units	Dual Core PowerVR SGX544 3D GPU with API support for DirectX9, OpenGL-ES1.1 and 2.0, OpenVG 1.1 and OpenCL 1.1 Embedded Profile. Vivante GC320 2D GPU with API support for OpenWF, DirectFB, GDI/DirectDraw and Adobe Flash.	+

Table 4 I/O

Feature	Specifications	Option
Display	1x HDMI display interface (with HDMI Audio support)	+
	1x 24-bit Parallel RGB Display interface	+
	1x Remote Frame Buffer interface	+
	1x LVDS Display interface	L
	1x MIPI-DSI Display interface	NOT L
USB2.0 Host	3x USB2.0 high-speed host ports, 480Mbps, implemented with SMSC USB3503 USB2.0 Hub onboard	U4
USB3.0 Host + OTG	1x USB3.0 super-speed host + OTG port, 5Gbps (backwards compatible)	U1
SATA	1x SATA II interface, 3.0 Gbps, integrated controller and PHY	+
100Mbps Ethernet	1x 100Base-T Ethernet MAC+PHY onboard, implemented with SMSC LAN9730 USB-to-LAN bridge.	E
Serial Ports (UARTs)	1x RS-232 port - TX, RX Only, RS-232 levels. (UART4)	+
	3x UART ports - TX, RX, CTS, RTS Only, 1.8V levels (UART1, UART2, UART5).	+
	1x UART / IrDA / CIR port - TX, RX, CTS, RTS Only, 1.8V levels. (UART3)	+
Audio	1x On-board audio codec with analog stereo output, stereo input and electret microphone support	A
	1x I2S compliant interface (McBSP1)	+
	1x I2S compliant interface (McBSP3)	NOT A
	1x Digital Microphone interface (DMIC)	NOT A
Camera	1x Single Lane MIPI-CSI compatible serial camera interface (MIPI-CSI-C)	+
	1x Dual Lane MIPI-CSI compatible serial camera interface (MIPI-CSI-B)	+
	1x Quad Lane MIPI-CSI compatible serial camera interface (MIPI-CSI-A)	+
	1x Parallel camera port (up to 16 bit)	+
RTC	Real time clock, powered by external lithium battery	+
Resistive Touchscreen Controller	TSC2046 touchscreen controller. Supports 4-wire resistive panels	I
MMC/SD/SDIO	2x MMC/SD/SDIO ports 1/4-bit transfer modes. (SDACRD – bootable, SDIO4)	+
	1x MMC/SD/SDIO port 1/4-bit transfer modes. (WLSDIO)	NOT WB
WiFi and Bluetooth	Implements 802.11b/g/n wireless connectivity standard Based on Marvell 88W8787. On-board connector for external antenna Bluetooth 3.0 + High Speed (HS) (also compliant with Bluetooth 2.1 + EDR)	WB
I2C	3x I2C interfaces (I2C2, I2C3, I2C4)	+
SPI	2x SPI interfaces (SPI1, SPI3)	+
	1x SPI interface (SPI2)	NOT I
	1x SPI interface (SPI4)	NOT WB
HDQ / 1-Wire	1x HDQ/1-Wire interface	+

General Purpose I/O	Up to 106 multifunctional signals. Can be used as GPIOs (shared with other functions)	+
Keypad	1x Keypad interface with up-to 9x9 keys	+

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	3.0V to 5.5V (min 3.2V needed to boot, may be lowered after boot)
Active power consumption	TBD
Standby/Sleep consumption	TBD
Dimensions	72 x 68 x 8 mm
Weight	25 gram (w/o heat-plate)
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C Extended: -20° to 70° C Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	SODIMM-204
Connector insertion / removal	50 cycles

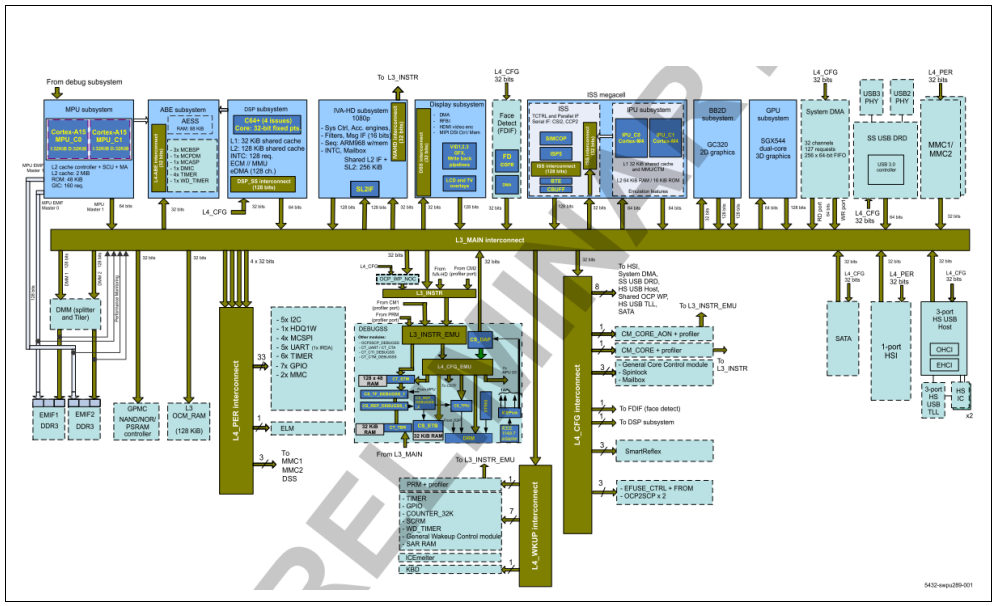
3 CORE SYSTEM COMPONENTS

3.1 OMAP5432 SoC

The Texas Instruments OMAP5432 SoC is a multimedia application device designed to provide best-in-class CPU performance, video, image and graphics processing for a broad range of multimedia-rich applications. The device includes comprehensive power management techniques required for high performance mobile products. The device is composed of the following major subsystems:

- Cortex-A15 microprocessor unit (MPU) subsystem, including two ARM Cortex-A15 cores.
  - ARMv7 ISA: standard ARM instruction set plus Thumb-2, Jazelle RCT, Java accelerator, hardware virtualization support and large physical address extensions (LPAE).
  - Neon SIMD coprocessor and VFPv4 per CPU.
  - 32-KiB instruction and 32-KiB data L1 cache per CPU.
  - Shared 2-MiB L2 cache.
- Digital signal processor (DSP) subsystem
- Image and video accelerator high-definition (IVA-HD) subsystem
- Cortex-M4 image processing unit (IPU) subsystem, including two ARM Cortex-M4 microprocessors.
- Display subsystem
- Audio back-end (ABE) subsystem
- Imaging subsystem (ISS) consisting of image processor (ISP) and still image coprocessor (SIMCOP) block.
- 3D-graphics accelerator subsystem, including POWERVR SGX544 dual-core GPU.

Figure 2 OMAP5432 Block Diagram



3.2 Multimedia System

3.2.1 3D and 2D Acceleration

OMAP5432 incorporates separate accelerators for 3D and 2D graphics. The dual-core PowerVR SGX544 GPU from Imagination Technologies is dedicated for 3D rendering tasks while the Vivante corporation GC230 core is dedicated for 2D graphics acceleration.

The 3D dedicated PowerVR SGX544 GPU supports the following features:

- API support for DirectX9, OpenGL-ES1.1 and 2.0, OpenVG 1.1 and OpenCL 1.1 Embedded Profile.
- Second generation universal scalable shader engines (USSE2), multithreaded engines incorporating pixel and vertex shader functionality.
- Programmable image antialiasing
- Bilinear, trilinear and anisotropic texture filtering
- RGB, ARGB, YUV422 and YUV420 surface formats

The 2D dedicated Vivante GC320 core supports the following features:

- API support for OpenWF, DirectFB, GDI/DirectDraw, Adobe Flash.
- BitBlt and StretchBlt
- DirectFB HW acceleration
- YUV-to-RGB color space rotation
- Programmable display format conversion with 14source and 7 destination formats
- 32-phase filter for image and video scaling at 1080p
- ROP2, ROP3 and ROP4 full alpha blending and transparency
- 90, 180, 270 degree rotation on every primitive
- Monochrome expansion for text rendering

3.2.2 DSP subsystem

The DSP subsystem is based on a derivative of the TMS320DMC64x+ VLIW DSP core and contains the following submodules:

- TMS320DM64 32-bit fixed DSP core for audio processing and general purpose imaging and video processing, backward compatible with existing C64x video codecs.
  - 32-KiB L1 4-way associative cache
  - 128-KiB L2 8-way associative cache
- Dedicated DMA engine with 128 channels for video/audio data transfer between on-chip memories and DDR3 / peripherals.
- Dedicated Memory management unit (MMU) for virtual/physical address translation.
- Interrupt controller with up to 128 IRQs.

3.2.3 IVA-HD Subsystem

The IVA-HD subsystem is a set of video encoder/decoder hardware accelerators which supports resolutions up to 1080i/p with full performance of 60fps (or 120 fields), achievable for encode or decode (not for simultaneous encode and decode). The IVA-HD subsystem supports the following coder/decoder (codec) standards natively (all functional of these standards are accelerated without intervention of the DSP).

- H.264 BP/MP/HP encode and decode
- H.264 fast profile/RCDO encode and decode
- MPEG-4 SP/ASP encode and decode (no support for GMC)
- DivX 5.02 and higher encode/decode (no lower versions such as 3.11 and 4.x).
- H.263 P0 encode and decode, P3 decode.
- Sorenson Spark V0 and V1 decode (no encode support).
- MPEG-2 SP/MP encode/decode
- MPEG-1 encode/decode
- VC-1/WMV9/RTV SP/MP/AP encode and decode
- On2 VP6.2/VP7 decode
- RealVideo 8/9/10 decode
- AVS 1.0 encode and decode
- JPEG (also MJPEG) baseline encode and decode
- H.264 Annex G (SVC) scalable baseline profile 480p-720p30
- H.264 Annex H (MVC) up to 720p30

3.3 Memory

3.3.1 DRAM

CM-T54 is equipped with up to 4GB of onboard dual-channel DDR3 memory. Each DDR3 channel is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

NOTE: CM-T54 boards with 512MB of DRAM (D05 option) utilize only one DDR3 channel.

3.3.2 On-board eMMC storage

CM-T54 is available with an eMMC based onboard storage device. eMMC is the main non-volatile memory of CM-T54. It is used for boot-loader, operating system and general purpose data storage. CM-T54 (depending on board configuration) can be equipped with a 4GB, 8GB, 16GB or 32GB eMMC device.

4 PERIPHERAL INTERFACES

CM-T54 implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of the CM-T54 CoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Many of the CM-T54 carrier board interface pins are multifunctional. Up-to 8 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the CM-T54 digital interfaces operate at 1.8V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CM-T54 Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-T54. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"OD"** – Open Drain Signal (not pulled up on-board CM-T54 unless otherwise noted).
- **"P"** – Power
- "**SPU" –** Software controlled pull up to 1.8V
- "**SPD" –** Software controlled pull down to GND
- **"PU18**" – Always pulled up to 1.8V on-board CM-T54, (typ. 5KΩ-15KΩ).
- **"PD" -** Always pulled down on-board CM-T54, (typ. 5KΩ-15KΩ).

4.1 Serial ATA Interface

The CM-T54 incorporates a single SATA-II port implemented with the OMAP5432 integrated SATA controller and PHY. The interface supports the following main features:

- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Support for all SATA power management features.
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.
- Activity LED

Table 6 SATA signals

Signal Name	Pin #	Type	Description	Availability
SATA_RXM	29	AI	SATA receive data pair	Always available
SATA_RXP	27	AI		Always available
SATA_TXM	23	AO	SATA transmit data pair	Always available
SATA_TXP	21	AO		Always available
SATA_ACTLED	60*	O	Activity led control signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.2 Display Interfaces

The CM-T54 display subsystem is responsible for grabbing an image from the system memory (frame buffer) and displaying that image on an LCD panel or a TV set.

The subsystem can simultaneously display different pictures using 3 independent LCD outputs (LCD1, LCD2 and LCD3) in addition a TV output. Each of the LCD outputs can be available through one of the following CM-T54 interfaces:

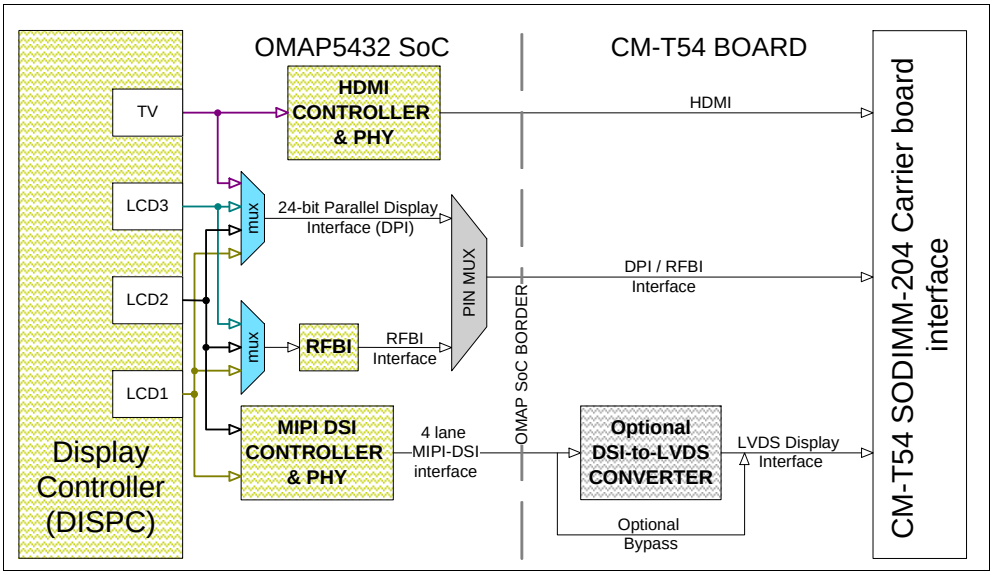
- Display serial interface (DSI / MIPI-DSI)
- Remote Frame Buffer interface (RFBI / MIPI DBI 2.0)
- 24 bit Parallel Display Interface (DPI)

The TV output can be available through one of the following CM-T54 interfaces:

- 24 bit Parallel Display Interface (DPI)
- High-definition multimedia interface (HDMI)

Figure 3 summarizes the display sources, relevant interfaces and architecture of the CM-T54 display subsystem.

Figure 3 CM-T54 Display subsystem



4.2.1 Parallel Display Interface (DPI)

The Parallel Display interface of CM-T54 can be used to drive data from any of the display sources (LCD1, LCD2, LCD3 or TV) available with CM-T54 (see Figure 3 above). The interface is compatible with MIPI DPI protocol.

When LCD1, LCD2 or LCD3 are accessed through the parallel display interface 12, 16, 18 and 24 bit RGB modes are supported. The TV output is a 30-bit RGB interface, however only the MSB (R[9:2],G[9:2],B[9:2]) are available through the parallel RGB interface. The following standards are supported:

Table 7 Parallel Display Interface signals

Signal Name	Pin #	Type	Description					Availability
			12-bit	16-bit	18-bit	24-bit	30-bit	
DISPC_PCLK	98*	O	Pixel clock					Always available
DISPC_HSYNC	100*	O	Horizontal synchronization					Always available
DISPC_VSYNC	102*	O	Vertical synchronization					Always available
DISPC_DE	104*	O	Data validation/blank, data enable					Always available
DISPC_FID	66*	O	The FID signal indicates the field identifier of the LCD# output field: 0 means even 1 means odd					Without "**I**" option
DISPC_DATA0	106*	O	B0	B0	B0	B0	B2	Always available
DISPC_DATA1	108*	O	B1	B1	B1	B1	B3	Always available
DISPC_DATA2	110*	O	B2	B2	B2	B2	B4	Always available
DISPC_DATA3	112*	O	B3	B3	B3	B3	B5	Always available
DISPC_DATA4	116*	O	G0	B4	B4	B4	B6	Always available
DISPC_DATA5	118*	O	G1	G0	B5	B5	B7	Always available
DISPC_DATA6	120*	O	G2	G1	G0	B6	B8	Always available
DISPC_DATA7	122*	O	G3	G2	G1	B7	B9	Always available
DISPC_DATA8	124*	O	R0	G3	G2	G0	G2	Always available
DISPC_DATA9	126*	O	R1	G4	G3	G1	G3	Always available
DISPC_DATA10	128*	O	R2	G5	G4	G2	G4	Always available
DISPC_DATA11	130*	O	R3	R0	G5	G3	G5	Always available
DISPC_DATA12	134*	O		R1	R0	G4	G6	Always available
DISPC_DATA13	136*	O		R2	R1	G5	G7	Always available
DISPC_DATA14	138*	O		R3	R2	G6	G8	Always available
DISPC_DATA15	140*	O		R4	R3	G7	G9	Always available
DISPC_DATA16	94*	O			R4	R0	R2	Always available
DISPC_DATA17	92*	O			R5	R1	R3	Always available

DISPC_DATA18	142*	O				R2	R4	Always available
DISPC_DATA19	144*	O				R3	R5	Always available
DISPC_DATA20	146*	O				R4	R6	Always available
DISPC_DATA21	148*	O				R5	R7	Always available
DISPC_DATA22	74*	O				R6	R8	Always available
DISPC_DATA23	76*	O				R7	R9	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.2.2 Remote Frame buffer interface (RFBI)

The RFBI interface can be used to drive data from LCD1, LCD2 or LCD outputs of DISPC T54 (see Figure 3 above). The interface supports the following features:

- MIPI DBI protocol support.
- 8, 9, 12 and 16-bit parallel interface.
- Programmable pixel memory formats
- Programmable output formats on one or multiple cycles per pixel.

Please refer to OMAP5432 reference manual for detailed information on the RFBI interface.

Table 8 Parallel Display Interface signals

Signal Name	Pin #	Type	Description	Availability
RFBI_RE	98*	O	Read access signal	Always available
RFBI_WE	102*	O	Write access signal	Always available
RFBI_A0	104*	O	Command/Data selection signal	Always available
RFBI_CS0	100*	O	Chip select signal for LCD	Always available
RFBI_TE_VSYNC0	94*	I	Tearing effect synchronization signal (TE or VSYNC for LCD panel 1)	Always available
RFBI_HSYNC0	92*	I	HSYNC from LCD panel	Always available
RFBI_DATA0	106*	IO	RFBI I/O Data 0	Always available
RFBI_DATA1	108*	IO	RFBI I/O Data 1	Always available
RFBI_DATA2	110*	IO	RFBI I/O Data 2	Always available
RFBI_DATA3	112*	IO	RFBI I/O Data 3	Always available
RFBI_DATA4	116*	IO	RFBI I/O Data 4	Always available
RFBI_DATA5	118*	IO	RFBI I/O Data 5	Always available
RFBI_DATA6	120*	IO	RFBI I/O Data 6	Always available
RFBI_DATA7	122*	IO	RFBI I/O Data 7	Always available
RFBI_DATA8	124*	IO	RFBI I/O Data 8	Always available
RFBI_DATA9	126*	IO	RFBI I/O Data 9	Always available
RFBI_DATA10	128*	IO	RFBI I/O Data 10	Always available
RFBI_DATA11	130*	IO	RFBI I/O Data 11	Always available
RFBI_DATA12	134*	IO	RFBI I/O Data 12	Always available
RFBI_DATA13	136*	IO	RFBI I/O Data 13	Always available
RFBI_DATA14	138*	IO	RFBI I/O Data 14	Always available
RFBI_DATA15	140*	IO	RFBI I/O Data 15	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.2.3 LVDS Display interface

The LVDS interface can be used to transmit either LCD1 or LCD2 data of OMAP5432 DISPC (see Figure 3 above). The LVDS interface available with CM-T54 is derived by converting the MIPI-DSI data originating from OPMAP5432 into LVDS compatible data. The conversion is achieved by a

MIPI-DSI to LVDS bridge component populated onboard CM-T54. The bridge component supports the following features:

- Supports 18bpp and 24bpp DSI video packets with RGB666 and RGB888 formats.
- Max resolution up to 60fps WUXGA 1920x1200 at 18bpp and 24bpp color with reduced blanking.
- LVDS output clock range of 25MHz – 154MHz.

The bridge component can send pixel data in one of the following formats (software configurable).

Figure 4 LVDS Data format A – 18bpp

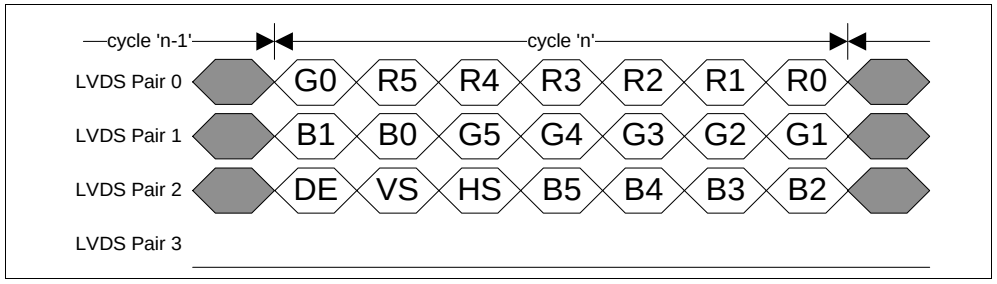


Figure 5 LVDS Data format B – 18bpp (24bpp source to 18bpp display)

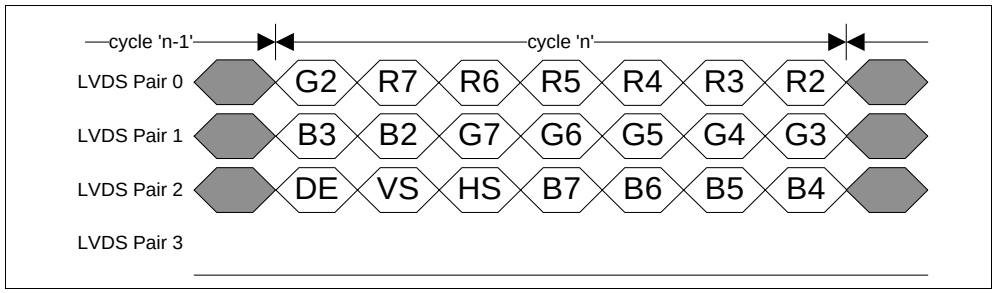


Figure 6 LVDS Data format C – 24bpp option 1

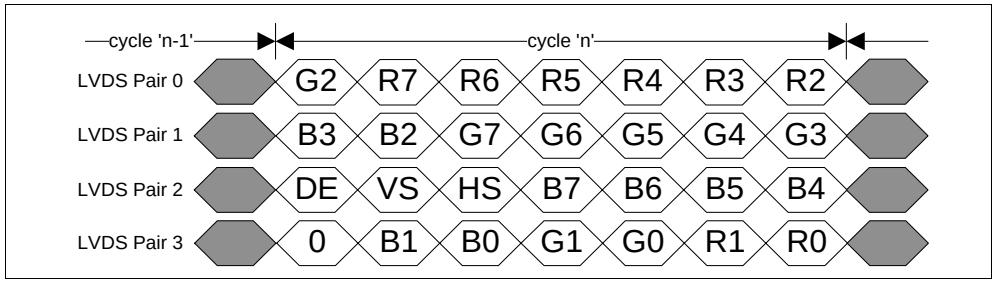


Figure 7 LVDS Data format D – 24bpp option 2

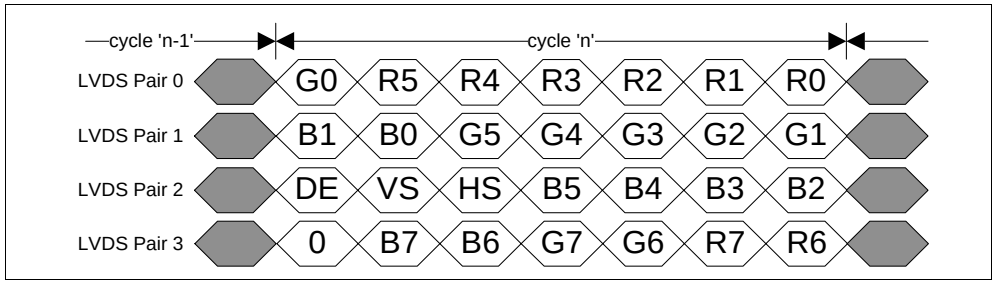


Table 9 LVDS Display Interfaces signals

Signal Name	Pin #	Type	Description	Availability
LVDS_CLK_N	35	AO	Differential clock pair	Only with "**L**" option
LVDS_CLK_P	33	AO		
LVDS_TX0_N	41	AO	Differential data 0 pair	Only with "**L**" option
LVDS_TX0_P	39	AO		
LVDS_TX1_N	47	AO	Differential data 1 pair	Only with "**L**" option
LVDS_TX1_P	45	AO		
LVDS_TX2_N	53	AO	Differential data 2 pair	Only with "**L**" option
LVDS_TX2_P	51	AO		
LVDS_TX3_N	59	AO	Differential data 3 pair	Only with "**L**" option
LVDS_TX3_P	57	AO		

4.2.4 MIPI Display Interface

The MIPI Display interface included with CM-T54 is derived from the MIPI-DSI protocol engine and the MIPI-DSI PHY integrated into the OMAP5432 SoC. The MIPI-DSI port can be used to transmit either LCD1 or LCD2 data of OMAP5432 DISPC (see Figure 3 above). The MIPI DSI interface supports the following main features:

- Up-to four data-configurable lanes in addition to one clock lane.
- Video mode and command mode support
- Bidirectional data link support for command mode (only one data lane is used in reverse direction)
- RGB16, RGB18 nonpacked, and RGB24 format support for command mode
- RGB16, RGB18 packed and nonpacked, and RGB24 format support for video mode.
- Burst for video mode
- Maximum data rate of 1256Mbps per data pair for four data lane configuration (627.75MHz)
- Data splitter for 2, 3 and 4-date lane configurations.

Please refer to OMAP5432 reference manual for detailed information on the MIPI-DSI interface.

Table 10 MIPI Display Interface signals

Signal Name	Pin #	Type	Description	Availability
DSIPORTA_LANE0Y	35	IO	1st lane (serial data/clock)	Without "**L**" option
DSIPORTA_LANE0X	33	IO		
DSIPORTA_LANE1Y	41	IO	2nd lane (serial data/clock)	Without "**L**" option
DSIPORTA_LANE1X	39	IO		
DSIPORTA_LANE2Y	47	IO	3rd lane (serial data/clock)	Without "**L**" option
DSIPORTA_LANE2X	45	IO		
DSIPORTA_LANE3Y	53	IO	4th lane (serial data/clock)	Without "**L**" option
DSIPORTA_LANE3X	51	IO		
DSIPORTA_LANE4Y	59	IO	5th lane (serial data only)	Without "**L**" option
DSIPORTA_LANE4X	57	IO		
DSIPORTA_TE0	75*	I	DSI1 tearing effect (TE) input 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.2.5 HDMI port

Please refer to chapter 4.5 of this document for detailed description of HDMI port.

4.3 Camera Interfaces

CM-T54 Camera interfaces are derived from the OMAP5432 imaging subsystem (ISS). The OMAP5432 imaging subsystem deals with the processing of the pixel data coming from an external image sensor, data from memory (image format encoding and decoding can be done to and from memory) or from the IVA-HD subsystem. The ISS external image sensor interfaces include three serial camera interfaces and a single parallel camera interface.

4.3.1 Parallel Camera Interface

The parallel camera interface available with CM-T54 supports the following features:

- 8bit, 12bit or 16bit input data bus.
- Interface Clock frequency of up to 148.5MPix/s
- Configurable pixel clock polarity
- BT656 and SYNC mode (HS, VS, FIELD, WEN)

Please refer to OMAP5432 reference manual for detailed information on the parallel camera interface.

Table 11 Parallel Camera Interface signals

Signal Name	Pin #	Type	Description	Availability
CAM_STROBE	93*	O	Flash strobe control signal	Always available
CAM_SHUTTER	81*	O	Mechanical shutter control signal	Always available
	99*			Always available
CAM_GLOBALRESET		IO	Camera global reset release signal	Always available
CPI_FID		IO	Pixel clock field signal	Always available
CPI_PCLK	95*	I	Pixel clock input	Always available
CPI_WEN	97*	I	Write enable signal input	Always available
CPI_VSYNCIN	113*	I	Vertical frame synchronization	Always available
CPI_HSYNCIN	115*	I	Horizontal frame synchronization	Always available
CPI_DATA0	101*	I	Input data 0	Always available
CPI_DATA1	103*	I	Input data 1	Always available
CPI_DATA2	89*	I	Input data 2	Always available
CPI_DATA3	91*	I	Input data 3	Always available
CPI_DATA4	77*	I	Input data 4	Always available
CPI_DATA5	79*	I	Input data 5	Always available
CPI_DATA6	83*	I	Input data 6	Always available
CPI_DATA7	85*	I	Input data 7	Always available
CPI_DATA8	107*	I	Input data 8	Always available
CPI_DATA9	109*	I	Input data 9	Always available
CPI_DATA10	121*	I	Input data 10	Always available
CPI_DATA11	119*	I	Input data 11	Always available
CPI_DATA12	73*	I	Input data 12	Always available
	131*			Always available
CPI_DATA13	61*	I	Input data 13	Always available
	133*			Always available
CPI_DATA14	67*	I	Input data 14	Always available
	127*			Always available
CPI_DATA15	125*	I	Input data 15	Always available
	194*			Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.3.2 MIPI camera interfaces MIPI-CSI

OMAP5432 is equipped with three on-chip instances of MIPI D-PHY / SMIA CCP2 compliant PHY receivers. Serial pixel data sourced from a compliant image sensor is sent over the MIPI-CSI interface, de-serialized by the MIPI D-PHY receiver block and re-sent into the OMAP5432 ISS. The following main features are supported:

- Maximum data rate of 1.5Gbps per lane
- Data merger for 2, 3 or 4 data lane configuration
- All primary and secondary MIPI defined formats

Please refer to OMAP5432 reference manual for detailed information on the MIPI-CSI / SMIA CCP2 camera interfaces.

Table 12 MIPI Camera Interface signals

Signal Name	Pin #	Type	Description	Availability
MIPI-CSI-A				
CSIPORTA_LANE0X	95*	I	Differential clock positive input	Always available
CSIPORTA_LANE0Y	97*	I	Differential clock negative input	Always available
CSIPORTA_LANE1X	103*	I	Differential data positive input	Always available
CSIPORTA_LANE1Y	101*	I	Differential data negative input	Always available
CSIPORTA_LANE2X	91*	I	Differential data positive input	Always available
CSIPORTA_LANE2Y	89*	I	Differential data negative input	Always available
CSIPORTA_LANE3X	77*	I	Differential data positive input	Always available
CSIPORTA_LANE3Y	79*	I	Differential data negative input	Always available
CSIPORTA_LANE4X	83*	I	Differential data positive input	Always available
CSIPORTA_LANE4Y	85*	I	Differential data negative input	Always available
MIPI-CSI-B				
CSIPORTB_LANE0X	131*	I	Differential clock positive input	Always available
CSIPORTB_LANE0Y	133*	I	Differential clock negative input	Always available
CSIPORTB_LANE1X	125*	I	Differential data positive input	Always available
CSIPORTB_LANE1Y	127*	I	Differential data negative input	Always available
CSIPORTB_LANE2X	113*	I	Differential data positive input	Always available
CSIPORTB_LANE2Y	115*	I	Differential data negative input	Always available
MIPI-CSI-B				
CSIPORTC_LANE0X	109*	I	Differential clock positive input	Always available
CSIPORTC_LANE0Y	107*	I	Differential clock negative input	Always available
CSIPORTC_LANE1X	119*	I	Differential data positive input	Always available
CSIPORTC_LANE1Y	121*	I	Differential data negative input	Always available
Discrete control signals (common to all camera interfaces)				
CAM_STROBE	93*	O	Flash strobe control signal	Always available
CAM_SHUTTER	81*	O	Mechanical shutter control signal	Always available
	99*			Always available
CAM_GLOBALRESET		IO	Camera global reset release signal	Always available

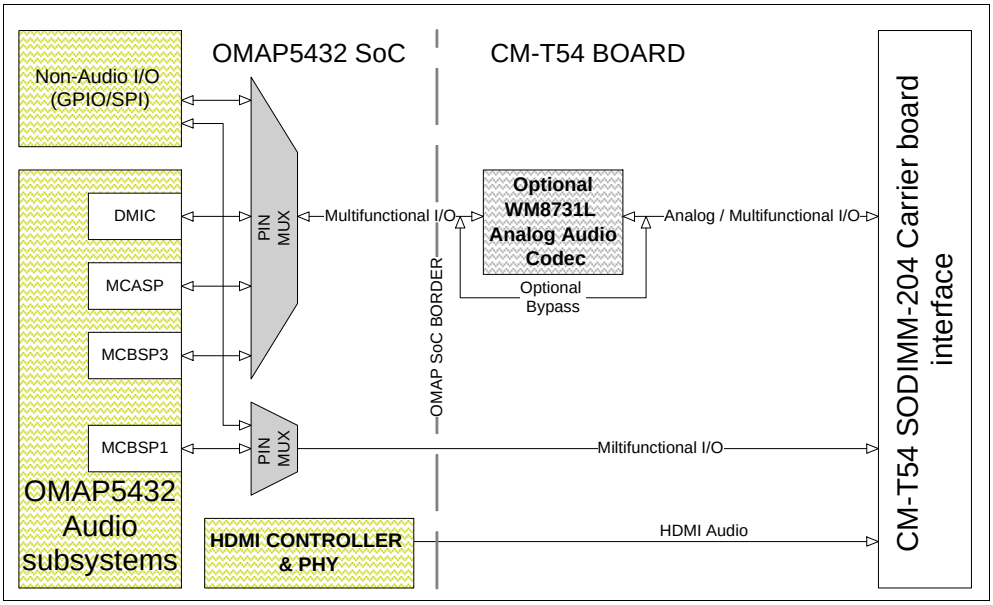
NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.4 Audio Subsystem

The following audio interfaces are available with CM-T54:

- Analog audio interface, including stereo in, stereo out and an analog microphone (Optional)
- Dedicated digital audio interfaces including McBSP, McASP (partial) and Digital microphone interface.
- HDMI Audio.

Figure 8 Audio Subsystem



4.4.1 Analog Audio CODEC

The CM-T54 analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with OMAP5432 McBSP3 interface. The Wolfson WM8731L supports the following features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

The analog audio interface implementation is illustrated in Figure 8 above.

Table 13 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted, (see Notes 1 and 2 below)			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB

Parameter	Test conditions	Min	Typ	Max	Unit
	Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVpp		45		
Programmable gain	1 kHz output	-73	0	6	dB
Programmable-gain step size	1 kHz		1		dB
Mute attenuation	1 kHz output, 0dB		80		dB
Line Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2 below)	A-weighted, 0dB gain, Fsample = 48 kHz.	85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.		90		
Dynamic range, (see note 3 below)	A-weighted, −60-dB full-scale input	85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain		-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVpp		45		
ADC Channel Separation	1 kHz input tone		90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω	-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic		1.5		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance	12 dB input gain	10	15		kΩ
	0 dB input gain	20	30		
Input capacitance			10		pF
Microphone Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2)	A-weighted, 0-dB gain		85		dB
Dynamic range, (see Note 3)	A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion,	0dB input, 0dB gain		-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVpp		45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,		14		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance			10		kΩ
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

For additional details, please refer to the Wolfson WM8731L datasheet.

Table 14 Analog Audio signals

Signal Name	Pin #	Type	Description	Availability
HP_OUT_R	201	AO	Right channel headphone output	Only with "**A**" option
HP_OUT_L	203	AO	Left channel headphone output	Only with "**A**" option
LINEIN_R	197	AI	Right channel line input	Only with "**A**" option
LINEIN_L	199	AI	Left channel line input	Only with "**A**" option
MIC_IN	193	AI	Microphone input	Only with "**A**" option
MIC_BIAS	191	AP	Electret microphone bias supply	Only with "**A**" option

NOTE: The analog audio codec and interface are only available with the 'A' configuration option.

4.4.2 Digital Audio Interfaces

4.4.2.1 McBSP interface

CM-T54 is equipped with two Multi-channel Buffered Serial Ports (McBSP). The McBSP provides a full-duplex direct serial interface between OMAP5432 and other application devices (such as a digital base band), audio and voice codec, etc. McBSP can accommodate a wide range of peripherals and clocked frame oriented protocols. The following main features are supported:

- Full Duplex communication
- Direct interface to I2S compliant, PCM and TDM bus devices
- Support for 8, 12, 16, 20, 24 and 32 bit data sizes.
- Bit Reordering support (send/receive LSB)
- Independent clocking and framing for receive/transmit up to 48MHz.
- External clock and frame sync signals support
- Configurable frame sync and clock signals polarity

McBSP integration within CM-T54 is illustrated in Figure 8 above. Please refer to OMAP5432 reference manual for detailed information on the McBSP interface.

Table 15 McBSP signals

Signal Name	Pin #	Type	Description	Availability
McBSP1				
McBSP1_CLKX/R	137*	IO	Transmit/Receive clock (direction is software configurable)	Always available
McBSP1_DR	143*	I	Serial data receive	Always available
McBSP1_DX	139*	O	Serial data transmit	Always available
McBSP1_FSX/R	145*	IO	Transmit/Receive frame sync (direction is configurable)	Always available
McBSP3				
McBSP3_CLKX	199*	IO	Transmit/Receive clock (direction is configurable)	Without "**A**" option
McBSP3_DR	203*	I	Serial data receive	Without "**A**" option
McBSP3_DX	197*	O	Serial data transmit	Without "**A**" option
McBSP3_FSX	201*	IO	Transmit/Receive frame sync (direction is software configurable)	Without "**A**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.4.2.2 McASP interface

CM-T54 features a partial implementation of the Multi-channel Audio Serial Port (McASP). The McASP module can cooperate in both transmit and receive modes, it is useful for TDM, I2S and DIT (digital audio interface transmission) data. McASP can also operate as an S/PDIF source PHY. The following main features are supported:

- A 32-bit buffer for transmit/receive operations (either receive or transmit at a time).
- Dedicated transmit interrupt signal to MPU and DSP subsystems

- Dedicated transmit DMA request signal to MPU and DSP subsystems

McASP integration within CM-T54 is illustrated in Figure 8 above . Please refer to OMAP5432 reference manual for detailed information on the McASP interface.

Table 16 McASP signals

Signal Name	Pin #	Type	Description	Availability
McASP_ACLKR	143*	IO	Receive bit clock	Always available
McASP_ACLKX	139*	IO	Transmit bit clock	Always available
McASP_AFSR	137*	IO	Receive frame sync	Always available
McASP_AFSX	200*	IO	Transmit frame sync	Always available
McASP_AHCLKR	201*	IO	Receive high-frequency master clock	Without "**A**" option
McASP_AMUTEIN	145*	I	Mute in signal from external device	Always available
McASP_AXR	191*	IO	Audio transmit/receive data (OMAP5432 channel 0)	Without "**A**" option
	197*			Without "**A**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

NOTE: Part of McASP interface signals available with OMAP5432, are not accessible through the CM-T54 carrier board interface.

4.4.2.3 Digital Microphone Interface

CM-T54 digital microphone interface is derived from the OMAP5432 DMIC module interface. The DMIC module can support up to 6 digital microphones through the 6-wire DMIC serial interface. The following main features are supported by the DMIC module:

- 3 clock signals (same frequency, individually gateable) for all digital microphones.
- Up to 3 stereo or 6 mono digital microphones.
- Each data signal can support two microphones (working in clock phase opposition).
- Programmable output clock frequency (32×FS, 50×FS, 64×FS or 80×FS where FS=48KHz.)
- Programmable data sampling sensibility (rising or falling edge).
- One RX FIFO (16 words of 144bits)
- IRQ & DMA access to MPU & DSP.

DMIC integration within CM-T54 is illustrated in Figure 8 above. Please refer to OMAP5432 reference manual for detailed information on the DMIC module.

Table 17 Digital Microphone signals

Signal Name	Pin #	Type	Description	Availability
DMIC_CLK1	199*	O	Digital (stereo) microphone clock output 1	Without "**A**" option
DMIC_CLK2	145*	O	Digital (stereo) microphone clock output 2	Always available
DMIC_CLK3	139*	O	Digital (stereo) microphone clock output 3	Always available
DMIC_DIN1	201*	I	Digital (stereo) microphone data input 1	Without "**A**" option
DMIC_DIN2	197*	I	Digital (stereo) microphone data input 2	Without "**A**" option
DMIC_DIN3	203*	I	Digital (stereo) microphone data input 3	Without "**A**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.5 High-Definition Multimedia Interface (HDMI)

The HDMI interface available with CM-T54 is based on the HDMI module of the OMAP5432 SoC. The video data sourced into the HDMI module from the DISPC TV port (see Figure 3 above). The HDMI module supports the following standards & features:

- HDMI 1.4, HDCP 1.4 and DVI 1.0 compliant, includes support for 3D stereoscopic frame-packing formats of the HDMI v1.4 standard: 1080p24Hz, 720p50Hz, 720p60Hz + side-by-side half structure: 1080p60Hz).
- EIA/CEA-861-D video format support
- VESA DMT video format support
- Deep color mode support (12-bit and 10-bit deep-color component up to 1080p @60Hz).
- Up to 148.5MHz pixel clock (1920 × 1080p @ 60Hz)
- 24/30/36-bit RGB/YCbCr 4:4:4 (deep color) and 16/20/24-bit YCbCr 4:2:2 video formats.
- Uncompressed multichannel (up to 8 channels) audio (L-PCM) support
- Master I2C interface for display data channel (DDC connection)
- Consumer electronic control (CEC) interface
- Integrated high-bandwidth digital content protection (DES_HDCP) encryption engine to transmit protected content (authentication performed by SW).

Please refer to OMAP5432 reference manual for detailed information on the DMIC module.

Table 18 HDMI signals

Signal Name	Pin #	Type	Description	Availability
HDMI_CLK_DX	30	AO	TMDS clock pair	Always available
HDMI_CLK_DY	32	AO		Always available
HDMI_DATA0_DX	36	AO	TMDS data 0 pair	Always available
HDMI_DATA0_DY	38	AO		Always available
HDMI_DATA1_DX	42	AO	TMDS data 1 pair	Always available
HDMI_DATA1_DY	44	AO		Always available
HDMI_DATA2_DX	48	AO	TMDS data 2 pair	Always available
HDMI_DATA2_DY	50	AO		Always available
HDMI_CEC	34*	IO	Consumer Electronics Control signal	Always available
HDMI_HPD	40*	I	Hot Plug Detect signal, 5V tolerant.	Always available
HDMI_DDC_SCL	25*	IO	VESA Data Display Channel clock signal	Always available
HDMI_DDC_SDA	31*	IO	VESA Data Display Channel data signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.6 WLAN and Bluetooth

CM-T54 features 802.11b/g/n and Bluetooth 3.0 + HS wireless connectivity solution, implemented by interfacing the AzureWave AW-NH387 WLAN + Bluetooth combo controller module with the OMAP5432 WLSDIO (MMC-3) interface. The AW-NH387 is based on the Marvell 88W8787 chipset.

WLAN Standards supported:

- 802.11b: 1, 2, 5.5, 11Mbps
- 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11n up to 150Mbps

WLAN Security features:

- WAPI
- WEP 64-bit and 128-bit encryption with H/W TKIP processing
- WPA/WPA2 (Wi-Fi Protected Access)
- AES-CCMP hardware implementation as part of 802.11i security standard

Bluetooth standards supported:

- Bluetooth 2.1+EDR data rates of 1, 2 and 3 Mbps

Co-Existence:

- Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence

Antenna Connection

The AW-NH387 requires a single 2.4GHz antenna for WIFI & Bluetooth. The antenna is connected via the on-board UFL high frequency connector J1. Any type of 2.4GHz antenna can be used. Please refer to section 6.3 for connector location.

Table 19 J1 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 20 802.11b/g (WLAN) RF system specifications

Feature	Description
Frequency Band	2.4 GHz ISM radio band
Number of Channels	802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4, Japan – 14 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~13(2412~2472) 802.11n(HT40): Channel 3~11(2422~2462)
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM for WLAN GFSK (1Mbps), Π/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Medium Access Protocol	CSMA/CA with ACK
Receive Sensitivity	WLAN: 802.11b: Minimum -86+-2dBm at 11Mbps 802.11g: Minimum -71+-2dBm at 54Mbps 802.11n: Minimum -68+-2dBm at HT20 MCS7 Minimum -65+-2dBm at HT40 MCS7 Bluetooth: GFSK: typical -87dBm Π/4 DQPSK: typical -88dBm 8DPSK: typical -81dBm
Output Power	WLAN: 802.11b(Ch1~13): typical 17dBm +/- 2dBm 802.11b(Ch14): typical 10dBm +/- 2dBm 802.11g: typical 14dBm +/- 2dBm 802.11n: typical HT20 13dBm +/- 2dBm HT40 12dBm +/- 2dBm Bluetooth Bluetooth Class 1.5>1dBm

For additional details, please refer to the AzureWave AW-NH387 datasheet.

NOTE: The WLAN and Bluetooth module is available only with the 'WB' configuration option.

4.7 Ethernet

CM-T54 incorporates a full-featured 10/100 Ethernet interface. The interface is implemented with an HSIC interfaced LAN9730 controller with from SMSC.

The CM-T54 Ethernet interface supports the following main features:

- Fully compliant with IEEE 802.3/802.3u
- 10BASE-T and 100BASE-TX support.
- TCP/UDP/IP/ICMP checksum offload support.
- Full- and Half-duplex
- Flexible address filtering modes
- Wakeup packet support
- PHY support for auto negotiation
- PHY support for automatic polarity detection correction
- PHY support for HP Auto-MDIX
- Activity and speed indicator LED controls

Please refer to LAN9730 datasheet for additional information.

Table 21 Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
ETH_TXP	8	AIO	Differential transmit data pair	Only with "**E**" option
ETH_TXN	6	AIO		Only with "**E**" option
ETH_RXP	14	AIO	Differential receive data pair	Only with "**E**" option
ETH_RXN	12	AIO		Only with "**E**" option
ETH_CTAP	2	P	Magnetics central TAP voltage	Only with "**E**" option
ETH_LED1	4	OD^	Driven low when link is detected. When link activity is detected, drives high pulse (80mS).	Only with "**E**" option
ETH_LED2	16	OD^	Driven low when link speed is 100Mbps, Driven high during 10Mbps operation or during line isolation.	Only with "**E**" option
ETH_LED3	22	OD^	Driven low when full duplex operation is detected.	Only with "**E**" option

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

NOTE: Signal denoted with ^ are pulled to ETH_CTAP onboard CM-T54 with 50Ohm resistors.

4.8 USB interfaces

4.8.1 USB 3.0 On-The-Go

The USB 3.0 OTG interface is implemented with the combination of OMAP5432 super-speed USB OTG subsystem with the TWL6037 PMIC. The OMAP5432 integrated super-speed USB OTG

subsystem is comprised from a USB3.0 PHY compliant with USB3.0 specification rev1.0 and a USB3.0 OTG dual-role-device (DRD) link controller supporting the following modes:

- USB2.0 peripheral (function controller) in full and high speed (12 and 480 Mbps respectively)
- USB2.0 host in low, full and high-speed (1.5, 12 and 480 Mbps respectively) with one downstream port with split transaction support (allows multiple ports through a hub).
- USB3.0 peripheral (function controller) in super speed (5Gbps)
- USB3.0 host in super speed with one downstream port (allows multiple ports through a hub).

CM-T54 implementation of the USB3.0 OTG interface allows a CM-T54 based system to boot upon USB power source connection, draw system power from USB and charge the main battery from USB (appropriate circuitry such as charger must be implemented on carrier board). For additional information please refer to chapter 5.2.3 and 5.5 of this document.

Please refer to OMAP5432 reference manual for detailed information on the USB3 controller and PHY.

NOTE: The OMAP5432 implementation of USB3.0 OTG subsystem does not support the dynamic role switching, that is, OTG protocols HNP, SRP and ADP.

Table 22 USB 3.0 OTG interface signals

Signal Name	Pin #	Type	Description	Availability
USBD0_HS_DP	176*	AIO	USB2.0 OTG positive data	Always available
USBD0_HS_DM	178*	AIO	USB2.0 OTG negative data	Always available
USBD0_SS_RX	182	AI	USB3.0 OTG receive data positive	Always available
USBD0_SS_RY	184	AI	USB3.0 OTG receive data negative	Always available
USBD0_SS_TX	188	AO	USB3.0 OTG transmit data positive	Always available
USBD0_SS_TY	190	AO	USB3.0 OTG transmit data negative	Always available
USBOTG_ID	174*	AIO	USB OTG ID signal	Always available
VBUS_5V_OTG	180	P	VBUS Power input/output/sense. When USB-OTG is in HOST mode, CM-T54 sources 5V (up to 500mA) at this pin. When USB-OTG is in DEVICE mode, CM-T54 draws VBUS power from the USB host through this pin. **NOTE: CM-T54 can change power state upon voltage sensed through this pin. If not used, should be grounded.**	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.8.2 USB 2.0 Host

The CM-T54 high-speed USB interface is implemented with an optional HSIC interfaced USB3503 USB Hub from SMSC. The USB hub supports the following main features:

- Three USB 2.0 High Speed (480Mbps) compatible downstream ports
- Supports either Single-TT or Multi-TT configurations for Full-Speed (12Mbps) and Low-Speed (1.5Mbps) connections
- DP/DM ± 15kV ESD protection (air and contact discharge). IEC 61000-4-2 level 4 ESD protection without external devices.

Please refer to USB3503 datasheet for additional information.

Table 23 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
Host Port-1				
USB1_DP	172	AIO	USB host port 1 positive data	Only with "**U4**" option
USB1_DN	170	AIO	USB host port 1 negative data	Only with "**U4**" option
Host Port-2				
USB2_DP	166	AIO	USB host port 2 positive data	Only with "**U4**" option
USB2_DN	164	AIO	USB host port 2 negative data	Only with "**U4**" option
Host Port-3				
USB3_DP	160	AIO	USB host port 3 positive data	Only with "**U4**" option
USB3_DN	158	AIO	USB host port 3 negative data	Only with "**U4**" option
Discrete control signals (common to all USB2.0 interfaces)				
VBUS_EN_REQ	156	O	Active high port power control output. Signals an external VBUS power supply to enable/disable VBUS for all ports.	Only with "**U4**" option
VBUS_nOVC	162	I	Active low over current sense input. Indicates that an overcurrent condition is detected by external VBUS supply.	Only with "**U4**" option

4.9 UARTs

Up to 4 UART ports are available with CM-T54. All the UART ports are derived from the OMAP5432 SoC integrated UARTs and support the following features:

- 16C750 compatibility.
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter.
- Programmable interrupt trigger levels for FIFOs.
- Programmable baud rate up to 3.6864Mbps.
- Programmable parity (even, odd, and no parity).
- Programmable data size (5, 6, 7 or 8 bits)
- Programmable stop bits (1, 1.5 or 2bits)
- Hardware flow control (RTS/CTS) or software (XON/XOFF)

While all UART interfaces are similar, only UART3 module features IrDA and CIR modes operation capabilities.

The following IrDA (UART3 only) features are supported:

- IrDA 1.4 slow (SIP), medium (MIR) and fast infrared (FIR) communications.
- Uplink/downlink CRC generation/detection
- Asynchronous transparency (automatic insertion of break character)
- Programmable baud rate up-to 4Mbps.

The following CIR (UART3 only) features are supported:

- Transmit mode only (receive mode is not supported).
- Free data forma (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency

- 1/2, 5/2, 1/3 or 1/4 carrier duty cycle.

Please refer to OMAP5432 reference manual for detailed information on the integrated UART controllers.

Table 24 UART signals

Signal Name	Pin #	Type	Description	Availability
UART-1				
UART1_TX	73*	O	UART-1 serial data transmit	Always available
UART1_RX	67*	I	UART-1 serial data receive	Always available
UART1_CTS	61*	O	UART-1 clear to send.	Always available
UART1_RTS	194*	I	UART-1 request to send.	Always available
UART-2				
UART2_TX	3*	O	UART-2 serial data transmit	Always available
UART2_RX	5*	I	UART-2 serial data receive	Always available
UART2_CTS	7*	O	UART-2 clear to send.	Always available
UART2_RTS	9*	I	UART-2 request to send	Always available
UART-3				
UART3_TX_IRTX	178*	O	UART-3 serial / IrDA data transmit	Always available
	157*			Always available
	110*			Always available
UART3_RX_IRRX	176*	I	UART-3 serial / IrDA data receive	Always available
	147*			Always available
	108*			Always available
UART3_CTS_RCTX	60*	O	UART-3 clear to send / CIR RC	Always available
UART3_RTS_IRSD	62*	I	UART-3 request to send /CIR SD/MODE	Always available
UART-5				
UART5_TX	151*	O	UART-5 serial data transmit	Always available
UART5_RX	153*	I	UART-5 serial data receive	Always available
UART5_CTS	155*	O	UART-5 clear to send.	Always available
UART5_RTS	149*	I	UART-5 request to send.	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.10 RS232

The CM-T54 incorporates a single RS232 port. The following features are supported:

- Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Programmable baud rate of up to 500 kbit/s
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART-4 of OMAP5432.

Please refer to OMAP5432 reference manual for detailed information on UART4.

NOTE: The RS232 port operates at RS232 voltage levels.

Table 25 RS232 signals

Signal Name	Pin #	Type	Description	Availability
RS232_TXD	117	O	RS232 serial data out	Always available
RS232_RXD	111	I	RS232 serial data in	Always available

4.11 MMC / SD / SDIO

The CM-T54 features 3 MMC / SD / SDIO host interfaces implemented with the OMAP5432 integrated MMC/SDIO host controller modules. The following main features are supported by MMC/SDIO modules:

- Full compliance with SD command/response sets as defined in SD physical layer specification V3.01.
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v3.00.
- Full compliance with SD host controller standard specification sets as defined in the SD card specification part A2 v3.00.
- The interfaces support SD v3.0 data transfer rates of up to 48Mbps (at 1.8V).
- Software configurable 3.3V and 1.8V operation (MMC-1 only).
- Up-to 4-bit transfer modes.

Each MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

The MMC-1 can operate in both 3.3V and 1.8V voltage levels (software configurable). This is a bootable interface, meaning CM-T54 can download initial boot software (such as u-boot) from an SD/MMC card over the MMC-1 interface.

The MMC-2 interface is used for the onboard eMMC storage and is not available through the CM-T54 carrier board interface.

The MMC-3 operates only at 1.8V levels. The interface is (optionally) used for CM-T54 WLAN and Bluetooth functionality ("WB" product option). In case the "WB" option is not populated on-board CM-T54, the interface is accessible through the carrier board interface.

The MMC-4 operates only at 1.8V levels and is always accessible through the carrier board interface.

Please refer to OMAP5432 reference manual for detailed information on the integrated MMC/SDIO host controller modules.

NOTE: MMC/SDIO modules implemented by OMAP5432 slightly differ from the SD card specification. Please refer to OMAP5432 for full differences coverage.

NOTE: 33Ω serial resistors must be populated on the MMC-1 (SDCARD) interface signals if used on the carrier board. Please refer to SB-T54 for SDCARD interface reference design.

Table 26 MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description	Availability
MMC-1 (SDCARD)				
SDCARD_CLK	80*	O	Interface clock	Always available
SDCARD_CMD	82*	IO	Command signal	Always available
SDCARD_DATA0	84*	IO	Card data bit 0	Always available
SDCARD_DATA1	86*	IO	Card data bit 1	Always available
SDCARD_DATA2	88*	IO	Card data bit 2	Always available
SDCARD_DATA3	90*	IO	Card data bit 3	Always available
SDCARD_CD	61*	I	Active low card detection signal	Always available
SDCARD_WP	67*	I	Active low write protection signal	Always available
	194*			Always available
MMC-3 (WLSDIO)				
WLSDIO_CLK	54*	O	Interface clock	Without "**WB**" option

Signal Name	Pin #	Type	Description	Availability
WLSDIO_CMD	56*	IO	Command signal	Without "**WB**" option
WLSDIO_DATA0	11*	IO	Card data bit 0	Without "**WB**" option
WLSDIO_DATA1	13*	IO	Card data bit 1	Without "**WB**" option
WLSDIO_DATA2	15*	IO	Card data bit 2	Without "**WB**" option
WLSDIO_DATA3	17*	IO	Card data bit 3	Without "**WB**" option
MMC-4 (SDIO4)				
SDIO4_CLK	157*	O	MMC3 Interface clock	Always available
SDIO4_CMD	147*	IO	Command signal	Always available
SDIO4_DATA0	155*	IO	Card data bit 0	Always available
SDIO4_DATA1	153*	IO	Card data bit 1	Always available
SDIO4_DATA2	151*	IO	Card data bit 2	Always available
SDIO4_DATA3	149*	IO	Card data bit 3	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.12 Touch-Screen

CM-T54 features an optional on-board resistive touch-screen controller. The controller is communicating with the OMAP5432 SoC over the McSPI-2 interface. The interface supports 4-wire touch panels and is available through the CM-T54 carrier board interface.

Table 27 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_XP	66	AIO	Touch screen X+ (right)	Only with "**I**" option
TS_XN	68	AIO	Touch screen X- (left)	Only with "**I**" option
TS_YP	70	AIO	Touch screen Y+ (top)	Only with "**I**" option
TS_YN	72	AIO	Touch screen Y- (bottom)	Only with "**I**" option

4.13 Keypad

The CM-T54 CoM features a 9x9 matrix keypad interface derived from the keyboard module (KBD) included with the OMAP5432 SoC. The KBD supports the following features:

- Event detection on key press and key release
- Multikey-press detection and decoding
- Long-key detection on prolonged key press (duration of long-key press is reconfigurable on-the fly)
- Key press repeat timing reconfigurable on-the-fly
- Programmable interrupt generation on key events

Please refer to OMAP5432 reference manual for detailed information on the integrated keyboard controller module.

Table 28 Keypad signals

Signal Name	Pin #	Type	Description	Availability
KBD_ROW0	148*	SPU	Row 0 feed	Always available
KBD_ROW1	74*	SPU	Row 1 feed	Always available
KBD_ROW2	76*	SPU	Row 2 feed	Always available
KBD_ROW3	126*	SPU	Row 3 feed	Always available
KBD_ROW4	104*	SPU	Row 4 feed	Always available
KBD_ROW5	94*	SPU	Row 5 feed	Always available
KBD_ROW6	134*	SPU	Row 6 feed	Always available
KBD_ROW7	130*	SPU	Row 7 feed	Always available

Signal Name	Pin #	Type	Description	Availability
KBD_ROW8	128*	SPU	Row 8 feed	Always available
KBD_COL0	142*	O	Column 0 feed, active low	Always available
KBD_COL1	144*	O	Column 1 feed, active low	Always available
KBD_COL2	146*	O	Column 2 feed, active low	Always available
KBD_COL3	124*	O	Column 3 feed, active low	Always available
KBD_COL4	98*	O	Column 4 feed, active low	Always available
KBD_COL5	92*	O	Column 5 feed, active low	Always available
KBD_COL6	140*	O	Column 6 feed, active low	Always available
KBD_COL7	138*	O	Column 7 feed, active low	Always available
KBD_COL8	136*	O	Column 8 feed, active low	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.14 GPIO

Up to 106 GPIO signals are available with CM-T54. Most of the available GPIOs are derived from the OMAP5432 integrated General-Purpose Interface. OMAP5432 GPIOs are divided into 8 blocks with 32 GPIOs in each block (a total of 8 x 32 = 256 GPIOs). The OMAP5432 GPIO signals can be configured for the following applications:

- Data input / output
- Keyboard interface with a debounce cell
- Interrupt generation (in ACTIVE power state)
- Wake-up request generation when idle

Please refer to OMAP5432 reference manual for detailed information on the integrated General-Purpose Interface.

NOTE: GPIO[n]_WK[m] signals are "always-on" GPIOs, meaning these GPIO signals are active even while the OMAP5432 is in low power state.

NOTE: Not all GPIO signals supported by the OMAP5432 SoC are available through the CM-T54 carrier board interface.

Table 29 GPIO availability

Signal name	Pin #	Type	Availability	Notes
GPIO1_WK12	193*	IO	Without "**A**" option	Wakeable GPIO
GPIO1_WK6	152*	IO	Always available	Wakeable GPIO
GPIO1_WK7	154*	IO	Always available	Wakeable GPIO
GPIO3_84	9*	IO	Always available	
GPIO3_85	7*	IO	Always available	
GPIO3_86	5*	IO	Always available	
GPIO3_87	3*	IO	Always available	
GPIO4_100	199*	IO	Always available	
GPIO4_101	145*	IO	Always available	
GPIO4_102	139*	IO	Always available	
GPIO4_103	137*	IO	Always available	
GPIO4_104	143*	IO	Always available	
GPIO4_107	200*	IO	Always available	
GPIO4_96	191*	IO	Without "**A**" option	
GPIO4_97	201*	IO	Without "**A**" option	
GPIO4_98	197*	IO	Without "**A**" option	
GPIO4_99	203*	IO	Without "**A**" option	

Signal name	Pin #	Type	Availability	Notes
GPIO5_128	54*	IO	Without "**WB**" option	
GPIO5_129	56*	IO	Without "**WB**" option	
GPIO5_130	11*	IO	Without "**WB**" option	
GPIO5_131	13*	IO	Without "**WB**" option	
GPIO5_132	15*	IO	Without "**WB**" option	
GPIO5_133	17*	IO	Without "**WB**" option	
GPIO5_134	153*	IO	Always available	
GPIO5_135	151*	IO	Always available	
GPIO5_136	155*	IO	Always available	
GPIO5_137	149*	IO	Always available	
GPIO5_138	43*	IO	Always available	
GPIO5_139	49*	IO	Always available	
GPIO5_140	69*	IO	Always available	
GPIO5_141	63*	IO	Always available	
GPIO5_142	65*	IO	Always available	
GPIO5_143	58*	IO	Always available	
GPIO5_144	52*	IO	Always available	
GPIO5_153	60*	IO	Always available	
GPIO5_154	62*	IO	Always available	
GPIO5_155	157*	IO	Always available	
GPIO5_156	147*	IO	Always available	
GPIO6_160	92*	IO	Always available	
GPIO6_161	94*	IO	Always available	
GPIO6_162	102*	IO	Always available	
GPIO6_163	100*	IO	Always available	
GPIO6_164	98*	IO	Always available	
GPIO6_165	104*	IO	Always available	
GPIO6_166	106*	IO	Always available	
GPIO6_167	108*	IO	Always available	
GPIO6_168	110*	IO	Always available	
GPIO6_169	112*	IO	Always available	
GPIO6_170	116*	IO	Always available	
GPIO6_171	118*	IO	Always available	
GPIO6_172	120*	IO	Always available	
GPIO6_173	122*	IO	Always available	
GPIO6_174	124*	IO	Always available	
GPIO6_175	126*	IO	Always available	
GPIO6_176	128*	IO	Always available	
GPIO6_177	130*	IO	Always available	
GPIO6_178	134*	IO	Always available	
GPIO6_179	136*	IO	Always available	
GPIO6_180	138*	IO	Always available	
GPIO6_181	140*	IO	Always available	
GPIO6_182	142*	IO	Always available	
GPIO6_183	144*	IO	Always available	
GPIO6_184	146*	IO	Always available	
GPIO6_185	148*	IO	Always available	
GPIO6_186	74*	IO	Always available	
GPIO6_187	76*	IO	Always available	
GPIO6_189	75*	IO	Always available	
GPIO7_192	34*	IO	Always available	
GPIO7_193	40*	IO	Always available	
GPIO7_194	25*	IO	Always available	
GPIO7_195	31*	IO	Always available	
GPIO7_196	68*	IO	Without "**I**" option	
GPIO7_197	66*	IO	Without "**I**" option	
GPIO7_198	70*	IO	Without "**I**" option	
GPIO7_199	72*	IO	Without "**I**" option	
GPIO7_200	161*	IO	Always available	
GPIO7_201	163*	IO	Always available	
GPIO8_224	81*	IO	Always available	
GPIO8_225	93*	IO	Always available	
GPIO8_226	99*	IO	Always available	
GPIO8_227	73*	IO	Always available	
GPIO8_228	61*	IO	Always available	
GPIO8_229	67*	IO	Always available	
GPIO8_230	194*	IO	Always available	

Signal name	Pin #	Type	Availability	Notes
GPIO8_231	129*	IO	Always available	
GPIO8_232	135*	IO	Always available	
GPIO8_IN236	95*	I	Always available	Input Only
GPIO8_IN237	97*	I	Always available	Input Only
GPIO8_IN238	101*	I	Always available	Input Only
GPIO8_IN239	103*	I	Always available	Input Only
GPIO8_IN240	89*	I	Always available	Input Only
GPIO8_IN241	91*	I	Always available	Input Only
GPIO8_IN242	77*	I	Always available	Input Only
GPIO8_IN243	79*	I	Always available	Input Only
GPIO8_IN244	83*	I	Always available	Input Only
GPIO8_IN245	85*	I	Always available	Input Only
GPIO8_IN246	131*	I	Always available	Input Only
GPIO8_IN247	133*	I	Always available	Input Only
GPIO8_IN248	127*	I	Always available	Input Only
GPIO8_IN249	125*	I	Always available	Input Only
GPIO8_IN250	115*	I	Always available	Input Only
GPIO8_IN251	113*	I	Always available	Input Only
GPIO8_IN252	107*	I	Always available	Input Only
GPIO8_IN253	109*	I	Always available	Input Only
GPIO8_IN254	121*	I	Always available	Input Only
GPIO8_IN255	119*	I	Always available	Input Only

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.15 I²C

The CM-T54 features three general purpose I²C interfaces. The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s), fast mode (up to 400K bits/s) and HS mode (up to 3.4Mbps)
- 7-bit and 10-bit device addressing modes
- Programmable multi-slave channel (responds to four separate addresses)

The I²C interfaces are implemented with OMAP5432 integrated HS I²C controllers. Please refer to OMAP5432 reference manual for detailed information on the integrated HS I²C controllers.

Table 30 I²C signals

Signal Name	Pin #	Type	Description	Availability
I²C-2				
I2C2_SDA	49*	SPU/SPD	I²C serial data line	Always available
I2C2_SCL	43*	SPU/SPD	I²C serial clock line	Always available
I²C-3				
I2C3_SDA	135*	SPU/SPD	I²C serial data line	Always available
I2C3_SCL	129*	SPU/SPD	I²C serial clock line	Always available
I²C-4				
I2C4_SDA	163*	SPU/SPD	I²C serial data line	Always available
I2C4_SCL	161*	SPU/SPD	I²C serial clock line	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.16 SPI

CM-T54 features four SPI ports. All CM-T54 SPI ports are derived from the OMAP5432 integrated Multichannel Serial Port Interface (McSPI). McSPI modules support the following main features:

- Master/Slave operation support
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to 2 master channels or a single slave channel per port
- Full/Half duplex
- Transmit only/receive only/transmit-and-receive modes
- Two DMA requests per channel
- Start-bit mode support

Please refer to OMAP5432 reference manual for detailed information on the integrated Multichannel Serial Port Interfaces.

Table 31 SPI signals

Signal Name	Pin #	Type	Description	Availability
SPI-1				
MCSPI1_CLK	66*	IO	SPI-1 Master clock out; slave clock in	Always available
MCSPI1_CS0	58*	IO	SPI-1 Chip select 0	Always available
MCSPI1_CS1	52*	IO	SPI-1 Chip select 1	Always available
MCSPI1_MOSI	65*	IO	SPI-1 Master data out; slave data in	Always available
MCSPI1_MISO	63*	IO	SPI-1 Master data in; slave data out	Always available
SPI-2				
MCSPI2_CLK	66*	IO	SPI-2 Master clock out; slave clock in	Without "**I**" option
MCSPI2_CS0	68*	IO	SPI-2 Chip select 0	Without "**I**" option
MCSPI2_CS1	140*	IO	SPI-2 Chip select 1	Always available
MCSPI2_SIMO	70*	IO	SPI-2 Master data out; slave data in	Without "**I**" option
MCSPI2_SOMI	72*	IO	SPI-2 Master data in; slave data out	Without "**I**" option
SPI-3				
MCSPI3_CLK	3*	IO	SPI-3 Master clock out; slave clock in	Always available
MCSPI3_CS0	7*	IO	SPI-3 Chip select 0	Always available
MCSPI3_SIMO	5*	IO	SPI-3 Master data out; slave data in	Always available
MCSPI3_SOMI	9*	IO	SPI-3 Master data in; slave data out	Always available
SPI-4				
MCSPI4_CLK	54*	IO	SPI-4 Master clock out; slave clock in	Without "**WB**" option
MCSPI4_CS0	15*	IO	SPI-4 Chip select 0	Without "**WB**" option
MCSPI4_SIMO	11*	IO	SPI-4 Master data out; slave data in	Without "**WB**" option
MCSPI4_SOMI	13*	IO	SPI-4 Master data in; slave data out	Without "**WB**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.17 General Purpose Timers and PWM

CM-T54 features 11 timers derived from the OMAP5432 integrated General-Purpose. The following features are supported:

- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal.
- Interrupts generated on overflow, compare and capture
- Free-running 32-bit upward counter

- Autoreload mode
- Start/stop mode
- Programmable divider clock source (1 to 256)
- On-The-Fly read/write register (while counting)

Software can configure the timer signals available through CM-T54 carrier board interface to act as either an "EVENT CAPTURE" input or a "PWM" output of the respective OMAP5432 timer.

Please refer to OMAP5432 reference manual for detailed information on the integrated General Purpose timers.

NOTE: Not all timers available with OMAP5432 are accessible through the CM-T54 carrier board interface.

Table 32 GP Timers and PWM signals

Signal Name	Pin #	Type	Description	Availability
TIMER5_PWM_EVT	61*	IO	Timer5 event capture (input) or PWM5 output	Always available
TIMER6_PWM_EVT	67*	IO	Timer6 event capture (input) or PWM6 output	Always available
TIMER8_PWM_EVT	73*	IO	Timer8 event capture (input) or PWM8 output	Always available
TIMER11_PWM_EVT	194*	IO	Timer11 event capture (input) or PWM11 output	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.18 HDQ / 1-Wire

The HDQ/1-Wire interface available with CM-T54 is derived from the HDQ1W module integrated into OMAP5432. The HDQ1W module implements the hardware protocol of the master functions of the TI/Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols.

The following main features are supported:

- Benchmark HDQ protocol
- Dallas Semiconductor 1-Wire® protocol
- Power-down mode
- 5Kbps communication rate
- 128byte address space

Please refer to OMAP5432 reference manual for detailed information on the HDQ/1-Wire interface.

Table 33 HDQ / 1-Wire signals

Signal Name	Pin #	Type	Description	Availability
HDQ_SIO	62*	OD	Serial data input/output	Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.6 of this document.

4.19 General Purpose ADC (GPADC)

CM-T54 is equipped with a general purpose 12-bit sigma-delta ADC combined with a 16-input analog multiplexer. The ADC functionality is derived from the GPADC module of TWL6037 power management companion of OMAP5432. The GPADC allows CM-T54 to monitor a variety of analog signals using analog-to-digital conversion on the input source. After the conversion completes, the TWL6037 can inform OMAP5432 that data is ready by generating an interrupt.

Ten of the available inputs are used internally by the TWL6037. Three of the inputs are accessible through the CM-T54 carrier board interface. The reference voltage GPADC_VREF is supplied to external components to improve measurement accuracy.

Please refer to TWL6037 reference manual for detailed information on GPADC.

Table 34 GPADC signals

Signal Name	Pin #	Type	Description	Availability
GPADC_VREF	62	P	GPADC output reference voltage	Always available
GPADC_IN0	175	AI	GPADC input 0	Always available
GPADC_IN1	173	AI	GPADC input 1	Always available
GPADC_IN2	169	AI	GPADC input 2	Always available

4.20 General purpose clock

CM-T54 features a general purpose, software configurable clock output signal. The signal is derived from the OMAP5432 SCRM module. The clock polarity, source frequency and divider are fully configurable. Please refer to OMAP5432 reference manual for detailed information on the SCRM module.

Table 35 General purpose clock signal

Signal Name	Pin #	Type	Description	Availability
FREF_CLK0_OUT	193*	O	OMAP5432 auxiliary clock output 0 signal.	Without "**A**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.21 JTAG

The CM-T54 JTAG interface is derived from the OMAP5432 integrated Debug interface. The following features and standards are supported:

- Five standard IEEE1149.1 JTAG signals: nTRST, TCK, TMS, TDI and TDO.
- Partial support for IEEE1149.7 features.
- A return clock (RTCK) due to the clocking requirements of the ARM968 processor

- Two EMU[1:0] TI extensions. For 14pin JTAG header.

Please refer to OMAP5432 reference manual for detailed information on the integrated debug interface.

Table 36 JTAG signals

Signal Name	Pin #	Type	Description	Availability
JTAG_TCK	90*	I	Test clock (pulled down)	Always available
JTAG_RTCK	80*	O	Returned test clock (synchronized)	Always available
JTAG_TDO	82*	O	Test data out (pulled up)	Always available
JTAG_TDI	84*	I	Test data in (pulled up)	Always available
JTAG_TMSC	88*	IO	TMS - Test mode select (pulled up) TMSC - Test mode control and data scan (pulled up)	Always available
JTAG_nTRST	86*	I	Test reset (pulled down)	Always available
DRM_EMU0	152*	IO	Emulation 0 (pulled up)	Always available
DRM_EMU1	154*	IO	Emulation 1 (pulled up)	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

5 SYSTEM LOGIC

CM-T54 allows access to several system logic related signals through the carrier board interface. Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Supply

The CM-T54 supports two power supply options:

- Regulated DC supply (5V Typical).
- Lithium-ion polymer battery.

CM-T54 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board.

Table 37 Power signals

Signal Name	Type	Description
VSYS	P	Main power supply. Connect either to a regulated DC supply (5V Typ.) or directly to a Lithium-ion polymer battery.
PMID	P	In a battery powered design where the TI BQ2xxxx series battery charges are used, this pin should be connected to the charger PMID pin. Otherwise this pin can be connected to VSYS.
VCC_RTC	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Short to GND if RTC back-up is not required.
GND	P	Common ground.

5.2 Power Management

CM-T54 employs several power management techniques implemented by the combination of OMAP5432 SoC with the TWL6037 onboard Power Management IC (PMIC). Software can control power delivery to most of the CM-T54 onboard peripherals by communicating with the TWL6037 PMIC. The OMAP5432 internal power consumption is controlled by a dedicated on-chip Power, Reset and Clock Management subsystem (PRCM) which is capable of gating power & clocks to on-chip peripherals as well as controlling power and clock functions derived from TWL6037 PMIC (through the integrated SmartReflex framework). The PRCM, based on the SmartReflex framework, supports the following features:

- Dynamic clock gating
- Dynamic voltage and frequency scaling (DVFS)
- Dynamic power switching (DPS)
- Static leakage management (SLM)
- Adaptive body bias (ABB)

5.2.1 Power Resources & control signals.

The term “power resource” refers to every power rail generated onboard CM-T54 as well as some of the signals controlled by TWL6037 PMIC. Power rails generated by the carrier board can also be considered as power resources provided their enable/disable logic is controlled by CM-T45 power resource signal (PMIC_REGEN1). Most power resources are only used onboard the CM-T54 CoM and are not accessible through the carrier board interface.

A power resource is always in one of three states:

- OFF state - The power resource is not operating.

- MODE_ACTIVE state - The power resource is operating in a mode defined by the MODE_ACTIVE bits of the respective resource control register in TWL6037.
- MODE_SLEEP state - The power resource is operating in a mode defined by the MODE_SLEEP bits of the respective resource control register in TWL6037.

Transition of a power resource between MODE_SLEEP and MODE_ACTIVE states can only be triggered when the resource is assigned (by software) to one or both control signals (all resources are not assigned by default). When a resource is assigned to a control signal, the resource power-state will follow the logical value of the control signal. A resource can be assigned to one or both control signals. A resource assigned to both control signals will only enter MODE_SLEEP state in case both signals request that, the resource will exit MODE_SLEEP when any of the control signals indicates MODE_ACTIVE.

Table 38 Resource control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_ENABLE_1	171	I	A power resource control signal allowing carrier board components to control power-resources of TWL6037. **NOTE:** no TWL6037 power resources are assigned to PMIC_ENABLE_1 by default.	Always available
NSLEEP	N/A	N/A	This signal is not available through the carrier board interface. This signal is driven by OMAP5432 SoC and sensed by (is an input to) TWL6037 PMIC, allowing OMAP5432 to trigger TWL6037 power resources transition into MODE_SLEEP state. **NOTE:** no TWL6037 power resources are assigned to NSLEEP by default.	Always available

Table 39 Power resource signals accessible from carrier board

Signal Name	Pin #	Type	Description	Availability
PMIC_REGEN1	171	O	This signal is a TWL6037 power-resource. It can be assigned to one/both resource control signals and be used to enable/disable carrier board power supplies and peripherals upon a request from carrier board, or when CM-T54 transitions between power states. **Leave floating if not used.**	Always available

5.2.2 CM-T54 Power states

CM-T54 power state is defined by the state of all CM-T54 power-resources.

The following power states are supported by CM-T54 (derived from TWL6037 power states)

Table 40 CM-T54 Power States

CM-T54 State Name	Default Power Resources state	State Description
NO SUPPLY	OFF	All of the following inputs are below valid voltage range (threshold): VSYS, VCC_RTC, PMID, VAC_DETECT and VBUS_5V_OTG.
BACKUP	OFF	CM-T54 is not powered by a valid supply (VSYS < 2.75V), while any of the following conditions apply: 1. BKBAT > POR (POR threshold is between 2.0V and 2.5V) 2. VBUS_5V_OTG > VBUS_DET (VBUS_DET threshold is between 2.9V and 3.6V). 3. VAC_DETECT > VAC_DET (VAC_DET threshold is between 2.9V and 3.6V).
OFF	OFF (except RTC power)	CM-T54 is powered by a valid supply (VSYS > 2.75V), and it is waiting for an ON-request or condition. All CM-T54 power resources (except RTC power) are in the OFF state.
ACTIVE	MODE_ACTIVE	CM-T54 is powered by a valid supply (VSYS > 2.75V), and CM-T54 has transitioned to an ACTIVE state upon an ON-request or NSLEEP signal negation. All CM-T54 power resources are in their MODE_ACTIVE state.

CM-T54 State Name	Default Power Resources state	State Description
SLEEP	MODE_ACTIVE	CM-T54 is powered by a valid supply (VSYS > 2.75V), and the NSLEEP resource control signal assertion has triggered transition to SLEEP mode. **Note:** Power resources assigned to the NSLEEP resource control signal (none by default) will enter MODE_SLEEP state.

5.2.3 Power-On & Power-Off

CM-T54 first boot sequence (first transition from OFF to ACTIVE state) starts as soon main power rail (VSYS) becomes available.

5.2.3.1 ON, OFF requests and gating conditions

CM-T54 will transition from ACTIVE or SLEEP to OFF state upon an OFF request. An OFF request is a condition upon which the TWL6037 PMIC executes a power-state transition sequence resulting in CM-T54 transition to OFF state. Some OFF requests have software configurable parameters.

When CM-T54 is in OFF state, only a non-gated/non-masked ON-request will trigger transition to ACTIVE state. Software can pre-define (mask/unmask and configure) some of the ON-requests before CM-T54 transitions from ACTIVE or SLEEP states to OFF state.

Table 41 ON-requests effective by default.

Request Name	Description
PWRON	While CM-T54 is in the OFF state, This request is registered if the system senses a short low pulse (Tpulse > 15mS) on the PMIC_PWRON pin of the carrier board interface. While CM-T54 is either in the ACTIVE or SLEEP states, This request is registered by means of an interrupt when CM-T54 detects a falling edge on the PMIC_PWRON signal of the carrier board interface.
VBAT_MON	Triggered when battery voltage crosses the 3.4V threshold. Battery voltage (vs. GND) is monitored through the VBAT_SENSE pin of the carrier board interface.
VAC_OK	Triggered when voltage on VAC_DETECT signal crosses (up/down) the VAC_DET threshold. The VAC_DET threshold is between 2.9V and 3.6V when rising, between 2.8V and 3.3V when falling.
SHORT	Triggered in case one or more of CM-T54 onboard power resources detects an over-current and under-voltage condition. A thermal event on some of the power resources can also trigger this interrupt.
VBUS	Triggered when voltage on VBUS_5V_OTG pin of carrier board interface rises above VBUS_DET threshold. VBUS_DET threshold is between 2.9V and 3.6V when rising. **Note: Transition to ACTIVE state upon this request is delayed by 1 second during which CM-T54 draws power only from the PMID carrier board pin.**
OTG_OVV_CH	Triggered upon an over-voltage condition on the VBUS_5V_OTG pin of carrier board interface.

Table 42 On-Request gating conditions.

Request Name	Description
VSYS_HI	This conditions applies if the voltage available on the VSYS power rail is less than 3.2V
HOTDIE	This condition applies if TWL6037 device temperature exceeds threshold. The threshold is software selectable. Default value for the threshold is between 118ºC and 141ºC when rising, between 108ºC and 132ºC when falling.
RESET	This condition applies when the COLD_RESET_IN signal is asserted.

Table 43 OFF-requests effective by default.

Request Name	Description
PWRON_LPK	A long (12sec by default) assertion of the PMIC_PWRON signal, causes CM-T54 to transition into OFF state.

Request Name	Description
THERMAL SHUTDOWN	This condition applies if TWL6037 device temperature exceeds thermal shutdown threshold. CM-T54 transitions into OFF state upon this request. Thermal shutdown threshold is between 136ºC and 160ºC when rising, between 126ºC and 150ºC when falling.
RESET	This condition applies when the COLD_RESET_IN signal is asserted. CM-T54 transitions into OFF state, and immediately executes transition to ACTIVE state, effectively causing a cold reset to the system.
SW_RST	This condition applies whenever software writes a logic 1 into the SW_RST field of TWL6037 FUNC_PMU_CONTROL register. By default, CM-T54 transitions into OFF state, and immediately executes transition to ACTIVE state, effectively causing a cold reset to the system.
DEV_ON	This condition applies whenever software writes a logic 0 into the DEV_ON field of TWL6037 FUNC_PMU_CONTROL register. By default, CM-T54 transitions into OFF state.
VSYS_LO	This condition applies whenever voltage on the VSYS power rail is falling below 2.75V.

NOTE: Table 41 and Table 43 only describe requests effective by default. Software may change effective requests, change thresholds and add additional requests. For detailed information on start-up events and ON/OFF/SLEEP/WAKE requests please refer to TWL6037 documentation.

5.2.3.2 ON, OFF and gating signals active by default

The following signals are sources of ON, OFF and gating conditions by default

Table 44 ON, OFF and Gating signals active by default

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. If Asserted, serves as an ON Gating condition.	Always available
VBAT_SENSE	179	AI	Allows CM-T54 to directly sense main battery voltage. ON and OFF requests can be triggered upon voltage sensed through this signal. **NOTE: short to VSYS if not used.**	Always available
VAC_DETECT	181	AI	Allows CM-T54 to directly sense DC power source. ON and OFF requests can be triggered upon voltage sensed through this signal. **NOTE: short to GND if not used.**	Always available
PMIC_PWRON	165	I	Pulled-Up Active low PWRON signal (designed for an ON/OFF switch). ON and OFF requests can be triggered upon voltage sensed through this signal. VSYS referenced logic. **NOTE: leave floating if not used.**	Always available
VBUS_5V_OTG	180	AI	VBUS Power input/output/sense. ON requests can be triggered upon voltage sensed through this signal. **NOTE: short to GND if not used.**	Always available
VSYS	multiple	P	Main system power input and sense. If VSYS voltage is too low (<3.2V), serves as an ON Gating condition	Always available

5.3 Reset

CM-T54 supports two reset signals: cold reset input (COLD_RESET_IN) and warm reset input/output (SYS_nRESWARM).

- Cold reset is an input to the TWL6037 PMIC, which triggers a full logic reset to CM-T54. Cold reset is a global reset that affects every module on the device. The cold reset assertion also causes SYS_nRESWARM assertion.
- Warm reset is also a global reset, but it does not affect all the modules on the device. Usually, the device does not require a complete reboot on a warm reset.

The COLD_RESET_IN signal should be used as the main system reset.

Table 45 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset	Always available
SYS_nRESWARM	187	IO	Active low reset signal, triggered by asserting cold reset	Always available

5.4 Boot Sequence

CM-T54 boot sequence defines which interface/media is used by CM-T54 to load and execute the initial software (such as U-boot). CM-T54 can load initial software from following interfaces/media:

- The on-board eMMC device.
- A USB host using the USB3.0 OTG port (CM-T54 acts as a USB device)
- An external SATA drive using the SATA interface.
- An external SD/MMC card using the MMC-1 (SDCARD) interface.

CM-T54 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CM-T54:

- Standard sequence: Designed for normal system operation with the on-board eMMC device as the boot media.
- Alternate sequence: Designed to bypass the eMMC device. Using the alternate sequence allows CM-T54 to boot from external devices such as SATA drive and external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 46 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Boot sequence selector signal. Leave floating or low for standard boot sequence.	Always available

Table 47 CM-T54 Boot sequences

Boot sequence	ALT_BOOT	First device	Second device	Third device
Standard	Low or floating	Onboard eMMC	USB OTG Host	N/A
Alternate	High	External SATA Drive	External SD card	USB OTG Host

5.5 Battery & Charger signals

CM-T54 can be used as part of a battery powered device. The signals described in this section define system behavior in some of the special cases that apply to battery powered devices.

Using USB wall adapters to recharge the main battery is a very common approach. In many cases, effective battery charging is possible only while the system is active (after boot). Charging the battery in a scenario where the main battery is fully discharged and the system is powered off must be taken

into consideration. While CM-T54 requires more than 100mA current for successful boot, the USB specification limits initial current from a USB host (before USB device initialization) to 100mA.

NOTE: Initial VBUS current limitation to 100mA (if desired) must be implemented on carrier board

The PMID and USB_PSEL signals allow CM-T54 based designs to overcome the above scenario. Once the USB charger is connected to the system, a VBUS On-request is detected by CM-T54. Upon a VBUS On-request, CM-T54 delays system boot by 1sec. During this 1st second, CM-T54 draws power only from the PMID pin.

This approach allows CM-T54 to enable only the USB charger detection subsystem before drawing power from VSYS (which is sourced from the 100mA limited VBUS). In case a USB charger is detected, CM-T54 can assert the USB_PSEL signal, to remove the 100mA current limit, allowing CM-T54 to boot while still complying with the USB specification.

Figure 9 Booting upon VBUS detection with discharged battery (example)

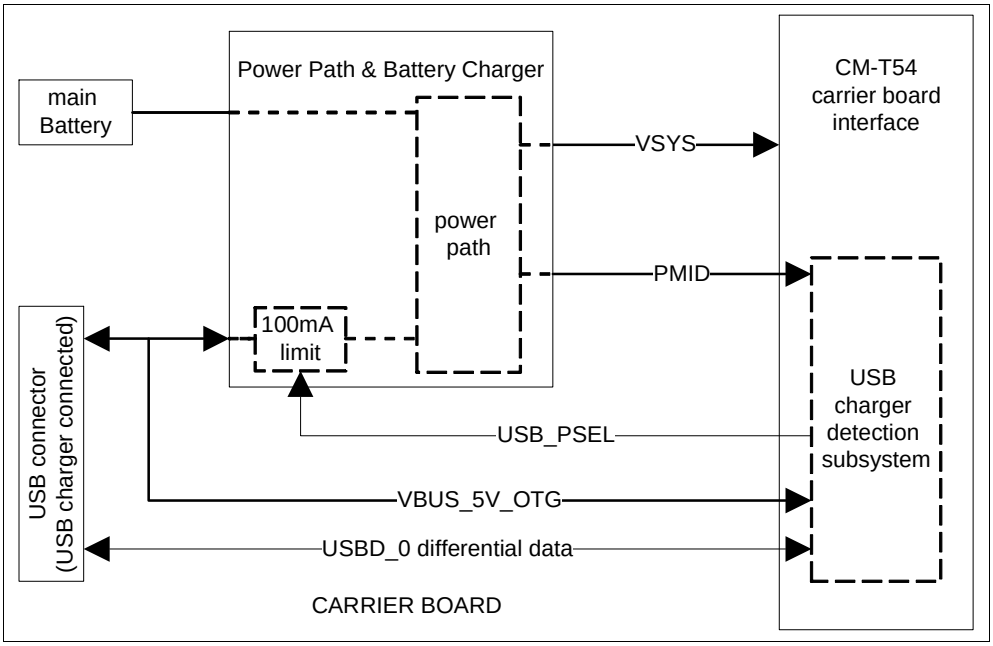


Table 48 PMID & USB_PSEL signals

Signal Name	Pin #	Type	Description	Availability
PMID	196	PI	Allow proper transition of CM-T54 from OFF to ACTIVE state upon a USB charger connection to the VBUS_5V_OTG signal (in case the main battery is either discharged or disconnected). **NOTE: Leave USB_PSEL floating if not used.** **NOTE: Short PMID to VSYS if not used.**	Always available
USB_PSEL	192	IO		Always available

5.6 Signal Multiplexing Characteristics

Up to 114 of the CM-T54 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CM-T54 CoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 8 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CM-T54 pins are derived from the OMAP5432 SoC control module.

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode must be considered as a "RESERVED" function and must not be used.

For additional details, please refer to the OAMP5432 reference manual.

Table 49 Multifunctional Signals

Pin #	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7	Availability
3	UART2_TX	MCSPI3_CLK					GPIO3_87	SAFE_MODE	Always available
5	UART2_RX	MCSPI3_SIMO					GPIO3_86	SAFE_MODE	Always available
7	UART2_CTS	MCSPI3_CS0					GPIO3_85	SAFE_MODE	Always available
9	UART2_RTS	MCSPI3_SOMI					GPIO3_84	SAFE_MODE	Always available
11	WLSDIO_DATA0	MCSPI4_SIMO					GPIO5_130	SAFE_MODE	Without "**WB**" option
13	WLSDIO_DATA1	MCSPI4_SOMI					GPIO5_131	SAFE_MODE	Without "**WB**" option
15	WLSDIO_DATA2	MCSPI4_CS0					GPIO5_132	SAFE_MODE	Without "**WB**" option
17	WLSDIO_DATA3						GPIO5_133	SAFE_MODE	Without "**WB**" option
25	HDMI_DDC_SCL						GPIO7_194	SAFE_MODE	Always available
31	HDMI_DDC_SDA						GPIO7_195	SAFE_MODE	Always available
34	HDMI_CEC						GPIO7_192	SAFE_MODE	Always available
40	HDMI_HPD						GPIO7_193	SAFE_MODE	Always available
43	I2C2_SCL						GPIO5_138	SAFE_MODE	Always available
49	I2C2_SDA						GPIO5_139	SAFE_MODE	Always available
52	MCSPI1_CS1						GPIO5_144	SAFE_MODE	Always available
54	WLSDIO_CLK	MCSPI4_CLK					GPIO5_128	SAFE_MODE	Without "**WB**" option
56	WLSDIO_CMD						GPIO5_129	SAFE_MODE	Without "**WB**" option
58	MCSPI1_CS0						GPIO5_143	SAFE_MODE	Always available
60	UART3_CTS_RCTX	SATA_ACTLED					GPIO5_153	SAFE_MODE	Always available
61	TIMER5_PWM_EVT	SDCARD_CD	UART1_CTS	CPI_DATA13			GPIO8_228	SAFE_MODE	Always available
62	UART3_RTS_IRSD	HDQ_SIO					GPIO5_154	SAFE_MODE	Always available
63	MCSPI1_SOMI						GPIO5_141	SAFE_MODE	Always available
65	MCSPI1_SIMO						GPIO5_142	SAFE_MODE	Always available
66	MCSPI2_CLK						GPIO7_197	SAFE_MODE	Without "**T**" option
67	TIMER6_PWM_EVT	SDCARD_WP	UART1_RX	CPI_DATA14			GPIO8_229	SAFE_MODE	Always available
68	MCSPI2_CS0			DISPC_FID			GPIO7_196	SAFE_MODE	Without "**T**" option
69	MCSPI1_CLK						GPIO5_140	SAFE_MODE	Always available
70	MCSPI2_SIMO						GPIO7_198	SAFE_MODE	Without "**T**" option
72	MCSPI2_SOMI						GPIO7_199	SAFE_MODE	Without "**T**" option
73	TIMER11_PWM_EVT		UART1_TX	CPI_DATA12			GPIO8_227	SAFE_MODE	Always available
74	GPIO6_186			DISPC_DATA22	KBD_ROW1		GPIO6_186	SAFE_MODE	Always available
75	DSIPORTA_TE0						GPIO6_189	SAFE_MODE	Always available
76	GPIO6_187			DISPC_DATA23	KBD_ROW2		GPIO6_187	SAFE_MODE	Always available
77	CSIPORTA_LANE3X			CPI_DATA4			GPIO8_IN242	SAFE_MODE	Always available
79	CSIPORTA_LANE3Y			CPI_DATA5			GPIO8_IN243	SAFE_MODE	Always available
80	SDCARD_CLK			JTAG_RTCK				SAFE_MODE	Always available
81	CAM_SHUTTER						GPIO8_224	SAFE_MODE	Always available
82	SDCARD_CMD			JTAG_TDO				SAFE_MODE	Always available
83	CSIPORTA_LANE4X			CPI_DATA6			GPIO8_IN244	SAFE_MODE	Always available
84	SDCARD_DATA0			JTAG_TDI				SAFE_MODE	Always available
85	CSIPORTA_LANE4Y			CPI_DATA7			GPIO8_IN245	SAFE_MODE	Always available
86	SDCARD_DATA1			JTAG_NTRST				SAFE_MODE	Always available
88	SDCARD_DATA2			JTAG_TMSC				SAFE_MODE	Always available
89	CSIPORTA_LANE2Y			CPI_DATA2			GPIO8_IN240	SAFE_MODE	Always available
90	SDCARD_DATA3			JTAG_TCK				SAFE_MODE	Always available
91	CSIPORTA_LANE2X			CPI_DATA3			GPIO8_IN241	SAFE_MODE	Always available
92	RFBI_HSYNC0			DISPC_DATA17	KBD_COL5		GPIO6_160	SAFE_MODE	Always available
93	CAM_STROBE						GPIO8_225	SAFE_MODE	Always available
94	RFBI_TE_VSYNC0			DISPC_DATA16	KBD_ROW5		GPIO6_161	SAFE_MODE	Always available
95	CSIPORTA_LANE0X			CPI_PCLK			GPIO8_IN236	SAFE_MODE	Always available
97	CSIPORTA_LANE0Y			CPI_WEN			GPIO8_IN237	SAFE_MODE	Always available
98	RFBI_RE			DISPC_PCLK	KBD_COL4		GPIO6_164	SAFE_MODE	Always available
99	CAM_GLOBALRESET	CAM_SHUTTER		CPI_FID			GPIO8_226	SAFE_MODE	Always available
100	RFBI_CS0			DISPC_HSYNC			GPIO6_163	SAFE_MODE	Always available
101	CSIPORTA_LANE1Y			CPI_DATA0			GPIO8_IN238	SAFE_MODE	Always available
102	RFBI_WE			DISPC_VSYNC			GPIO6_162	SAFE_MODE	Always available
103	CSIPORTA_LANE1X			CPI_DATA1			GPIO8_IN239	SAFE_MODE	Always available
104	RFBI_A0			DISPC_DE	KBD_ROW4		GPIO6_165	SAFE_MODE	Always available
106	RFBI_DATA0			DISPC_DATA0			GPIO6_166	SAFE_MODE	Always available
107	CSIPORTC_LANE0Y			CPI_DATA8			GPIO8_IN252	SAFE_MODE	Always available
108	RFBI_DATA1			DISPC_DATA1	UART3_RX_IRRX		GPIO6_167	SAFE_MODE	Always available
109	CSIPORTC_LANE0X			CPI_DATA9			GPIO8_IN253	SAFE_MODE	Always available
110	RFBI_DATA2			DISPC_DATA2	UART3_TX_IRTX		GPIO6_168	SAFE_MODE	Always available

Pin #	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7	Availability
112	RFBI_DATA3			DISPC_DATA3			GPIO6_169	SAFE_MODE	Always available
113	CSIPORTB_LANE2X				CPI_VSYNCIN		GPIO8_IN251	SAFE_MODE	Always available
115	CSIPORTB_LANE2Y				CPI_HSYNCIN		GPIO8_IN250	SAFE_MODE	Always available
116	RFBI_DATA4			DISPC_DATA4			GPIO6_170	SAFE_MODE	Always available
118	RFBI_DATA5			DISPC_DATA5			GPIO6_171	SAFE_MODE	Always available
119	CSIPORTC_LANE1X			CPI_DATA11			GPIO8_IN255	SAFE_MODE	Always available
120	RFBI_DATA6			DISPC_DATA6			GPIO6_172	SAFE_MODE	Always available
121	CSIPORTC_LANE1Y			CPI_DATA10			GPIO8_IN254	SAFE_MODE	Always available
122	RFBI_DATA7			DISPC_DATA7			GPIO6_173	SAFE_MODE	Always available
124	RFBI_DATA8			DISPC_DATA8	KBD_COL3		GPIO6_174	SAFE_MODE	Always available
125	CSIPORTB_LANE1X				CPI_DATA15		GPIO8_IN249	SAFE_MODE	Always available
126	RFBI_DATA9			DISPC_DATA9	KBD_ROW3		GPIO6_175	SAFE_MODE	Always available
127	CSIPORTB_LANE1Y				CPI_DATA14		GPIO8_IN248	SAFE_MODE	Always available
128	RFBI_DATA10			DISPC_DATA10	KBD_ROW8		GPIO6_176	SAFE_MODE	Always available
129	I2C3_SCL						GPIO8_231	SAFE_MODE	Always available
130	RFBI_DATA11			DISPC_DATA11	KBD_ROW7		GPIO6_177	SAFE_MODE	Always available
131	CSIPORTB_LANE0X				CPI_DATA12		GPIO8_IN246	SAFE_MODE	Always available
133	CSIPORTB_LANE0Y				CPI_DATA13		GPIO8_IN247	SAFE_MODE	Always available
134	RFBI_DATA12			DISPC_DATA12	KBD_ROW6		GPIO6_178	SAFE_MODE	Always available
135	I2C3_SDA						GPIO8_232	SAFE_MODE	Always available
136	RFBI_DATA13			DISPC_DATA13	KBD_COL8		GPIO6_179	SAFE_MODE	Always available
137		MCBSP1_CLKX		MCASP_AFSR			GPIO4_103	SAFE_MODE	Always available
138	RFBI_DATA14			DISPC_DATA14	KBD_COL7		GPIO6_180	SAFE_MODE	Always available
139	DMIC_CLK3	MCBSP1_DX		MCASP_ACLKX			GPIO4_102	SAFE_MODE	Always available
140	RFBI_DATA15	MCSPI2_CS1		DISPC_DATA15	KBD_COL6		GPIO6_181	SAFE_MODE	Always available
142	GPIO6_182			DISPC_DATA18	KBD_COL0		GPIO6_182	SAFE_MODE	Always available
143		MCBSP1_DR		MCASP_ACLKR			GPIO4_104	SAFE_MODE	Always available
144	GPIO6_183			DISPC_DATA19	KBD_COL1		GPIO6_183	SAFE_MODE	Always available
145	DMIC_CLK2	MCBSP1_FSX		MCASP_AMUTEIN			GPIO4_101	SAFE_MODE	Always available
146	GPIO6_184			DISPC_DATA20	KBD_COL2		GPIO6_184	SAFE_MODE	Always available
147	UART3_RX_IRRX				SDIO4_CMD		GPIO5_156	SAFE_MODE	Always available
148	GPIO6_185			DISPC_DATA21	KBD_ROW0		GPIO6_185	SAFE_MODE	Always available
149	UART5_RTS				SDIO4_DATA3		GPIO5_137	SAFE_MODE	Always available
151	UART5_TX				SDIO4_DATA2		GPIO5_135	SAFE_MODE	Always available
152	DRM_EMU0						GPIO1_WK6	SAFE_MODE	Always available
153	UART5_RX				SDIO4_DATA1		GPIO5_134	SAFE_MODE	Always available
154	DRM_EMU1						GPIO1_WK7	SAFE_MODE	Always available
155	UART5_CTS				SDIO4_DATA0		GPIO5_136	SAFE_MODE	Always available
157	UART3_TX_IRTX				SDIO4_CLK		GPIO5_155	SAFE_MODE	Always available
161	I2C4_SCL						GPIO7_200	SAFE_MODE	Always available
163	I2C4_SDA						GPIO7_201	SAFE_MODE	Always available
176	USBD0_HS_DP				UART3_RX_IRRX			SAFE_MODE	Always available
178	USBD0_HS_DM				UART3_TX_IRTX			SAFE_MODE	Always available
191				MCASP_AXR			GPIO4_96	SAFE_MODE	Without "**A**" option
193	FREF_CLK0_OUT						GPIO1_WK12	SAFE_MODE	Without "**A**" option
194	TIMER8_PWM_EVT	SDCARD_WP	UART1_RTS	CPI_DATA15			GPIO8_230	SAFE_MODE	Always available
197	DMIC_DIN2			MCASP_AXR	MCBSP3_DX		GPIO4_98	SAFE_MODE	Without "**A**" option
199	DMIC_CLK1				MCBSP3_CLKX		GPIO4_100	SAFE_MODE	Without "**A**" option
200	MCBSP2_FSX			MCASP_AFSX			GPIO4_107	SAFE_MODE	Always available
201	DMIC_DIN1			MCASP_AHCLKR	MCBSP3_FSX		GPIO4_97	SAFE_MODE	Without "**A**" option
203	DMIC_DIN3				MCBSP3_DR		GPIO4_99	SAFE_MODE	Without "**A**" option

5.7 RTC

The CM-T54 RTC is implemented with the internal RTC of the OMAP5432 SoC. The RTC provides time and calendar information.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present. The backup battery should be connected to the VCC_RTC power input.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

5.8 LED

The CM-T54 features a single general purpose green LED controlled by GPIO3_80 signal of the OMAP5432 SoC. The LED is ON when GPIO3_80 is set high.

6 CARRIER BOARD INTERFACE

The CM-T54 connects to the carrier board a SODIMM-204 edge connector.

6.1 Connector Pinout

Table 50 Connector P1

Pin #	CM-T54 Signal Name	Reference Section		Pin #	CM-T54 Signal Name	Reference Section
1	GND	5.1		2	ETH_CTAP	4.7
3	MCSPI3_CLK GPIO3_87 UART2_TX	4.16 4.14 4.9		4	ETH_LED1	4.7
5	MCSPI3_SIMO UART2_RX GPIO3_86	4.16 4.9 4.14		6	ETH_TXN	4.7
7	MCSPI3_CS0 UART2_CTS GPIO3_85	4.16 4.9 4.14		8	ETH_TXP	4.7
9	MCSPI3_SOMI UART2_RTS GPIO3_84	4.16 4.9 4.14		10	VSYS	5.1
11	MCSPI4_SIMO WLSDIO_DATA0 GPIO5_130	4.16 4.11 4.14		12	ETH_RXN	4.7
13	MCSPI4_SOMI WLSDIO_DATA1 GPIO5_131	4.16 4.11 4.14		14	ETH_RXP	4.7
15	MCSPI4_CS0 WLSDIO_DATA2 GPIO5_132	4.16 4.11 4.14		16	ETH_LED2	4.7
17	GPIO5_133 WLSDIO_DATA3	4.14 4.11		18	NOT CONNECTED	
19	GND	5.1		20	NOT CONNECTED	
21	SATA_TX	4.1		22	ETH_LED3	4.7
23	SATA_TY	4.1		24	NOT CONNECTED	
25	HDMI_DDC_SCL GPIO7_194	4.5 4.14		26	NOT CONNECTED	
27	SATA_RX	4.1		28	VSYS	5.1
29	SATA_RY	4.1		30	HDMI_CLK_DX	4.5
31	GPIO7_195 HDMI_DDC_SDA	4.14 4.5		32	HDMI_CLK_DY	4.5
33	LVDS_CLK_P DSIPORTA_LANE0X	4.2.3 4.2.4		34	GPIO7_192 HDMI_CEC	4.14 4.5
35	LVDS_CLK_N DSIPORTA_LANE0Y	4.2.3 4.2.4		36	HDMI_DATA0_DX	4.5
37	GND	5.1		38	HDMI_DATA0_DY	4.5
39	LVDS_TX0_P DSIPORTA_LANE1X	4.2.3 4.2.4		40	GPIO7_193 HDMI_HPD	4.14 4.5
41	LVDS_TX0_N DSIPORTA_LANE1Y	4.2.3 4.2.4		42	HDMI_DATA1_DX	4.5
43	GPIO5_138 I2C2_SCL	4.14 4.15		44	HDMI_DATA1_DY	4.5
45	LVDS_TX1_P DSIPORTA_LANE2X	4.2.3 4.2.4		46	VSYS	5.1
47	LVDS_TX1_N DSIPORTA_LANE2Y	4.2.3 4.2.4		48	HDMI_DATA2_DX	4.5
49	GPIO5_139 I2C2_SDA	4.14 4.15		50	HDMI_DATA2_DY	4.5
51	LVDS_TX2_P DSIPORTA_LANE3X	4.2.3 4.2.4		52	GPIO5_144 MCSPI1_CS1	4.14 4.16
53	LVDS_TX2_N DSIPORTA_LANE3Y	4.2.3 4.2.4		54	GPIO5_128 MCSPI4_CLK WLSDIO_CLK	4.14 4.16 4.11

Pin #	CM-T54 Signal Name	Reference Section	Pin #	CM-T54 Signal Name	Reference Section
55	GND	5.1	56	GPIO5_129 WLSDIO_CMD	4.14 4.11
57	LVDS_TX3_P DSIPORTA_LANE4X	4.2.3 4.2.4	58	GPIO5_143 MCSPI1_CS0	4.14 4.16
59	LVDS_TX3_N DSIPORTA_LANE4Y	4.2.3 4.2.4	60	SATA_ACTLED GPIO5_153 UART3_CTS_RCTX	4.1 4.14 4.9
61	CPI_DATA13 SDCARD_CD TIMER5_PWM_EVT GPIO8_228 UART1_CTS	4.3.1 4.11 4.17 4.14 4.9	62	HDQ_SIO GPIO5_154 UART3_RTS_IRSD	4.18 4.14 4.9
63	GPIO5_141 MCSPI1_SOMI	4.14 4.16	64	VSYS	5.1
65	GPIO5_142 MCSPI1_SIMO	4.14 4.16	66	GPIO7_197 TS_XP MCSPI2_CLK	4.14 4.12 4.16
67	CPI_DATA14 GPIO8_229 SDCARD_WP TIMER6_PWM_EVT UART1_RX	4.3.1 4.14 4.11 4.17 4.9	68	DISPC_FID MCSPI2_CS0 GPIO7_196 TS_XN	4.2.1 4.16 4.14 4.12
69	GPIO5_140 MCSPI1_CLK	4.14 4.16	70	GPIO7_198 MCSPI2_SIMO TS_YP	4.14 4.16 4.12
71	GND	5.1	72	GPIO7_199 MCSPI2_SOMI TS_YN	4.14 4.16 4.12
73	GPIO8_227 CPI_DATA12 TIMER11_PWM_EVT UART1_TX	4.14 4.3.1 4.17 4.9	74	DISPC_DATA22 GPIO6_186 KBD_ROW1	4.2.1 4.14 4.13
75	GPIO6_189 DSIPORTA_TE0	4.14 4.2.4	76	GPIO6_187 DISPC_DATA23 KBD_ROW2	4.14 4.2.1 4.13
77	CPI_DATA4 GPIO8_IN242 CSIPORTA_LANE3X	4.3.1 4.14 4.3.2	78	VSYS	5.1
79	CPI_DATA5 GPIO8_IN243 CSIPORTA_LANE3Y	4.3.1 4.14 4.3.2	80	JTAG_RTCK SDCARD_CLK	4.21 4.11
81	GPIO8_224 CAM_SHUTTER	4.14 4.3	82	JTAG_TDO SDCARD_CMD	4.21 4.11
83	CPI_DATA6 GPIO8_IN244 CSIPORTA_LANE4X	4.3.1 4.14 4.3.2	84	JTAG_TDI SDCARD_DATA0	4.21 4.11
85	CPI_DATA7 GPIO8_IN245 CSIPORTA_LANE4Y	4.3.1 4.14 4.3.2	86	JTAG_NTRST SDCARD_DATA1	4.21 4.11
87	GND	5.1	88	JTAG_TMSC SDCARD_DATA2	4.21 4.11
89	CPI_DATA2 GPIO8_IN240 CSIPORTA_LANE2Y	4.3.1 4.14 4.3.2	90	JTAG_TCK SDCARD_DATA3	4.21 4.11
91	CPI_DATA3 GPIO8_IN241 CSIPORTA_LANE2X	4.3.1 4.14 4.3.2	92	DISPC_DATA17 KBD_COL5 GPIO6_160 RFBI_HSYNC0	4.2.1 4.13 4.14 4.2.2
93	GPIO8_225 CAM_STROBE	4.14 4.3	94	DISPC_DATA16 KBD_ROW5 GPIO6_161 RFBI_TE_VSYNC0	4.2.1 4.13 4.14 4.2.2
95	CPI_PCLK GPIO8_IN236 CSIPORTA_LANE0X	4.3.1 4.14 4.3.2	96	VSYS	5.1
97	CPI_WEN GPIO8_IN237 CSIPORTA_LANE0Y	4.3.1 4.14 4.3.2	98	DISPC_PCLK GPIO6_164 KBD_COL4 RFBI_RE	4.2.1 4.14 4.13 4.2.2

Pin #	CM-T54 Signal Name	Reference Section	Pin #	CM-T54 Signal Name	Reference Section
99	CAM_GLOBALRESET GPIO8_226 CAM_SHUTTER CPI_FID	4.3 4.14 4.3 4.3.1	100	GPIO6_163 DISPC_HSYNC RFBI_CS0	4.14 4.2.1 4.2.2
101	CPI_DATA0 GPIO8_IN238 CSIPORTA_LANE1Y	4.3.1 4.14 4.3.2	102	DISPC_VSYNC GPIO6_162 RFBI_WE	4.2.1 4.14 4.2.2
103	CPI_DATA1 GPIO8_IN239 CSIPORTA_LANE1X	4.3.1 4.14 4.3.2	104	DISPC_DE KBD_ROW4 GPIO6_165 RFBI_A0	4.2.1 4.13 4.14 4.2.2
105	GND	5.1	106	DISPC_DATA0 GPIO6_166 RFBI_DATA0	4.2.1 4.14 4.2.2
107	CPI_DATA8 GPIO8_IN252 CSIPORTC_LANE0Y	4.3.1 4.14 4.3.2	108	DISPC_DATA1 RFBI_DATA1 GPIO6_167 UART3_RX_IRRX	4.2.1 4.2.2 4.14 4.9
109	CPI_DATA9 GPIO8_IN253 CSIPORTC_LANE0X	4.3.1 4.14 4.3.2	110	DISPC_DATA2 RFBI_DATA2 GPIO6_168 UART3_TX_IRTX	4.2.1 4.2.2 4.14 4.9
111	RS232_TXD	4.10	112	DISPC_DATA3 GPIO6_169 RFBI_DATA3	4.2.1 4.14 4.2.2
113	CPI_VSYNCIN GPIO8_IN251 CSIPORTB_LANE2X	4.3.1 4.14 4.3.2	114	VSYS	5.1
115	CPI_HSYNCIN GPIO8_IN250 CSIPORTB_LANE2Y	4.3.1 4.14 4.3.2	116	DISPC_DATA4 GPIO6_170 RFBI_DATA4	4.2.1 4.14 4.2.2
117	RS232_RXD	4.10	118	DISPC_DATA5 GPIO6_171 RFBI_DATA5	4.2.1 4.14 4.2.2
119	CPI_DATA11 GPIO8_IN255 CSIPORTC_LANE1X	4.3.1 4.14 4.3.2	120	DISPC_DATA6 GPIO6_172 RFBI_DATA6	4.2.1 4.14 4.2.2
121	CPI_DATA10 GPIO8_IN254 CSIPORTC_LANE1Y	4.3.1 4.14 4.3.2	122	DISPC_DATA7 GPIO6_173 RFBI_DATA7	4.2.1 4.14 4.2.2
123	GND	5.1	124	DISPC_DATA8 KBD_COL3 GPIO6_174 RFBI_DATA8	4.2.1 4.13 4.14 4.2.2
125	CPI_DATA15 GPIO8_IN249 CSIPORTB_LANE1X	4.3.1 4.14 4.3.2	126	DISPC_DATA9 KBD_ROW3 GPIO6_175 RFBI_DATA9	4.2.1 4.13 4.14 4.2.2
127	CPI_DATA14 GPIO8_IN248 CSIPORTB_LANE1Y	4.3.1 4.14 4.3.2	128	DISPC_DATA10 KBD_ROW8 GPIO6_176 RFBI_DATA10	4.2.1 4.13 4.14 4.2.2
129	GPIO8_231 I2C3_SCL	4.14 4.15	130	DISPC_DATA11 KBD_ROW7 GPIO6_177 RFBI_DATA11	4.2.1 4.13 4.14 4.2.2
131	CPI_DATA12 GPIO8_IN246 CSIPORTB_LANE0X	4.3.1 4.14 4.3.2	132	VSYS	5.1
133	CPI_DATA13 GPIO8_IN247 CSIPORTB_LANE0Y	4.3.1 4.14 4.3.2	134	DISPC_DATA12 KBD_ROW6 GPIO6_178 RFBI_DATA12	4.2.1 4.13 4.14 4.2.2
135	GPIO8_232 I2C3_SDA	4.14 4.15	136	DISPC_DATA13 KBD_COL8 GPIO6_179 RFBI_DATA13	4.2.1 4.13 4.14 4.2.2

Pin #	CM-T54 Signal Name	Reference Section		Pin #	CM-T54 Signal Name	Reference Section
137	MCASP_AFSR MCBSP1_CLKX GPIO4_103	4.4.2.2 4.4.2.1 4.14		138	DISPC_DATA14 KBD_COL7 GPIO6_180 RFBI_DATA14	4.2.1 4.13 4.14 4.2.2
139	DMIC_CLK3 MCASP_ACLKX GPIO4_102 MCBSP1_DX	4.4.2.3 4.4.2.2 4.14 4.4.2.1		140	DISPC_DATA15 KBD_COL6 MCSPI2_CS1 GPIO6_181 RFBI_DATA15	4.2.1 4.13 4.16 4.14 4.2.2
141	GND	5.1		142	DISPC_DATA18 GPIO6_182 KBD_COL0	4.2.1 4.14 4.13
143	MCASP_ACLKR MCBSP1_DR GPIO4_104	4.4.2.2 4.4.2.1 4.14		144	DISPC_DATA19 GPIO6_183 KBD_COL1	4.2.1 4.14 4.13
145	DMIC_CLK2 GPIO4_101 MCASP_AMUTEIN MCBSP1_FSX	4.4.2.3 4.14 4.4.2.2 4.4.2.1		146	DISPC_DATA20 GPIO6_184 KBD_COL2	4.2.1 4.14 4.13
147	SDIO4_CMD GPIO5_156 UART3_RX_IRRX	4.11 4.14 4.9		148	DISPC_DATA21 GPIO6_185 KBD_ROW0	4.2.1 4.14 4.13
149	SDIO4_DATA3 GPIO5_137 UART5_RTS	4.11 4.14 4.9		150	VSYS	5.1
151	SDIO4_DATA2 GPIO5_135 UART5_TX	4.11 4.14 4.9		152	GPIO1_WK6 DRM_EMU0	4.14 4.21
153	SDIO4_DATA1 GPIO5_134 UART5_RX	4.11 4.14 4.9		154	GPIO1_WK7 DRM_EMU1	4.14 4.21
155	SDIO4_DATA0 GPIO5_136 UART5_CTS	4.11 4.14 4.9		156	VBUS_EN_REQ	4.8.2
157	SDIO4_CLK GPIO5_155 UART3_TX_IRTX	4.11 4.14 4.9		158	USB3_DN	4.8.2
159	GND	5.1		160	USB3_DP	4.8.2
161	GPIO7_200 I2C4_SCL	4.14 4.15		162	VBUS_nOVC	4.8.2
163	GPIO7_201 I2C4_SDA	4.14 4.15		164	USB2_DN	4.8.2
165	PMIC_PWRON	5.2.3.2		166	USB2_DP	4.8.2
167	GPADC_VREF	4.19		168	VSYS	5.1
169	GPADC_IN2	4.19		170	USB1_DN	4.8.2
171	COLD_RESET_IN	5.3		172	USB1_DP	4.8.2
173	GPADC_IN1	4.19		174	USBOTG_ID	4.8.1
175	GPADC_IN0	4.19		176	UART3_RX_IRRX USBD0_HS_DP	4.9 4.8.1
177	GND	5.1		178	UART3_TX_IRTX USBD0_HS_DM	4.9 4.8.1
179	VBAT_SENSE	5.2.3.2		180	VBUS_5V_OTG	4.8.1
181	VAC_DETECT	5.2.3.2		182	USBD0_SS_RX	4.8.1
183	VCC_RTC	5.1		184	USBD0_SS_RY	4.8.1
185	ALT_BOOT	5.4		186	VSYS	5.1
187	SYS_nRESWARM	5.3		188	USBD0_SS_TX	4.8.1
189	RESERVED			190	USBD0_SS_TY	4.8.1
191	MCASP_AXR GPIO4_96 MIC_BIAS	4.4.2.2 4.14 4.4.1		192	USB_PSEL	5.5
193	FREF_CLK0_OUT GPIO1_WK12 MIC_IN	4.20 4.14 4.4.1		194	CPI_DATA15 SDCARD_WP TIMER8_PWM_EVT GPIO8_230 UART1_RTS	4.3.1 4.11 4.17 4.14 4.9
195	GND	5.1		196	PMID	5.1 / 5.5

Pin #	CM-T54 Signal Name	Reference Section		Pin #	CM-T54 Signal Name	Reference Section
197	DMIC_DIN2 MCASP_AXR GPIO4_98 MCBSP3_DX LINEIN_R	4.4.2.3 4.4.2.2 4.14 4.4.2.1 4.4.1		198	PMIC_ENABLE_1	5.2.1
199	DMIC_CLK1 GPIO4_100 MCBSP3_CLKX LINEIN_L	4.4.2.3 4.14 4.4.2.1 4.4.1		200	MCASP_AFSX GPIO4_107	4.4.2.2 4.14
201	DMIC_DIN1 MCASP_AHCLKR GPIO4_97 MCBSP3_FSX HP_OUT_R	4.4.2.3 4.4.2.2 4.14 4.4.2.1 4.4.1		202	PMIC_REGEN1	5.2.1
203	DMIC_DIN3 MCBSP3_DR GPIO4_99 HP_OUT_L	4.4.2.3 4.4.2.1 4.14 4.4.1		204	VSYS	5.1

6.2 Mating Connectors

Table 51 Connector type

CM-T54 connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 10 CM-T54 Top

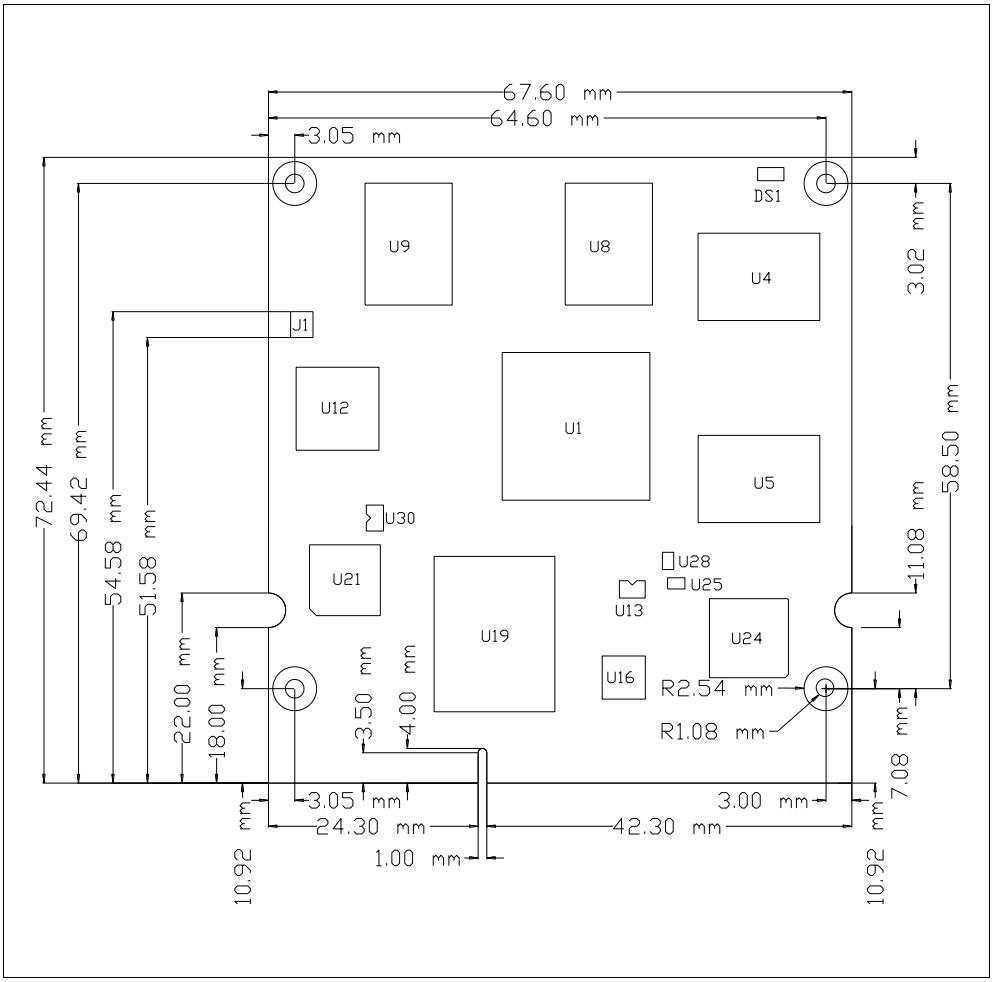
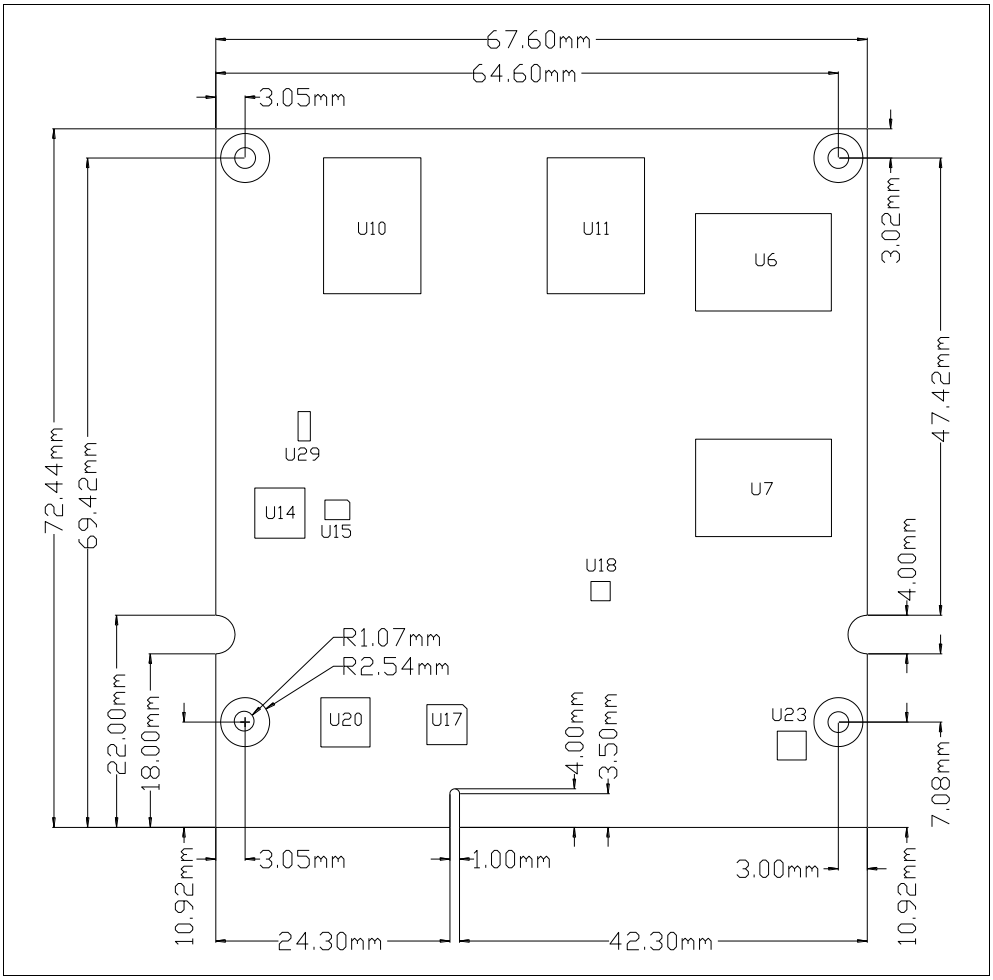


Figure 11 CM-T54 bottom (X-Ray view - as seen from top side)



1. All dimensions are in millimeters.

2. Height of all components is < 3.5mm.

3. Baseboard connectors provide 2mm board-to-board clearance.

4. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at http://compulab.co.il/products/computer-on-modules/CM-T54/#devres

6.4 Standoffs/Spacers

CM-T54 has four mounting holes to physically secure the CoM to the carrier board. Secure CM-T54 to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 2.2±0.2 mm length

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 52 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)		-0.3	3.8/5.0	5.5	V
Backup battery supply voltage (VCC_RTC)		2.8		3.3	V
USB OTG VBUS		-0.3		5.25	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 53 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	Normal operation	3.0	3.8/5.0	5.5	V
	During boot	3.3	3.8/5.0	5.5	V
Backup battery supply voltage (VCC_RTC)		2.8	3.0	3.3	V
VBUS_5V_OTG	If supplied externally	4.4		5.25	V

7.3 DC Electrical Characteristics

Table 54 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{IH}		1.26		2.3	V
V_{IL}		-0.5		0.54	V
$V_{OH\ (2mA)}$		1.35			V
$V_{OL\ (2mA)}$				0.45	V
SDCARD interface					
V_{IH}	1.8V mode	1.27			V
	3.3V mode	2.07			V
V_{IL}	1.8V mode			0.58	V
	3.3V mode			0.75	V
$V_{OH\ (2mA)}$	1.8V mode	1.4			V
	3.3V mode	2.25			V
$V_{OL\ (2mA)}$	1.8V mode			0.45	V
	3.3V mode			0.42	V
RS232					
TX Voltage Swing		-5.5		5.5	V
RX Voltage Swing		-25		25	V

7.4 ESD Performance

Table 55 ESD Performance

Interface	ESD Performance
RS232	15kV using Human Body Model (HBM)
Multifunctional pins	1kV using Human Body Model (HBM)
USB Host ports (with U4 option)	5kV using Human Body Model (HBM) (differential signals only)

7.5 Operating Temperature Ranges

The CM-T54 is available with three options of operating temperature range.

Table 56 CM-T54 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-T54 operation. All power-up circuitry and all required pullups/pulldowns are available onboard CM-T54.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CM-T54 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CM-T54.
- Refer to the SB-T54 carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 0. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus

- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CM-T54, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-T54 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of “Qualified Magnetics” contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 57 Qualified Magnetics

Vendor	P/N	Package
UDE	RTA-1D4B8V1A	Integrated RJ45
PULSE	J1011F01PNL	Integrated RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-T54 reference design schematics

8.4 Heat-plate Integration

To be added in a future revision of this document.