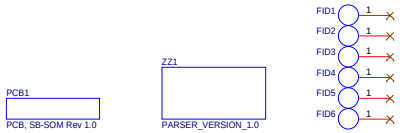
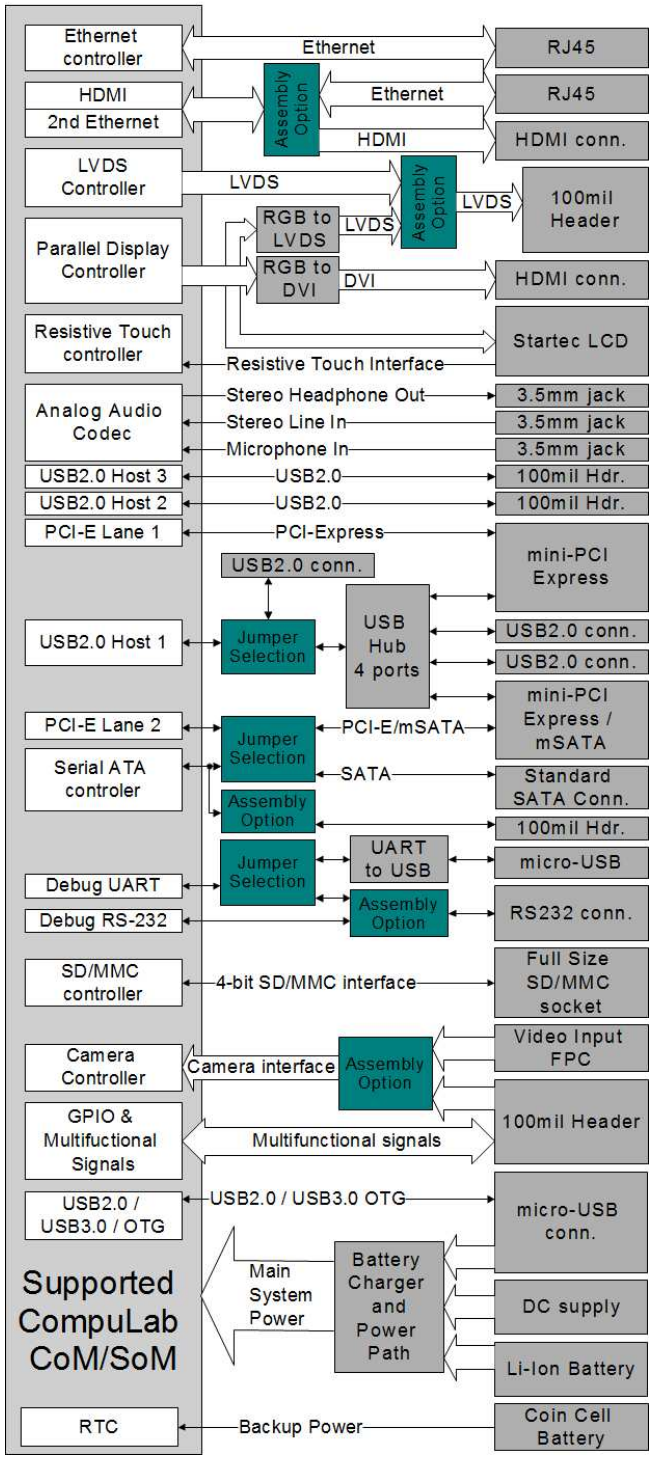
SB-SOM

BOARD REVISION: 1.0


```
CARRIER BOARD PRIMARY I2C BUS SLAVES (7bit address):
-----------------------------------------------------------------
0b010,0000 - Carrier GPIO Expander
0b011,0110 - DS2786 Battery Supervisor
0b011,1000 - DVI Transmitter
0b101,0000 - Carrier ID EEPROM
0b110,1011 - BQ24161 battery charger & power-path
0b110,1110 - PCI-E REFCLK fanout
```



SB-SOM rev1v0



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BOARD REVISION: 1.0

1. Initial Revision with support for the following SoMs:
1.1. CM-T43
1.2. CM-T54
1.3. CM-QS600

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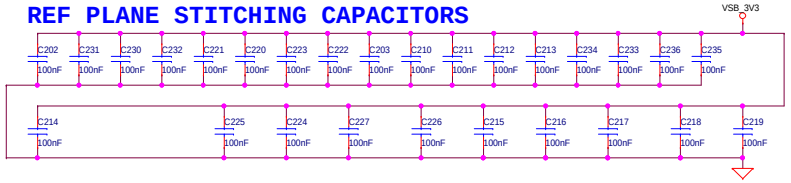
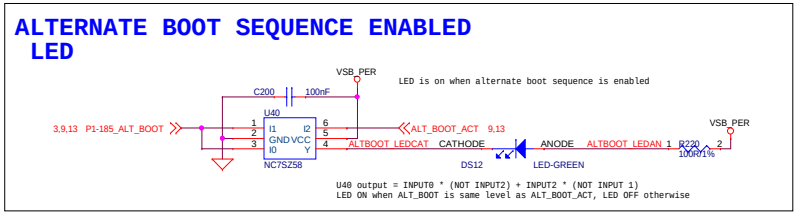
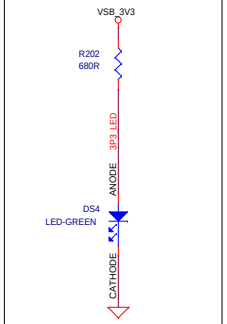
REF PLANE STITCHING CAPACITORS



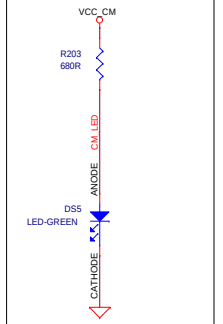
ALTERNATE BOOT SEQUENCE ENABLED LED



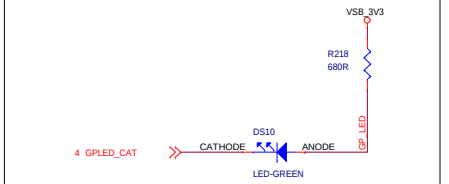
Carrier Board Peripherals Power LED



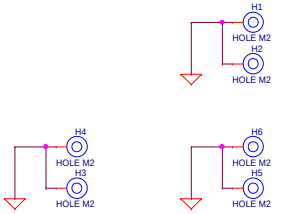
SoM/CoM Primary Power LED



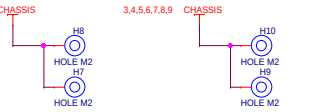
Carrier Board GPIO Controlled LED

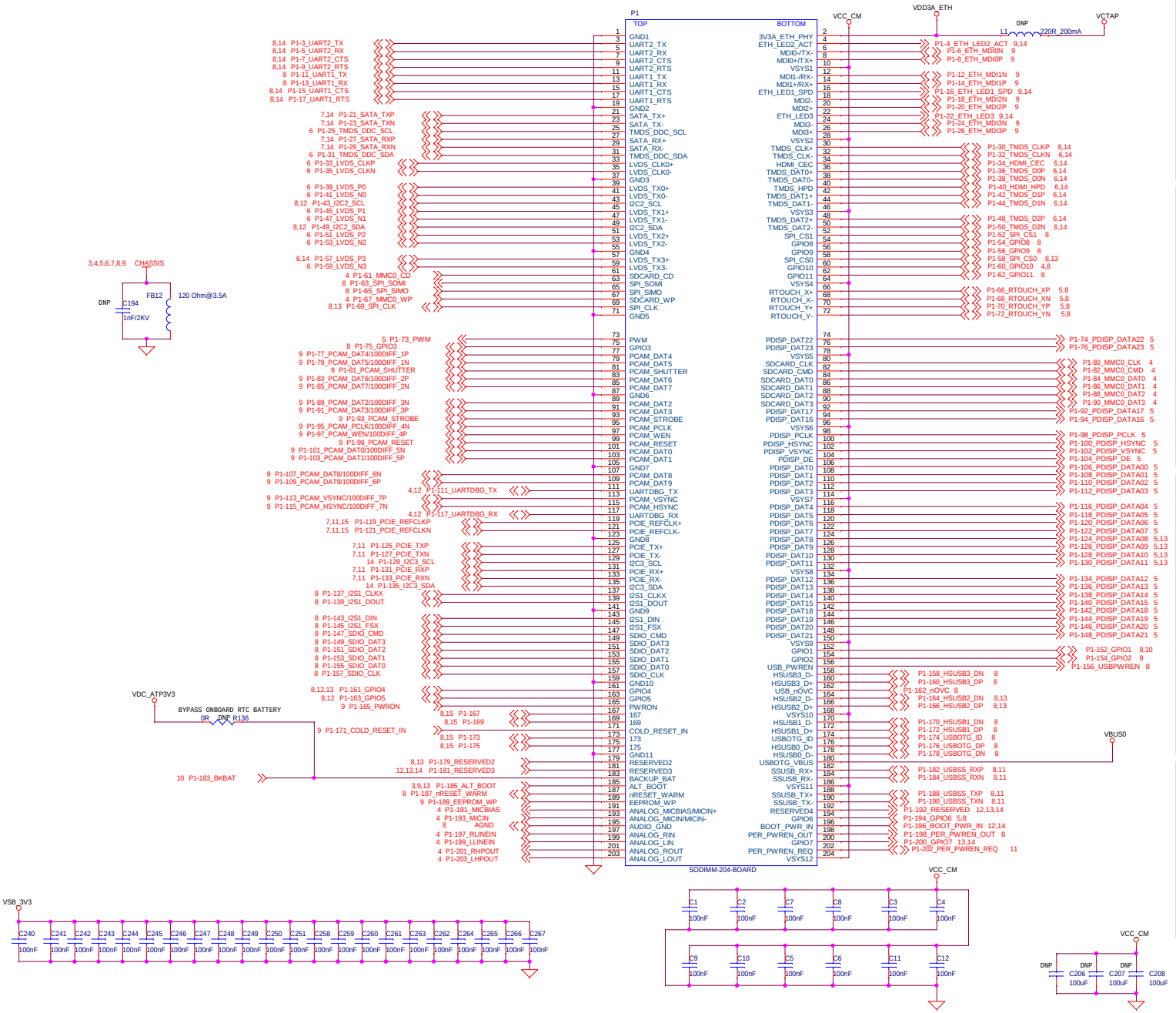


CoM/SoM Mechanic Holes



Carrier Board Mechanic Holes





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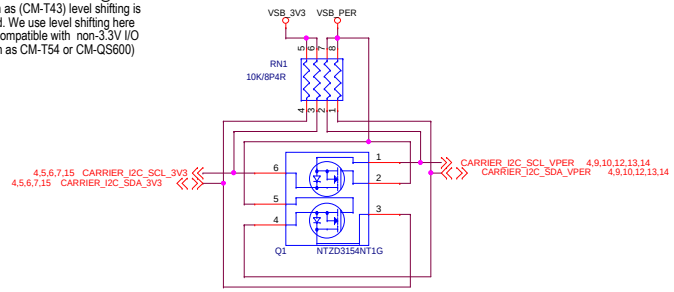
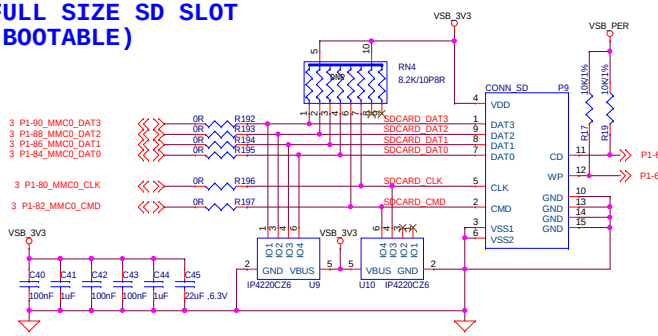
CARRIER BOARD PRIMARY I2C BUS LEVEL SHIFT

Circuitry is designed to shift
I2C signals logic levels between
VSB_PER (1.8 or 3.3V) and 3.3V.

NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as (CM-T43) level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)

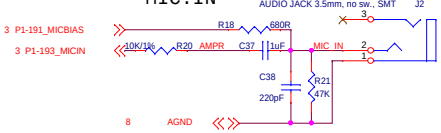


FULL SIZE SD SLOT (BOOTABLE)



ANALOG AUDIO

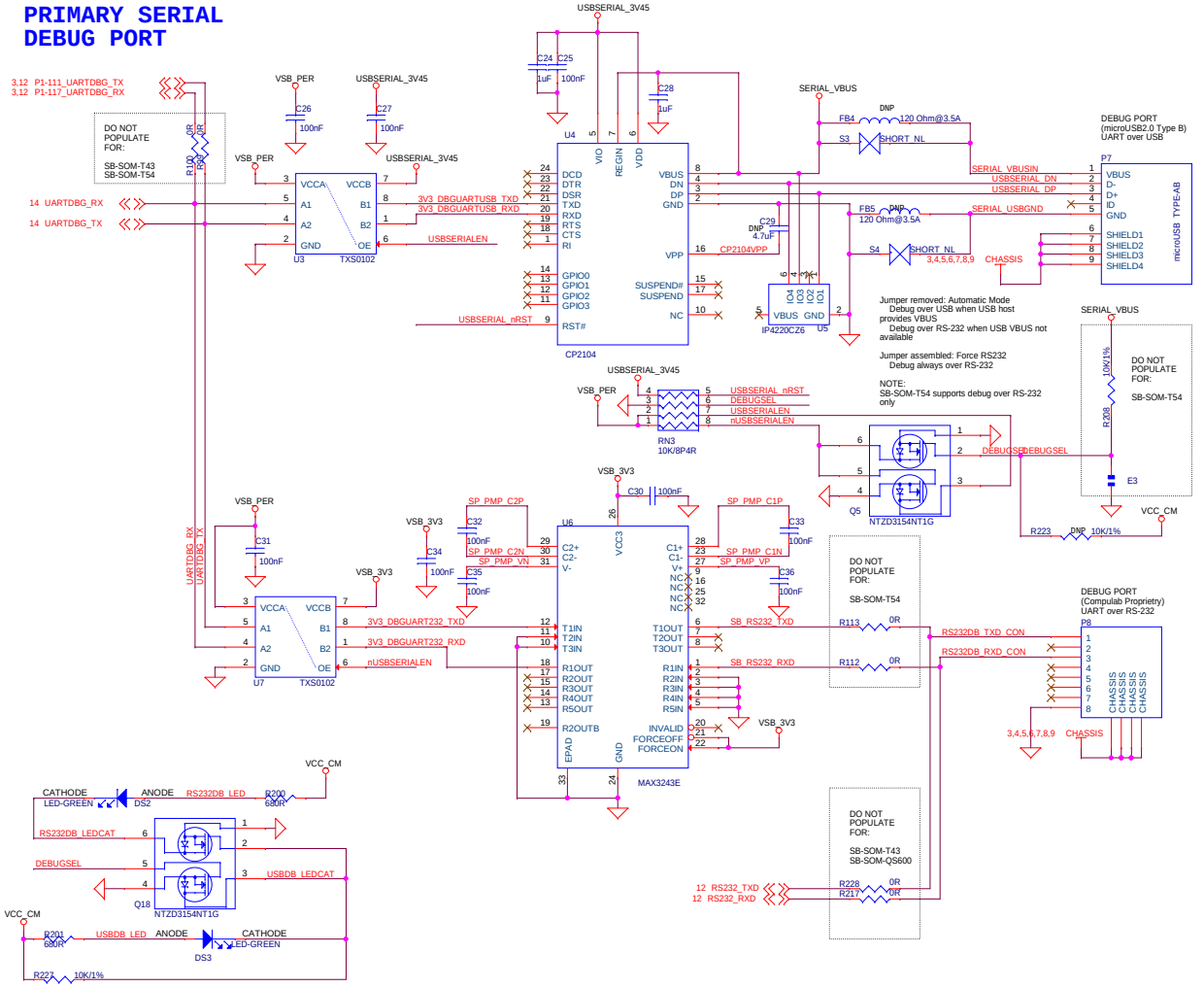
MIC.IN



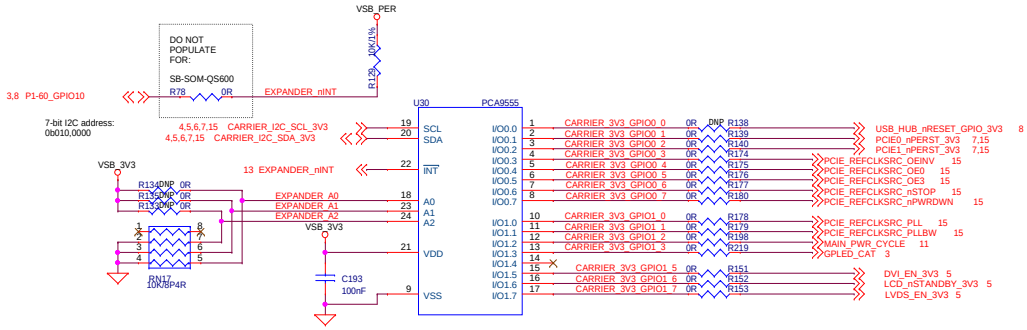
AUDIO OUT

LINE IN

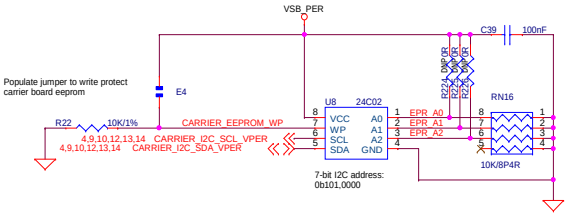
PRIMARY SERIAL DEBUG PORT



CARRIER GPIO EXPANDER



CARRIER BOARD EEPROM



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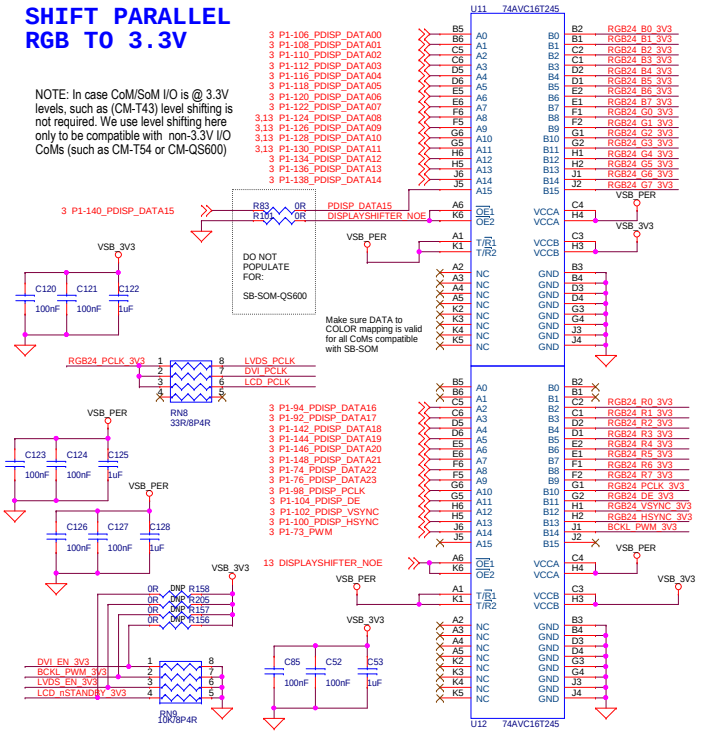
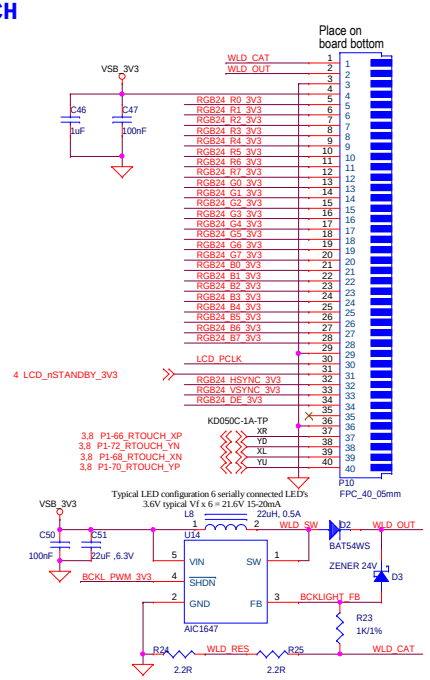
SHIFT PARALLEL RGB TO 3.3V

NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as (CM-T43) level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)

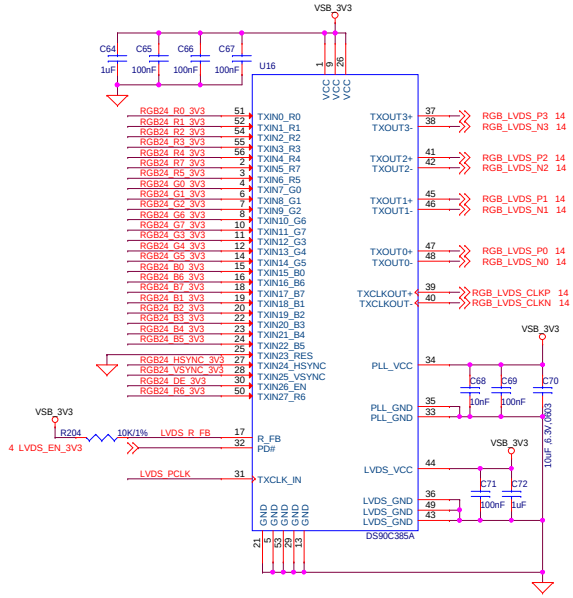


PARALLEL RGB LCD & TOUCH

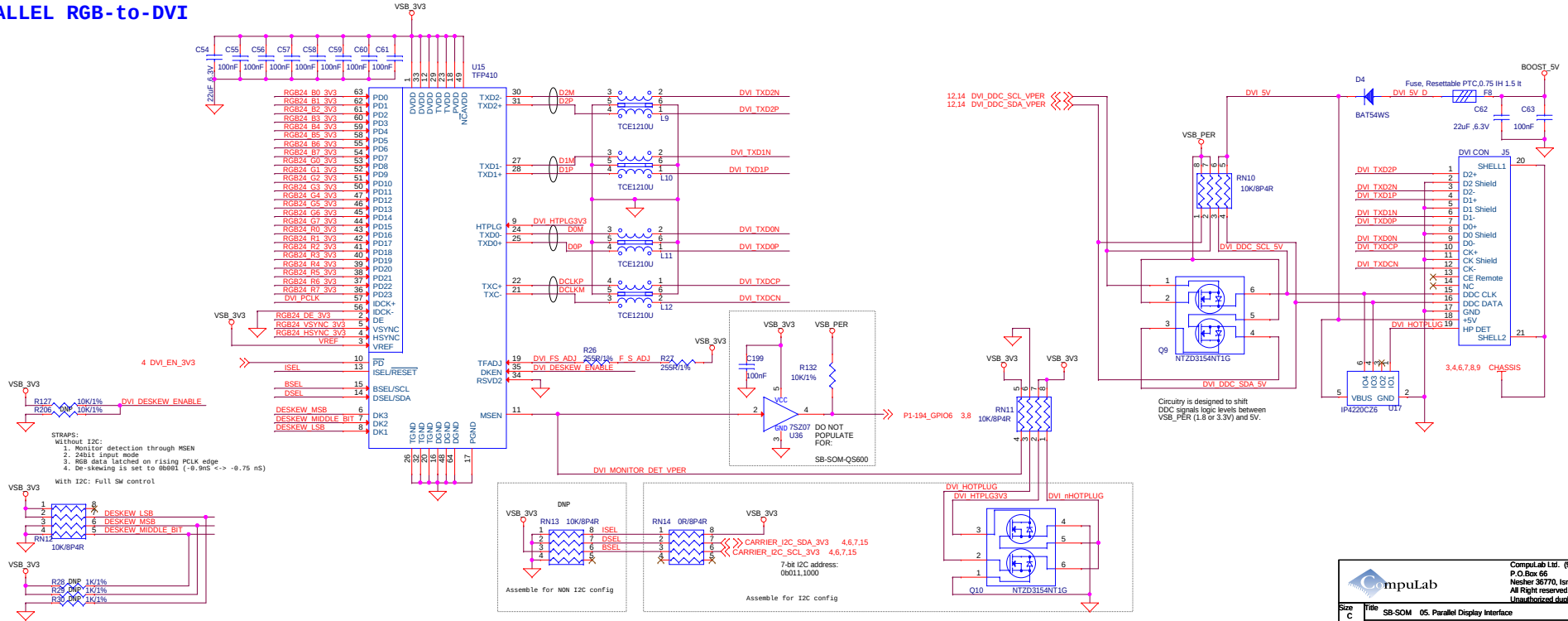
SHENZHEN STARTEK
ELECTRONIC TECHNOLOGY
KD050C-1A-TP LCD



PARALLEL RGB to LVDS



PARALLEL RGB-to-DVI



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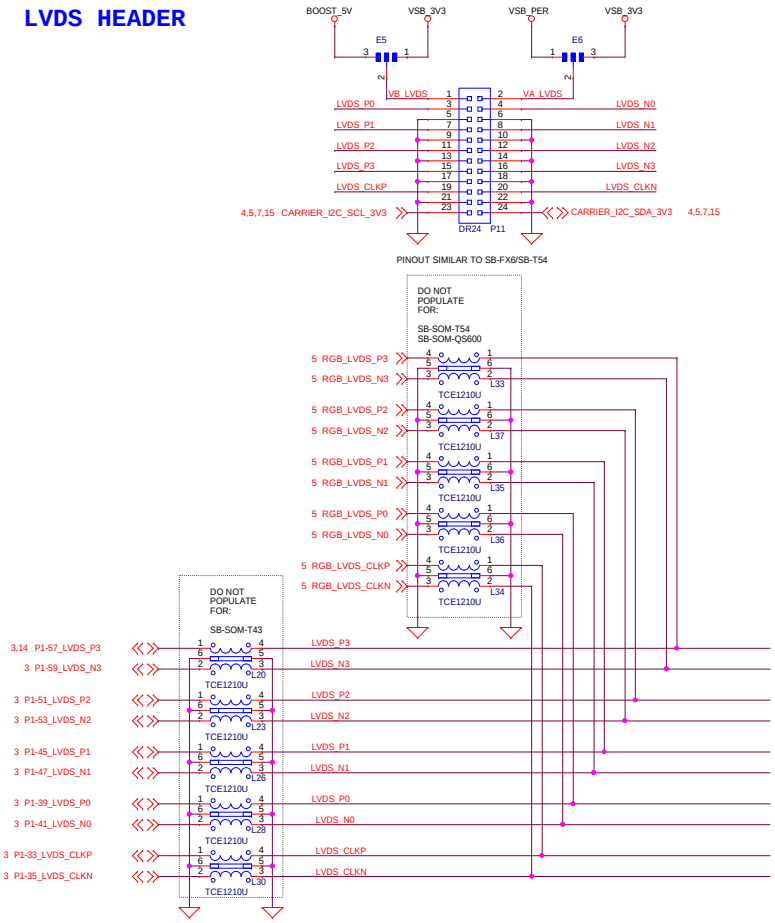
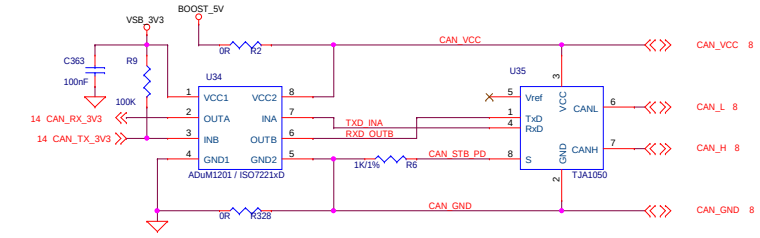
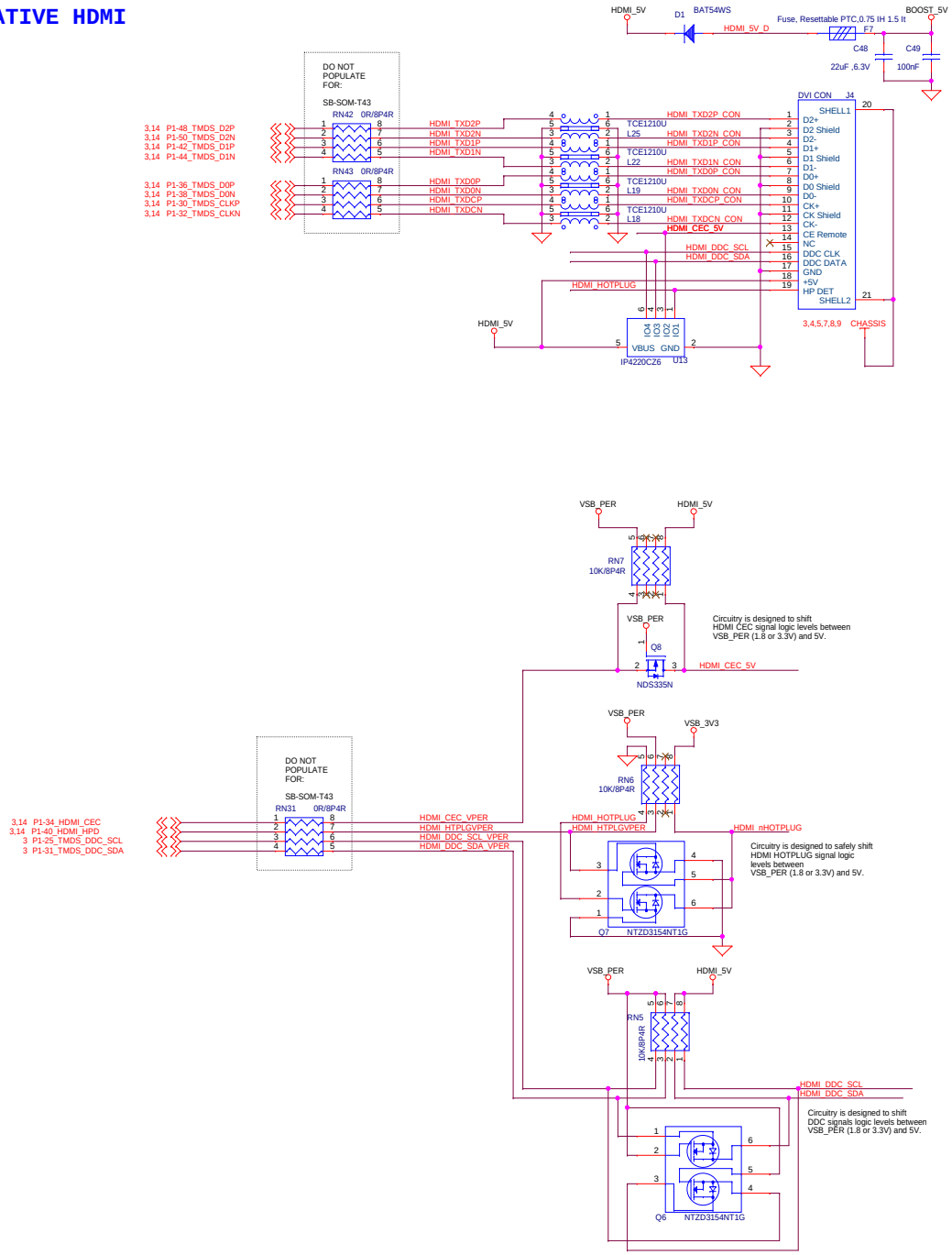
LVDS HEADER



CAN TRANSCEIVER



CoM NATIVE HDMI



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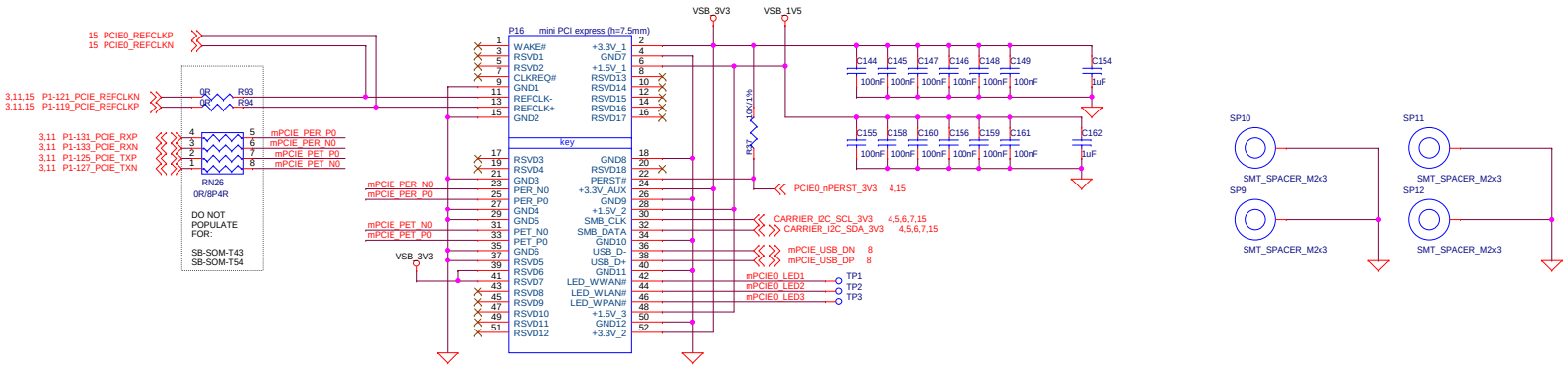
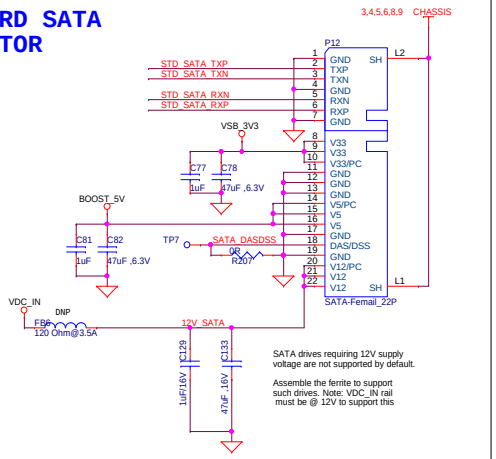
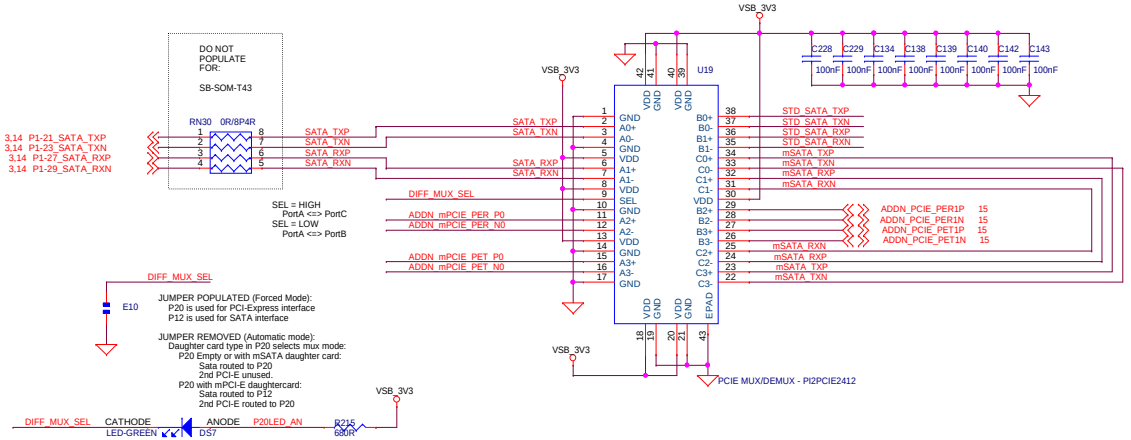
PRIMARY mini-PCIE



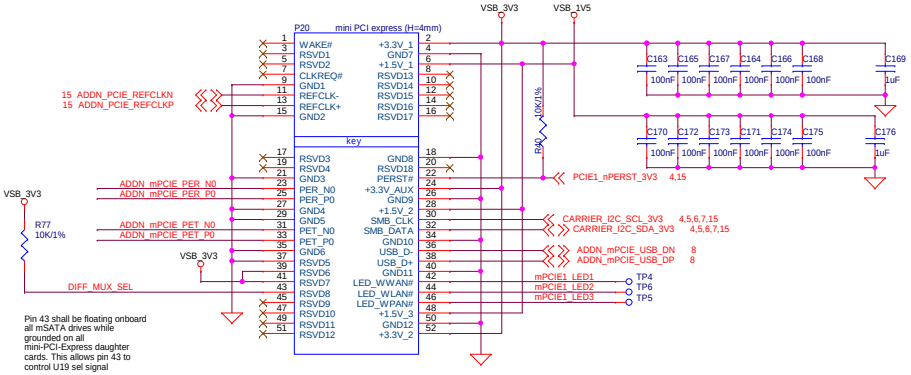
STANDARD SATA CONNECTOR

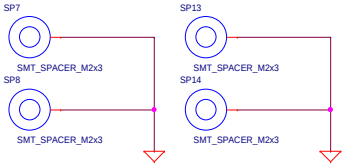


PCIE/SATA/mSATA MUX



SECONDARY PCIE/mSATA/USB





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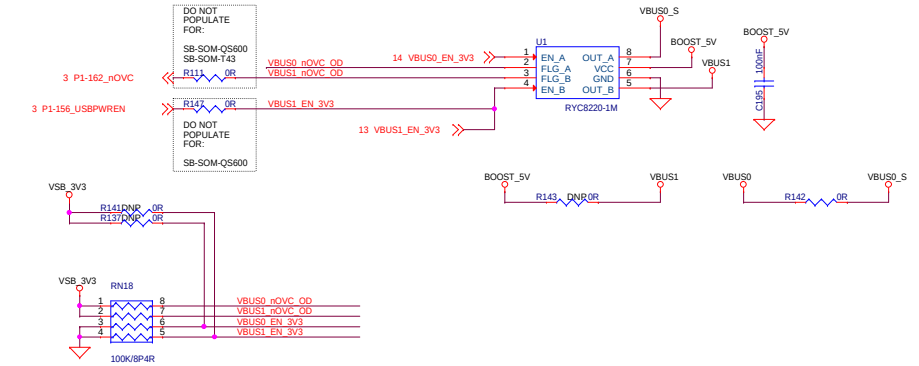
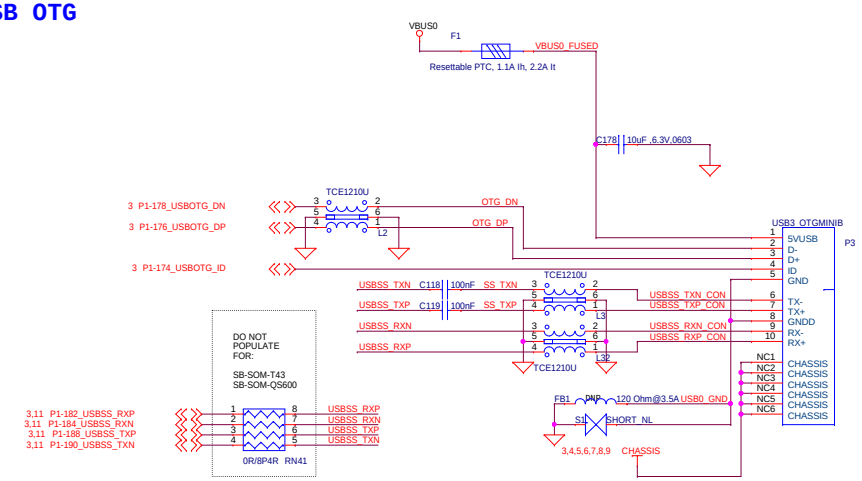
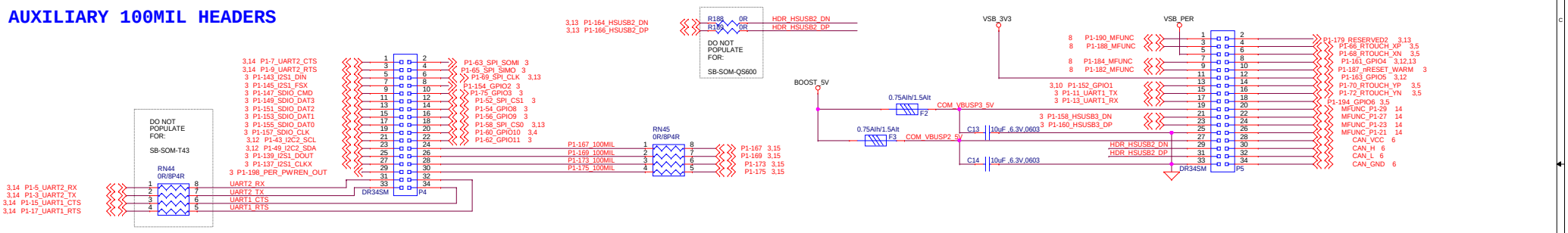
VBUS SOURCE



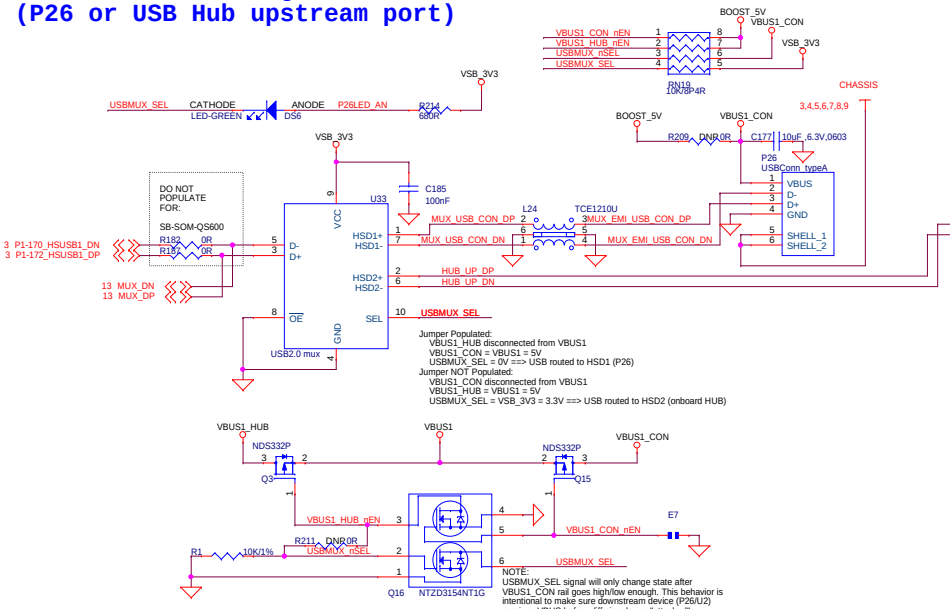
USB OTG



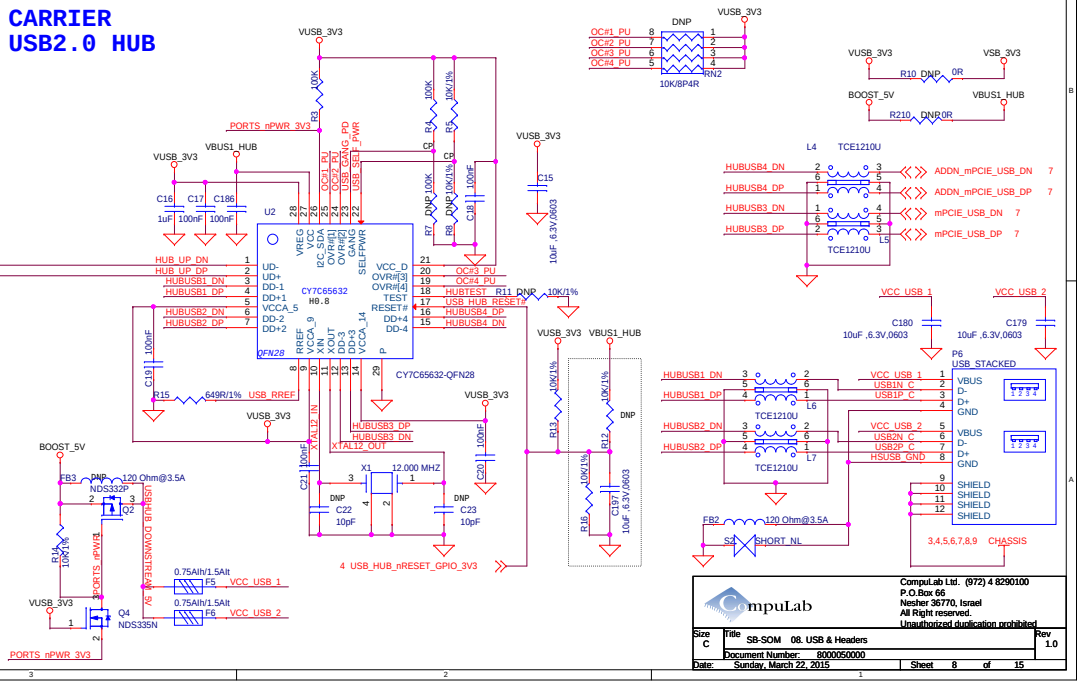
AUXILIARY 100MIL HEADERS



SoM/CoM USB2.0 usage selecor (P26 or USB Hub upstream port)



CARRIER USB2.0 HUB



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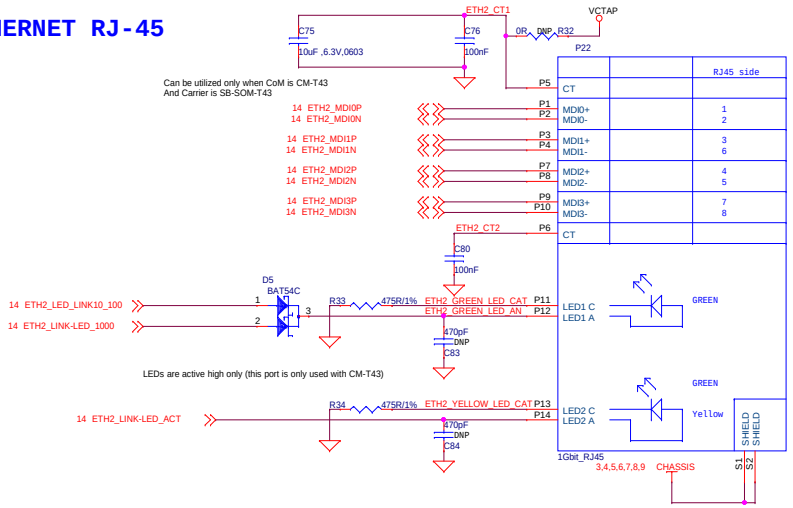
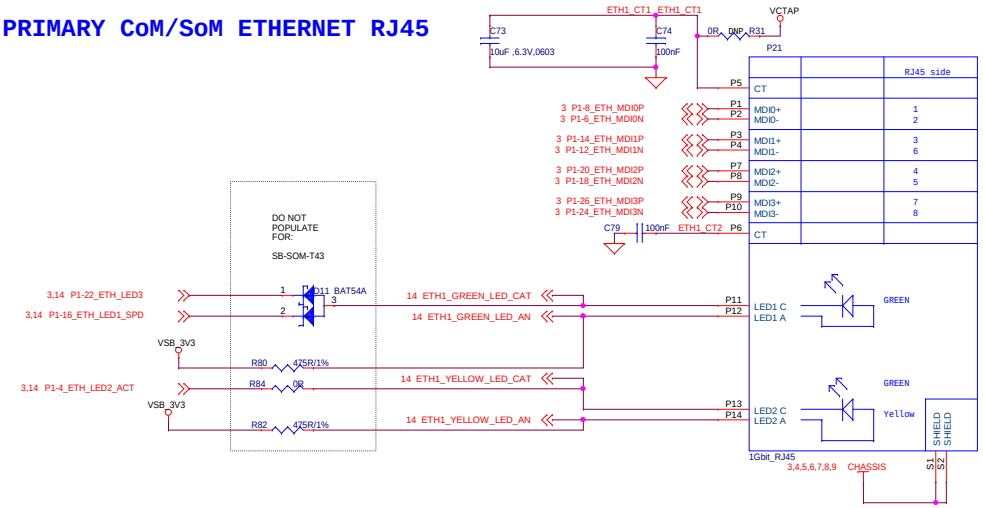
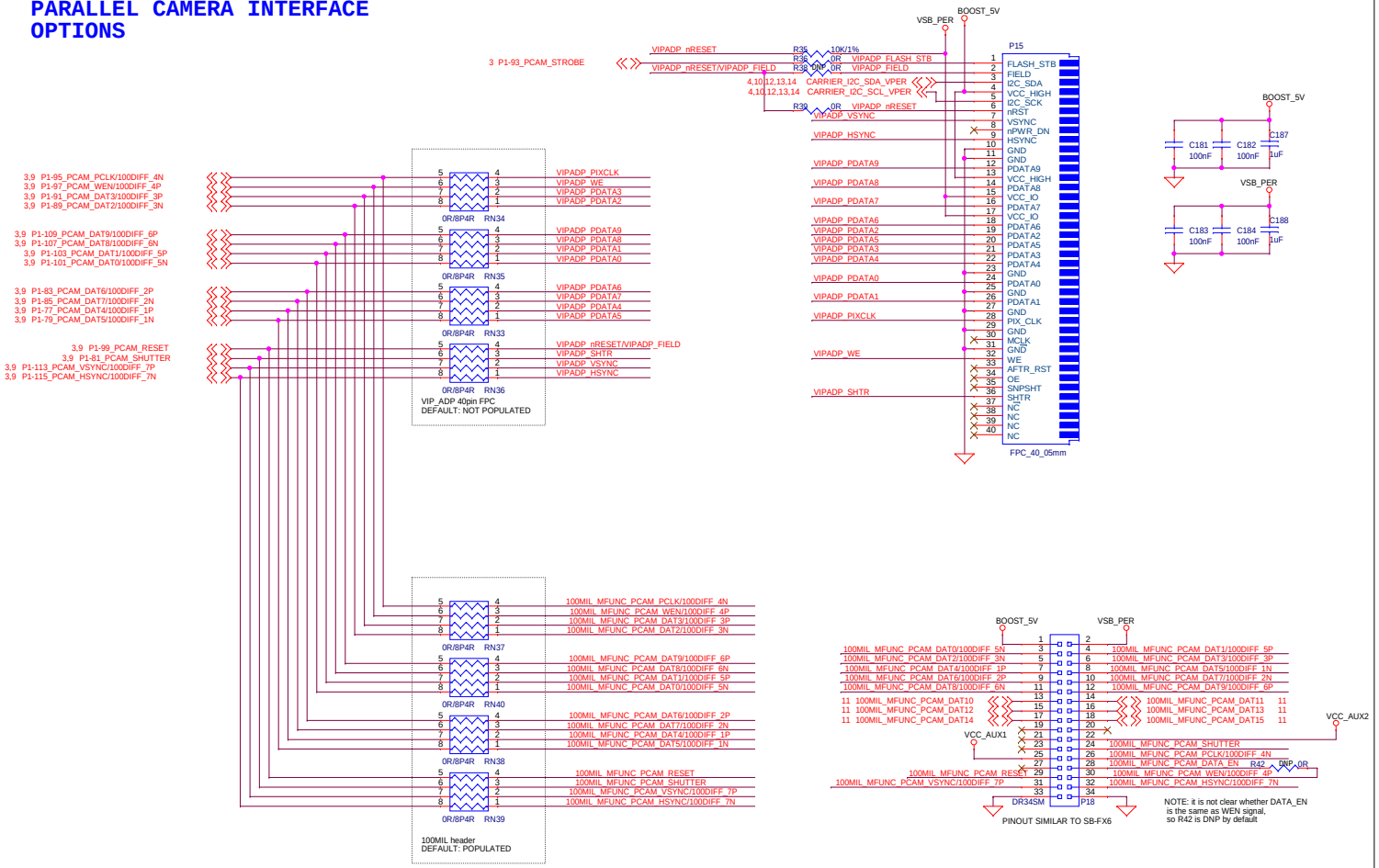
SECONDARY ETHERNET RJ-45



PRIMARY CoM/SoM ETHERNET RJ45



PARALLEL CAMERA INTERFACE OPTIONS

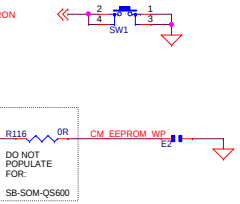


POWER/RESET/BOOT SWITCHES

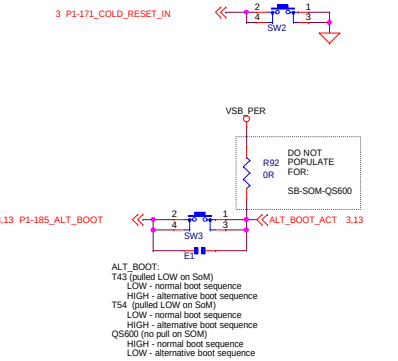
SODIMM165_PWRON:
T43 (pulled to VCC_CM on SoM):
HIGH --> LOW = SoM wake/pwron event
held low for more than 8s/15s = SoM power-cycle
constantly LOW = constant SoM power-cycling (8s/15s cycles)

T54 (pulled to VCC_CM on SoM PMIC):
HIGH --> LOW = PMIC Interrupt to CPU
low for more than 15mS = SoM wake/pwron request
held low for more than 12s = SoM power-off request

QS600 (pulled high on SoM):
ON and OFF requests can be triggered
upon voltage sensed by CM-QS600 here.



CM_FLASH_nWP:
T43 (pulled HIGH on SoM)
LOW - CoM EEPROM & SPI FLASH write protection enabled/allowed respectively
HIGH - CoM EEPROM & SPI FLASH write protection disabled
T54 (pulled HIGH on SoM)
LOW - CoM EEPROM write protection disabled
HIGH - CoM EEPROM write protection enabled
QS600 (VREF_BATT signal. must never be grounded)
CM-QS600 onboard EEPROM always writeable



ALT_BOOT:
T43 (pulled LOW on SoM)
LOW - normal boot sequence
HIGH - alternative boot sequence
T54 (pulled LOW on SoM)
LOW - normal boot sequence
HIGH - alternative boot sequence
QS600 (no pull on SOM)
HIGH - normal boot sequence
LOW - alternative boot sequence

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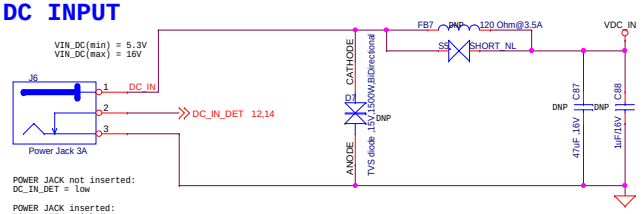
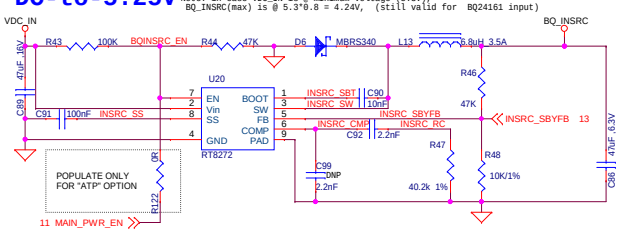
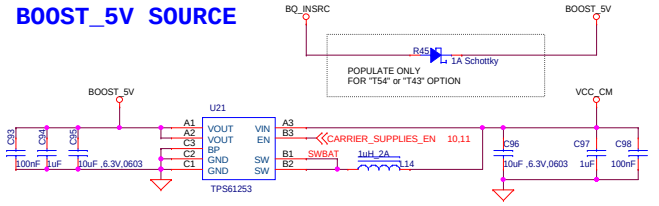
DC INPUT



DC-to-5.25V

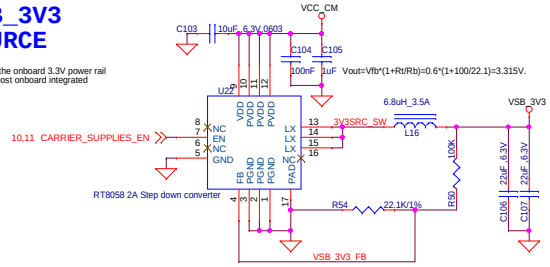


BOOST_5V SOURCE



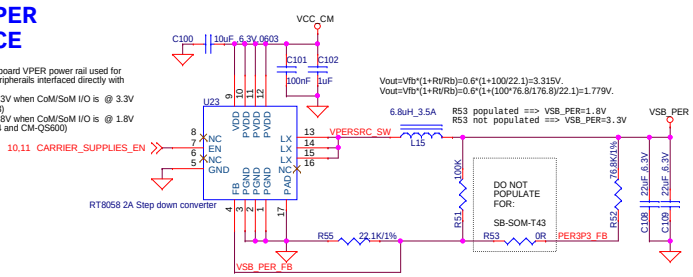
VSB_3V3 SOURCE

Source of the onboard 3.3V power rail used for most onboard integrated circuitry



VSB_PER SOURCE

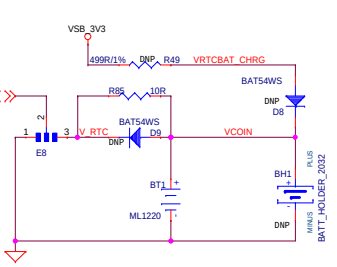
Source of the onboard VPER power rail used for most onboard peripherals interfaced directly with CoM I/O signals.
1. VPER rail is 3.3V when CoM/SoM I/O is @ 3.3V (such as CM-T43)
2. VPER rail is 1.8V when CoM/SoM I/O is @ 1.8V (such as CM-T54 and CM-QS600)



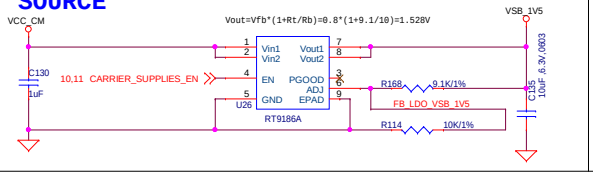
RTC BATTERY

RTC function:
Enable: Short pins 2 <-> 3
Disable:
CM-T54/CM-T43: Short pins 2 <-> 1
CM-QS600: Open

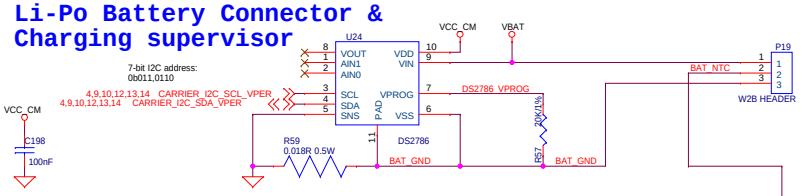
Backup Battery Charger
Available with:
CM-QS600
CM-T54
Not Available with:
CM-T43



1V5 SOURCE



Li-Po Battery Connector & Charging supervisor

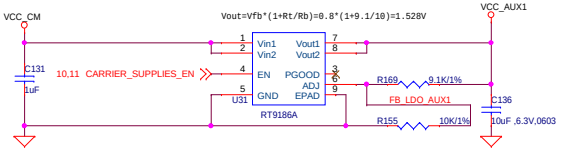


POWER PROVISIONS NOT POPULATED BY DEFAULT

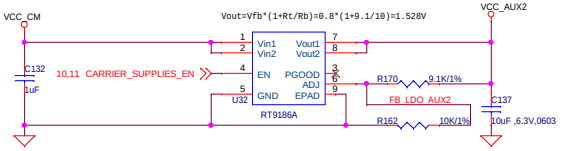
These placeholders allow generating additional voltages rails often required by different camera sensors.
The VCC_AUX1 & VCC_AUX2 voltages can be sourced into the sensor from the 100mil camera header

VCC_AUX1 & VCC_AUX2 voltage can be changed by changing the resistance of R169, R155, R170 & R162

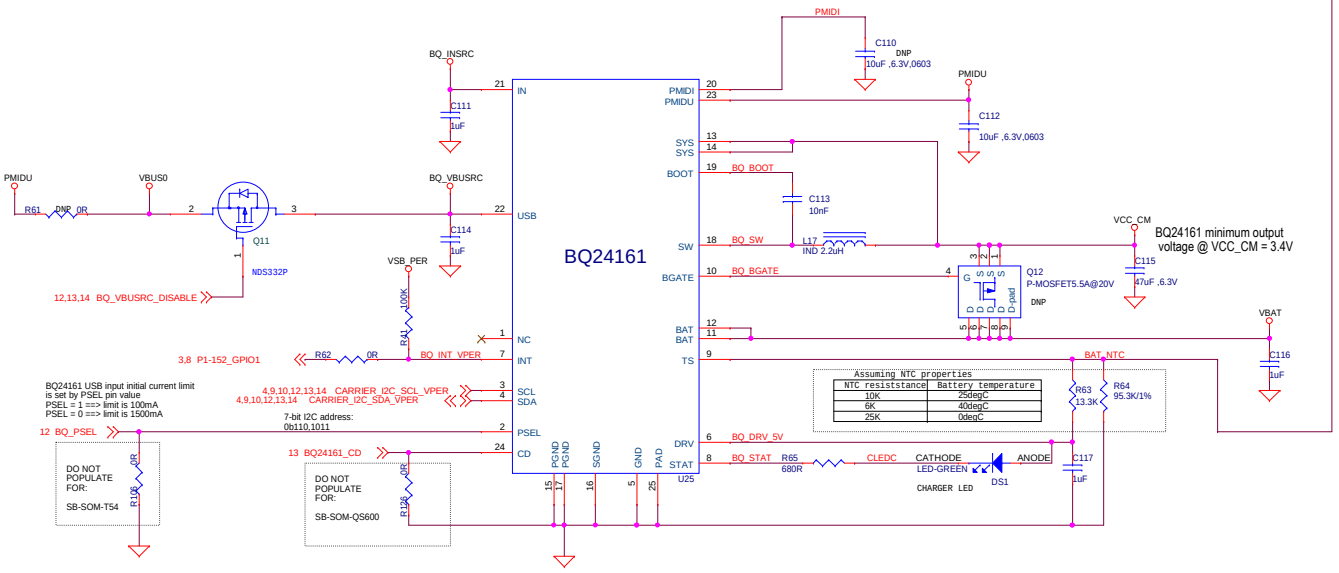
VCC_AUX1 source



VCC_AUX2 source



PRIMARY POWER SOURCE & BATTERY CHARGER



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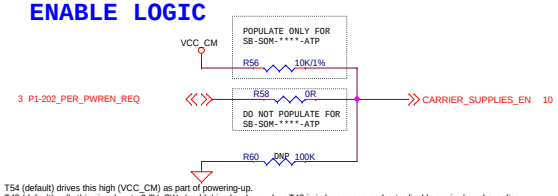
Additional PCI-E Provisions (Not Populated by default)

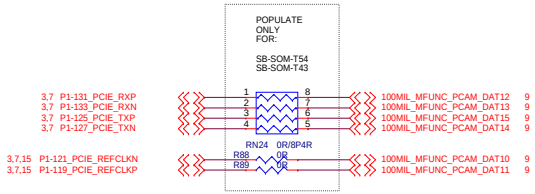
CARRIER SUPPLIES ENABLE LOGIC



T54 (default) drives this high (VCC_CM) as part of powering-up.
T43 (default) pulls this signal up to 3.3V, SW should drive low here when T43 is in low power modes to disable carrier board supplies.
QS600: remove R58, a voltage divider formed by R56 & R60 should result in constant voltage between 1.5V and 3.3V on "CARRIER_SUPPLIES_EN" pin.

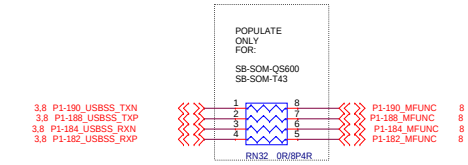
PCI-Express BYPASS

Allows using the PCI-Express lane differential pairs for alternate functions through a 100MIL header. Useful with CoM/SoM where PCI-Express function is not available

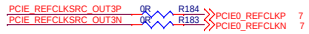


USB3.0 BYPASS

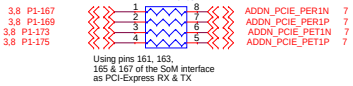
Allows using the USB 3.0 RX & TX differential pairs for alternate functions through a 100MIL header. Useful with CoM/SoM where USB3.0 function is not available



Provision to source PCIE0 REFCLK from GENERATOR to mini-PCI-E connector



2nd PCI-Express Provision

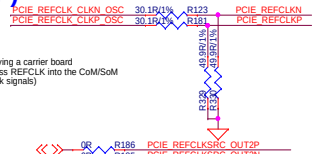


Using pins 161, 163, 165 & 167 of the SoM interface as PCI-Express RX & TX

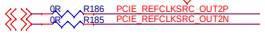
Provision to drive REFCLK GENERATOR from CoM/SoM sourced PCIE0 REFCLK

Provision to allow cloning of a CoM/SoM generated PCIE-Express REFCLK, into PCI-Express devices on the carrier

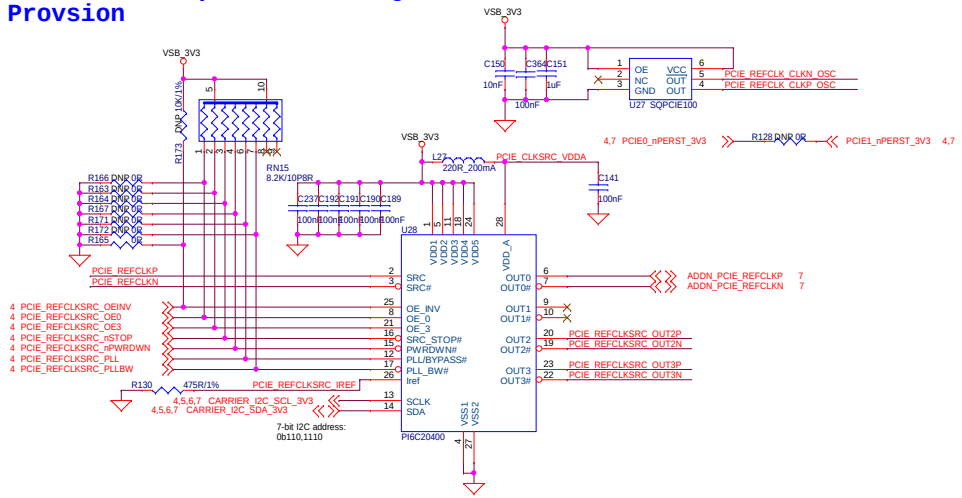
Provision to source generator source REFCLK from onboard source (U27)



Provision to allow driving a carrier board generated PCI-Express REFCLK into the CoM/SoM (through PCI-E0 refclk signals)

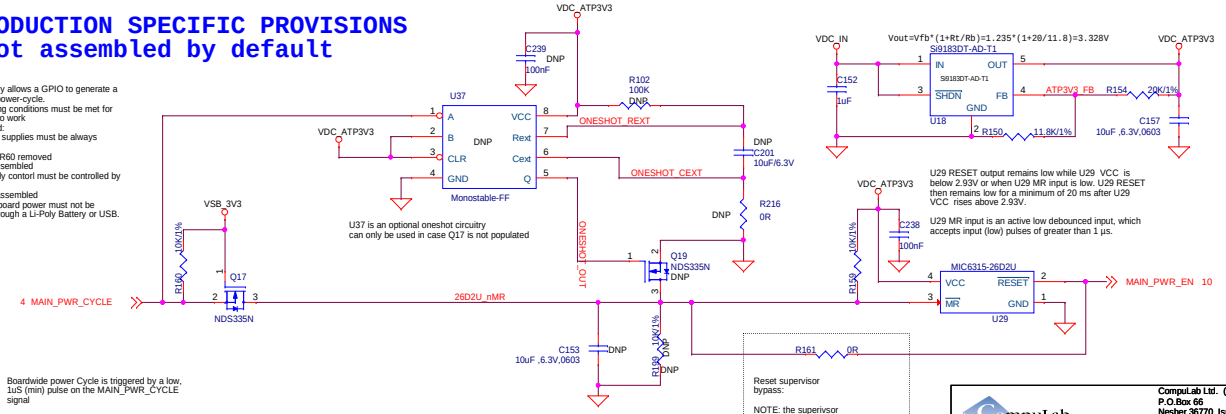


SB-SOM PCI-Express REFCLK generator Provsion



PRODUCTION SPECIFIC PROVISIONS not assembled by default

NOTE:
This circuitry allows a GPIO to generate a full board power-cycle.
The following conditions must be met for this circuit to work as designed:
1. All board supplies must be always enabled
1.1. R58 & R60 removed
1.2. R56 assembled
2. DC supply contorl must be controlled by U29
2.1. R122 assembled
3. Primary board power must not be supplied through a Li-Poly Battery or USB.



Boardwide power Cycle is triggered by a low, 1uS (min) pulse on the MAIN_PWR_CYCLE signal

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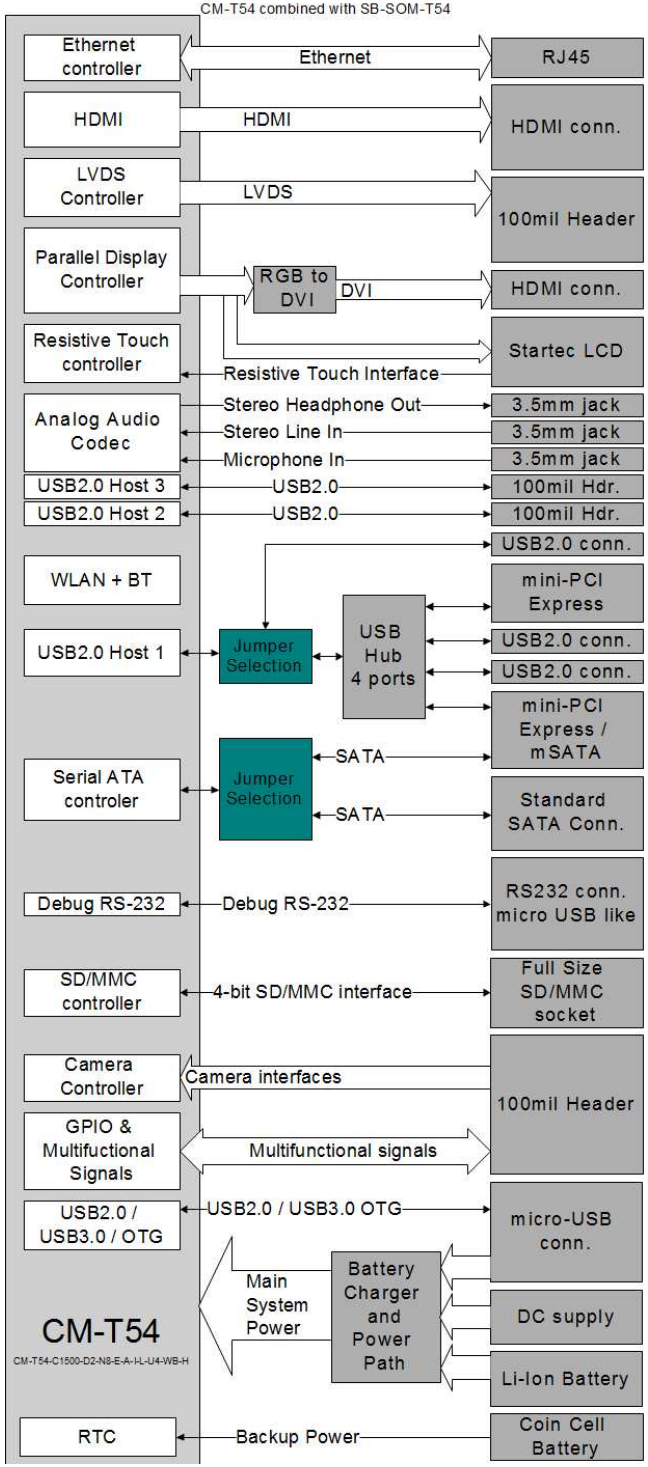
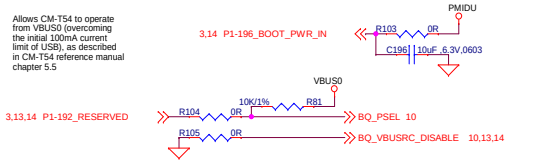
SBC2-T54

CM-T54 combined with SB-SOM-T54



SB-SOM-T54 Specific Provisions
Populated only for SB-SOM-T54

SB-SOM-T54 PRIMARY POWER from USB-OTG

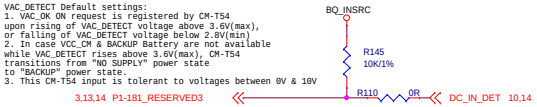


SB-SOM-T54 PRIMARY I2C BUS

SB-SOM-T54 PRIMARY DEBUG UART/RS-232

SB-SOM-T54 I2C USED FOR DVI DDC

SB-SOM-T54 AC-Adapter detection



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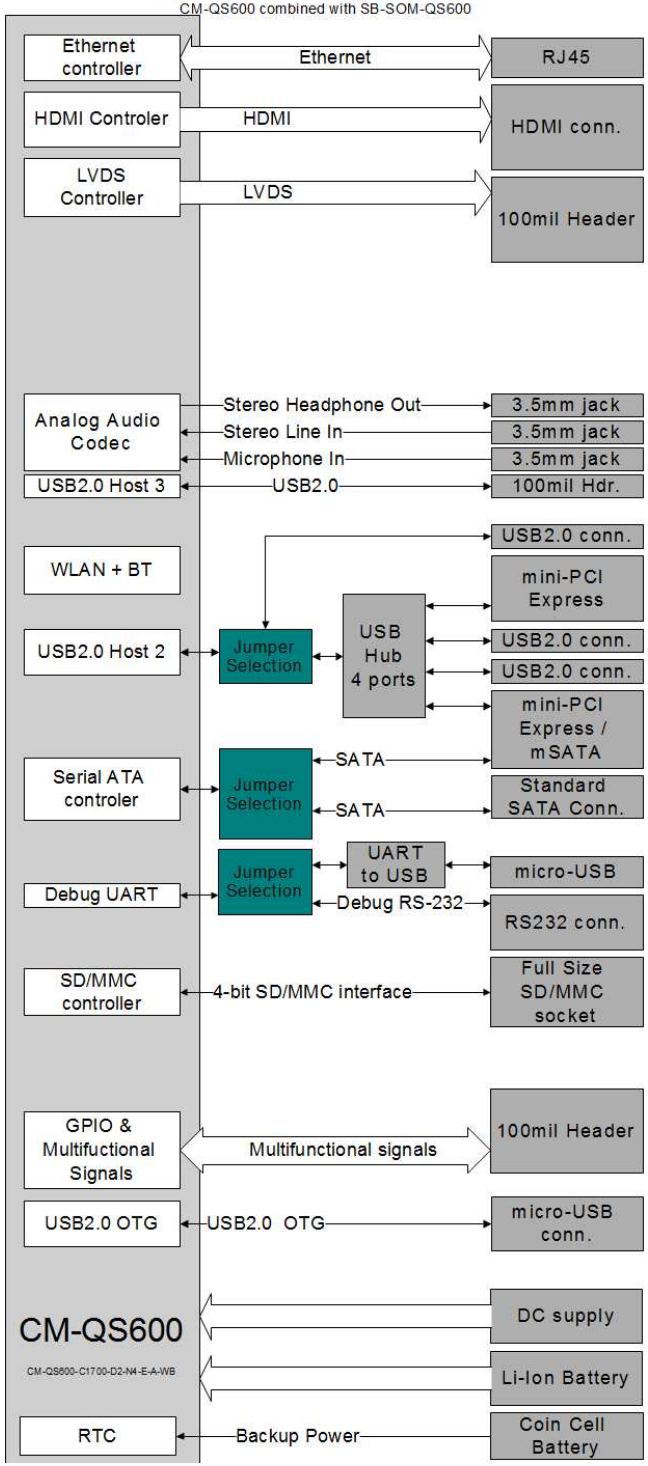
SBC2-QS600

CM-QS600 combined with SB-SOM-QS600



SB-SOM-QS600 Specific Provisions
Populated only for SB-SOM-QS600

SB-SOM-QS600 USB HOST POWER CONTROL

SB-SOM-XXX uses the 3.3V USBPWR_EN function on pin 156 of SoM/CoM interface to enable VBUS (VBUS1 rail) for the USB Hub / P26 USB conenctor (page8). Using pin 156 with SB-SOM-QS600 is not possible since a 3.3V signal is required to enable VBUS1, while a 1.8V GPIO is routed to pin 156 onboard CM-QS600.

To overcome this, we are using pin 200 of CM-QS600 interface, (which has 3.3V GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600, allowing VBUS1 control by means of 3.3V GPIO.

3,14 P1-200_GPIO7 — R149 0R — VBUS1_EN_3V3 8

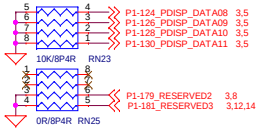
SB-SOM-QS600 USB Hub upstream port

Normally, SB-SOM-XXX uses the SoM USB2.0 port on pins 170 & 172 as the upstream USB port of the carrier USB Hub (page8). CM-QS600 does not implement a USB2.0 interface on pins 170 & 172.

To overcome this, we are using the USB port CM-QS600 implements on pins 164 & 166 as the upstream USB port of SB-SOM-QS600 USB Hub

3,8 P1-164_HSUSB2_DN — R190 0R — MUX_DN 8
3,8 P1-166_HSUSB2_DP — R191 0R — MUX_DP 8

CM-QS600 BOOT STRAPS & SEQUENCES

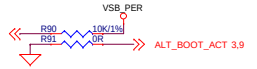


Normal Boot sequence:
1st device: CM-QS600 onboard eMMC.
2nd device: None

Alternate Boot Sequence:
1st device: SD card in SB-SOM-QS600 full size SD slot
2nd device (if bootloader no found in first device): CM-QS600 onboard eMMC.

NOTE:
While the ALT_BOOT signal logic of most CoM/SoMs is as follows:
0 ==> Normal Boot Sequence
1 ==> Alternate Boot Sequence
CM-QS600 ALT_BOOT signal logic is inverted as shown below:
0 ==> Alternate Boot Sequence.
1 ==> Normal boot sequence.

3,9 P1-185_ALT_BOOT



Power-Down Parallel RGB Shifters

Keep Parallel RGB interface disabled with SB-SOM-QS600 since this interface is not available with CM-QS600 SoM/CoM

SB-SOM-QS600 PRIMARY I2C BUS

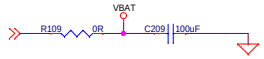
3,8 P1-69_SPI_CLK — 0R R66 — CARRIER_I2C_SCL_VPER 4,9,10,12,14
3,8 P1-58_SPI_CS0 — 0R R67 — CARRIER_I2C_SDA_VPER 4,9,10,12,14

SB-SOM-QS600 POWER

SB-SOM-QS600 power from USB is not supported.
BQ24161 VBUS input is always disabled

This enables operation of CM-QS600 from battery
Please note that while CM-QS600 power can be supplied directly from battery, most carrier board components require DC power source to be available for normal operation

3,12,14 P1-192_RESERVED

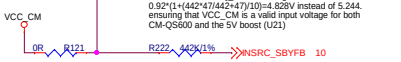


This makes sure U25 is in HIGH-Z mode as soon as voltage BQ_INSRC is available

10 BQ24161_CD — 0R R221 — BQ_INSRC

This makes sure BQ_INSRC voltage is set to 0.92*(1+(442*47/442+47)/10)=4.828V instead of 5.244. ensuring that VCC_CM is a valid input voltage for both CM-QS600 and the 5V boost (U21)

This bypasses U25 entirely, so that VCC_CM is valid for CM-QS600 (4.35V < VCC_CM < 5.5V)



SB-SOM-QS600 GPIO Expander Interrupt

SB-SOM-XXX uses the GPIO function on pin 60 of SoM/CoM interface as an interrupt for SB-SOM-XXX onboard gpio-expander.
Using pin 60 with CM-QS600 is not possible since no GPIO is available on CM-QS600 pin 60 under certain conditions (with WB option of SoM).
To overcome this we are using pin 161 of SoM/CoM interface, (which has GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600

3,8,12 P1-161_GPIO4 — R131 0R — EXPANDER_nINT 4

SB-SOM-QS600 Ethernet LEDs

NOTE: QS600 ethernet controller must be properly configured for ethernet LEDs to operate correctly since default config does not comply with SODIMM204 pinout

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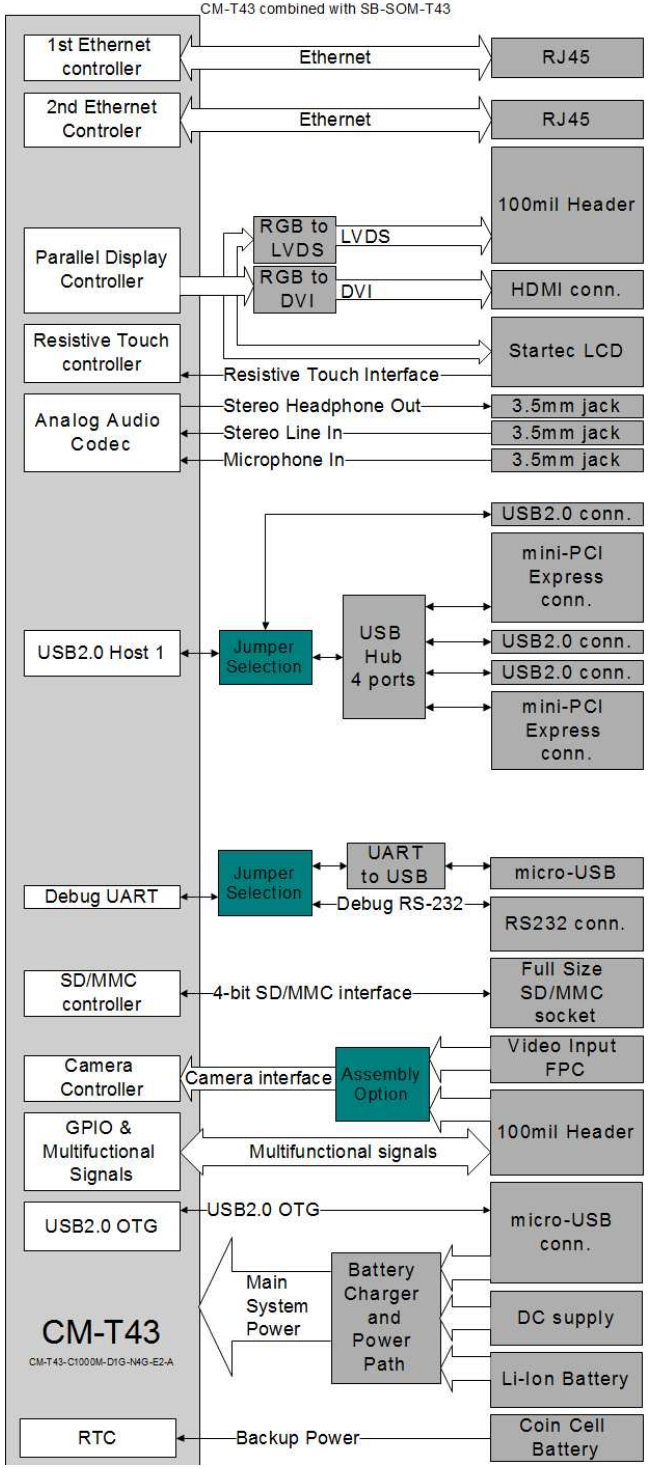
SBC-T43

CM-T43 combined with SB-SOM-T43

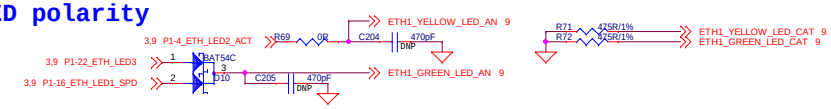


SB-SOM-T43 Specific Provisions
Populated only for SB-SOM-T43

Ethernet LED polarity

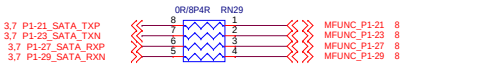
While in most cases the ethernet LED control signals (SoM pins 4, 16 & 22) are active Low, CM-T43 ethernet leds are active high.

This provision allows correct LED control with SB-SOM-T43



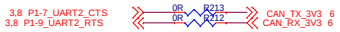
Alternate usage of SATA signals

CM-T43 does not implement the SATA interface.
This provision allows SB-SOM-T43 to route signals otherwise used for SATA, to a 100mil header



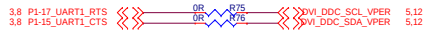
SB-SOM-T43 PRIMARY I2C BUS

SB-SOM-T43 CAN BUS



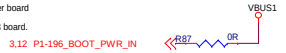
SB-SOM-T43 PRIMARY DEBUG UART/RS-232

SB-SOM-T43 I2C USED FOR DVI DDC



USB1 Host VBUS monitoring

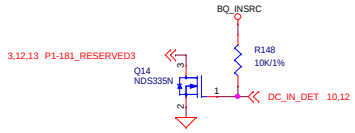
CM-T43 does not implement the BOOT_PWR_IN function on carrier board interface pin 196.
This provision allows CM-T43 to monitor VBUS1 with SB-SOM-T43 board.



SB-SOM-T43 AC POWER & Detection

CM-T43 pin 181 = AC_DET

AC_DET Default settings:
1. Pulled to VCC_CM onboard CM-T43
2. Falling edge on AC_DET triggers transition of CM-T43 from OFF/SUSPED to WAIT_PWR_EN state.
Normally, CM-T43 then transitions from WAIT_PWR_EN to ACTIVE state within 20seconds.

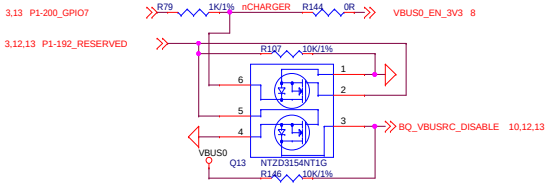


USB CHARGER LOGIC

CM-T43 drives P1-192_RESERVED HIGH (3.3V) whenever a USB charger is detected on the device/host USB port (pins 176 & 178).

This circuitry will make sure of the following:
When CM-T43 detects a charger
1. Carrier board cannot generate VBUS0
2. VCC_CM generation from VBUS0 is allowed

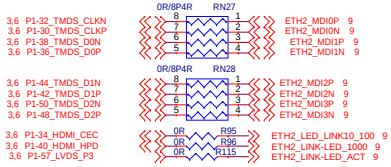
When CM-T43 does not detect a charger
1. Carrier board can generate VBUS0
2. VCC_CM cannot be generated from VBUS0



CM-T43 2nd ETHERNET (Alternate usage of HDMI signals)

CM-T43 does not implement the HDMI interface.
CM-T43 implements a 2nd ethernet interface, using the signals normally used for HDMI.

This provision allows SB-SOM-T43 to route signals otherwise used for HDMI, to the secondary RJ-45 connector allowing SB-SOM-T43 to make use of the 2nd ethernet port available with CM-T43



LVDS SOURCE

The LVDS display connector is driven by the SB-SOM-T43 onboard RGB-to-LVDS transceiver since CM-T43 does not implement the LVDS interface on the SoM itself

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