CL-SOM-AM57x

Reference Guide

Compulab

CompuLab Ltd.
P.O. Box 687 Yokneam Illit
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.co.il
Fax: +972 (4) 8325251

Table of Contents

Table 1 Revision Notes

Date	Description
Nov 2015	First release

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-AM57x System-on-Module.

1.2 CL-SOM-AM57x Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-AM57x part number: http://www.compulab.co.il/products/computer-on-modules/cl-som-am57x-ti-am5728-am5718-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-AM57x Developer Resources	http://www.compulab.com/

2 OVERVIEW

2.1 Highlights

- Texas Instruments Sitara AM57x processors, 1.5GHz
- Up to 4GB DDR3 and 32GB on-board eMMC
- PowerVR SGX544 GPU, 1080p VPU and C66x DSP
- Dual-band 802.11a/b/g/n WiFi and Bluetooth 4.1 BLE
- 2x PCIe, 2x GbE, SATA, USB3, 3x USB2, 9x UART, 87x GPIO
- Miniature size: 60 x 68 x 5 mm

CL-SOM-AM57x is a miniature System-on-Module / Computer-on-Module designed as a building block for integration into embedded applications. CL-SOM-AM57x is built around the Texas Instruments Sitara AM57x ARM Cortex-A15 System-on-Chip family. The SoC is supplemented with up-to 4GB DDR3 and 32GB of on-board eMMC storage.

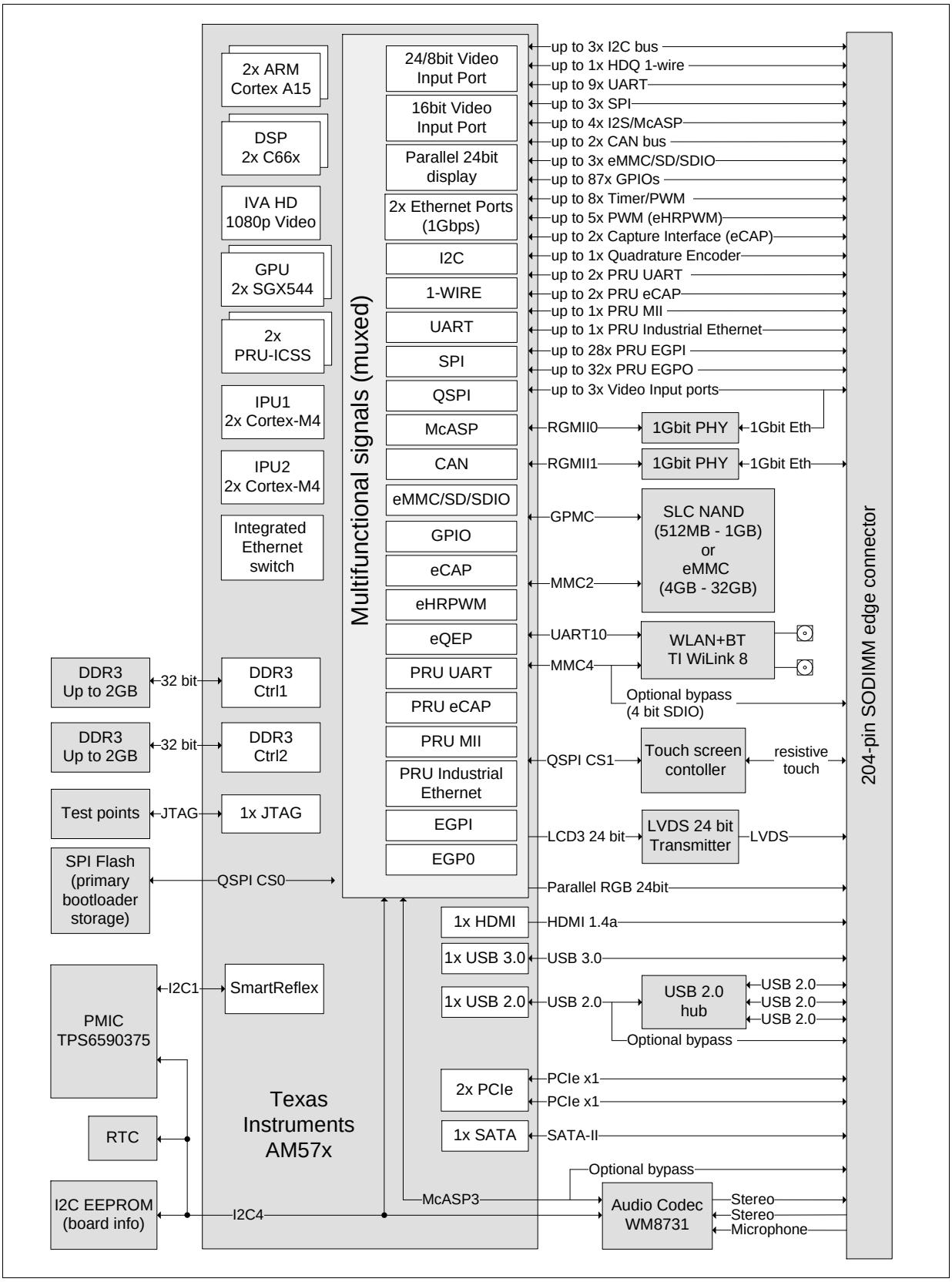
Featuring an unprecedented set of dedicated graphics acceleration and video processing engines, CL-SOM-AM57x delivers high-performance multimedia and image processing capabilities. Dual C66x DSP cores and dedicated dual-core ARM Cortex-M4 IPUs make CL-SOM-AM57x a powerful platform for image and video processing systems, while dual PowerVR SGX544 GPU and IVA-HD video sub-system enable multimedia demanding applications.

Delivering a wide range of embedded interfaces and a PRU-ICSS coprocessor dedicated for real-time processing and industrial protocols, CL-SOM-AM57x is an ideal selection for industrial automation and control systems. Dual Gbit Ethernet, 2x2 MIMO dual-band 802.11a/b/g/n WiFi and Bluetooth 4.1 make CL-SOM-AM57x an excellent solution for networking, communications and IoT applications.

CL-SOM-AM57x is provided with comprehensive documentation and full ready-to-run SW packages for the Linux operating system.

2.2 Block Diagram

Figure 1 CL-SOM-AM57x Block Diagram



2.3 CL-SOM-AM57x Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “not”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	Texas Instruments Sitara AM5728 dual-core ARM Cortex-A15, 1.5GHz NEON SIMD and VFPv4	C1500D
	Texas Instruments Sitara AM5718 single-core ARM Cortex-A15, 1.5GHz. NEON SIMD and VFPv4	C1500
DSP	Up to 2x TMS320C66x DSP cores	C1500x
GPU	Up to 2x PowerVR SGX544 3D GPU cores	C1500x
	Vivante GC320 2D GPU	+
Video	IVA-HD video sub-system supporting 1080p HD decoding / encoding	+
Image Processing	2x dual-core ARM Cortex-M4 IPU, 213MHz	+
Real-Time Coprocessor	2x PRU-ICSS supporting EtherCAT, PROFIBUS, PROFINET, EtherNet/IP and Powerlink protocols	+
Memory and Storage		
RAM	512MB – 4GB, DDR3-1333, single / dual channel 32-bit data bus	D
Storage	On-board SLC NAND flash, 512MB – 1GB	N
	On-board eMMC flash, 4GB - 32GB	
Display and Camera		
Display	Parallel RGB, 24-bit, up to 1920 x 1200	+
	HDMI 1.4a, up to 1920 x 1200	+
	LVDS, up to 1920 x 1080	L
Touchscreen	On-board 4-wire resistive touch-screen controller	I
	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	Up to 3x parallel camera interfaces	+
Network		
Gigabit Ethernet	Up to 2x 10/100/1000Mbps Ethernet ports (MAC+PHY)	E1/E2
WiFi	802.11b/g/n WiFi interface TI WiLink 8 WL1801 chipset	W
	Dual-band 2x2 802.11a/b/g/n WiFi interface TI WiLink 8 WL1837 chipset	WAB
Bluetooth	Bluetooth 4.1 BLE	WAB
Audio		
Analog Audio	Audio codec with stereo output, stereo input and microphone support	A
Digital Audio	Up to 4x I2S digital audio interfaces	+
	HDMI audio output	+
I/O		
PCI Express	2x PCIe x1 Gen. 2	+
SATA	SATA-II, 3Gbps	+
USB	1x USB3.0 dual-role + 1x USB2.0 host	U2
	1x USB3.0 dual-role + 3x USB2.0 host	U4
Serial Ports (UARTs)	Up to 9x UART ports, 16C750 compatible, up to 12 Mbps	+
CAN bus	Up to 2x CAN bus	+
MMC/SD/SDIO	Up to 3x MMC/SD/SDIO interfaces	+
SPI	Up to 3x SPI bus interfaces	+
I2C	Up to 3x I2C interfaces	+
1-Wire	1-Wire interface	+
Timer/PWM	Up to 8x Timer/PWM outputs	+
GPIO	Up to 87x GPIO signals (shared with other functions)	+
System Logic		
RTC	Real time clock, powered by external lithium battery	+

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	4.2V to 5V
Digital I/O voltage	3.3V
Active power consumption	2.5 – 6.5 W, depending on board configuration and system workload
Mechanical Specifications	
Dimensions	60 x 68 x 5 mm
Weight	35 gram
Connectors	204-pin SO-DIMM edge connector
Environmental and Reliability	
MTTF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 AM57x SoC

The TI Sitara AM57x system-on-chip (SoC) is built around dual-core ARM Cortex-A15 CPU. Dual C66x VLIW DSP cores and dedicated ARM Cortex-M4 IPUs make AM572x a powerful platform for image and video processing systems, while dual PowerVR SGX544 GPU and IVA-HD video sub-system enable multimedia demanding applications.

- Up to 1500-MHz Sitara™ ARM® Single/Dual Cortex®-A15 32-Bit RISC processor
  - NEON™ SIMD Coprocessor and Vector Floating Point (VFPv4) per CPU
  - 32-KiB instruction and 32-KiB data level 1 (L1) cache per CPU
  - Shared 1-MiB/2-MiB level 2 (L2) cache
  - On-Chip 512KiB/2.5MiB Shared Memory (RAM)
  - 48-KiB bootable ROM
- Up to 2 C66x™ Floating-Point VLIW DSP
- Image and video accelerator high-definition (IVA-HD) subsystem
- Two ARM® Dual Cortex®-M4 Image Processing Units (IPUs)
- Single/Dual-Core PowerVR® SGX544™ 3D GPU
- 2D-Graphics Accelerator (BB2D) Subsystem, including Vivante™ GC320 Core
- Crypto Hardware Accelerators (AES, SHA, RNG, DES and 3DES)
- Two dual-core Programmable Real-time Unit and Industrial Communication Subsystems (PRUICSS)

Figure 2 AM572x Block Diagram

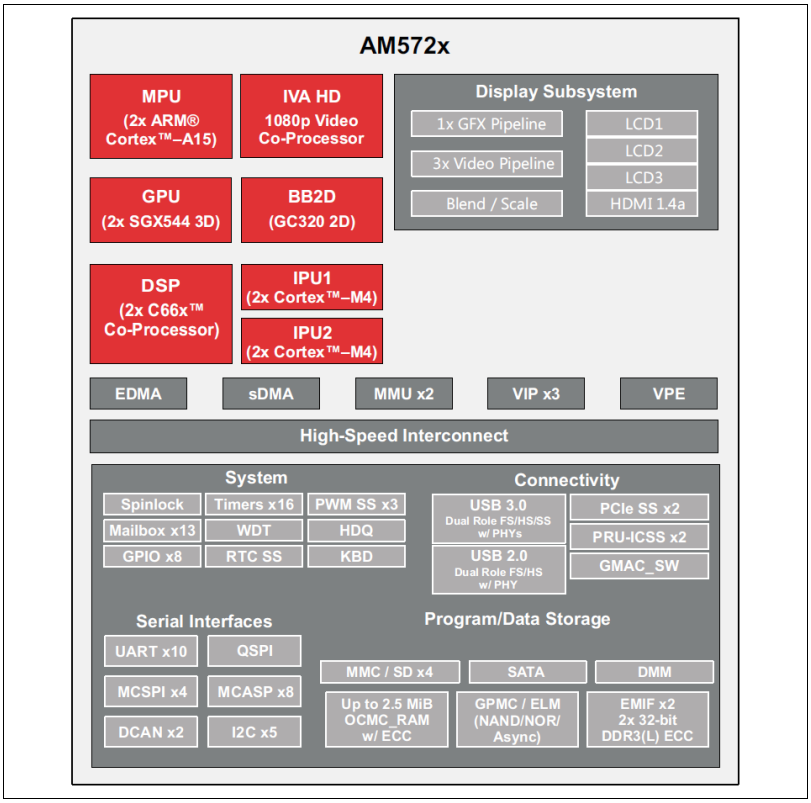
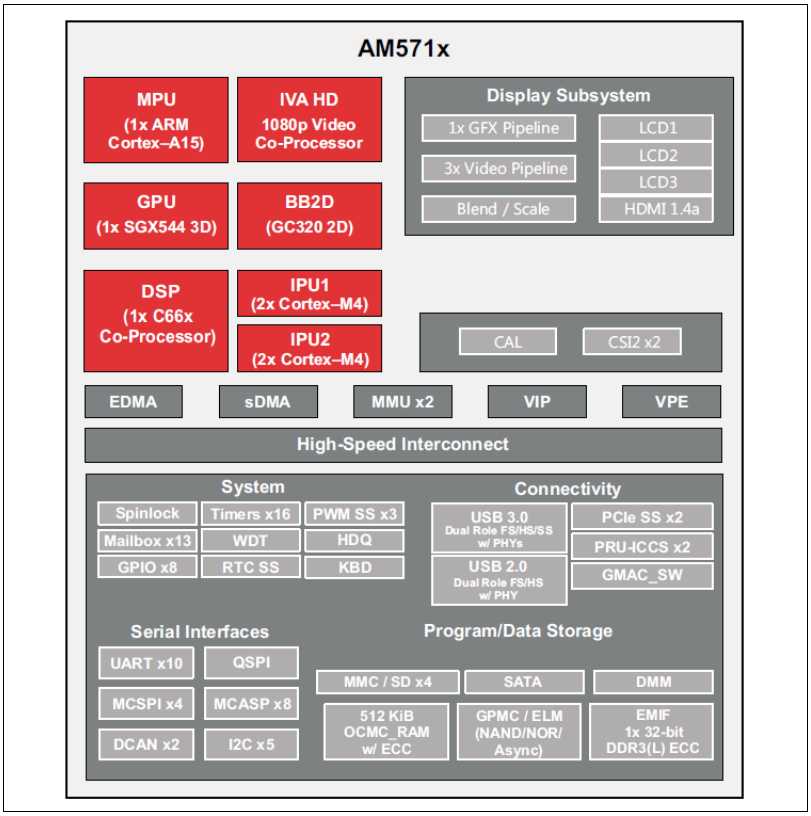


Figure 3 AM571x Block Diagram



3.1.1 DSP Subsystem

The AM57x SoC includes up to two identical instances (DSP1 and DSP2) of a digital signal processor (DSP), based on the TI's standard TMS320C66x™ DSP CorePac core.

Each of the two DSP subsystems integrated in the device includes the following components:

- A TMS320C66x™ CorePac DSP core
- Dedicated enhanced data memory access engine – EDMA
- A level 2 (L2) interconnect network (DSP NoC)
- Two memory management units (on EDMA L2 interconnect and DSP MDMA paths)
- Dedicated system control logic (DSP_SYSTEM)

3.1.2 Dual Cortex-M4 IPU Subsystem

The AM57x SoC instantiates two dual Cortex™-M4 image processor unit (IPU) subsystems:

- IPU1 subsystem is available for general purpose usage
- IPU2 subsystem is dedicated to IVA support and is not available for other processing

Each IPU subsystem integrates the following:

- Two ARM Cortex-M4 microprocessors
  - ARMv7-M and Thumb®-2 instruction set architecture (ISA)
  - ARMv6 SIMD and digital signal processor (DSP) extensions
  - Single-cycle MAC
  - Integrated nested vector interrupt controller (NVIC)
  - Integrated bus matrix
- Unicache interface
- Level 2 (L2) master interface (MIF) splitter
- On-chip ROM and banked RAM memory

3.1.3 Display Subsystem

The AM57x display subsystem provides the control signals required to interface the device system memory frame buffer (SDRAM) directly to the displays. It supports hardware cursor, independent gamma curve on all interfaces, multiple-buffer, and programmable color phase rotation.

3.1.4 3D Graphics Accelerator

The AM57x 3D graphics processing unit (GPU) accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications. It is based on the POWERVR® SGX544 core from Imagination Technologies which includes the following key features:

- 2D and 3D graphics
- API support for industry standards: OpenGL® - ES 1.1 and 2.0
- Multicore GPU architecture (with SGX544-MP2 core)
- Tile-based deferred rendering architecture
- Universal Scalable Shader Engine (USSE™)
- Present and texture load accelerator (PTLA)

3.1.5 2D Graphics Accelerator

The 2D graphics accelerator subsystem accelerates 2D graphics applications. The 2D graphics accelerator subsystem is based on the GC320 2D GPU core from Vivante Corporation. The hardware acceleration is brought to numerous 2D applications, including on-screen display and touch screen user interfaces, graphical user interfaces (GUIs) and menu displays, flash animation, and gaming. The GC320 2D Main Features include the following:

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw™
- BB2D architecture
- Hardware acceleration for DirectFB

3.1.6 PRU-ICSS

There are two Programmable Real-time Unit and Industrial Communication Subsystems (PRU-ICSS) in the device. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos and others.

Each PRU-ICSS consists of dual 32-bit RISC cores (Programmable Real-Time Units, or PRUs), shared data and instruction memories, internal peripheral modules, and an interrupt controller (INTC). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device. The PRU-ICSS Key Features are:

- Supports Protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos and more
- Two Programmable Real-Time Units (PRUs) Subsystems With Two PRU Cores Each
  - Each Core is a 32-bit load/store RISC CPU core
  - 12-KiB program RAM per PRU CPU
  - 8-KiB data RAM per PRU CPU
  - Enhanced General-Purpose Inputs (EGPI) and Enhanced General-Purpose Outputs (EGPO)
- 32-KiB general purpose memory RAM (signified RAM2) shared between PRU0 and PRU1
- Peripherals Inside the PRU-ICSS:
  - One Ethernet MII_RT module
  - One MDIO Port
  - Industrial Ethernet Peripheral (IEP)
  - 16550-compatible UART with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS
  - Industrial Ethernet timer with 7/9 capture and 8 compare events
  - Enhanced Capture Module (ECAP)
  - Interrupt Controller

3.2 Memory

3.2.1 DRAM

AM5728 includes two 32-bit DDR controllers (EMIF1 and EMIF2). AM5718 includes one 32-bit DDR controller (EMIF1).

CL-SOM-AM57x is equipped with up to 4GB of onboard DDR3 memory. The DDR3 data bus is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

NOTE: 2GB and 4GB DDR3 memory capacities are available with C1500D option only.

3.2.2 SPI Flash (Boot-loader)

CL-SOM-AM57x is assembled with 2MBytes of SPI NOR flash. The SPI NOR flash is used for boot-loader and configuration blocks storage.

3.2.3 NAND and eMMC (OS & User data)

CL-SOM-AM57x is available with optional on-board storage designed to store the operating system and user data. One of the following storage devices can be used as the main on-board storage:

- eMMC flash (up to 32GB).
- SLC NAND Flash (up to 1GB).

NOTE: SLC NAND and eMMC are mutually exclusive configuration options.

4 PERIPHERAL INTERFACES

CL-SOM-AM57x implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-AM57x CoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Many of the CL-SOM-AM57x carrier board interface pins are multifunctional. Up-to 16 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5 of this document.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the CL-SOM-AM57x digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-AM57x Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CL-SOM-AM57x. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"IOD"**– Digital Input/Output with Open Drain buffer (not pulled up on-board CL-SOM-AM57x unless otherwise noted).
- **"D"** – Open Drain Signal (not pulled up on-board CL-SOM-AM57x unless otherwise noted).
- **"DS"** – Differential Signaling
- **"PWR"** – Power
- "**SPU" –** Software controlled pull up to 3.3V

- "**SPD" –** Software controlled pull down to GND
- **"PU18**" – Always pulled up to 1.8V on-board CL-SOM-AM57x, (typ. 5KΩ-15KΩ).
- **"PUSUPPLY**" – Always pulled up to CoM/SoM Supply Voltage on-board CL-SOM-AM57x, (typ. 5KΩ-15KΩ).
- **"PD" -** Always pulled down on-board CL-SOM-AM57x, (typ. 5KΩ-15KΩ).

4.1 Display Interface

CL-SOM-AM57x display interface is derived from the AM57x display subsystem. The display subsystem key features are:

- Support of hardware cursor, independent gamma curve on all interfaces, multiple-buffer, and programmable color phase rotation
- Display controller:
  - Three video pipelines, one graphic pipeline, and one write-back pipeline
  - Three LCD outputs, each one with dedicated overlay manager, for support of active matrix color displays (up to 24-bit interface)
  - One TV output with dedicated overlay manager to support HDMI v1.4a interface (1080p @ 60 fps video and multichannel audio)

For additional details on display subsystem, please refer to the Sitara AM57x technical reference manual.

4.1.1 Parallel RGB

CL-SOM-AM57x provides access to the main LCD output (DPI1), referred in Sitara AM57x technical reference manual as "VOUT1". The main features of VOUT1 interface are:

- 24-bit parallel CMOS output interface (DPI) (MIPI DPI 2.0, BT-656, or BT-1120)
- Supporting up to WUXGA (1920 x 1200) with reduced blanking periods.

For additional details on display subsystem, please refer to the Sitara AM57x technical reference manual.

The table below summarizes the Parallel RGB interface signals.

Table 5 Parallel RGB Interface Signals

Signal Name	Pin #	Type	Description	Availability
VOUT1_CLK	98*	O	Video Output 1 Clock output	Always
VOUT1_DE	104*	O	Video Output 1 Data Enable output	Always
VOUT1_FLD	161*	O	Video Output 1 Field ID output. This signal is not used for embedded sync modes.	Always
VOUT1_HSYNC	100*	O	Video Output 1 Horizontal Sync output.This signal is not used for embedded sync modes.	Always
VOUT1_VSYNC	102*	O	Video Output 1 Vertical Sync output.This signal is not used for embedded sync modes.	Always
VOUT1_D0	106*	O	Video Output 1 Data output	Always
VOUT1_D1	108*	O	Video Output 1 Data output	Always
VOUT1_D2	110*	O	Video Output 1 Data output	Always
VOUT1_D3	112*	O	Video Output 1 Data output	Always
VOUT1_D4	116*	O	Video Output 1 Data output	Always
VOUT1_D5	118*	O	Video Output 1 Data output	Always
VOUT1_D6	120*	O	Video Output 1 Data output	Always
VOUT1_D7	122*	O	Video Output 1 Data output	Always
VOUT1_D8	124*	O	Video Output 1 Data output	Always
VOUT1_D9	126*	O	Video Output 1 Data output	Always
VOUT1_D10	128*	O	Video Output 1 Data output	Always
VOUT1_D11	130*	O	Video Output 1 Data output	Always
VOUT1_D12	134*	O	Video Output 1 Data output	Always
VOUT1_D13	136*	O	Video Output 1 Data output	Always
VOUT1_D14	138*	O	Video Output 1 Data output	Always
VOUT1_D15	140*	O	Video Output 1 Data output	Always
VOUT1_D16	94*	O	Video Output 1 Data output	Always
VOUT1_D17	92*	O	Video Output 1 Data output	Always
VOUT1_D18	142*	O	Video Output 1 Data output	Always
VOUT1_D19	144*	O	Video Output 1 Data output	Always

Signal Name	Pin #	Type	Description	Availability
VOUT1_D20	146*	O	Video Output 1 Data output	Always
VOUT1_D21	148*	O	Video Output 1 Data output	Always
VOUT1_D22	74*	O	Video Output 1 Data output	Always
VOUT1_D23	76*	O	Video Output 1 Data output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.1.2 HDMI

CL-SOM-AM57x HDMI interface is derived from the Sitara AM57x HDMI module. The HDMI module converts the RGB video into standard high-definition digital video format. The HDMI module provides the following key features:

- HDMI 1.4a (1080p @ 60 fps video and multichannel audio)
  - HDMI 1.4a and DVI 1.0 compliant
  - 36-bit RGB color
  - HDCP 1.4 key protection
  - Deep color mode support (10-bit/12-bit for 148.5-MHz pixel clock)

The table below summarizes the HDMI interface signals.

Table 6 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI1_CEC	34*	IOD	HDMI consumer electronic control	Always
HDMI1_CEC	56*	IOD	HDMI consumer electronic control	With "C1500"
HDMI1_HPD	40*	I	HDMI display hot plug detect	Always
HDMI1_HPD	54*	I	HDMI display hot plug detect	With "C1500"
HDMI1_DDC_SCL	25*	IOD	HDMI display data channel clock	Always
HDMI1_DDC_SDA	31*	IOD	HDMI display data channel data	Always
HDMI1_CLOCKX	30	ODS	HDMI clock differential positive or negative	Always
HDMI1_CLOCKY	32	ODS	HDMI clock differential positive or negative	Always
HDMI1_DATA0X	36	ODS	HDMI data 0 differential positive or negative	Always
HDMI1_DATA0Y	38	ODS	HDMI data 0 differential positive or negative	Always
HDMI1_DATA1X	42	ODS	HDMI data 1 differential positive or negative	Always
HDMI1_DATA1Y	44	ODS	HDMI data 1 differential positive or negative	Always
HDMI1_DATA2X	48	ODS	HDMI data 2 differential positive or negative	Always
HDMI1_DATA2Y	50	ODS	HDMI data 2 differential positive or negative	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.1.3 LVDS

LVDS interface is derived from an on-board SN75LVDS83B FlatLink™ transmitter. The transmitter is interfaced with the AM57x Parallel RGB interface "vout3". The LVDS transmitter supports the following key features:

- Transfer rate up to 135 Mpps, pixel clock frequency range 10 MHz to135 MHz
- Suited for display resolutions ranging from HVGA up to HD with low EMI
- Operates From a Single 3.3-V Supply

For additional details on the LVDS Transmitter, please refer to the TI SN75LVDS83B datasheet. The table below summarizes the LVDS interface signals.

Table 7 LVDS Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS_P0	39	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_N0	41	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_P1	45	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_N1	47	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_P2	51	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_N2	53	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_P3	57	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_N3	59	ODS	Differential LVDS data output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_CLKN	33	ODS	Differential LVDS pixel clock output, high-impedance when device in SHTDN	With "C1500D" AND "L"
LVDS_CLKP	35	ODS	Differential LVDS pixel clock output, high-impedance when device in SHTDN	With "C1500D" AND "L"

4.2 Video input port (VIP)

The camera interface available with CL-SOM-AM57x is based on the AM57x integrated Video Input Port (VIP) modules.

NOTE: All of the Camera interface pins on CL-SOM-AM57x are multifunctional. For additional details please refer to chapter 5.5 of this document.

With C1500D option (AM5728) there are 3 instantiations of the VIP (VIP1, VIP2, and VIP3) for connection to CCD cameras or BT656 compliant video encoders. On CL-SOM-AM57x based on "C1500D" the following main features are supported:

- VIP1 module with support of:
  - One 8-bit video port for parallel RGB/YUV/RAW data, up to 165 MHz
- VIP2 module with support of:
  - One 24-bit video port for parallel RGB/YUV/RAW data, up to 165 MHz
  - One 8-bit (out of 24) video port for parallel RGB/YUV/RAW data, up to 165 MHz
- VIP3 module with support of:
  - One 16-bit video port for parallel RGB/YUV/RAW data, up to 165 MHz

With C1500 option (AM5718) there is one instantiations of the VIP (VIP1) for connection to CCD cameras or BT656 compliant video encoders. On CL-SOM-AM57x based on "C1500" the following main features are supported:

- One separate 24-bit video ports for parallel RGB/YUV/RAW data, up to 165 MHz
- One separate 8-bit video ports for YUV/RAW data, up to 165 MHz

For additional details on VIP modules, please refer to the AM572x or AM571x technical reference manual.

The tables below summarizes the camera interface signals

Table 8 Camera VIP1: VIN1A (24-bit) Interface Signals

Signal Name	Type	Description
VIN1A_FLD0	I	Video Input 1 Port A Field ID input
VIN1A_DE0	I	Video Input 1 Port A Data Enable input
VIN1A_CLK0	I	Video Input 1 Port A Clock input
VIN1A_HSYNC0	I	Video Input 1 Port A Horizontal Sync input
VIN1A_VSYNC0	I	Video Input 1 Port A Vertical Sync input
VIN1A_D16	I	Video Input 1 Port A Data input
VIN1A_D17	I	Video Input 1 Port A Data input
VIN1A_D18	I	Video Input 1 Port A Data input
VIN1A_D19	I	Video Input 1 Port A Data input
VIN1A_D20	I	Video Input 1 Port A Data input
VIN1A_D21	I	Video Input 1 Port A Data input
VIN1A_D22	I	Video Input 1 Port A Data input
VIN1A_D23	I	Video Input 1 Port A Data input
VIN1A_D8	I	Video Input 1 Port A Data input
VIN1A_D9	I	Video Input 1 Port A Data input
VIN1A_D10	I	Video Input 1 Port A Data input
VIN1A_D11	I	Video Input 1 Port A Data input
VIN1A_D12	I	Video Input 1 Port A Data input
VIN1A_D13	I	Video Input 1 Port A Data input
VIN1A_D14	I	Video Input 1 Port A Data input
VIN1A_D15	I	Video Input 1 Port A Data input
VIN1A_D0	I	Video Input 1 Port A Data input
VIN1A_D1	I	Video Input 1 Port A Data input
VIN1A_D2	I	Video Input 1 Port A Data input
VIN1A_D3	I	Video Input 1 Port A Data input
VIN1A_D4	I	Video Input 1 Port A Data input
VIN1A_D5	I	Video Input 1 Port A Data input
VIN1A_D6	I	Video Input 1 Port A Data input
VIN1A_D7	I	Video Input 1 Port A Data input

NOTE: VIP1: vin1a (24-bit) Camera Interface is available with "C1500" option only.

Table 9 Camera VIP1: VIN2A (24-bit) Interface Signals

Signal Name	Type	Description
VIN2A_FLD0	I	Video Input 2 Port A Field ID input
VIN2A_DE0	I	Video Input 2 Port A Data Enable input
VIN2A_CLK0	I	Video Input 2 Port A Clock input
VIN2A_HSYNC0	I	Video Input 2 Port A Horizontal Sync input
VIN2A_VSYNC0	I	Video Input 2 Port A Vertical Sync input
VIN2A_D16	I	Video Input 2 Port A Data input
VIN2A_D17	I	Video Input 2 Port A Data input
VIN2A_D18	I	Video Input 2 Port A Data input
VIN2A_D19	I	Video Input 2 Port A Data input
VIN2A_D20	I	Video Input 2 Port A Data input
VIN2A_D21	I	Video Input 2 Port A Data input
VIN2A_D22	I	Video Input 2 Port A Data input
VIN2A_D23	I	Video Input 2 Port A Data input
VIN2A_D8	I	Video Input 2 Port A Data input
VIN2A_D9	I	Video Input 2 Port A Data input
VIN2A_D10	I	Video Input 2 Port A Data input

VIN2A_D11	I	Video Input 2 Port A Data input
VIN2A_D12	I	Video Input 2 Port A Data input
VIN2A_D13	I	Video Input 2 Port A Data input
VIN2A_D14	I	Video Input 2 Port A Data input
VIN2A_D15	I	Video Input 2 Port A Data input
VIN2A_D0	I	Video Input 2 Port A Data input
VIN2A_D1	I	Video Input 2 Port A Data input
VIN2A_D2	I	Video Input 2 Port A Data input
VIN2A_D3	I	Video Input 2 Port A Data input
VIN2A_D4	I	Video Input 2 Port A Data input
VIN2A_D5	I	Video Input 2 Port A Data input
VIN2A_D6	I	Video Input 2 Port A Data input
VIN2A_D7	I	Video Input 2 Port A Data input

NOTE: VIP1: vin2a (24-bit) Camera Interface is available with "C1500" option only.

Table 10 Camera VIP1: vin2b (8-bit) Interface Signals

Signal Name	Type	Description
VIN2B_FLD1	I	Video Input 2 Port B Field ID input
VIN2B_HSYNC1	I	Video Input 2 Port B Horizontal Sync input
VIN2B_VSYNC1	I	Video Input 2 Port B Vertical Sync input
VIN2B_D7	I	Video Input 2 Port B Data input
VIN2B_D6	I	Video Input 2 Port B Data input
VIN2B_D5	I	Video Input 2 Port B Data input
VIN2B_D4	I	Video Input 2 Port B Data input
VIN2B_D3	I	Video Input 2 Port B Data input
VIN2B_D2	I	Video Input 2 Port B Data input
VIN2B_D1	I	Video Input 2 Port B Data input
VIN2B_D0	I	Video Input 2 Port B Data input
VIN2B_DE1	I	Video Input 2 Port B Data input
VIN2B_CLK1	I	Video Input 2 Port B Clock input

Table 11 Camera VIP2: VIN4A (8-bit) Interface Signals

Signal Name	Type	Description
VIN4A_CLK0	I	Video Input 4 Port A Clock input
VIN4A_DE0	I	Video Input 4 Port A Data Enable input I
VIN4A_FLD0	I	Video Input 4 Port A Field ID input
VIN4A_HSYNC0	I	Video Input 4 Port A Horizontal Sync input
VIN4A_VSYNC0	I	Video Input 4 Port A Vertical Sync input
VIN4A_D0	I	Video Input 4 Port A Data input
VIN4A_D1	I	Video Input 4 Port A Data input
VIN4A_D2	I	Video Input 4 Port A Data input
VIN4A_D3	I	Video Input 4 Port A Data input
VIN4A_D4	I	Video Input 4 Port A Data input
VIN4A_D5	I	Video Input 4 Port A Data input
VIN4A_D6	I	Video Input 4 Port A Data input
VIN4A_D7	I	Video Input 4 Port A Data input

NOTE: VIP2: vin4a (8-bit) Camera Interface is available with "C1500D" option only.

Table 12 Camera VIP2: VIN3A (24-bit) Interface Signals

Signal Name	Type	Description
VIN3A_FLD0	I	Video Input 3 Port A Field ID input
VIN3A_DE0	I	Video Input 3 Port A Data Enable input
VIN3A_CLK0	I	Video Input 3 Port A Clock input
VIN3A_HSYNC0	I	Video Input 3 Port A Horizontal Sync input
VIN3A_VSYNC0	I	Video Input 3 Port A Vertical Sync input
VIN3A_D16	I	Video Input 3 Port A Data input
VIN3A_D17	I	Video Input 3 Port A Data input
VIN3A_D18	I	Video Input 3 Port A Data input
VIN3A_D19	I	Video Input 3 Port A Data input

VIN3A_D20	I	Video Input 3 Port A Data input
VIN3A_D21	I	Video Input 3 Port A Data input
VIN3A_D22	I	Video Input 3 Port A Data input
VIN3A_D23	I	Video Input 3 Port A Data input
VIN3A_D8	I	Video Input 3 Port A Data input
VIN3A_D9	I	Video Input 3 Port A Data input
VIN3A_D10	I	Video Input 3 Port A Data input
VIN3A_D11	I	Video Input 3 Port A Data input
VIN3A_D12	I	Video Input 3 Port A Data input
VIN3A_D13	I	Video Input 3 Port A Data input
VIN3A_D14	I	Video Input 3 Port A Data input
VIN3A_D15	I	Video Input 3 Port A Data input
VIN3A_D0	I	Video Input 3 Port A Data input
VIN3A_D1	I	Video Input 3 Port A Data input
VIN3A_D2	I	Video Input 3 Port A Data input
VIN3A_D3	I	Video Input 3 Port A Data input
VIN3A_D4	I	Video Input 3 Port A Data input
VIN3A_D5	I	Video Input 3 Port A Data input
VIN3A_D6	I	Video Input 3 Port A Data input
VIN3A_D7	I	Video Input 3 Port A Data input

NOTE: VIP2: vin3a (24-bit) Camera Interface is available with "C1500D" option only.

Table 13 Camera VIP2: VIN4A (24-bit) Interface Signals

Signal Name	Type	Description
VIN4A_FLD0	I	Video Input 4 Port A Field ID input
VIN4A_DE0	I	Video Input 4 Port A Data Enable input
VIN4A_CLK0	I	Video Input 4 Port A Clock input
VIN4A_HSYNC0	I	Video Input 4 Port A Horizontal Sync input
VIN4A_VSYNC0	I	Video Input 4 Port A Vertical Sync input
VIN4A_D16	I	Video Input 4 Port A Data input
VIN4A_D17	I	Video Input 4 Port A Data input
VIN4A_D18	I	Video Input 4 Port A Data input
VIN4A_D19	I	Video Input 4 Port A Data input
VIN4A_D20	I	Video Input 4 Port A Data input
VIN4A_D21	I	Video Input 4 Port A Data input
VIN4A_D22	I	Video Input 4 Port A Data input
VIN4A_D23	I	Video Input 4 Port A Data input
VIN4A_D8	I	Video Input 4 Port A Data input
VIN4A_D9	I	Video Input 4 Port A Data input
VIN4A_D10	I	Video Input 4 Port A Data input
VIN4A_D11	I	Video Input 4 Port A Data input
VIN4A_D12	I	Video Input 4 Port A Data input
VIN4A_D13	I	Video Input 4 Port A Data input
VIN4A_D14	I	Video Input 4 Port A Data input
VIN4A_D15	I	Video Input 4 Port A Data input
VIN4A_D0	I	Video Input 4 Port A Data input
VIN4A_D1	I	Video Input 4 Port A Data input
VIN4A_D2	I	Video Input 4 Port A Data input
VIN4A_D3	I	Video Input 4 Port A Data input
VIN4A_D4	I	Video Input 4 Port A Data input
VIN4A_D5	I	Video Input 4 Port A Data input
VIN4A_D6	I	Video Input 4 Port A Data input
VIN4A_D7	I	Video Input 4 Port A Data input

NOTE: VIP2: vin4a (24-bit) Camera Interface is available with "C1500D" option only.

Table 14 Camera VIP3: vin5a (16-bit) Interface Signals

Signal Name	Type	Description
VIN5A_CLK0	I	Video Input 5 Port A Clock input
VIN5A_DE0	I	Video Input 5 Port A Data Enable input
VIN5A_FLD0	I	Video Input 5 Port A Field ID input
VIN5A_HSYNC0	I	Video Input 5 Port A Horizontal Sync input
VIN5A_VSYNC0	I	Video Input 5 Port A Vertical Sync input
VIN5A_D0	I	Video Input 5 Port A Data input
VIN5A_D1	I	Video Input 5 Port A Data input
VIN5A_D2	I	Video Input 5 Port A Data input
VIN5A_D3	I	Video Input 5 Port A Data input
VIN5A_D4	I	Video Input 5 Port A Data input
VIN5A_D5	I	Video Input 5 Port A Data input
VIN5A_D6	I	Video Input 5 Port A Data input
VIN5A_D7	I	Video Input 5 Port A Data input
VIN5A_D8	I	Video Input 5 Port A Data input
VIN5A_D9	I	Video Input 5 Port A Data input
VIN5A_D10	I	Video Input 5 Port A Data input
VIN5A_D11	I	Video Input 5 Port A Data input
VIN5A_D12	I	Video Input 5 Port A Data input
VIN5A_D13	I	Video Input 5 Port A Data input
VIN5A_D14	I	Video Input 5 Port A Data input
VIN5A_D15	I	Video Input 5 Port A Data input

NOTE: VIP2: vin4a (24-bit) Camera Interface is available with "C1500D" option only.

4.3 PCI Express

CL-SOM-AM57x PCI Express interface is derived from the AM57x integrated PCIe module. Two instances of the PCIe are available. Two operation modes are supported with CL-SOM-AM57x:

- A single controller with two lanes (PCIe_SS1 only)
- Two separate controllers with one lane each

Each PCI Express interface supports the following features:

- Each PCIe subsystem controller has support for PCIe 2.0 mode (5.0 Gbps per lane) and 1.0 mode (2.5 Gbps per lane)
- Supports either root complex (RC) or in end point (EP) PCIe mode
- Complies with PCI local bus specification v3.0 and PCI express base standard v3.0
- Support of EP legacy mode
- Legacy PCI Interrupts reception (RC) and generation (EP)
- Automatic Lane reversal as specified in the PCI Express standard 2.0 specification (transmit and receive)

For additional details on PCI Express modules, please refer to the AM572x or AM571x technical reference manual. The tables below summarize the PCIe interface signals.

Table 15 PCIe interface signals

Signal Name	Pin #	Type	Description	Availability
LJCB_CLKP	119	IODS	PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (positive)	Always
LJCB_CLKN	121	IODS	PCIe1_PHY / PCIe2_PHY shared Reference Clock Input / Output Differential Pair (negative)	Always
PCIE_RXN0	133	IDS	PCIe1_PHY_RX Receive Data Lane 0 (negative) - mapped to PCIe_SS1 only	Always
PCIE_RXP0	131	IDS	PCIe1_PHY_RX Receive Data Lane 0 (positive) - mapped to PCIe_SS1 only	Always
PCIE_TXN0	127	ODS	PCIe1_PHY_TX Transmit Data Lane 0 (negative) - mapped to PCIe_SS1 only	Always
PCIE_TXP0	125	ODS	PCIe1_PHY_TX Transmit Data Lane 0 (positive) - mapped to PCIe_SS1 only	Always
PCIE_RXN1	167	IDS	PCIe2_PHY_RX Receive Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	With "C1500D"
PCIE_RXP1	169	IDS	PCIe2_PHY_RX Receive Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	With "C1500D"
PCIE_TXN1	173	ODS	PCIe2_PHY_TX Transmit Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	With "C1500D"
PCIE_TXP1	175	ODS	PCIe2_PHY_TX Transmit Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual lane- mode) or PCIe_SS2 (single lane- mode)	With "C1500D"
PCIE_RXN1	184*	IDS	PCIe2_PHY_RX Receive Data Lane 1 (negative) AM5718 ONLY	With "C1500"
PCIE_RXP1	182*	IDS	PCIe2_PHY_RX Receive Data Lane 1 (positive) AM5718 ONLY	With "C1500"
PCIE_TXN1	190*	ODS	PCIe2_PHY_TX Transmit Data Lane 1 (negative) AM5718 ONLY	With "C1500"
PCIE_TXP1	188*	ODS	PCIe2_PHY_TX Transmit Data Lane 1 (positive) AM5718 ONLY	With "C1500"

NOTE: Pins denoted with "*" are multifunctional when used with "C1500" option. For additional details please refer to chapter 5.5 of this document.

4.4 SATA

CL-SOM-AM57x incorporates one SATA-2 (3-Gbps) interface. The SATA controller supports the following key features:

- Serial ATA 1.5-Gbps and 3-Gbps speeds (SATA-1 and SATA-2)
- Support of all SATA power management features
- HBA port associated Internal DMA engine
- Activity LED generation

For additional details on the SATA subsystem, please refer to the Sitara AM57x technical reference manual.

The table below summarizes the SATA interface signals.

Table 16 SATA interface signals

Signal Name	Pin #	Type	Description	Availability
SATA1_RXN0	29	IDS	SATA differential negative receiver lane 0	Always
SATA1_RXP0	27	IDS	SATA differential positive receiver lane 0	Always
SATA1_TXN0	23	ODS	SATA differential negative transmitter lane 0	Always
SATA1_TXP0	21	ODS	SATA differential positive transmitter lane 0	Always
SATA1_LED	181*	O	SATA channel activity indicator	Always
SATA1_LED	56*	O	SATA channel activity indicator	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.5 USB 3.0

USB3.0 interface is derived from the Sitara AM57x SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem. USB 3.0 DRD subsystem supports following features:

- Integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY
- Supports USB Peripheral (or Device) mode at speeds SS (5Gbps), HS, FS, and LS.
- Supports USB Host mode at speeds SS (5Gbps), HS, FS, and LS.
- USB static peripheral operation
- USB static host operation
- Flexible stream allocation
- Stream priority

The table below summarizes the USB 3.0 interface signals.

Table 17 USB 3.0 (USB1 port) interface signals

Signal Name	Pin #	Type	Description	Availability
USB1_DP	176	IODS	USB1 USB2.0 differential signal pair (positive)	Always
USB1_DM	178	IODS	USB1 USB2.0 differential signal pair (negative)	Always
USB1_DRVVBUS	200*	O	USB1 Drive VBUS signal	Always
USB_RXN0	184	IDS	USB1 USB3.0 receiver negative lane	Always
USB_RXP0	182	IDS	USB1 USB3.0 receiver positive lane	Always
USB_TXN0	190	ODS	USB1 USB3.0 transmitter negative lane	Always
USB_TXP0	188	ODS	USB1 USB3.0 transmitter positive lane	Always

4.6 USB 2.0

USB2.0 interface is derived from the Sitara AM57x High-Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem. USB 2.0 DRD subsystem supports following features:

- Integrated HS/FS PHY
- Supports USB Peripheral (or Device) mode at speeds HS(480 Mbps), FS, and LS.
- Supports USB Host mode at speeds HS(480 Mbps), FS, and LS.
- USB static peripheral operation
- USB static host operation

In addition to the AM57x integrated USB2.0 DRD subsystem, the CL-SOM-AM57x is equipped with a USB2.0 hub, providing three downstream host ports. The implementation of USB2.0 hub precludes access to AM57x integrated USB2.0 DRD subsystem. The hub supports following features:

- Compliant with USB 2.0 specification

- Three downstream ports
- Downstream ports are backward compatible with FS, LS

For additional details on USB2.0 DRD subsystem of the Sitara AM57x, please refer to the AM57x technical reference manual.

Figure 3 AM572x USB2.0 sub-system

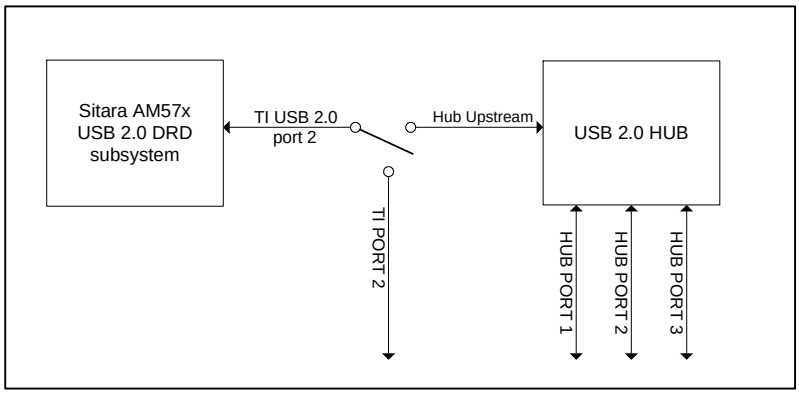


Table 18 USB 2.0 interface signals

Signal Name	Pin #	Type	Description	Availability
TI Port 1				
USB2_DP	172	IODS	USB2 USB2.0 differential signal pair (positive)	With "U2" Without "U4"
USB2_DM	170	IODS	USB2 USB2.0 differential signal pair (negative)	With "U2" Without "U4"
USB2_DRVVBUS	156	O	USB2 Drive VBUS signal. 10KΩ Pull Up onboard SOM-AM57x	With "U2" Without "U4"
HUB control				
HUB_USB_OCn	162	I	Active LOW Overcurrent Condition Detection Input. Pad internal 100K pull-up.	With "U4" Without "U2"
HUB_USB_PWREN	156	O	Power Switch Driver Output. 10KΩ Pull Up onboard SOM-AM57x	With "U4" Without "U2"
HUB Port 1				
HUBUSB1_DP	172	IODS	Downstream Port 1 differential signal pair (positive)	With "U4" Without "U2"
HUBUSB1_DN	170	IODS	Downstream Port 1 differential signal pair (negative)	With "U4" Without "U2"
HUB Port 2				
HUBUSB2_DP	166	IODS	Downstream Port 2 differential signal pair (positive)	With "U4" Without "U2"
HUBUSB2_DN	164	IODS	Downstream Port 2 differential signal pair (negative)	With "U4" Without "U2"
HUB Port 3				
HUBUSB3_DP	160	IODS	Downstream Port 3 differential signal pair (positive)	With "U4" Without "U2"
HUBUSB3_DN	158	IODS	Downstream Port 3 differential signal pair (negative)	With "U4" Without "U2"

4.7 Ethernet

CL-SOM-AM57x incorporates two full-featured 10/100/1000 Ethernet ports implemented with the Sitara AM57x integrated MAC and 3-port switch coupled with two Atheros AR8033 RGMII Ethernet PHYs. Both Ethernet interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Wire rate switching (802.1d)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D and Annex F) - inside the MAC
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation

For additional details on the Ethernet subsystem, please refer to the Sitara AM57x technical reference manual and Atheros AR8033 data sheet. For magnetics selection recommendations, please refer to section 8.3 of this document. The tables below summarize the Ethernet interface signals.

Table 19 Ethernet Port 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH1_MDI0N	6	AIO	Negative part of 100ohm diff-pair 0	With "E1" OR "E2"
ETH1_MDI0P	8	AIO	Positive part of 100ohm diff-pair 0	With "E1" OR "E2"
ETH1_MDI1N	12	AIO	Negative part of 100ohm diff-pair 1	With "E1" OR "E2"
ETH1_MDI1P	14	AIO	Positive part of 100ohm diff-pair 1	With "E1" OR "E2"
ETH1_MDI2N	18	AIO	Negative part of 100ohm diff-pair 2	With "E1" OR "E2"
ETH1_MDI2P	20	AIO	Positive part of 100ohm diff-pair 2	With "E1" OR "E2"
ETH1_MDI3N	24	AIO	Negative part of 100ohm diff-pair 3	With "E1" OR "E2"
ETH1_MDI3P	26	AIO	Positive part of 100ohm diff-pair 3	With "E1" OR "E2"
ETH1_LED_ACT	4	IO	Active High, activity LED driver, fixed 2.5V logic. 10KΩ Pull Down onboard SOM-AM57x	With "E1" OR "E2"
ETH1_LED_LINK10_100	22	IO	Active High, 10/100 link LED driver, fixed 2.5V logic. 10KΩ Pull Down onboard SOM-AM57x	With "E1" OR "E2"
ETH1_LED_LINK1000	16	IO	Active High, 1Gbps link LED driver, fixed 2.5V logic.	With "E1" OR "E2"

Table 20 Ethernet Port 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH0_MDI0N	83	AIO	Negative part of 100ohm diff-pair 0	With "E2"
ETH0_MDI0P	85	AIO	Positive part of 100ohm diff-pair 0	With "E2"
ETH0_MDI1N	77	AIO	Negative part of 100ohm diff-pair 1	With "E2"
ETH0_MDI1P	79	AIO	Positive part of 100ohm diff-pair 1	With "E2"
ETH0_MDI2N	89	AIO	Negative part of 100ohm diff-pair 2	With "E2"
ETH0_MDI2P	91	AIO	Positive part of 100ohm diff-pair 2	With "E2"
ETH0_MDI3N	101	AIO	Negative part of 100ohm diff-pair 3	With "E2"
ETH0_MDI3P	103	AIO	Positive part of 100ohm diff-pair 3	With "E2"
ETH0_LED_ACT	107	IO	Active High, activity LED driver, fixed 2.5V logic. 10KΩ Pull Down onboard SOM-AM57x	With "E2"
ETH0_LED_LINK10_100	97	IO	Active High, 10/100 link LED driver, fixed 2.5V logic. 10KΩ Pull Down onboard SOM-AM57x	With "E2"
ETH0_LED_LINK1000	109	IO	Active High, 1Gbps link LED driver, fixed 2.5V logic.	With "E2"

4.8 WLAN and Bluetooth

CL-SOM-AM57x features IEEE 802.11a/b/g/n WiFi and Bluetooth 4.1. The functionality is implemented by interfacing the TI WL1837MOD/WL1801MOD combo controller module with the Sitara AM57x MMC, McASP, and UART interfaces. Based on WiLink 8 combo chip from TI, the WL1837MOD/ WL1801MOD supports the following features:

Wi-Fi:

- WLAN Baseband Processor and RF Transceiver Support of IEEE Std 802.11a, 802.11b, 802.11g, and 802.11n
- 20- and 40-MHz SISO and 20-MHz 2 x 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP)
- 2.4-GHz MRC Support for Extended Range and 5-GHz Diversity Capable
- Fully Calibrated: Production Calibration Not Required
- Wi-Fi Direct Concurrent Operation (Multichannel, Multirole)

Bluetooth and BLE:

NOTE: Bluetooth and BLE are available with "WAB" option only

- Bluetooth 4.1 Compliance and CSA2 Support
- Host Controller Interface (HCI) Transport for Bluetooth Over UART
- Dedicated Audio Processor Support of SBC Encoding + A2DP
- Dual-Mode Bluetooth and BLE
- TI's Bluetooth and LE Certified Stack

Co-Existence:

- Wi-Fi-Bluetooth Single Antenna Coexistence

CL-SOM-AM57x is equipped with two U.FL high frequency connectors:

- Primary WLAN/BT antenna connector J1. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality.
- Secondary WLAN antenna connector J2. Can be used for 5GHz ANT diversity TX/RX , 2.4GHz MRC/MIMO only. J2 is available with "WAB" option only.

NOTE: J2 is available only with the 'WAB' configuration option.

Please refer to section 6.3 for locations of J1 and J2.

Table 21 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-SMT(01)	Hirose U.FL-LP-040

For additional details, please refer to the TI WL1837MOD or WL1801MOD datasheets.

NOTE: The WiFi module is available only with the 'W' and 'WAB' configuration option. The WiFi and Bluetooth module is available only with the 'WAB' configuration option.

4.9 Analog Audio

The CL-SOM-AM57x analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with the Sitara AM57x McASP3 interface. The codec supports the following features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

Table 22 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	R_{load} = 32Ω			30		mW
	R_{load} = 16Ω			50		
Signal-to-noise ratio, A-weighted			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω	P_{out} = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		P_{out} = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mV_{p-p}			50		dB
	20Hz – 20kHz, 100mV_{p-p}			45		
Programmable gain	1 kHz output		-73	0	6	dB
Programmable-gain step size	1 kHz			1		dB
Mute attenuation	1 kHz output, 0dB			80		dB
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0dB gain, Fsample = 48 kHz.		85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.			90		
Dynamic range	A-weighted, −60-dB full-scale input		85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain			-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mV_{p-p}			50		dB
	20Hz – 20kHz, 100mV_{p-p}			45		
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω		-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10	15		kΩ
	0 dB input gain		20	30		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0-dB gain			85		dB
Dynamic range,	A-weighted, −60-dB full-scale input			85		dB
Total harmonic distortion,	0dB input, 0dB gain			-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mV_{p-p}			50		dB
	20Hz – 20kHz, 100mV_{p-p}			45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.			34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,			14		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance				10		kΩ

Parameter	Test conditions	Min	Typ	Max	Unit
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

For additional details on the codec, please refer to the Wolfson WM8731L datasheet. The table below summarizes the analog audio interface signals.

Table 23 Analog Audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
MICBIAS	191	AP	Electret microphone bias supply	With "A"
MICIN	193	AI	Microphone input	With "A"
RLINEIN	197	AI	Right channel line input	With "A"
LLINEIN	199	AI	Left channel line input	With "A"
RHPOUT	201	AO	Right Channel Headphone Output	With "A"
LHPOUT	203	AO	Left Channel Headphone Output	With "A"

4.10 Digital Audio (McASP)

The multichannel digital audio interface available with CL-SOM-AM57x is based on the multichannel audio serial port module integrated into Sitara AM57x SoC. Up to four instances of the McASP block are available with CL-SOM-AM57x. McASP supports the following main features:

- S/PDIF, IEC60958-1, AES-3 formats
- Wide variety of I2S and similar bit-stream format
- S/PDIF, IEC60958-1, AES-3 formats - Transmit section only.
- TDM stream of 384 time slots specifically designed for easy interface to external digital interface receiver (DIR) device transmitting DIR frames to MCASP using the I2S protocol (one time slot for each DIR subframe) - Receive section.
- Programmable clock and frame sync polarity (rising or falling edge): ACLKR/X, AHCLKR/X, and AFSR/X.
- Slot length (number of bits per time slot): 8, 12, 16, 20, 24, 28, 32 bits supported.
- Word length (bits per word): 8, 12, 16, 20, 24, 28, 32 bits; always less than or equal to the time slot length.

For additional details on McASP, please refer to the Sitara AM57x technical reference manual.

NOTE: Usage of the McASP3 interface signals on the carrier board when CL-SOM-AM57x configuration includes the "A" option, will render the onboard analog audio codec inoperable.

The tables below summarize the McASP interface signals.

Table 24 McASP2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MCASP2_ACLKX	137*	IO	MCASP2 Transmit Bit Clock I/O	Always
MCASP2_FSX	145*	IO	MCASP2 Transmit Frame Sync I/O	Always
MCASP2_AXR0	139*	IO	MCASP2 Transmit/Receive Data I/O	Always
MCASP2_AXR1	143*	IO	MCASP2 Transmit/Receive Data I/O	Always
MCASP2_AHCLKX	154*	O	MCASP2 Transmit High-Frequency Master Clock I/O	Always

Table 25 McASP3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MCASP3_ACLKX	199*	IO	MCASP3 Transmit Bit Clock I/O	Without "A"
MCASP3_ACLKR	199*	IO	MCASP3 Receive Bit Clock I/O	Without "A"
MCASP3_FSX	203*	IO	MCASP3 Transmit Frame Sync I/O	Without "A"
MCASP3_FSR	203*	IO	MCASP3 Receive Frame Sync I/O	Without "A"
MCASP3_AXR0	201*	IO	MCASP2 Transmit/Receive Data I/O	Without "A"
MCASP3_AXR1	197*	IO	MCASP2 Transmit/Receive Data I/O	Without "A"
MCASP3_AHCLKX	193*	O	MCASP3 Transmit High-Frequency Master Clock I/O	Without "A"

Table 26 McASP4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MCASP4_ACLKX	13*	IO	MCASP4 Transmit Bit Clock I/O	Always
MCASP4_ACLKR	13*	IO	MCASP4 Receive Bit Clock I/O	Always
MCASP4_FSX	11*	IO	MCASP4 Transmit Frame Sync I/O	Always
MCASP4_FSR	11*	IO	MCASP4 Receive Frame Sync I/O	Always
MCASP4_AXR0	15*	IO	MCASP4 Transmit/Receive Data I/O	Always
MCASP4_AXR1	17*	IO	MCASP4 Transmit/Receive Data I/O	Always
MCASP4_AHCLKX	97*	O	MCASP4 Transmit High-Frequency Master Clock I/O	Without "E2"

Table 27 McASP5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MCASP5_ACLKX	5*	IO	MCASP5 Transmit Bit Clock I/O	Always
MCASP5_ACLKR	5*	IO	MCASP5 Receive Bit Clock I/O	Always
MCASP5_FSX	3*	IO	MCASP5 Transmit Frame Sync I/O	Always
MCASP5_FSR	3*	IO	MCASP5 Receive Frame Sync I/O	Always
MCASP5_AXR0	7*	IO	MCASP5 Transmit/Receive Data I/O	Always
MCASP5_AXR1	9*	IO	MCASP5 Transmit/Receive Data I/O	Always
MCASP5_AHCLKX	152*	O	MCASP5 Transmit High-Frequency Master Clock I/O	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.11 MMC / SD / SDIO

Up to three full featured eMMC/SD/SDIO ports are available with CL-SOM-AM57x. The ports are implemented with three instances of the eMMC/SD/SDIO host controller integrated into the Sitara AM57x SoC. The eMMC/SD/SDIOi controller is also referred to as MMCi. The following general features are supported:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MMC/eMMC standard specification, v4.5
- Full compliance with SD command/response sets as defined in the SD Physical Layer specification v3.01
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 specification v3.00
- Full compliance with SD Host Controller Standard Specification sets as defined in the SD card specification Part A2 v3.00
- Built-in 1024-byte buffer for read or write
- Supported SD v3.0 data transfer rates:
    - DS mode (3.3V IOs): up to 12 MBps (24 MHz clock)
    - HS mode (3.3V IOs): up to 24 MBps (48 MHz clock)

Each controller has the following features:

- MMC1 - 4-bit wide data bus, supports 1- and 4-bit data transfers (mainly used for connection with SD cards).
- MMC3 - 8-bit wide data bus, supports 1-, 4-, and 8-bit data transfers (mainly used for connection with SDIO cards).
- MMC4 - 4-bit wide data bus, supports 1- and 4-bit data transfers (mainly used for connection with SDIO cards).

For additional details on the MMC subsystem, please refer to the Sitara AM57x technical reference manual. The tables below summarize the MMC interface signals

Table 28 MMC 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MMC1_CLK	80	IO	MMC1 clock	Always
MMC1_CMD	82	IO	MMC1 command	Always
MMC1_SDCD	61*	I	MMC1 Card Detect	Always
MMC1_SDWP	67*	I	MMC1 Write Protect	Always
MMC1_DAT0	84	IO	MMC1 data bit 0	Always
MMC1_DAT1	86	IO	MMC1 data bit 1	Always
MMC1_DAT2	88	IO	MMC1 data bit 2	Always
MMC1_DAT3	90	IO	MMC1 data bit 3	Always

Table 29 MMC 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MMC3_CLK	75*	IO	MMC3 clock	Always
MMC3_CMD	69*	IO	MMC3 command	Always
MMC3_DAT0	63*	IO	MMC3 data bit 0	Always
MMC3_DAT1	65*	IO	MMC3 data bit 1	Always
MMC3_DAT2	58*	IO	MMC3 data bit 2	Always
MMC3_DAT3	52*	IO	MMC3 data bit 3	Always
MMC3_DAT4	202*	IO	MMC3 data bit 4	Always
MMC3_DAT5	163*	IO	MMC3 data bit 5	Always
MMC3_DAT6	194*	IO	MMC3 data bit 6	Always
MMC3_DAT7	179*	IO	MMC3 data bit 7	Always
MMC3_SDCD	40*	I	MMC3 Card Detect	Always
MMC3_SDWP	34*	I	MMC3 Write Protect	Always

Table 30 MMC 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
MMC4_CLK	157*	IO	MMC4 clock	Without "W"/ "WAB"
MMC4_CMD	147*	IO	MMC4 command	Without "W"/ "WAB"
MMC4_DAT0	155*	IO	MMC4 data bit 0	Without "W"/ "WAB"
MMC4_DAT1	153*	IO	MMC4 data bit 1	Without "W"/ "WAB"
MMC4_DAT2	151*	IO	MMC4 data bit 2	Without "W"/ "WAB"
MMC4_DAT3	149*	IO	MMC4 data bit 3	Without "W"/ "WAB"
MMC4_SDCD	60*	I	MMC4 Card Detect	Always
MMC4_SDWP	62*	I	MMC4 Card Detect	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.12 UART

CL-SOM-AM57x provides up to 9 UART ports. The functionality is derived from the UART modules integrated into the Sitara AM57x SoC. One UART port supports IrDA features. The following general features are supported:

- 16C750 compatibility
- Baud rate from 300 bps up to 12 Mbps
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- UART1 module has extended modem control signals (DCD, RI, DTR, DSR)
- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications (UART3 only).
- Support of consumer infrared (CIR) for remote control applications (UART3 only)

For additional details on UART, please refer to the Sitara AM57x technical reference manual. The tables below summarize the UART interface signals:

Table 31 UART1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1_RXD	60*	I	UART1 Receive Data Input	Always
UART1_TXD	62*	O	UART1 Transmit Data Output	Always
UART1_CTSN	157*	I	UART1 clear to send active low	Without "W"/ "WAB"
UART1_RTSN	147*	O	UART1 request to send active low	Without "W"/ "WAB"
UART1_DCDN	155*	I	UART1 Data Carrier Detect active low	Without "W"/ "WAB"
UART1_DSRN	153*	I	UART1 Data Set Ready Active Low	Without "W"/ "WAB"
UART1_DTRN	151*	O	UART1 Data Terminal Ready Active Low	Without "W"/ "WAB"
UART1_RIN	149*	I	UART1 Ring Indicator Input	Without "W"/ "WAB"

Table 32 UART2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2_RXD	155*	I	UART2 Receive Data Input	Without "W"/ "WAB"
UART2_TXD	153*	O	UART2 Transmit Data Output	Without "W"/ "WAB"
UART2_CTSN	151*	I	UART2 clear to send active low	Without "W"/ "WAB"
UART2_RTSN	149*	O	UART2 request to send active low	Without "W"/ "WAB"

Table 33 UART3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3_RXD	117*	I	UART3 Receive Data Input for both normal UART mode and IrDA mode.	Always
UART3_RXD	7*	I	UART3 Receive Data Input for both normal UART mode and IrDA mode.	Always
UART3_RXD	151*	I	UART3 Receive Data Input for both normal UART mode and IrDA mode.	Without "W"/ "WAB"
UART3_TXD	111*	O	UART3 Transmit Data Output	Always
UART3_TXD	9*	O	UART3 Transmit Data Output	Always
UART3_TXD	149*	O	UART3 Transmit Data Output	Without "W"/ "WAB"
UART3_CTSN	155*	I	UART3 clear to send active low	Without "W"/ "WAB"
UART3_RTSN	153*	O	UART3 request to send active low	Without "W"/ "WAB"
UART3_RCTX	155*	O	Remote control data output	Without "W"/ "WAB"
UART3_SD	153*	O	Infrared transceiver configure/shutdown	Without "W"/ "WAB"
UART3_IRTX	149*	O	Infrared data output	Without "W"/ "WAB"

NOTE: UART3_RXD and UART3_TXD used for debug UART by default software shipped with CL-SOM-AM57x.

Table 34 UART4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4_RXD	15*	I	UART4 Receive Data Input.	Always
UART4_RXD	40*	I	UART4 Receive Data Input.	Always
UART4_TXD	17*	O	UART4 Transmit Data Output	Always
UART4_TXD	34*	O	UART4 Transmit Data Output	Always

Table 35 UART5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART5_RXD	101*	I	UART5 Receive Data Input	Without "E2"
UART5_RXD	106*	I	UART5 Receive Data Input	Always
UART5_RXD	201*	I	UART5 Receive Data Input	Without "A"
UART5_RXD	63*	I	UART5 Receive Data Input	Always
UART5_TXD	103*	O	UART5 Transmit Data Output	Without "E2"
UART5_TXD	108*	O	UART5 Transmit Data Output	Always
UART5_TXD	197*	O	UART5 Transmit Data Output	Without "A"
UART5_TXD	65*	O	UART5 Transmit Data Output	Always
UART5_CTSN	89*	I	UART5 clear to send active low	Without "E2"
UART5_CTSN	58*	I	UART5 clear to send active low	Always
UART5_RTSN	91*	O	UART5 request to send active low	Without "E2"
UART5_RTSN	52*	O	UART5 request to send active low	Always

Table 36 UART6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART6_RXD	77*	I	UART6 Receive Data Input	Without "E2"
UART6_RXD	124*	I	UART6 Receive Data Input	Always
UART6_RXD	135*	I	UART6 Receive Data Input	Always
UART6_RXD	61*	I	UART6 Receive Data Input	Always
UART6_TXD	79*	O	UART6 Transmit Data Output	Without "E2"
UART6_TXD	126*	O	UART6 Transmit Data Output	Always
UART6_TXD	129*	O	UART6 Transmit Data Output	Always
UART6_TXD	67*	O	UART6 Transmit Data Output	Always
UART6_CTSN	83*	I	UART6 clear to send active low	Without "E2"
UART6_RTSN	85*	O	UART6 request to send active low	Without "E2"

Table 37 UART7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART7_RXD	89*	I	UART7 Receive Data Input	Without "E2"
UART7_RXD	94*	I	UART7 Receive Data Input	Always
UART7_RXD	199*	I	UART7 Receive Data Input	Without "A"
UART7_TXD	91*	O	UART7 Transmit Data Output	Without "E2"
UART7_TXD	92*	O	UART7 Transmit Data Output	Always
UART7_TXD	203*	O	UART7 Transmit Data Output	Without "A"
UART7_CTSN	201*	I	UART7 clear to send active low	Without "A"
UART7_RTSN	197*	O	UART7 request to send active low	Without "A"

Table 38 UART8 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART8_RXD	13*	I	UART8 Receive Data Input	Always
UART8_RXD	83*	I	UART8 Receive Data Input	Without "E2"
UART8_RXD	54*	I	UART8 Receive Data Input	Always
UART8_RXD	11*	O	UART8 Receive Data Input	Always
UART8_TXD	85*	O	UART8 Transmit Data Output	Without "E2"
UART8_TXD	56*	O	UART8 Transmit Data Output	Always
UART8_CTSN	15*	I	UART8 clear to send active low	Always
UART8_RTSN	17*	O	UART8 request to send active low	Always

Table 39 UART9 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART9_RXD	5*	I	UART9 Receive Data Input	Always
UART9_RXD	157*	I	UART9 Receive Data Input	Always
UART9_TXD	3*	O	UART9 Receive Data Input	Always
UART9_TXD	73*	O	UART9 Receive Data Input	Always
UART9_TXD	147*	O	UART9 Receive Data Input	Always
UART9_CTSN	7*	I	UART9 clear to send active low	Always
UART9_RTSN	9*	O	UART9 request to send active low	Always

Table 40 UART10 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART10_RXD	115*	I	UART9 Receive Data Input	Always
UART10_RXD	202*	I	UART9 Receive Data Input	Always
UART10_RXD	151*	I	UART9 Receive Data Input	Always
UART10_TXD	113*	O	UART9 Receive Data Input	Always
UART10_TXD	163*	O	UART9 Receive Data Input	Always
UART10_TXD	149*	O	UART9 Receive Data Input	Always
UART10_CTSN	194*	I	UART9 clear to send active low	Always
UART10_RTSN	179*	O	UART9 request to send active low	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.13 SPI

Up-to three SPI interfaces are accessible through the CL-SOM-AM57x carrier board interface. The SPI interfaces are derived from Sitara AM57x integrated multichannel serial port interface (McSPI). Each instance of McSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Serial clock with programmable frequency, polarity, and phase for each channel.
- Wide selection of SPI word lengths, ranging from 4 to 32 bits.
- Up to four master channels, or single channel in slave mode.
- Master multichannel mode: Full duplex/half duplex.

For additional details on McSPI, please refer to the Sitara AM57x technical reference manual. The tables below summarize the SPI interface signals

Table 41 SPI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI1_SCLK	70*	I/O	SPI1 Clock I/O	Without "I"
SPI1_D0	66*	I/O	SPI1 Data I/O. Can be configured as either MISO or MOSI.	Without "I"
SPI1_D1	68*	I/O	SPI1 Data I/O. Can be configured as either MISO or MOSI.	Without "I"
SPI1_CS0	72*	I/O	SPI1 Chip Select I/O	Without "I"
SPI1_CS1	181*	I/O	SPI1 Chip Select I/O	Always
SPI1_CS2	40*	I/O	SPI1 Chip Select I/O	Always
SPI1_CS3	34*	I/O	SPI1 Chip Select I/O	Always

Table 42 SPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI3_SCLK	117*	I/O	SPI3 Clock I/O	Always
SPI3_SCLK	102*	I/O	SPI3 Clock I/O	Always
SPI3_SCLK	69*	I/O	SPI3 Clock I/O	Always
SPI3_SCLK	13*	I/O	SPI3 Clock I/O	Always
SPI3_D0	100*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D0	65*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D0	15*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D1	111*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D1	104*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D1	63*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_D1	11*	I/O	SPI3 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI3_CS0	98*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS0	58*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS0	17*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS1	161*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS1	52*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS2	106*	I/O	SPI3 Chip Select I/O	Always
SPI3_CS3	76*	I/O	SPI3 Chip Select I/O	Always

Table 43 SPI4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI4_SCLK	5*	I/O	SPI4 Clock I/O	Always
SPI4_SCLK	202*	I/O	SPI4 Clock I/O	Always
SPI4_D0	7*	I/O	SPI4 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI4_D0	194*	I/O	SPI4 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI4_D1	73*	I/O	SPI4 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI4_D1	3*	I/O	SPI4 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI4_D1	163*	I/O	SPI4 Data I/O. Can be configured as either MISO or MOSI.	Always
SPI4_CS0	9*	I/O	SPI4 Chip Select I/O	Always
SPI4_CS0	179*	I/O	SPI4 Chip Select I/O	Always
SPI4_CS1	95*	I/O	SPI4 Chip Select I/O	Always
SPI4_CS2	111*	I/O	SPI4 Chip Select I/O	Always
SPI4_CS3	81*	I/O	SPI4 Chip Select I/O	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.14 I2C

CL-SOM-AM57x is equipped with three I2C bus interfaces: I2C2, I2C3, and I2C5. The I2C interfaces are derived from Sitara AM57x I2C controllers. I2C2 controller support Fast mode (up to 400Kbps). I2C3 and I2C5 controller support HS mode (up to 3.4Mbps). The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports a standard mode (up to 100 kbps) and fast mode (up to 400 kbps)
- Supports HS mode for transfer up to 3.4 Mbps (only for I2C3 and I2C5)
- 7-bit and 10-bit device addressing modes
- Multimaster transmitter/receiver modes (master or slave)

NOTE: I2C1 and I2C4 are used on CL-SOM-AM57x and not accessible on the interface connector.

For additional details on I2C, please refer to the Sitara AM57x technical reference manual. The tables below summarize the I2C interface signals

Table 44 I2C2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_SCL	25*	IOD	I2C2 Clock I/O	Always
I2C2_SDA	31*	IOD	I2C2 Data I/O	Always

Table 45 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SDA	49*	IOD	I2C2 Data I/O	Always
I2C3_SDA	115*	IOD	I2C2 Data I/O	Always
I2C3_SCL	43*	IOD	I2C2 Clock I/O	Always
I2C3_SCL	113*	IOD	I2C2 Clock I/O	Always

Table 46 I2C5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C5_SDA	135*	IOD	I2C2 Data I/O	Always
I2C5_SDA	5*	IOD	I2C2 Data I/O	Always
I2C5_SDA	79*	IOD	I2C2 Data I/O	Without "E2"
I2C5_SCL	129*	IOD	I2C2 Clock I/O	Always
I2C5_SCL	3*	IOD	I2C2 Clock I/O	Always
I2C5_SCL	77*	IOD	I2C2 Clock I/O	Without "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.15 CAN Bus

CL-SOM-AM57x is equipped with two instances of the CAN bus controller. Each interface is implemented with a Sitara AM57x integrated DCAN module. The following features are supported by the DCAN module:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects in a dedicated message RAM
- Support for DMA access

For additional details on DCAN, please refer to the Sitara AM57x technical reference manual. The tables below summarize the CAN bus interface signals

Table 47 CAN Bus 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
DCAN1_TX	54*	I/O	DCAN1 transmit data pin	Always
DCAN1_RX	56*	I/O	DCAN1 receive data pin	Always

Table 48 CAN Bus 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
DCAN2_TX	115*	I/O	DCAN2 transmit data pin	Always
DCAN2_TX	40*	I/O	DCAN2 transmit data pin	Always
DCAN2_RX	113*	I/O	DCAN2 receive data pin	Always
DCAN2_RX	34*	I/O	DCAN2 receive data pin	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.16 Resistive Touch-Screen

CL-SOM-AM57x features an optional on-board resistive touch-screen controller. The controller is communicating with the Sitara AM57x over the QSPI interface. The interface supports 4-wire touch panels and is available through the SBC-AM57x carrier board interface.

Table 49 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_XP	66	AIO	Touch screen X+ (right)	With "I"
TS_XN	68	AIO	Touch screen X- (left)	With "I"
TS_YP	70	AIO	Touch screen Y+ (top)	With "I"
TS_YN	72	AIO	Touch screen Y- (bottom)	With "I"

4.17 HDQ / 1-Wire

CL-SOM-AM57x features a single instance of the HDQ/1-Wire interface. The interface is derived from the HDQ1W module integrated into the Sitara AM57x SoC. HDQ1W supports the following features:

- Software selectable HDQ or 1-Wire mode
- Benchmarq HDQ protocol
- Dallas Semiconductor 1-Wire protocol
- Power-down mode

For additional details on HDQ1W, please refer to the Sitara AM57x technical reference manual. The table below summarizes the HDQ/1-wire interface signals

Table 50 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
HDQ0	152*	IOD	HDQ or 1-wire protocol single interface pin	Always
HDQ0	97*	IOD	HDQ or 1-wire protocol single interface pin	Without "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.18 GPIO

CL-SOM-AM57x provides up-to 95 GPIO signals. All GPIO signals are derived from the Sitara AM57x on-SoC GPIO modules. The GPIO pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation sub-modules to support bi-processor operations.
- Wake-up request generation in idle mode upon the detection of external events (GPIO1_* only)

For additional details on GPIO modules, please refer to the Sitara AM437x technical reference manual. The table below summarizes the GPIO interface signals

Table 51 GPIO Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1_1	192*	I	General-Purpose Input. 10K PD onboard CL-SOM-AM57x.	With "C1500D"
GPIO1_14	54*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_15	56*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_16	151*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO1_17	149*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO1_22	202*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_23	163*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_24	194*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_25	179*	IO	General-Purpose Input/Output (I/O)	Always
GPIO1_26	77*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO1_27	79*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO1_28	83*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO1_29	85	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO2_2	95*	IO	General-Purpose Input/Output (I/O)	Always
GPIO2_4	81*	IO	General-Purpose Input/Output (I/O)	Always
GPIO3_29	93*	IO	General-Purpose Input/Output (I/O)	Always
GPIO4_0	73*	IO	General-Purpose Input/Output (I/O)	Always

GPIO4_19	98*	IO	General-Purpose Input/Output (I/O)	Always
GPIO4_20	104*	IO	General-Purpose Input/Output (I/O)	Always
GPIO4_21	161*	IO	General-Purpose Input/Output (I/O)	Always
GPIO4_22	100*	IO	General-Purpose Input/Output (I/O)	Always
GPIO4_23	102*	IO	General-Purpose Input/Output (I/O)	Always
GPIO5_4	162*	IO	General-Purpose Input/Output (I/O)	Without "U4"
GPIO5_13	199*	IO	General-Purpose Input/Output (I/O)	Without "A"
GPIO5_14	203*	IO	General-Purpose Input/Output (I/O)	Without "A"
GPIO5_18	117*	IO	General-Purpose Input/Output (I/O)	Always
GPIO5_19	111*	IO	General-Purpose Input/Output (I/O)	Always
GPIO5_2	135*	IO	General-Purpose Input/Output (I/O)	Always
GPIO5_3	129*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_10	49*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_11	43*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_12	200*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_13	156*	IO	General-Purpose Input/Output (I/O)	Without "U4"
GPIO6_14	115*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_15	113*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_16	99*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_17	152*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_18	154*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_19	193*	IO	General-Purpose Input/Output (I/O)	Without "A"
GPIO6_20	97*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO6_21	80*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_22	82*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_23	84*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_24	86*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_25	88*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_26	90*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_27	61*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_28	67*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_29	75*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_30	69*	IO	General-Purpose Input/Output (I/O)	Always
GPIO6_31	63*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_0	65*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_1	58*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_10	72*	IO	General-Purpose Input/Output (I/O)	Without "I"
GPIO7_11	181*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_12	40*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_13	34*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_2	52*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_22	60*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_23	62*	IO	General-Purpose Input/Output (I/O)	Always
GPIO7_24	157*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO7_25	147*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO7_26	155*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO7_27	153*	IO	General-Purpose Input/Output (I/O)	Without "W"/ "WAB"
GPIO7_3	101*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO7_4	103*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO7_5	89*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO7_6	91*	IO	General-Purpose Input/Output (I/O)	Without "E2"
GPIO7_7	70*	IO	General-Purpose Input/Output (I/O)	Without "I"
GPIO7_8	68*	IO	General-Purpose Input/Output (I/O)	Without "I"
GPIO7_9	66*	IO	General-Purpose Input/Output (I/O)	Without "I"
GPIO8_0	106*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_1	108*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_2	110*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_3	112*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_4	116*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_5	118*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_6	120*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_7	122*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_8	124*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_9	126*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_10	128*	IO	General-Purpose Input/Output (I/O)	Always

GPIO8_11	130*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_12	134*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_13	136*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_14	138*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_15	140*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_16	94*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_17	92*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_18	142*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_19	144*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_20	146*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_21	148*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_22	74*	IO	General-Purpose Input/Output (I/O)	Always
GPIO8_23	76*	IO	General-Purpose Input/Output (I/O)	Always

4.19 Enhanced High Resolution PWM module (eHRPWM)

Three enhanced high resolution pulse width modulator (eHRPWM) module instances are accessible through the CL-SOM-AM57x carrier board interface. All eHRPWM modules are derived from the Sitara AM57x on-SoC. Each eHRPWM module supports the following features:

- Dedicated 16 bit time-base with Period / Frequency control
- Two PWM outputs (EHRPWMA and EHRPWMB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Supports Dead-band generation with independent Rising and Falling edge delay control
- Provides asynchronous over-ride control of PWM signals during fault conditions
- Supports “trip zone” allocation of both latched and un-latched fault conditions
- Allows events to trigger both CPU interrupts and start of ADC conversions
- Support PWM chopping by high frequency carrier signal, used for pulse transformer gate drives.

For additional details on eHRPWM, please refer to the Sitara AM57x technical reference manual. The tables below summarize the eHRPWM interface signals

Table 52 eHRPWM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EHRPWM1A	73*	O	EHRPWM1 Output A	Always

Table 53 eHRPWM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EHRPWM2_TRIPZONE_INPUT	75*	IO	EHRPWM2 Trip Zone Input	Always
EHRPWM2A	49*	O	EHRPWM2 Output A	Always
EHRPWM2B	43*	O	EHRPWM2 Output B	Always

Table 54 eHRPWM3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EHRPWM3_TRIPZONE_INPUT	194*	IO	EHRPWM3 Trip Zone Input	Always
EHRPWM3A	202*	O	EHRPWM3 Output A	Always
EHRPWM3B	163*	O	EHRPWM3 Output B	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.20 Enhanced Capture module (eCAP)

Two enhanced capture (eCAP) module instances are accessible through the CL-SOM-AM57x carrier board interface. All eCAP modules are derived from the Sitara AM57x on-SoC. eCAP can be used for the following applications:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)

The following features are supported with eCAP:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

For additional details on eCAP, please refer to the Sitara AM57x technical reference manual. The table below summarizes the eCAP interface signals

Table 55 eCAP Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECAP2_IN_PWM2_OUT	69*	IO	ECAP2 Capture Iniput / PWM Output	Always
ECAP3_IN_PWM3_OUT	179*	IO	ECAP3 Capture Iniput / PWM Output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.21 Quadrature Encoder Pulse module (eQEP)

One enhanced quadrature encoder pulse (eQEP3) module instance is accessible through the CL-SOM-AM57x carrier board interface. eQEP3 module is derived from the Sitara AM57x on-SoC. The eQEP3 module allows effective sensing of wheel rotation parameters such as direction and speed without software intervention. The eQEP3 inputs include two pins for quadrature-clock mode or direction-count mode, an index (or 0 marker), and a strobe input.

For additional details on eQEP3, please refer to the Sitara AM57x technical reference manual. The table below summarize the eQEP3 interface signals

Table 56 eQEP3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EQEP3A_IN	63*	I	EQEP3 Quadrature Input A	Always
EQEP3B_IN	65*	I	EQEP3 Quadrature Input B	Always
EQEP3_INDEX	58*	IO	EQEP3 Index Input	Always
EQEP3_STROBE	52*	IO	EQEP3 Strobe Input	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22 PRU-ICSS

The following interfaces are a part of the PRU-ICSS blocks of CL-SOM-AM57x. Please refer to chapter 3.1.6 of this document for additional details on PRU-ICSS.

4.22.1 PRU-ICSS MII

The PRU-ICSS MII interface is derived from Sitara AM57x on-SoC MII_RT module, featuring two MII ports and configurable connections to PRUs. For additional details on PRU-ICSS MII interface, please refer to the Sitara AM57x technical reference manual. The tables below summarize the available PRU-ICSS MII interface signals.

Table 57 PRU-ICSS2 MII Phy Control Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR2_MDIO_MDCLK	7*	O	MDIO Clock	Always
PR2_MDIO_DATA	9*	IO	MDIO Data	Always

Table 58 PRU-ICSS2 MII Port 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR2_MDIO_MDCLK	7*	O	MDIO Clock	Always
PR2_MDIO_DATA	9*	IO	MDIO Data	Always
PR2_MII1_COL	152*	I	MII1 Collision Detect	Always
PR2_MII1_CRS	154*	I	MII1 Carrier Sense	Always
PR2_MII1_RXER	201*	I	MII1 Receive Error	Without "A"
PR2_MII1_RXLINK	197*	I	MII1 Receive Link	Without "A"
PR2_MII_MT1_CLK	49*	I	MII1 Transmit Clock	Always
PR2_MII1_TXEN	43*	O	MII1 Transmit Enable	Always
PR2_MII1_TXD3	75*	O	MII1 Transmit Data	Always
PR2_MII1_TXD2	69*	O	MII1 Transmit Data	Always
PR2_MII1_TXD1	63*	O	MII1 Transmit Data	Always
PR2_MII1_TXD0	65*	O	MII1 Transmit Data	Always
PR2_MII_MR1_CLK	58*	I	MII1 Receive Clock	Always
PR2_MII1_RXDV	52*	I	MII1 Data Valid	Always
PR2_MII1_RXD3	202*	I	MII1 Receive Data	Always
PR2_MII1_RXD2	163*	I	MII1 Receive Data	Always
PR2_MII1_RXD1	194*	I	MII1 Receive Data	Always
PR2_MII1_RXD0	179*	I	MII1 Receive Data	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22.2 PRU-ICSS UART

The UART peripheral within the PRU-ICSS is based on the industry standard TL16C550 asynchronous communications element, which is a functional upgrade of the TL16C450. CL-SOM-AM57x carrier board interface features two instances of the PRU UART interface. For additional details on PRU-ICSS UART, please refer to the Sitara AM57x technical reference manual. The table below summarizes the PRUSS1_UART0 and PRUSS2_UART0 interface signals

Table 59 PRU-ICSS1 UART0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR1_UART0_CTS_N	106*	I	UART Clear-To-Send	Always
PR1_UART0_RTS_N	108*	O	UART Ready-To-Send	Always
PR1_UART0_RXD	110*	I	UART Receive Data	Always
PR1_UART0_TXD	112*	O	UART Transmit Data	Always

Table 60 PRU-ICSS2 UART0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR2_UART0_CTS_N	130*	I	UART Clear-To-Send	Always
PR2_UART0_RTS_N	134*	O	UART Ready-To-Send	Always
PR2_UART0_RXD	136*	I	UART Receive Data	Always
PR2_UART0_TXD	138*	O	UART Transmit Data	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22.3 PRU-ICSS Industrial Ethernet Peripheral

CL-SOM-AM57x carrier board interface features one instance of the PRU-ICSS integrated "industial ethernet peripheral" (IEP) interface. The IEP performs hardware work required for industrial ethernet functions. The IEP module features an industrial ethernet timer with 16 compare events and a digital I/O port (DIGIO). The industrial ethernet peripheral supports the following features:

- One master 32-bit count-up counter with an overflow status bit
- Eight 32-bit compare registers
- 8 channel digital data input and 8 channel digital data output
- Digital data out enable (optional tri-state control)
- Supports direct sampling of data in signals
- Data input sampling upon external latch event trough a dedicated latch input signal

For additional details on PRU-ICSS IEP, please refer to the Sitara AM57x technical reference manual. The table below summarizes the PRU-ICSS industrial ethernet interface signals

Table 61 PRU-ICSS IEP Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR2_EDC_LATCH0_IN	118*	I	ECAT Distributed Clock Latch In	Always
PR2_EDC_LATCH1_IN	120*	I	ECAT Distributed Clock Latch In	Always
PR2_EDC_SYNC0_OUT	122*	O	ECAT Distributed Clock Sync Out	Always
PR2_EDC_SYNC1_OUT	124*	O	ECAT Distributed Clock Sync Out	Always
PR2_EDIO_LATCH_IN	126*	I	ECAT Digital I/O Latch In	Always
PR2_EDIO_SOF	128*	O	ECAT Digital I/O Start of Frame	Always
PR2_EDIO_DATA_IN0	94*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT0	94*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN1	92*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT1	92*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN2	142*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT2	142*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN3	144*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT3	144*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN4	146*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT4	146*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN5	148*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT5	148*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN6	74*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT6	74*	O	ECAT Digital I/Os Data Out	Always
PR2_EDIO_DATA_IN7	76*	I	ECAT Digital I/Os Data In	Always
PR2_EDIO_DATA_OUT7	76*	O	ECAT Digital I/Os Data Out	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22.4 PRU-ICSS Enhanced Capture Event Module (PRU-ICSS eCAP)

A PRU-ICSS eCAP module is available with CL-SOM-AM57x. The PRU eCAP module within the PRU-ICSS is identical to the eCAP module described in chapter 4.19 above. For additional details on PRU-ICSS eCAP, please refer to the Sitara AM57x technical reference manual. The table below summarizes the PRU-ICSS eCAP interface signals

Table 62 PRU-ICSS IEP Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR1_ECAP0_ECAP_CAPIN_APWM_O	116*	IO	Capture Input / PWM output	Always
PR2_ECAP0_ECAP_CAPIN_APWM_O	140*	IO	Capture Input / PWM output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22.5 PRU-ICSS GPI / GPO

CL-SOM-AM57x features PRU-ICSS dedicated general purpose input / output signals. This functionality is derived from the PRU-ICSS Enhanced GPIO submodule integrated within the Sitara AM57x. For additional details on PRU-ICSS GPI/GPO signals, please refer to the Sitara AM57x technical reference manual. The table below summarizes the PRU-ICSS GPI/GPO interface signals.

Table 63 PRU-ICSS GPI / GPO Interface Signals

Signal Name	Pin #	Type	Description	Availability
PR2_PRU0_GPI0	112*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI1	116*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI2	118*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI3	120*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI4	122*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI5	124*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI6	126*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI7	128*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI8	130*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI9	134*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI10	136*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI11	138*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI12	140*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI13	94*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI14	92*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI15	142*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI16	144*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI17	146*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI18	148*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI19	74*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI20	76*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI0	49*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI1	43*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI2	75*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI3	69*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI4	63*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI5	65*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI6	58*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI7	52*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI8	202*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI9	163*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI10	194*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI11	179*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPI12	199*	I	PRU0 General-Purpose Input	Without "A"
PR2_PRU0_GPI13	203*	I	PRU0 General-Purpose Input	Without "A"
PR2_PRU0_GPI14	201*	I	PRU0 General-Purpose Input	Without "A"
PR2_PRU0_GPI15	197*	I	PRU0 General-Purpose Input	Without "A"
PR2_PRU0_GPI18	137*	I	PRU0 General-Purpose Input	Always

PR2_PRU0_GPI19	145*	I	PRU0 General-Purpose Input	Always
PR2_PRU0_GPO0	112*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO1	116*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO2	118*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO3	120*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO4	122*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO5	124*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO6	126*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO7	128*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO8	130*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO9	134*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO10	136*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO11	138*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO12	140*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO13	94*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO14	92*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO15	142*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO16	144*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO17	146*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO18	148*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO19	74*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO20	76*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO0	49*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO1	43*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO2	75*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO3	69*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO4	63*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO5	65*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO6	58*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO7	52*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO8	202*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO9	163*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO10	194*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO11	179*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO12	199*	O	PRU0 General-Purpose Output	Without "A"
PR2_PRU0_GPO13	203*	O	PRU0 General-Purpose Output	Without "A"
PR2_PRU0_GPO14	201*	O	PRU0 General-Purpose Output	Without "A"
PR2_PRU0_GPO15	197*	O	PRU0 General-Purpose Output	Without "A"
PR2_PRU0_GPO18	137*	O	PRU0 General-Purpose Output	Always
PR2_PRU0_GPO19	145*	O	PRU0 General-Purpose Output	Always
PR2_PRU1_GPI3	117*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI4	111*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI17	102*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI18	106*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI19	108*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI20	110*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI0	17*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI1	5*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI2	3*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI3	7*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI4	9*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI5	152*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI6	154*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI8	135*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPI9	129*	I	PRU1 General-Purpose Input	Always
PR2_PRU1_GPO3	117*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO4	111*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO17	102*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO18	106*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO19	108*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO20	110*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO0	17*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO1	5*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO2	3*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO3	7*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO4	9*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO5	152*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO6	154*	O	PRU1 General-Purpose Output	Always
PR2_PRU1_GPO8	135*	O	PRU1 General-Purpose Output	Always

PR2_PRU1_GPO9	129*	O	PRU1 General-Purpose Output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.23 Timers

CL-SOM-AM57x features 9 instances of the Sitara AM57x integrated general-purpose (GP) timers. The following main features are supported:

- Free-running 32-bit upward counter
- Compare and capture modes
- Auto reload mode
- Programmable divider clock source (2n, where n = [0:8])
- Dedicated input trigger for capture mode and dedicated output trigger/PWM signal

For additional details on (GP) timers, please refer to the Sitara AM57x technical reference manual. The table below summarizes the timers interface signals

Table 64 Timers Interface Signals

Signal Name	Pin #	Type	Description	Availability
timer1	115*	IO	PWM output/event trigger input	Always
timer2	113*	IO	PWM output/event trigger input	Always
timer3	99*	IO	PWM output/event trigger input	Always
timer6	81*	IO	PWM output/event trigger input	Always
timer8	95*	IO	PWM output/event trigger input	Always
timer13	152*	IO	PWM output/event trigger input	Always
timer14	154*	IO	PWM output/event trigger input	Always
timer15	193*	IO	PWM output/event trigger input	Without "A"
timer15	156*	IO	PWM output/event trigger input	Without "D4"
timer16	200*	IO	PWM output/event trigger input	Always
timer16	97*	IO	PWM output/event trigger input	Without "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

4.24 General Purpose Clocks

CL-SOM-AM57x features three software controlled general purpose clock outputs which can be used for devices with noncritical timing requirements. For additional details on CLKOUT signals, please refer to the Sitara AM57x technical reference manual. The table below summarizes the general purpose clocks interface signals

Table 65 General Purpose Clocks Interface Signals

Signal Name	Pin #	Type	Description	Availability
CLKOUT1	99*	O	Device Clock output 1	Always
CLKOUT2	152*	O	Device Clock output 2	Always
CLKOUT3	97*	O	Device Clock output 3. Can be used externally for devices with noncritical timing requirements, or for debug.	Without "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document.

5 SYSTEM LOGIC

CL-SOM-AM57x allows access to several system logic related signals through the carrier board interface. Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Supply

The CL-SOM-AM57x recommended supply voltage is 4.2V to 5V.

Table 66 Power signals

Signal Name	Type	Description
VSYS	P	Main power supply (5V Typ).
BACKUP_BAT	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery through a 10Ω resistor. Should be grounded if RTC functionality is not required.
GND	P	Common ground.
AUDIO_GND	P	Audio GND

5.2 Power Management

All power-management capabilities of the CL-SOM-AM57x are derived from the combination of Sitara AM57x SoC with the TPS659037 PMIC. For additional details on power management capabilities, please refer to the Sitara AM57x & TPS659037 technical reference manuals. The following table summarizes carrier board accessible power-management signals

Table 67 Power Control signals

Signal Name	Pin #	Type	Description	Availability
PWRON	165	PU	External power-on event input. Fixed PU to VSYS (120KOhm TYP). A falling edge on this signal generates ON request, which transitions the CL-SOM-AM57x from the OFF to the ACTIVE state. If PWRON button is pressed (low) while the device is on, a power-on interrupt is triggered. Keeping this pin signal constantly low more than the long-press delay, results in system switch off. The duration of long-press delay can be set by software to either 6, 8, 10, or 12 seconds.	Always
ENABLE1	198	SPD	Peripheral power request input. Software-programmable PD (400KOhm TYP). ENABLE1 is active high. This input controls TPS659037 PMIC internal step-down converter enable. TPS659037 PMIC step-down converters enable and disable is part of the flexible power-up and power-down state-machine. As option, ENABLE1 input can be mapped to any resource (LDOs, SMPS converter, or GPIO) to enable or disable it.	Always
PER_PWREN	202*	SPU	By default, this pin is a standard GPIO from Sitara AM57x, with software-programmable PU. But as an option, this pin can be connected to output from TPS659037 PMIC: REGEN1, with OTP selectable Push Pull / Open Drain. The REGEN1 output can be configured and used as enable signals for external resources, which can be included into the power-up and power-down sequence.	Always

5.3 Reset

CL-SOM-AM57x supports two reset signals: cold reset input (COLD_RESET_IN) and warm reset input (RESETN).

- Cold reset is a non-blockable reset input to the Sitara AM57x SoC, which triggers a full logic reset to CL-SOM-AM57x. The cold reset is a global reset that affects every module in the device. Generally, occurs when the device powers up or an abnormal operation is detected.

- Warm reset is also a global reset, but it occurs when the device is in normal operating state and does not affect all the modules in the device. This is often done to speed up reset recovery time. Warm reset events include software-triggered reset per power domain, watchdog time-out, externally triggered via RESETN input and emulation initiated.

The COLD_RESET_IN signal should be used as the main system reset.

Table 68 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active low cold reset input signal. Pulled to 1.8V through 10KΩ onboard CL-SOM-AM57x.	Always available
RESETN	187	I	Active low warm reset input signal. Pulled to 3.3V through 10KΩ onboard CL-SOM-AM57x.	Always available

5.4 Boot Sequence

CL-SOM-AM57x boot sequence defines which interface/media is used by CL-SOM-AM57x to load and execute the initial software. CL-SOM-AM57x can load initial software from the following interfaces/media:

- The on-board SPI Flash
- An external SD card using the MMC/SD/SDIO1 interface

CL-SOM-AM57x will query boot devices/interfaces for initial software in the order defined by the active boot sequence. Two boot sequences are supported by CL-SOM-AM57x:

- Standard sequence: designed for normal system operation (production booting) with the on-board SPI flash device as the boot media.
- Alternate sequence: allows to configure CL-SOM-AM57x for boot from SD card as a primary boot source, and on-board SPI Flash as secondary boot source.

The initial logic value of ALT_BOOT signal defines which of supported boot sequences is used by the system.

Table 69 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Boot sequence selector signal. PD through 10KΩ onboard CL-SOM-AM57x. Leave floating or low for standard boot sequence.	Always available

Table 70 CL-SOM-AM57x Boot sequences

Boot sequence	ALT_BOOT	First device	Second device
Standard	Low or floating	Onboard SPI Flash (Primary storage)	
Alternate	High	SD card	Onboard SPI Flash

5.5 Signal Multiplexing Characteristics

Up to 110 of the CL-SOM-AM57x carrier board interface signals are multifunctional. Up-to 16 functions (MUX modes) are accessible through each multifunctional signal. The multifunctional capabilities of CL-SOM-AM57x pins are derived from the Sitara AM57x SoC control module.

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 71 Multifunctional Signals

Please see the excel files attached to this document "C1500D PINMUX.xlsx" and "C1500 PINMUX.xlsx".

NOTE: In some cases "C1500 PINMUX.xlsx" table may present more than one signal per muxmode for the same ball. For more information, please refer to the Sitara AM571x technical reference manual.

5.6 RTC

The CL-SOM-AM57x RTC is implemented with external real-time clock IC. The RTC provides time and calendar information. Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. The backup battery should be connected to the BACKUP_BAT power input.

NOTE: BACKUP_BAT must remain valid at all times for proper operation of the on-board RTC.

5.7 LED

The CL-SOM-AM57x features a single general purpose green LED controlled by GPIO2_5 signal of the AM57x. The LED is ON when GPIO2_5 is logic HIGH.

6 CARRIER BOARD INTERFACE

The CL-SOM-AM57x connects to the carrier board a SODIMM-204 edge connector.

6.1 Connector Pinout

Pin #	CL-SOM-AM57x Signal Name	Reference Section		Pin #	CL-SOM-AM57x Signal Name	Reference Section
1	GND	5.1		2	TBD	
3	I2C5_SCL MCASP5_FSR MCASP5_FSX SPI4_D1 UART9_TXD VIN4A_D21 VIN1A_D21 VIN2A_D21 VIN5A_D10 VIN1A_D10 PR2_PRU1_GPI2 PR2_PRU1_GPO2	4.13 4.9 4.9 4.12 4.11 4.2 4.2 4.2 4.2 4.2 4.21 4.21		4	ETH1_LED_ACT	4.6
5	I2C5_SDA MCASP5_ACLKR MCASP5_ACLKX SPI4_SCLK UART9_RXD VIN4A_D20 VIN1A_D20 VIN2A_D20 VIN5A_D11 VIN1A_D11 PR2_PRU1_GPI1 PR2_PRU1_GPO1	4.13 4.9 4.9 4.12 4.11 4.2 4.2 4.2 4.2 4.2 4.21 4.21		6	ETH1_MDI0N	4.6
7	MCASP5_AXR0 SPI4_D0 UART3_RXD UART9_CTSN VIN4A_D22 VIN1A_D22 VIN2A_D22 VIN5A_D9 VIN1A_D9 PR2_MDIO_MDCLK PR2_PRU1_GPI3 PR2_PRU1_GPO3	4.9 4.12 4.11 4.11 4.2 4.2 4.2 4.2 4.2 4.21 4.21 4.21		8	ETH1_MDI0P	4.6
9	MCASP5_AXR1 SPI4_CS0 UART3_TXD UART9_RTSN VIN4A_D23 VIN1A_D23 VIN2A_D23 VIN5A_D8 VIN1A_D8 PR2_MDIO_DATA PR2_PRU1_GPI4 PR2_PRU1_GPO4	4.9 4.12 4.11 4.11 4.2 4.2 4.2 4.2 4.2 4.21 4.21 4.21		10	VSYS	5.1
11	MCASP4_FSR MCASP4_FSX SPI3_D1 UART8_RXD VIN4A_D17 VIN1A_D17 VIN2A_D17 VIN5A_D14 VIN1A_D14	4.9 4.9 4.12 4.11 4.2 4.2 4.2 4.2 4.2		12	ETH1_MDI1N	4.6
13	MCASP4_ACLKR MCASP4_ACLKX SPI3_SCLK UART8_RXD VIN4A_D16 VIN1A_D16 VIN2A_D16 VIN5A_D15 VIN1A_D15	4.9 4.9 4.12 4.11 4.2 4.2 4.2 4.2 4.2		14	ETH1_MDI1P	4.6

15	MCASP4_AXR0 SPI3_D0 UART4_RXD UART8_CTSN VIN4A_D18 VIN1A_D18 VIN2A_D18 VIN5A_D13 VIN1A_D13	4.9 4.12 4.11 4.11 4.2 4.2 4.2 4.2 4.2		16	ETH1_LED_LINK1000	4.6
17	MCASP4_AXR1 SPI3_CS0 UART4_TXD UART8_RTSN VIN4A_D19 VIN1A_D19 VIN2A_D19 VIN5A_D12 VIN1A_D12 PR2_PRU1_GPI0 PR2_PRU1_GPO0	4.9 4.12 4.11 4.11 4.2 4.2 4.2 4.2 4.2 4.21 4.21		18	ETH1_MDI2N	4.6
19	GND	5.1		20	ETH1_MDI2P	4.6
21	SATA1_TXP0	4.4		22	ETH1_LED_LINK10_100	4.6
23	SATA1_TXN0	4.4		24	ETH1_MDI3N	4.6
25	HDMI1_DDC_SCL I2C2_SCL	4.1.2 4.13		26	ETH1_MDI3P	4.6
27	SATA1_RXP0	4.4		28	VSYS	5.1
29	SATA1_RXN0	4.4		30	HDMI1_CLOCKX	4.1.2
31	HDMI1_DDC_SDA I2C2_SDA	4.1.2 4.13		32	HDMI1_CLOCKY	4.1.2
33	LVDS_CLKN	4.1.3		34	HDMI1_CEC DCAN2_RX GPIO7_13 MMC3_SDWP SPI1_CS3 UART4_TXD	4.1.2 4.14 4.17 4.10 4.12 4.11
35	LVDS_CLKP	4.1.3		36	HDMI1_DATA0X	4.1.2
37	GND	5.1		38	HDMI1_DATA0Y	4.1.2
39	LVDS_P0	4.1.3		40	HDMI1_HPD DCAN2_TX GPIO7_12 MMC3_SDCD SPI1_CS2 UART4_RXD	4.1.2 4.14 4.17 4.10 4.12 4.11
41	LVDS_N0	4.1.3		42	HDMI1_DATA1X	4.1.2
43	GPIO6_11 I2C3_SCL VIN2B_VSYNC1 VIN1A_DE0 VIN5A_DE0 EHRPWM2B PR2_MII1_TXEN PR2_PRU0_GPI1 PR2_PRU0_GPO1	4.17 4.13 4.2 4.2 4.2 4.18 4.21 4.21 4.21		44	HDMI1_DATA1Y	4.1.2
45	LVDS_P1	4.1.3		46	VSYS	5.1
47	LVDS_N1	4.1.3		48	HDMI1_DATA2X	4.1.2
49	GPIO6_10 I2C3_SDA VIN2B_HSYNC1 VIN1A_CLK0 VIN5A_CLK0 EHRPWM2A PR2_MII_MT1_CLK PR2_PRU0_GPI0 PR2_PRU0_GPO0	4.17 4.13 4.2 4.2 4.2 4.18 4.21 4.21 4.21		50	HDMI1_DATA2Y	4.1.2

51	LVDS_P2	4.1.3		52	GPIO7_2 MMC3_DAT3 SPI3_CS1 UART5_RTSN VIN2B_D2 VIN1A_D2 VIN5A_D2 EQEP3_STROBE PR2_MII1_RXDV PR2_PRU0_GPI7 PR2_PRU0_GPO7	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.20 4.21 4.21 4.21
53	LVDS_N2	4.1.3		54	GPIO1_14 DCAN1_TX UART8_RXD HDMI1_HPD	4.17 4.14 4.11 4.1.2
55	GND	5.1		56	SATA1_LED DCAN1_RX GPIO1_15 UART8_TXD HDMI1_CEC	4.4 4.14 4.17 4.11 4.1.2
57	LVDS_P3	4.1.3		58	GPIO7_1 MMC3_DAT2 SPI3_CS0 UART5_CTSN VIN2B_D3 VIN5A_D3 VIN1A_D3 EQEP3_INDEX PR2_MII_MR1_CLK PR2_PRU0_GPI6 PR2_PRU0_GPO6	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.20 4.21 4.21 4.21
59	LVDS_N3	4.1.3		60	GPIO7_22 MMC4_SDCD UART1_RXD	4.17 4.10 4.11
61	MMC1_SDCD GPIO6_27 UART6_RXD	4.10 4.17 4.11		62	GPIO7_23 MMC4_SDWP UART1_TXD	4.17 4.10 4.11
63	GPIO6_31 MMC3_DAT0 SPI3_D1 UART5_RXD VIN2B_D5 VIN1A_D5 VIN5A_D5 EQEP3A_IN PR2_MII1_TXD1 PR2_PRU0_GPI4 PR2_PRU0_GPO4	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.20 4.21 4.21 4.21		64	VSYS	5.1
65	GPIO7_0 MMC3_DAT1 SPI3_D0 UART5_TXD VIN2B_D4 VIN5A_D4 EQEP3B_IN PR2_MII1_TXD0 PR2_PRU0_GPI5 PR2_PRU0_GPO5	4.17 4.10 4.12 4.11 4.2 4.2 4.20 4.21 4.21 4.21		66	TS_XP GPIO7_9 SPI1_D0	4.15 4.17 4.12
67	MMC1_SDWP GPIO6_28 UART6_TXD	4.10 4.17 4.11		68	TS_XN GPIO7_8 SPI1_D1	4.15 4.17 4.12
69	GPIO6_30 MMC3_CMD SPI3_SCLK VIN2B_D6 VIN1A_D6 VIN5A_D6 ECAP2_IN_PWM2_OUT PR2_MII1_TXD2 PR2_PRU0_GPI3 PR2_PRU0_GPO3	4.17 4.10 4.12 4.2 4.2 4.2 4.19 4.21 4.21 4.21		70	TS_YP GPIO7_7 SPI1_SCLK	4.15 4.17 4.12

71	GND	5.1		72	TS_YN GPIO7_10 SPI1_CS0	4.15 4.17 4.12
73	GPIO4_0 SPI4_D1 UART9_TXD VIN2B_VSYNC1 EHRPWM1A	4.17 4.12 4.11 4.2 4.18		74	VOUT1_D22 GPIO8_22 VIN3A_D6 VIN4A_D6 VIN1A_D6 VIN2A_D6 PR2_EDIO_DATA_IN6 PR2_EDIO_DATA_OUT6 PR2_PRU0_GPI19 PR2_PRU0_GPO19	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
75	GPIO6_29 MMC3_CLK VIN2B_D7 VIN1A_D7 VIN5A_D7 EHRPWM2_TRIPZONE_INPUT PR2_MII1_TXD3 PR2_PRU0_GPI2 PR2_PRU0_GPO2	4.17 4.10 4.2 4.2 4.2 4.18 4.21 4.21 4.21		76	VOUT1_D23 GPIO8_23 SPI3_CS3 VIN3A_D7 VIN4A_D7 VIN1A_D7 VIN2A_D7 PR2_EDIO_DATA_IN7 PR2_EDIO_DATA_OUT7 PR2_PRU0_GPI20 PR2_PRU0_GPO20	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
77	ETH0_MDI1N VIN4A_D4 VIN1A_D20 VIN1A_D4 VIN2A_D4 GPIO1_26 I2C5_SCL UART6_RXD	4.6 4.2 4.2 4.2 4.2 4.17 4.13 4.11		78	VSYS	5.1
79	ETH0_MDI1P VIN4A_D5 VIN1A_D21 VIN1A_D5 VIN2A_D5 GPIO1_27 I2C5_SDA UART6_TXD	4.6 4.2 4.2 4.2 4.2 4.17 4.13 4.11		80	MMC1_CLK GPIO6_21	4.10 4.17
81	GPIO2_4 SPI4_CS3 VIN1A_VSYNC0 VIN2A_VSYNC0 TIMER6	4.17 4.12 4.2 4.2 4.22		82	MMC1_CMD GPIO6_22	
83	ETH0_MDI0N VIN4A_D6 VIN1A_D22 VIN1A_D6 VIN2A_D6 GPIO1_28 UART6_CTSN UART8_RXD	4.6 4.2 4.2 4.2 4.2 4.17 4.11 4.11		84	MMC1_DAT0 GPIO6_23	4.10 4.17
85	ETH0_MDI0P GPIO1_29 VIN4A_D7 VIN1A_D23 VIN1A_D7 VIN2A_D7 UART6_RTSN UART8_TXD	4.6 4.17 4.2 4.2 4.2 4.11 4.11		86	MMC1_DAT1 GPIO6_24	4.10 4.17
87	GND	5.1		88	MMC1_DAT2 GPIO6_25	4.10 4.17
89	ETH0_MDI2N VIN4A_D2 VIN1A_D18 VIN1A_D2 VIN2A_D2 GPIO7_5 UART5_CTSN UART7_RXD	4.6 4.2 4.2 4.2 4.2 4.17 4.11 4.11		90	MMC1_DAT3 GPIO6_26	4.10 4.17

91	ETH0_MDI2P VIN4A_D3 VIN1A_D19 VIN1A_D3 VIN2A_D3 GPIO7_6 UART5_RTSN UART7_TXD	4.6 4.2 4.2 4.2 4.2 4.17 4.11 4.11		92	VOUT1_D17 GPIO8_17 UART7_TXD VIN3A_D1 VIN4A_D1 VIN1A_D1 VIN2A_D1 PR2_EDIO_DATA_IN1 PR2_EDIO_DATA_OUT1 PR2_PRU0_GPI14 PR2_PRU0_GPO14	4.1.1 4.17 4.11 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
93	GPIO3_29 VIN2B_FLD1	4.17 4.2		94	VOUT1_D16 GPIO8_16 UART7_RXD VIN3A_D0 VIN4A_D0 VIN1A_D0 VIN2A_D0 PR2_EDIO_DATA_IN0 PR2_EDIO_DATA_OUT0 PR2_PRU0_GPI13 PR2_PRU0_GPO13	4.1.1 4.17 4.11 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
95	VIN4A_CLK0 VIN1A_CLK0 VIN2A_CLK0 GPIO2_2 SPI4_CS1 TIMER8	4.2 4.2 4.2 4.17 4.12 4.22		96	VSYS	5.1
97	ETH0_LED_LINK10_100 VIN4A_DE0 VIN1A_DE0 VIN2A_DE0 HDQ0 CLKOUT3 GPIO6_20 MCASP4_AHCLKX TIMER16	4.6 4.2 4.2 4.2 4.16 4.23 4.17 4.9 4.22		98	VOUT1_CLK GPIO4_19 SPI3_CS0 VIN3A_FLD0 VIN4A_FLD0 VIN1A_FLD0 VIN2A_FLD0	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2
99	VIN4A_FLD0 VIN1A_FLD0 VIN2A_FLD0 CLKOUT1 GPIO6_16 TIMER3	4.2 4.2 4.2 4.23 4.17 4.22		100	VOUT1_HSYNC GPIO4_22 SPI3_D0 VIN3A_HSYNC0 VIN4A_HSYNC0 VIN1A_VSYNC0 VIN2A_VSYNC0	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2
101	ETH0_MDI3N VIN4A_D0 VIN1A_D0 VIN2A_D0 VIN1A_D16 GPIO7_3 UART5_RXD	4.6 4.2 4.2 4.2 4.2 4.17 4.11		102	VOUT1_VSYNC GPIO4_23 SPI3_SCLK VIN3A_VSYNC0 VIN4A_VSYNC0 VIN1A_VSYNC0 VIN2A_VSYNC0 PR2_PRU1_GPI17 PR2_PRU1_GPO17	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2 4.21 4.21
103	ETH0_MDI3P VIN4A_D1 VIN1A_D17 VIN1A_D1 VIN2A_D1 GPIO7_4 UART5_TXD	4.6 4.2 4.2 4.2 4.2 4.17 4.11		104	VOUT1_DE GPIO4_20 SPI3_D1 VIN3A_DE0 VIN4A_DE0 VIN1A_DE0 VIN2A_DE0	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2
105	GND	5.1		106	VOUT1_D0 GPIO8_0 SPI3_CS2 UART5_RXD VIN3A_D16 VIN4A_D16 VIN1A_D16 VIN2A_D16 PR1_UART0_CTS_N PR2_PRU1_GPI18 PR2_PRU1_GPO18	4.1.1 4.17 4.12 4.11 4.2 4.2 4.21 4.21 4.21

107	ETH0_LED_ACT	4.6		108	VOUT1_D1 GPIO8_1 UART5_TXD VIN3A_D17 VIN4A_D17 VIN1A_D17 VIN2A_D17 PR1_UART0_RTS_N PR2_PRU1_GPI19 PR2_PRU1_GPO19	4.1.1 4.17 4.11 4.2 4.2 4.2 4.2 4.21 4.21 4.21
109	ETH0_LED_LINK1000	4.6		110	VOUT1_D2 GPIO8_2 VIN3A_D18 VIN4A_D18 VIN1A_D18 VIN2A_D18 PR1_UART0_RXD PR2_PRU1_GPI20 PR2_PRU1_GPO20	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
111	UART3_TXD GPIO5_19 SPI3_D1 SPI4_CS2 UART3_TXD PR2_PRU1_GPI4 PR2_PRU1_GPO4	4.11 4.17 4.12 4.12 4.11 4.20 4.20		112	VOUT1_D3 GPIO8_3 VIN3A_D19 VIN4A_D19 VIN1A_D19 VIN2A_D19 PR1_UART0_TXD PR2_PRU0_GPI0 PR2_PRU0_GPO0	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
113	VIN4A_VSYNC0 VIN1A_VSYNC0 VIN2A_VSYNC0 DCAN2_RX GPIO6_15 I2C3_SCL UART10_TXD TIMER2	4.2 4.2 4.2 4.14 4.17 4.13 4.11 4.22		114	VSYS	5.1
115	VIN4A_HSYNC0 VIN1A_HSYNC0 VIN2A_HSYNC0 DCAN2_TX GPIO6_14 I2C3_SDA UART10_RXD TIMER2	4.2 4.2 4.2 4.14 4.17 4.13 4.11 4.22		116	VOUT1_D4 GPIO8_4 VIN3A_D20 VIN4A_D20 VIN1A_D20 VIN2A_D20 PR1_ECAP0_ECAP_CAPIN_APW PR2_PRU0_GPI1 PR2_PRU0_GPO1	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
117	UART3_RXD GPIO5_18 SPI3_SCLK UART3_RXD PR2_PRU1_GPI3 PR2_PRU1_GPO3	4.11 4.17 4.12 4.11 4.19 4.19		118	VOUT1_D5 GPIO8_5 VIN3A_D21 VIN4A_D21 VIN1A_D21 VIN2A_D21 PR2_EDC_LATCH0_IN PR2_PRU0_GPI2 PR2_PRU0_GPO2	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
119	LJCB_CLKP	4.3		120	VOUT1_D6 GPIO8_6 VIN3A_D22 VIN4A_D22 VIN1A_D22 VIN2A_D22 PR2_EDC_LATCH1_IN PR2_PRU0_GPI3 PR2_PRU0_GPO3	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
121	LJCB_CLKN	4.3		122	VOUT1_D7 GPIO8_7 VIN3A_D23 VIN4A_D23 VIN1A_D23 VIN2A_D23 PR2_EDC_SYNC0_OUT PR2_PRU0_GPI4 PR2_PRU0_GPO4	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21

123	GND	5.1		124	VOUT1_D8 GPIO8_8 UART6_RXD VIN3A_D8 VIN4A_D8 VIN1A_D8 VIN2A_D8 PR2_EDC_SYNC1_OUT PR2_PRU0_GPI5 PR2_PRU0_GPO5	4.1.1 4.17 4.11 4.2 4.2 4.2 4.2 4.21 4.21 4.21
125	PCIE_TXP0	4.3		126	VOUT1_D9 GPIO8_9 UART6_TXD VIN3A_D9 VIN4A_D9 VIN1A_D9 VIN2A_D9 PR2_EDIO_LATCH_IN PR2_PRU0_GPI6 PR2_PRU0_GPO6	4.1.1 4.17 4.11 4.2 4.2 4.2 4.2 4.21 4.21 4.21
127	PCIE_TXN0	4.3		128	VOUT1_D10 GPIO8_10 VIN3A_D10 VIN4A_D10 VIN1A_D10 VIN2A_D10 PR2_EDIO_SOF PR2_PRU0_GPI7 PR2_PRU0_GPO7	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
129	GPIO5_3 I2C5_SCL UART6_TXD VIN1A_HSYNC0 PR2_PRU1_GPI9 PR2_PRU1_GPO9	4.17 4.13 4.11 4.2 4.21 4.21		130	VOUT1_D11 GPIO8_11 VIN3A_D11 VIN4A_D11 VIN1A_D11 VIN2A_D11 PR2_UART0_CTS_N PR2_PRU0_GPI8 PR2_PRU0_GPO8	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
131	PCIE_RXP0	4.3		132	VSYS	5.1
133	PCIE_RXN0	4.3		134	VOUT1_D12 GPIO8_12 VIN3A_D12 VIN4A_D12 VIN1A_D12 VIN2A_D12 PR2_UART0_RTS_N PR2_PRU0_GPI9 PR2_PRU0_GPO9	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
135	GPIO5_2 I2C5_SDA UART6_RXD VIN1A_VSYNC0 PR2_PRU1_GPI8 PR2_PRU1_GPO8	4.17 4.13 4.11 4.2 4.21 4.21		136	VOUT1_D13 GPIO8_13 VIN3A_D13 VIN4A_D13 VIN1A_D13 VIN2A_D13 PR2_UART0_RXD PR2_PRU0_GPI10 PR2_PRU0_GPO10	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
137	MCASP2_ACLKX VIN1A_D7 PR2_PRU0_GPI18 PR2_PRU0_GPO18	4.9 4.2 4.21 4.21		138	VOUT1_D14 GPIO8_14 VIN3A_D14 VIN4A_D14 VIN1A_D14 VIN2A_D14 PR2_UART0_TXD PR2_PRU0_GPI11 PR2_PRU0_GPO11	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21

139	MCASP2_AXR0 VIN4A_D10 VIN1A_D10 VIN2A_D10	4.9 4.2 4.2 4.2		140	VOUT1_D15 GPIO8_15 VIN3A_D15 VIN4A_D15 VIN1A_D15 VIN2A_D15 PR2_ECAP0_ECAP_CAPIN_APW PR2_PRU0_GPI12 PR2_PRU0_GPO12	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21
141	GND	5.1		142	VOUT1_D18 GPIO8_18 VIN3A_D2 VIN4A_D2 VIN1A_D2 VIN2A_D2 PR2_EDIO_DATA_IN2 PR2_EDIO_DATA_OUT2 PR2_PRU0_GPI15 PR2_PRU0_GPO15	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
143	MCASP2_AXR1 VIN4A_D11 VIN1A_D11 VIN2A_D11	4.9 4.2 4.2 4.2		144	VOUT1_D19 GPIO8_19 VIN3A_D3 VIN4A_D3 VIN1A_D3 VIN2A_D3 PR2_EDIO_DATA_IN3 PR2_EDIO_DATA_OUT3 PR2_PRU0_GPI16 PR2_PRU0_GPO16	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
145	MCASP2_FSX VIN1A_D6 PR2_PRU0_GPI19 PR2_PRU0_GPO19	4.9 4.2 4.21 4.21		146	VOUT1_D20 GPIO8_20 VIN3A_D4 VIN4A_D4 VIN1A_D4 VIN2A_D4 PR2_EDIO_DATA_IN4 PR2_EDIO_DATA_OUT4 PR2_PRU0_GPI17 PR2_PRU0_GPO17	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
147	GPIO7_25 MMC4_CMD UART1_RTSN UART9_TXD	4.17 4.10 4.11 4.11		148	VOUT1_D21 GPIO8_21 VIN3A_D5 VIN4A_D5 VIN1A_D5 VIN2A_D5 PR2_EDIO_DATA_IN5 PR2_EDIO_DATA_OUT5 PR2_PRU0_GPI18 PR2_PRU0_GPO18	4.1.1 4.17 4.2 4.2 4.2 4.2 4.21 4.21 4.21 4.21
149	GPIO1_17 MMC4_DAT3 UART1_RIN UART10_TXD UART2_RTSN UART3_IRTX UART3_TXD	4.17 4.10 4.11 4.11 4.11 4.11 4.11		150	VSYS	5.1
151	GPIO1_16 MMC4_DAT2 UART1_DTRN UART10_RXD UART2_CTSN UART3_RXD	4.17 4.10 4.11 4.11 4.11 4.11		152	VIN1A_D0 HDQ0 CLKOUT2 GPIO6_17 MCASP5_AHCLKX TIMER13 PR2_MII1_COL PR2_PRU1_GPI5 PR2_PRU1_GPO5	4.2 4.16 4.23 4.17 4.9 4.22 4.21 4.21 4.21
153	GPIO7_27 MMC4_DAT1 UART1_DSRN UART2_TXD UART3_RTSN UART3_SD	4.17 4.10 4.11 4.11 4.11 4.11		154	VIN1A_CLK0 MCASP2_AHCLKX GPIO6_18 TIMER14 PR2_MII1_CRS PR2_PRU1_GPI6 PR2_PRU1_GPO6	4.2 4.9 4.17 4.22 4.21 4.21 4.21

155	GPIO7_26 MMC4_DAT0 UART1_DCDN UART2_RXD UART3_CTSN UART3_RCTX	4.17 4.10 4.11 4.11 4.11 4.11		156	USB2_DRVVBUS HUB_USB_PWREN GPIO6_13 TIMER15	4.5.2.1 4.5.2.2 4.17 4.22
157	GPIO7_24 MMC4_CLK UART1_CTSN UART9_RXD	4.17 4.10 4.11 4.11		158	HUBUSB3_DN	4.5.2.2
159	GND	5.1		160	HUBUSB3_DP	4.5.2.2
161	VOUT1_FLD GPIO4_21 SPI3_CS1 VIN3A_CLK0 VIN4A_CLK0 VIN1A_CLK0 VIN1A_CLK0	4.1.1 4.17 4.12 4.2 4.2 4.2 4.2		162	HUB_USB_OCn	4.5.2.2
163	GPIO1_23 MMC3_DAT5 SPI4_D1 UART10_TXD VIN2B_D0 VIN5A_D0 VIN1A_D0 EHRPWM3B PR2_MII1_RXD2 PR2_PRU0_GPI9 PR2_PRU0_GPO9	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.18 4.21 4.21 4.21		164	HUBUSB2_DN	4.5.2.2
165	PWRON	5.2		166	HUBUSB2_DP	4.5.2.2
167	PCIE_RXN1	4.3		168	VSYS	5.1
169	PCIE_RXP1	4.3		170	USB2_DM HUBUSB1_DN	4.5.2.1 4.5.2.2
171	COLD_RESET_IN	5.3		172	USB2_DP HUBUSB1_DP	4.5.2.1 4.5.2.2
173	PCIE_TXN1	4.3		174	TBD	
175	PCIE_TXP1	4.3		176	USB1_DP	4.5.1
177	GND	5.1		178	USB1_DM	4.5.1
179	GPIO1_25 MMC3_DAT7 SPI4_CS0 UART10_RTSN VIN2B_CLK1 VIN5A_VSYNC0 VIN1A_VSYNC0 ECAP3_IN_PWM3_OUT PR2_MII1_RXD0 PR2_PRU0_GPI11 PR2_PRU0_GPO11	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.19 4.21 4.21 4.21		180	VBUS	5.1
181	SATA1_LED GPIO7_11 SPI1_CS1	4.4 4.17 4.12		182	USB_RXP0 PCIE_RXP1 (AM5718 only)	4.5.1 4.3
183	BACKUP_BAT	5.1		184	USB_RXN0 PCIE_RXN1 (AM5718 only)	4.5.1 4.3
185	ALT_BOOT	5.4		186	VSYS	5.1
187	RESETN	5.3		188	USB_TXP0 PCIE_TXP1 (AM5718 only)	4.5.1 4.3
189	FLASH_WPn			190	USB_TXN0 PCIE_TXN1 (AM5718 only)	4.5.1 4.3
191	MICBIAS	4.8		192	WAKEUP1 GPIO1_1	4.24 4.17
193	MICIN MCASP3_AHCLKX GPIO6_19 TIMER15	4.8 4.9 4.17 4.22		194	GPIO1_24 MMC3_DAT6 SPI4_D0 UART10_CTSN VIN2B_DE1 VIN5A_HSYNC0 VIN1A_HSYNC0 EHRPWM3_TRIPZONE_INPUT PR2_MII1_RXD1 PR2_PRU0_GPI10 PR2_PRU0_GPO10	4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.18 4.21 4.21 4.21

195	AUDIO_GND	5.1		196	LDOUSB_IN2	5.1
197	RLINEIN MCASP3_AXR1 UART5_TXD UART7_RTSN VIN5A_FLD0 VIN1A_D0 VIN1A_FLD0 PR2_MII1_RXLINK PR2_PRU0_GPI15 PR2_PRU0_GPO15	4.8 4.8 4.9 4.11 4.11 4.2 4.2 4.21 4.21 4.21		198	ENABLE1	5.2
199	LLINEIN MCASP3_ACLKX MCASP3_ACLKR GPIO5_13 UART7_RXD VIN1A_D3 PR2_PRU0_GPI12 PR2_PRU0_GPO12	4.8 4.9 4.9 4.17 4.11 4.2 4.21 4.21		200	USB1_DRVVBUS GPIO6_12 TIMER16	4.5.1 4.17 4.22
201	RHPOUT MCASP3_AXR0 UART5_RXD UART7_CTSN VIN1A_D1 PR2_MII1_RXER PR2_PRU0_GPI14 PR2_PRU0_GPO14	4.8 4.9 4.11 4.11 4.2 4.21 4.21 4.21		202	PER_PWREN GPIO1_22 MMC3_DAT4 SPI4_SCLK UART10_RXD VIN2B_D1 VIN5A_D1 VIN1A_D1 EHRPWM3A PR2_MII1_RXD3 PR2_PRU0_GPI8 PR2_PRU0_GPO8	5.2 4.17 4.10 4.12 4.11 4.2 4.2 4.2 4.18 4.21 4.21 4.21
203	LHPOUT MCASP3_FSX MCASP3_FSR GPIO5_14 UART7_TXD VIN1A_D2 PR2_PRU0_GPI13 PR2_PRU0_GPO13	4.8 4.9 4.9 4.17 4.11 4.2 4.21 4.21		204	VSYS	5.1

6.2 Mating Connectors

Table 72 Connector type

CL-SOM-AM57x connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 4 CL-SOM-AM57x Top

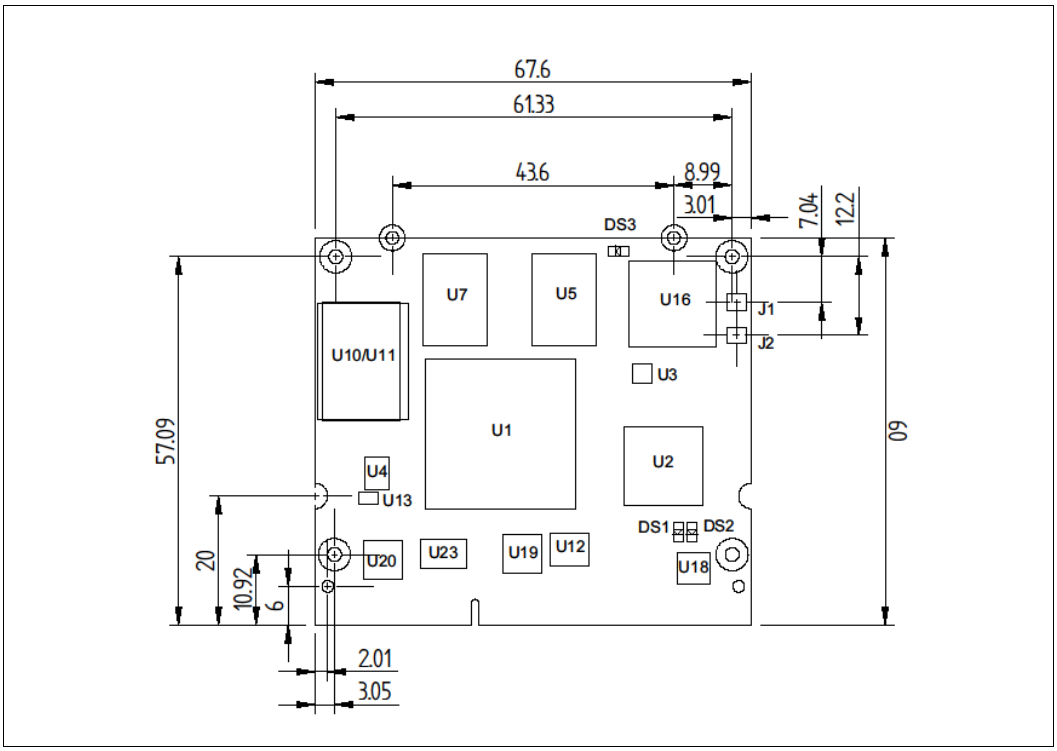
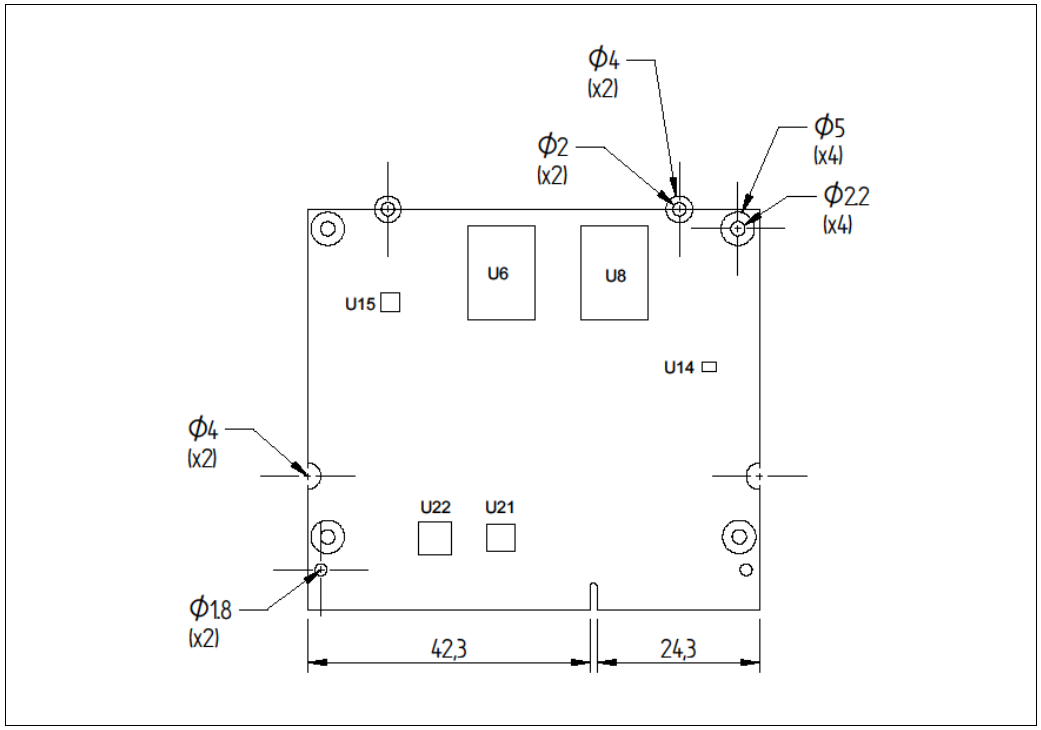


Figure 5 CL-SOM-AM57x bottom



1. All dimensions are in millimeters.
2. Max height of components on module Bottom Side is 2.8mm.
3. Baseboard connectors provide 2.8mm board-to-board clearance.
4. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at http://www.compulab.co.il/products/computer-on-modules/cl-som-am57x-ti-am5728-am5718-system-on-module/#devres

6.4 Heat Spreader and Cooling Solutions

CompuLab provides CL-SOM-AM57x with a dedicated heat-spreader assembly. The CL-SOM-AM57x heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the CL-SOM-AM57x temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

Documentation and CAD drawings for the CL-SOM-AM57x heat-spreader and cooling solutions are provided at http://www.compulab.co.il/products/computer-on-modules/cl-som-am57x-ti-am5728-am5718-system-on-module/#devres.

6.5 Standoffs/Spacers

CL-SOM-AM57x has two mounting half holes to physically secure the CoM/SoM to the carrier board. Secure CL-SOM-AM57x to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 2.2±0.2 mm length

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 73 Absolute Maximum ratings

Parameter	Condition	Min	Max	Unit
Main power supply voltage (VSYS)		-0.3	6	V
Backup battery supply voltage (BACKUP_BAT)		-0.3	6	V
VBUS input		-2	20	V
LDOUSB_IN2 (LDOUSB regulator input voltage in PMIC)		-0.3	20	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 74 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	Normal operation	3.8		5.25	V
Backup battery supply voltage (VCC_RTC)		1.4		5.5	V
VBUS input		0	5.0	5.25	V
LDOUSB_IN2 (LDOUSB regulator input voltage in PMIC)		4.3		5.25	V

7.3 DC Electrical Characteristics

Table 75 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{IH}		2			V
V_{IL}				0.8	V
V_{OH}	I_{OH}=100µA	3.1			V
V_{OL}	I_{OL}=100µA			0.2	V

7.4 ESD Performance

Table 76 ESD Performance

PARAMETER		ESD Performance
V_{ESD}	ESD stress voltage	±1kV Human Body Model (HBM) ±250V CDM (Charged Device Model)

7.5 Operating Temperature Ranges

The CL-SOM-AM57x is available with three options of operating temperature range.

Table 77 CL-SOM-AM57x Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CL-SOM-AM57x operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-AM57x.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CL-SOM-AM57x module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CL-SOM-AM57x.
- Refer to the SB-SOM-AM57x carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 0. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-AM57x, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-SOM-AM57xcarrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of "Qualified Magnetics" contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 78 Qualified Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-SOM-AM57xreference design schematics