CL-SOM-iMX6

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
Sep 2016	First release
March 2017	1. RS232_RXD & RS232_TXD description and direction corrected throughout the document 2. RTC chapter fixed to describe Ambiq Micro AM1805 RTC 3. Added note to UART chapter, describing usage of UART5 for Bluetooth.

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX6 Computer-on-Module.

1.2 CL-SOM-iMX6 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-iMX6 part number: http://www.compulab.co.il/products/computer-on-modules/cl-som-imx6-nxp-freescale-i-mx-6-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX6 Developer Resources	http://www.compulab.com/
i.MX6 Reference Manual	http://www.nxp.com/
i.MX6 Datasheet	http://www.nxp.com/

2 OVERVIEW

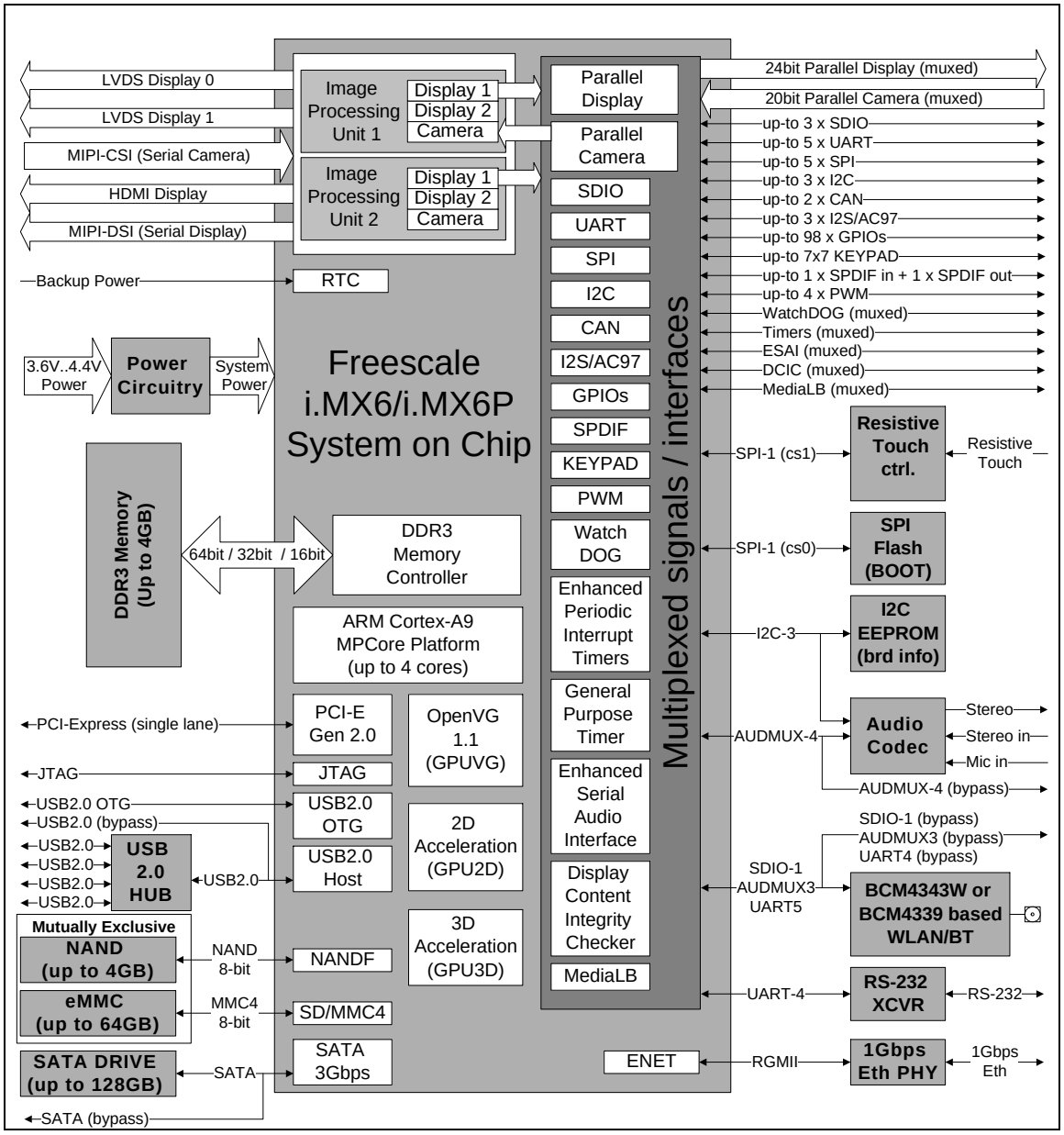
2.1 Highlights

- NXP (Freescale) i.MX6QuadPlus/i.MX6Dual/i.MX6Solo Cortex-A9 SoC, at 1GHz
- Up to 4GB DDR3-1066 with 32-bit data bus.
- Up to 32GB on-board eMMC/NAND/SSD storage.
- Video Processing Unit, 1080p decoding and encoding
- Integrated GPU with OpenGL-ES and OpenCL EP support
- Graphics controller with up-to 4 display interfaces. Up to 1920 x 1200 resolution
- Optional Gigabit Ethernet, PCI-Express, SATA, USB x5, UART x5, SDIO x3, CAN x2, GPIO x112
- Optional 802.11a/b/g/n/ac WiFi and Bluetooth 4.1 (LE)
- LVDS, MIPI-DSI, Parallel RGB, up to 1920 x 1080
- Miniature size: 75 x 65 x 8 mm

SB-FX6 (rev1v2 or higher) carrier board turns the CL-SOM-iMX6 module into SBC-iMX6 - a single board computer

2.2 Block Diagram

Figure 1 CL-SOM-iMX6 Block Diagram



2.3 CL-SOM-iMX6 Features

The "Option" column specifies the SoM configuration option required to have the particular feature. When a SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Specifications	Option
CPU Core, Video and Graphics		
CPU	NXP (Freescale) i.MX6Solo: Single-core ARM Cortex-A9, 1GHz NEON SIMD and VFPv3, up to 32-bit DRAM data bus width	C1000
	NXP (Freescale) i.MX6Dual: Dual-core ARM Cortex-A9, 1GHz NEON SIMD and VFPv3, up to 64-bit DRAM data bus width	C1000D
	NXP (Freescale) i.MX6Quad: Quad-core ARM Cortex-A9 , 1GHz NEON SIMD and VFPv3, up to 64-bit DRAM data bus width	C1000Q
	NXP (Freescale) i.MX6QuadPlus: Quad-core ARM Cortex-A9, 1GHz NEON SIMD and VFPv3, up to 64-bit DRAM data bus width	C1000QP
Video	Video Processing Unit supports HW decoding/encoding Up to 1080p plus SD 30fps decoding (H.264, VC1, RV10, DivX, etc.) Up to 1080p 30fps encoding (H.264, etc.)	+
GPU	3D: Vivante GC880, 35Mtri/s 266Mpxl/s, support for Open GL ES 2.0 2D: Vivante GC320, 600Mpxl/s, BLIT	C1000
	3D: Vivante GC2000+, 200Mtri/s 1000Mpxl/s, OpenGL ES 3.0 & Halti, OpenCL 2D: Vivante GC320, 600Mpxl/s, BLIT + Vivante GC355, 300Mpxl/s, OpenVG 1.1	Not C1000
Memory and Storage		
RAM	256MB – 4GB, up-to DDR3-1066, 16-64 bit data bus width	D
Storage	Boot flash, 2MB, SPI interface, reprogrammable	+
	On-board NAND flash disk, 512MB - 1GB, 8bit, SLC	N
	eMMC flash, 4GB or more	
	On-board SSD, MLC, through SATA interface	Contact Compulab
Display and Camera		
Display	Parallel 24-bit display interface, up to 1920 x 1080 @60Hz	+
	2x LVDS, up to 1920 x 1080 @60Hz	
	HDMI 1.4, up to 1920 x 1080 @60Hz	
	MIPI/DSI, 2 lanes @ 1 Gbps	
	Simultaneous operation of up to 2 interfaces (total raw pixel rate of up to 225 MPixels/sec at 24 bpp)	C1000
	Simultaneous operation of up to 4 interfaces (total raw pixel rate of up to 450 MPixels/sec at 24 bpp)	Not C1000
Touchscreen	On-board 4-wire resistive touch-screen controller	I
	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	1 parallel camera port (up to 20 bit and up to 240 MHz peak)	+
	MIPI CSI-2 serial port, supporting up to 1 Gbps speed per data lane	+
Connectivity		
Gigabit Ethernet	10/100/1000Mbps Copper Ethernet interface (MAC+PHY)	E
WiFi	802.11b/g/n WiFi interface Cypress (Broadcom) BCM4343W chipset	WB
	802.11a/b/g/n/ac WiFi interface Cypress (Broadcom) BCM4339 chipset	WAB
Bluetooth	Bluetooth 4.1 BLE	WB or WAB
Audio		
Analog Audio	Audio codec with analog stereo output, stereo input and electret microphone support	A
Digital Audio	AUDMUX port 3, I2S compliant digital audio port	not (WAB or WB)
	AUDMUX port 4, I2S compliant digital audio port	+
	AUDMUX port 5, I2S compliant digital audio port	+
	AUDMUX port 6, I2S compliant digital audio port	+

	HDMI audio support	+
	S/PDIF input/output (CMOS levels)	+
	Extended serial audio interface (ESAI)	+
I/O		
PCI-Express	PCI Express Gen 2.0 interface	+
USB2.0 (up to 5)	1 OTG + 1 host USB2.0 high-speed ports, 480 Mbps	U2
	1 OTG + 4 host USB2.0 high-speed ports, 480 Mbps	U5
SATA	SATA II interface, 3.0 Gbps, integrated controller and PHY	~~C1000~~ ~~ND~~
UART (up to 5)	1 RS-232 port, rx/tx only, RS-232 levels (precludes UART4)	+
	UART1, TIA/EIA-232-F compatible, up to 5.0 Mbps	+
	UART2, TIA/EIA-232-F compatible, up to 5.0 Mbps	+
	UART3, TIA/EIA-232-F compatible, up to 5.0 Mbps	+
	UART4, TIA/EIA-232-F compatible, up to 5.0 Mbps	+
	UART5, TIA/EIA-232-F compatible, up to 5.0 Mbps	Not (WB or WAB)
CAN bus	Up to 2 CAN bus interfaces (FlexCAN), 3.3V levels	+
MMC/SD/SDIO (up to 3)	SDIO1 – 1/4 bit transfer modes	Not (WB or WAB)
	SDIO2 – 1/4 bit transfer modes	Not A
	SDIO3 – 1/4/8bit transfer modes (bootable)	+
SPI (up to 5)	SPI1 master, supports up to 4 slave SPI devices	+
	SPI2 master, supports up to 4 slave SPI devices	+
	SPI3 master, supports up to 4 slave SPI devices	+
	SPI4 master, supports up to 2 slave SPI devices	+
	SPI5 master, supports up to 3 slave SPI devices (option1)	Not A
	SPI5 master, supports up to 3 slave SPI devices (option2)	Not (WB or WAB)
I2C (up to 4)	I2C1 bus master interface	+
	I2C2 bus master interface	+
	I2C3 bus master interface	+
	I2C4 bus master interface	C1000
PWM (up to 4)	PWM1 general purpose pulse width modulation signal	+
	PWM2 general purpose pulse width modulation signal	+
	PWM3 general purpose pulse width modulation signal (option1)	Not (N4 or higher)
	PWM3 general purpose pulse width modulation signal (option2)	Not (WAB or WB)
	PWM4 general purpose pulse width modulation signal (option1)	Not (N4 or higher)
	PWM4 general purpose pulse width modulation signal (option2)	Not (WB or WAB)
Timers (up to 5)	General Purpose timer interface (GPT)	Not (WB or WAB)
	Enhanced Periodic Interrupt Timer1 (EPIT)	+
	Enhanced Periodic Interrupt Timer2 (EPIT)	+
	Watchdog timer 1 (WDOG)	+
	Watchdog timer 2 (WDOG)	+
GPIO (Up to 112)	Up to 112xGPIO (multifunctional signals shared with other functions)	+
Debug & System		
RTC	Real time clock, powered by external battery	+
JTAG & ARM Trace interface	Standard JTAG interface	+
	ARM CoreSight debug/Trace Interface	Not (WB or WAB)

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	3.5V to 4.5V / Li-Ion battery
Digital I/O voltage	3.3V
Active power consumption	2.0 – 6.0 W, depending on configuration and system load
Mechanical Specifications	
Dimensions	75 x 65 x 8 mm
Weight	33 gram (w/o Heat-plate)
Connectors	2 x 140 pin, 0.6 mm
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

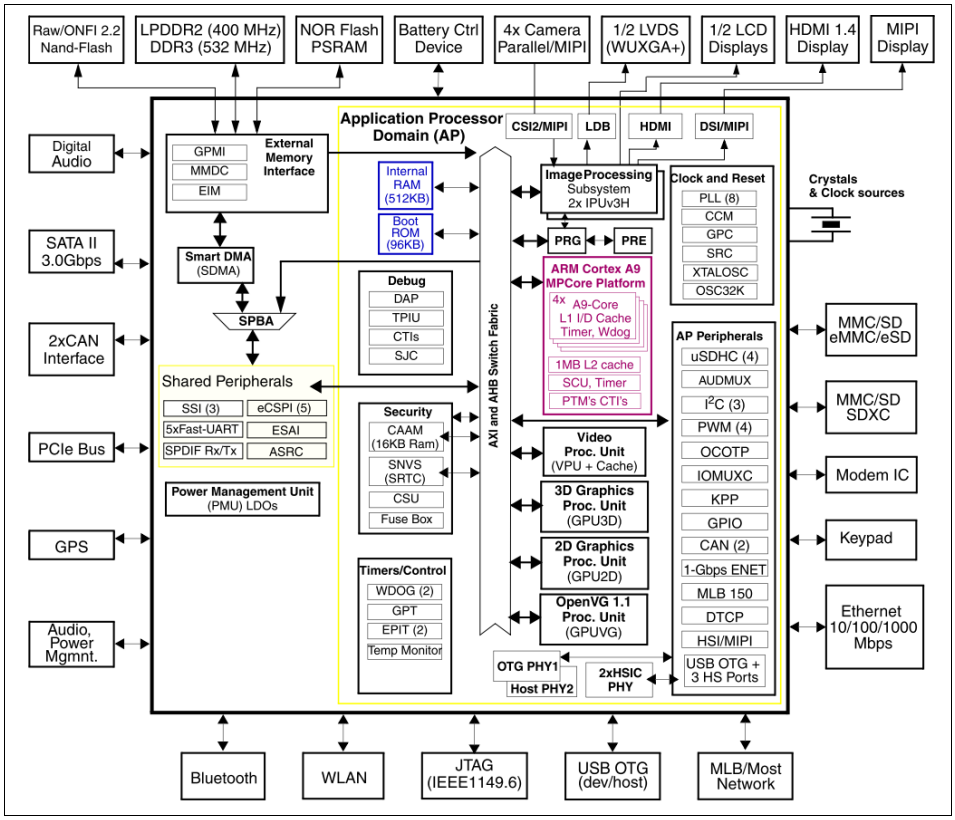
3.1 i.MX6QuadPlus / i.MX6Dual / i.MX6Solo SoC

The i.MX6 is an implementation of the quad ARM Cortex™-A9 core, which operates at frequencies up to 1.0 GHz (single and dual core variants are also available). The i.MX6 provides a variety of interfaces and supports the following main features:

- Quad / Dual / Single Core ARM Cortex™-A9. Core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- Level 2 Cache—Unified instruction and data (up to 1 MByte)
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- NEON MPE coprocessor:
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
- Integrated Power Management unit:
  - Temperature Sensor for monitoring the die temperature
  - DVFS techniques for low power modes
  - Flexible clock gating control scheme
- Multimedia Hardware Accelerators (Optional)

NOTE: Level 2 Cache is limited to 512KByte with the C1000 ordering option of CL-SOM-iMX6.

Figure 2 i.MX6QuadPlus Block Diagram



3.2 Video and Graphics subsystems

The CL-SOM-iMX6 video graphics subsystem consists of the following i.MX6 sub-blocks.

- VPU: A multi-standard high performance video codec engine supporting encode/decode operations of the following:
  - Decoding: H.264 BP/CBP/MP/HP, VC-1 SP/MP/AP, MPEG-4 SP/ASP, H.263 P0/P3, MPEG-1/2 MP, Divx (Xvid) HP/PP/HTP/HDP, VP8 (1280x720), AVS, H.264-MVC (1280x720), MJPEG BP (max. 8192x8192) up to full-HD 1920x1088 @30fps plus D1 @30fps.
  - Encoding: H.264 BP/CBP, MPEG-4 SP, H.263 P0/P3, MJPEG BP (max. 192x8192) up to full-HD 1920x1088@30fps.
- GPU3Dv4: A 3D GPU (Vivante GC2000), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.
- GPU3Dv5: A 3D GPU (Vivante GC880), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.
- GPU2Dv2: Hardware acceleration of 2D graphics (Bit BLT and Stretch BLT). Based on the Vivante GC320 IP core.
- GPUVG: An OpenVG 1.1 Graphics Processing Unit providing hardware acceleration of vector graphics. Based on the Vivante GC355 IP core

NOTE: GPU3Dv5 is available only with the C1000 ordering option of CL-SOM-iMX6.

NOTE: GPU3Dv4 and GPUVG are not available with the C1000 ordering option of CL-SOM-iMX6.

3.3 Memory

3.3.1 DRAM

CL-SOM-iMX6 is available with up to 4GBytes of DDR3. The DDR3 interface is up to 64-bits wide and operates at up to 533 MHz clock frequencies.

3.3.2 Boot-loader Storage

CL-SOM-iMX6 features an onboard 2 MBytes SPI NOR flash. The SPI NOR flash is the primary non-volatile memory device of CL-SOM-iMX6, used for the storing the boot-loader and configuration block.

3.3.3 On-board Storage

CL-SOM-iMX6 is available with optional secondary on-board flash memory, allowing the user to store the system and user data onboard the device without the need for additional external memory. The following types of secondary storage are available

- On-board eMMC (up to 32GBytes)
- On-board raw SLC NAND Flash (up to 1GBytes).
- On-board SATA-II SSD.

The table below summarizes available secondary storage options.

Table 5 Onboard Storage Options

Option	SoC Interface	Type	Description
'N05'	NANDF	NAND	On-board NAND flash disk, 512MB, 8bit, SLC
'N1'	NANDF	NAND	On-board NAND flash disk, 512MB, 8bit, SLC
'N4'	uSDHC4	eMMC	eMMC flash, 4GB
'N16'	uSDHC4	eMMC	eMMC flash, 16GB
'N32'	uSDHC4	eMMC	eMMC flash, 32GB
TBD	SATA	SSD	onboard SATA SSD

NOTE: eMMC and NAND storage types are mutually exclusive

4 PERIPHERAL INTERFACES

CL-SOM-iMX6 implements a variety of peripheral interfaces through the CAMI carrier board connector. The following notes apply to interfaces available through the CAMI interface:

- Some interfaces/signals are available only with/without certain configuration options of CL-SOM-iMX6. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Many of the CL-SOM-iMX6 carrier board interface pins are multifunctional. Up-to 10 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5 of this document.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the CL-SOM-iMX6 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-iMX6 ordering options, certain carrier board interface pins are physically disconnected (floating) from the carrier board interface connector on-board CL-SOM-iMX6. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Signal Input
- **"AO"** – Analog Signal Output
- **"AIO"** – Analog Signal Input/Output
- **"APO"** – Analog Power Output
- **"API"** – Analog Power Input
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"IOD"** – Open Drain Signal (not pulled up on-board CL-SOM-iMX6 unless otherwise noted).
- **"PI"** – Power Input
- **"PO"** – Power Output
- "**SPU" –** Software controlled pull up to 3.3V
- "**SPD" –** Software controlled pull down to GND
- **"PU18**" – Always pulled up to 1.8V on-board CL-SOM-iMX6, (typ. 5KΩ-15KΩ).

- **"PU33"** – Always pulled up to 3.3V on-board CL-SOM-iMX6, (typ. 5KΩ-15KΩ).
- **"PUSUPPLY"** – Always pulled up to 3.6V - 4.5V on-board CL-SOM-iMX6, (typ. 5KΩ-15KΩ).
- **"PD" -** Always pulled down on-board CL-SOM-iMX6, (typ. 5KΩ-15KΩ).

4.1 PCI-Express

CL-SOM-iMX6 is equipped with a single lane PCI Express interface, implemented in the i.MX6 SoC. The PCI Express interface complies with PCIe specification Gen 2.0 and supports the PCI Express 1.1/2.0 standards. The PCI Express module is a dual mode complex, supporting root complex operations and endpoint operations.

The PCI Express module in i.MX6 SoC does not generate the PCI Express ref clock differential signal. The i.MX6 SoC overcomes this limitation by driving a custom generated clock (by means of i.MX6 clock control module) through the i.MX6 LVDS buffered general purpose clock I/O. The LVDS buffered clock can in most cases (where clock jitter requirements are less strict than defined in the PCI-SIG) be used as the PCI Express ref clock. In cases where jitter requirements preclude usage of the LVDS buffered clock, a suitable clock generator must be implemented on the carrier board. Please refer to SB-FX6 (rev1v2 or higher) for an extensive reference design of PCI-Express ref clock circuitry.

Please refer to chapter 4.24 of this document for more details on the i.MX6 general purpose clock IO. The table below summarizes the PCI-Express interface signals

Table 6 PCI-Express Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_RXM	P2-106	AI	PCIe PHY Differential receiver negative-side	Always
PCIE_RXP	P2-108	AI	PCIe PHY Differential receiver positive-side	Always
PCIE_TXM	P2-112	AO	PCIe PHY Differential transmitter negative-side	Always
PCIE_TXP	P2-114	AO	PCIe PHY Differential transmitter positive-side	Always

4.2 Serial ATA Interface

The CL-SOM-iMX6 incorporates a single SATA-II port implemented with the Freescale i.MX6 integrated SATA controller and PHY. The interface supports the following main features:

- The SATA block fully complies with AHCI specification version 1.10 and partially complies with AHCI specification version 1.3 (FIS-based switching is currently not supported).
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Power management features including automatic partial-to-slumber transition.
- eSATA (external analog logic also needs to support eSATA).
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.

An optional onboard SATA solid state drive is supported with CL-SOM-iMX6. In case the onboard SSD is used, the SATA interface is not available through the carrier board connectors. The onboard SATA drive activity can be monitored by carrier board through a device activity signal available when onboard SATA drive is populated. The table below summarizes the SATA interface signals

Table 7 SATA Interface Signals

Signal Name	Pin #	Type	Description	Availability
SATA_RXN	P2-118	AI	SATA receive data (negative)	not 'C1000'
SATA_RXP	P2-120	AI	SATA receive data (positive)	not 'C1000'
SATA_TXN	P2-124	AO	SATA transmit data (negative)	not 'C1000'
SATA_TXP	P2-126	AO	SATA transmit data (positive)	not 'C1000'
SSD_NACT	P2-123	O	Onboard SATA SSD Device Activity Signal	Contact Compulab

4.3 Display and Camera Interfaces

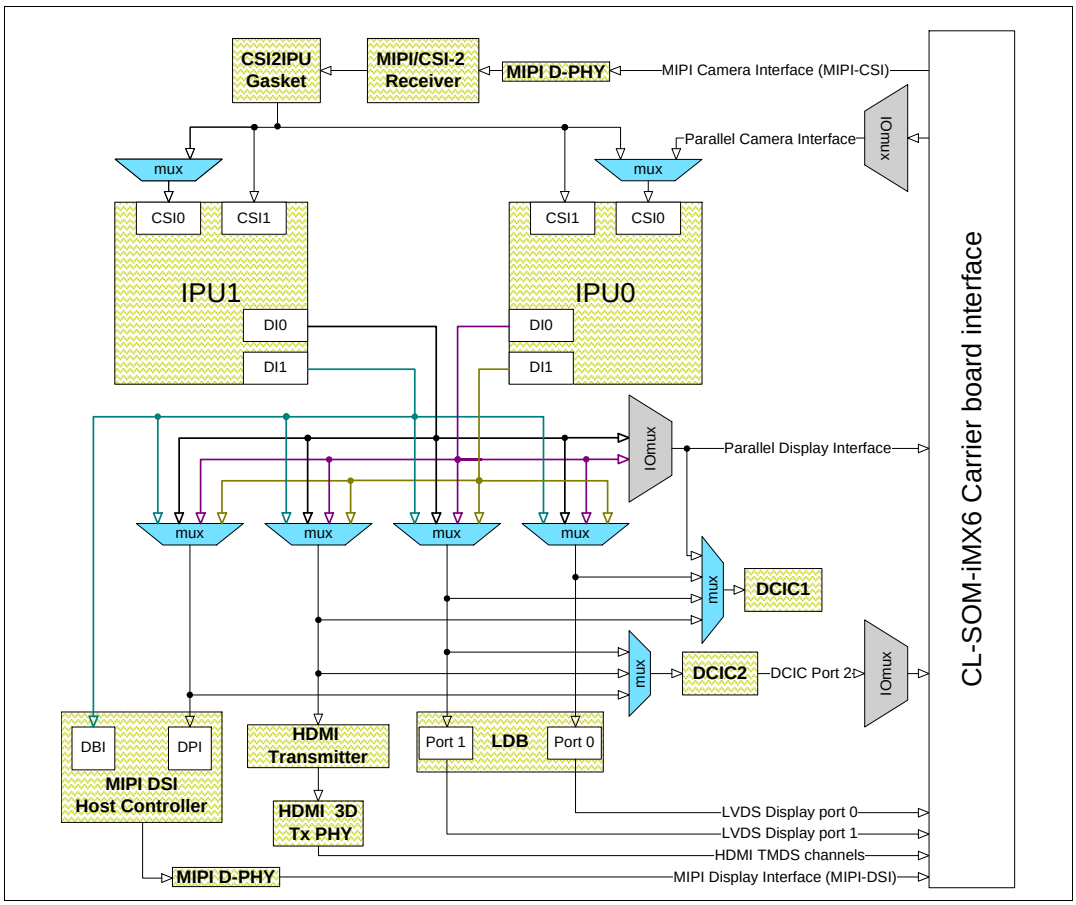
The Display and Camera subsystems of CL-SOM-iMX6 are derived from the following high level blocks integrated into the i.MX6 SoC:

- Up to 2 Image Processing Units (IPUs) providing connectivity to cameras and displays.
- Display Bridges & Interfaces:
- MIPI-DSI Host Controller and PHY
- HDMI Transmitter and PHY.
- Two port LVDS Display Bridge - LDB
- Two (identical) Display Content Integrity Checker components (DCIC) designed to authenticate sensitive displayed data.
- Parallel Display (through IOMUX)
- Camera Bridges & Interfaces:
- MIPI D-phy, Receiver and CSI2IP Gasket
- Parallel Camera (through IOMUX)

NOTE: The second IPU is not available with the C1000 ordering option of CL-SOM-iMX6.

The figure below illustrates the CL-SOM-iMX6 Display and Camera subsystems high level architecture.

Figure 3 CL-SOM-iMX6 Display and Camera subsystems architecture



4.3.1 CL-SOM-iMX6 Display interfaces

The CL-SOM-iMX6 CoM supports a total of up to 5 display interfaces. The display data flows from system memory into the i.MX6 integrated 'Image Processing Units' (IPUs), where the data is processed and retransmitted into the integrated display bridges (MIPI DSI / HDMI / LDB / Parallel Interface) using the IPU "Display interfaces" (IPU DI1 and DI0). Figure 3 summarizes the display sources, relevant interfaces and architecture of the CL-SOM-iMX6 display subsystem. The i.MX6 SoC can support simultaneous operation of up to 4 displays (up to 2 active IPUs, each driving DI0 and DI1). The following display interfaces are available with CL-SOM-iMX6:

- A Single Parallel Display interface with up to 200MHz pixel clock frequency
- Two LVDS Display ports with pixel clock rates up to 170MHz
- One HDMI port with pixel clock rates limited by IPU (source of data) to 240MHz max.
- One MIPI/DSI port

The below combinations of displays and max resolution are supported:

- Up to 2 displays: 2 x 4XGA (2048x1536).
- Up to 4 displays: 2 x 1080p (1920x1080) + 2 x WXGA (1280x720).

The following subchapters describe each of the CL-SOM-iMX6 display interfaces.

NOTE: Only 2 simultaneous displays are supported with the 'C1000' ordering option of CL-SOM-iMX6.

4.3.1.1 Parallel Display Interface

The Parallel Display interface of CL-SOM-iMX6 is derived directly from the DI0 port of the IPU, effectively bypassing all the i.MX6 integrated display bridges (see Figure 3 above).

Each DI port supports the following:

- Compatible with MIPI-DPI standard.
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols.
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- Scan Order: progressive or interlaced
- Synchronization:
- Programmable horizontal and vertical synchronization output signals
- Data enabling output signal
- The combined data rate for the two DI ports is up to 240 MP/sec
- Supported pixel data formats:
- RGB - color depth fully configurable; up to 8 bits/value (color component)
- YUV 4:2:2, 8 bits/value
- All mandatory formats in MIPI DBI, DPI and DSI

Each of the parallel display interface signals can be sourced either by IPU0 or IPU1 (DI0 port only.

NOTE: The "Type" column of signal tables below assumes that this interface is used in "Parallel RGB" mode. Signal type might be different (software controlled) in case a different operation mode is used.

NOTE: The display signal mapping (for example to R[7:0], G[7:0] & B[7:0]) is highly configurable. For examples of valid mappings, please refer to the "IPU Display Interface Signal Mapping" chapter of the i.MX6 datasheet. For detailed information please refer to the "Bus Mapping Unit" chapter of the "i.MX6 Reference Manual".

The tables below summarize the Parallel Display interface signals

Table 8 Parallel Display 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
IPU1_DI0_DISP_CLK	P1-108*	O	Pixel clock	Always
IPU1_DI0_PIN01	P2-104*	IO	May be required for anti-tearing	Always
IPU1_DI0_PIN02	P1-109*	O	Horizontal synchronization	Always
IPU1_DI0_PIN03	P1-107*	O	Vertical synchronization	Always
IPU1_DI0_PIN04	P1-60*	O	Additional frame/row synchronous signal with programmable timing	Always
IPU1_DI0_PIN13	P2-25*	O	Register select signal	Always
IPU1_DI0_PIN15	P1-105*	O	Data validation/blank, data enable	Always
IPU1_DI0_PIN17	P2-27*	O	Additional frame/row synchronous signal with programmable timing	Always
IPU1_DI1_PIN05	P1-71*	O	Additional frame/row synchronous signal with programmable timing	Always
IPU1_DI1_PIN06	P1-69*	O	Additional frame/row synchronous signal with programmable timing	Always
IPU1_DI1_PIN07	P1-63*	O	Additional frame/row synchronous signal with programmable timing	Always
IPU1_DI1_PIN13	P1-40*	O	Register select signal	Always
IPU1_DISP0_DATA00	P1-75*	IO	Pixel data bit 0	Always
IPU1_DISP0_DATA01	P1-76*	IO	Pixel data bit 1	Always
IPU1_DISP0_DATA02	P1-77*	IO	Pixel data bit 2	Always
IPU1_DISP0_DATA03	P1-78*	IO	Pixel data bit 3	Always

Signal Name	Pin #	Type	Description	Availability
IPU1_DISP0_DATA04	P1-81*	IO	Pixel data bit 4	Always
IPU1_DISP0_DATA05	P1-82*	IO	Pixel data bit 5	Always
IPU1_DISP0_DATA06	P1-83*	IO	Pixel data bit 6	Always
IPU1_DISP0_DATA07	P1-84*	IO	Pixel data bit 7	Always
IPU1_DISP0_DATA08	P1-85*	IO	Pixel data bit 8	Always
IPU1_DISP0_DATA09	P1-87*	IO	Pixel data bit 9	Always
IPU1_DISP0_DATA10	P1-88*	IO	Pixel data bit 10	Always
IPU1_DISP0_DATA11	P1-89*	IO	Pixel data bit 11	Always
IPU1_DISP0_DATA12	P1-90*	IO	Pixel data bit 12	Always
IPU1_DISP0_DATA13	P1-92*	IO	Pixel data bit 13	Always
IPU1_DISP0_DATA14	P1-93*	IO	Pixel data bit 14	Always
IPU1_DISP0_DATA15	P1-94*	IO	Pixel data bit 15	Always
IPU1_DISP0_DATA16	P1-95*	IO	Pixel data bit 16	Always
IPU1_DISP0_DATA17	P1-96*	IO	Pixel data bit 17	Always
IPU1_DISP0_DATA18	P1-97*	IO	Pixel data bit 18	Always
IPU1_DISP0_DATA19	P1-99*	IO	Pixel data bit 19	Always
IPU1_DISP0_DATA20	P1-100*	IO	Pixel data bit 20	Always
IPU1_DISP0_DATA21	P1-101*	IO	Pixel data bit 21	Always
IPU1_DISP0_DATA22	P1-102*	IO	Pixel data bit 22	Always
IPU1_DISP0_DATA23	P1-104*	IO	Pixel data bit 23	Always
IPU1_DISP1_DATA20	P1-44*	IO	Pixel data bit 20	Always
IPU1_DISP1_DATA21	P1-46*	IO	Pixel data bit 21	Always
IPU1_DISP1_DATA22	P1-42*	IO	Pixel data bit 22	Always
IPU1_DISP1_DATA23	P1-40*	IO	Pixel data bit 23	Always

Table 9 Parallel Display 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
IPU2_DI0_DISP_CLK	P1-108*	O	Pixel clock (MUXED)	not 'C1000'
IPU2_DI0_PIN02	P1-109*	O	Horizontal synchronization (MUXED)	not 'C1000'
IPU2_DI0_PIN03	P1-107*	O	Vertical synchronization (MUXED)	not 'C1000'
IPU2_DI0_PIN04	P1-60*	O	Additional frame/row synchronous signal with programmable timing (MUXED)	not 'C1000'
IPU2_DI0_PIN15	P1-105*	O	Data validation/blank, data enable (MUXED)	not 'C1000'
IPU2_DISP0_DATA00	P1-75*	O	Pixel data bit 0 (MUXED)	not 'C1000'
IPU2_DISP0_DATA01	P1-76*	O	Pixel data bit 1 (MUXED)	not 'C1000'
IPU2_DISP0_DATA02	P1-77*	O	Pixel data bit 2 (MUXED)	not 'C1000'
IPU2_DISP0_DATA03	P1-78*	O	Pixel data bit 3 (MUXED)	not 'C1000'
IPU2_DISP0_DATA04	P1-81*	O	Pixel data bit 4 (MUXED)	not 'C1000'
IPU2_DISP0_DATA05	P1-82*	O	Pixel data bit 5 (MUXED)	not 'C1000'
IPU2_DISP0_DATA06	P1-83*	O	Pixel data bit 6 (MUXED)	not 'C1000'
IPU2_DISP0_DATA07	P1-84*	O	Pixel data bit 7 (MUXED)	not 'C1000'
IPU2_DISP0_DATA08	P1-85*	O	Pixel data bit 8 (MUXED)	not 'C1000'
IPU2_DISP0_DATA09	P1-87*	O	Pixel data bit 9 (MUXED)	not 'C1000'
IPU2_DISP0_DATA10	P1-88*	O	Pixel data bit 10 (MUXED)	not 'C1000'
IPU2_DISP0_DATA11	P1-89*	O	Pixel data bit 11 (MUXED)	not 'C1000'
IPU2_DISP0_DATA12	P1-90*	O	Pixel data bit 12 (MUXED)	not 'C1000'
IPU2_DISP0_DATA13	P1-92*	O	Pixel data bit 13 (MUXED)	not 'C1000'
IPU2_DISP0_DATA14	P1-93*	O	Pixel data bit 13 (MUXED)	not 'C1000'
IPU2_DISP0_DATA15	P1-94*	O	Pixel data bit 15 (MUXED)	not 'C1000'
IPU2_DISP0_DATA16	P1-95*	O	Pixel data bit 16 (MUXED)	not 'C1000'
IPU2_DISP0_DATA17	P1-96*	O	Pixel data bit 17 (MUXED)	not 'C1000'
IPU2_DISP0_DATA18	P1-97*	O	Pixel data bit 18 (MUXED)	not 'C1000'
IPU2_DISP0_DATA19	P1-99*	O	Pixel data bit 19 (MUXED)	not 'C1000'
IPU2_DISP0_DATA20	P1-100*	O	Pixel data bit 20 (MUXED)	not 'C1000'
IPU2_DISP0_DATA21	P1-101*	O	Pixel data bit 21 (MUXED)	not 'C1000'
IPU2_DISP0_DATA22	P1-102*	O	Pixel data bit 22 (MUXED)	not 'C1000'
IPU2_DISP0_DATA23	P1-104*	O	Pixel data bit 23 (MUXED)	not 'C1000'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.3.1.2 LVDS Display interfaces

The CL-SOM-iMX6 is equipped with two LVDS Display interfaces. The LVDS Display interfaces are derived from the i.MX6 integrated LVDS Display Bridge (LDB). The main function of the LDB is to transmit display data from the IPU to one or two LVDS interfaced displays (see Figure 3 for LDB integration diagram). The LDB output complies with the EIA-644-A standard and supports the following features:

- Data input interface (inside the i.MX6 SoC)
- RGB Data of 18 or 24 bits
- Pixel clock
- Control signals: HSYNC, VSYNC, DE, and 1 additional optional general purpose control.
- Data output interfaces
- Single channel output
- Dual channel output (one input source, two channels outputs for two displays)
- Split channel output (one input source, 2 channels on output)
- Separate 2 channel output (2 input sources from IPU).
- Data Rates
- Overall: LDB supports rates needed by WUXGA 16:10 aspect ratio (1920 x 1200 @ 60 frames per second, data rate supported up to 170 MHz)
- For single input data interface case: Up to 170 MHz pixel clock (WUXGA 1920x1200)
- For dual input data interface case: Up to 85 MHz per interface. (WXGA 1366x768 @ 60 frames per second, 35% blanking).

For additional details, please refer to the "LVDS Display Bridge" chapter of the "i.MX6 Reference Manual". The tables below summarize the LVDS Display interface signals

Table 10 LVDS Display 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CLK_N	P1-15	AO	Positive part of differential clock	Always
LVDS0_CLK_P	P1-17	AO	Negative part of differential clock	Always
LVDS0_TX0_N	P1-16	AO	Positive part of differential data 0	Always
LVDS0_TX0_P	P1-18	AO	Negative part of differential data 0	Always
LVDS0_TX1_N	P1-22	AO	Positive part of differential data 1	Always
LVDS0_TX1_P	P1-24	AO	Negative part of differential data 1	Always
LVDS0_TX2_N	P1-28	AO	Positive part of differential data 2	Always
LVDS0_TX2_P	P1-30	AO	Negative part of differential data 2	Always
LVDS0_TX3_N	P1-34	AO	Positive part of differential data 3	Always
LVDS0_TX3_P	P1-36	AO	Negative part of differential data 3	Always

Table 11 LVDS Display 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS1_CLK_N	P2-9	AO	Positive part of differential clock	Always
LVDS1_CLK_P	P2-11	AO	Negative part of differential clock	Always
LVDS1_TX0_N	P2-28	AO	Positive part of differential data 0	Always
LVDS1_TX0_P	P2-30	AO	Negative part of differential data 0	Always
LVDS1_TX1_N	P2-34	AO	Positive part of differential data 1	Always
LVDS1_TX1_P	P2-36	AO	Negative part of differential data 1	Always
LVDS1_TX2_N	P2-15	AO	Positive part of differential data 2	Always
LVDS1_TX2_P	P2-17	AO	Negative part of differential data 2	Always
LVDS1_TX3_N	P2-21	AO	Positive part of differential data 3	Always
LVDS1_TX3_P	P2-23	AO	Negative part of differential data 3	Always

4.3.1.3 MIPI Display Interface

The MIPI Display interface included with CL-SOM-iMX6 is derived from the i.MX6 integrated MIPI-DSI Host controller. The MIPI-DSI Host controller implements all protocol functions defined in the MIPI-DSI specification, providing an interface between the IPU and the MIPI D-PHY, enabling the communication with a MIPI-DSI compliant display (see Figure 3 for MIPI

Display integration diagram). For additional details, please refer to the "MIPI DSI Host Controller" chapter of the "i.MX6 Reference Manual".

The MIPI DSI Host Controller supports the following features:

IPU SIDE (input):

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005. Supported DBI types are:
- Type B
- 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist (only one is operational at a time)
- Support all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009

D-PHY side (output):

- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Data Lanes:
- Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Programmable display resolutions, from 160x120(QQVGA) to 1024x768(XVGA).
- Multiple Peripheral Support capability, configurable Virtual Channels.
- Video Mode Pixel Formats, 16bpp(RGB565), 18bpp(RGB666) packed, 18bpp(RGB666) loosely, 24bpp(RGB888).

The table below summarizes the MIPI-DSI interface signals

Table 12 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI_CLK0M	P2-81	AO	D-PHY Negative D-Phy differential clock line transceiver output (also named CLKN in i.MX6 reference manual)	Always
DSI_CLK0P	P2-83	AO	D-PHY Positive D-Phy differential clock line transceiver output (also named CLKP in i.MX6 reference manual)	Always
DSI_D0M	P2-105	AO	D-PHY Negative D-Phy differential data line transceiver output, Lane 0 (also named DATAN0 in i.MX6 reference manual)	Always
DSI_D0P	P2-107	AO	D-PHY Positive D-Phy differential data line transceiver output, Lane 0 (also named DATAP0 in i.MX6 reference manual)	Always
DSI_D1M	P2-111	AO	D-PHY Negative D-Phy differential data line transceiver output, Lane 1 (also named DATAN1 in i.MX6 reference manual)	Always
DSI_D1P	P2-113	AO	D-PHY Positive D-Phy differential data line transceiver output, Lane 1 (also named DATAP1 in i.MX6 reference manual)	Always

4.3.1.4 HDMI port

The HDMI port available with CL-SOM-iMX6 is based on the HDMI transmitter & HDMI 3D Tx PHY integrated into the i.MX6 SoC. Figure 3 shows the video data path from the IPU to the CL-SOM-iMX6 carrier board interface through the HDMI transmitter & PHY.

Discussing HDMI in the "Display and camera" chapter is not appropriate since in addition to the video/display data from IPU, HDMI transmits audio and control/status data over the TMDS channels. Please refer to chapter 4.6 of this document for further description of HDMI.

4.3.2 Display content integrity checker (DCIC)

The goal of the DCIC is to verify that safety-critical information sent to a display is not corrupted. Such verification is mandatory for warning icons in the instrument cluster of a car, to comply with the ASIL B (Automotive Safety Integrity Level B) specification. It is also required in other safety-sensitive systems. DCIC can monitor either one of the IPU display port outputs or feedback signals going from IO pads of Parallel display interface. Figure 3 shows DCIC integration in CL-SOM-iMX6.

Each DCIC block can interrupt the ARM complex when data signature calculation is completed and/or a signature mismatch is detected. CL-SOM-iMX6 also allows notifying an external system (through the carrier board interface) when a signature mismatch is detected in the DCIC2 block.

For additional details, please refer to the "Display Content Integrity Checker" chapter of the "i.MX6 Reference Manual". The table below summarizes the DCIC interface signals

Table 13 DCIC Interface Signals

Signal Name	Pin #	Type	Description	Availability
DCIC2_OUT	P2-47*	O	Mismatch indication for external controller	not 'A'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.3.3 Still Image Synchronization Generator

CL-SOM-iMX6 allows access to the Still Image Synchronization Generator (SISG) interface of i.MX6. Each IPU is equipped with a single instance of the SISG block. The SISG is an IPU subsystem designed to provide time-sensitive control signals synchronizing the image sensor with camera peripherals, such as a flash lamp and a mechanical shutter. The SISG is implemented using a single time base counter, and six Time Compare Units. During the counting period, the SISG can generate up to 6 output strobe signals (up to 5 accessible through CL-SOM-iMX6 carrier board interface):

- Each strobe can be individually enabled or disabled and has a programmable polarity
- The edges of the strobes are generated at specified counter values - to achieve pixel-level resolution - as specified by programmable SISG_SET& SISG_CLR time tag registers
- The clock has 25 bits, to allow strobe generation during a time period of up to two 12M pixel frames

The SISG can repeat the above sequence for up to 32 cycles (this is provided to generate a train of flash pulses, for anti-red-eye or for measurements in low-light conditions). The repetition is implemented by resetting the counter, which can be triggered by one of the following events:

- A VSYNC signal
- A pre-defined value reached by the counter

After the last sequence, when the counter reaches its maximal value, it stops counting and the SISG remains in idle mode until the next activation. For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the SISG interface signals

Table 14 SISG 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
IPU1_SISG0	P2-97*	O	SISG Output Strobe signal	Always
IPU1_SISG2	P1-42*	O	SISG Output Strobe signal	Always
IPU1_SISG3	P1-40*	O	SISG Output Strobe signal	Always
IPU1_SISG4	P2-85*	O	SISG Output Strobe signal	Always
IPU1_SISG5	P2-87*	O	SISG Output Strobe signal	Always

Table 15 SISG 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
IPU2_SISG0	P2-97*	O	SISG Output Strobe signal (MUXED)	not 'C1000'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.3.4 Camera Interfaces

Pixel data from an externally connected image sensor or similar device can be transferred into the CL-SOM-iMX6 system memory by means of the IPU CSI ports and the i.MX6 integrated camera bridges. A total of two camera interfaces are accessible through the CL-SOM-iMX6 carrier board interface:

- Parallel camera interface (towards IPU0 CSI0 only).
- MIPI/CSI-2 receiver differential interface.

Figure 3 illustrates the pixel data path from the CL-SOM-iMX6 carrier board interface into the IPU CSI ports. Each IPU accommodates two camera sensor interfaces (CSIs). Each CSI supports both parallel and serial MIPI interfaces. CL-SOM-iMX6 implementation allows data from the parallel camera interface to be sourced only into the IPU0 CSI0 port, while the data from MIPI/CSI-2 interface can be sourced into any IPU CSI port. Each CSI port supports the following data formats:

- Bayer RGB (8, 9-10 or 11-16 bits per value)
- Full RGB, YUV 4:4:4, YUV 4:2:2
- Grayscale (8 or 16 bits per value)
- Generic Data

For the full list of features, limitations and additional details on the IPU CSI ports please refer to the “Image Processing Unit” chapter of the “i.MX6 Reference Manual”.

The following subchapters describe each of the CL-SOM-iMX6 camera interfaces.

4.3.4.1 Parallel Camera Interface

The parallel camera interface available with CL-SOM-iMX6 supports the following features (in addition to the CSI features described in chapter 4.3):

- Up-to 20bit input data bus.
- Programmable signal polarity
- Interface Clock frequency of up to 180MHz

Please refer to Figure 3 for a visual illustration of the pixel data path from CL-SOM-iMX6 carrier board interface into CSI0 port of IPU0 through the parallel camera interface.

NOTE: The parallel camera interface signal mapping (for example to R[7:0], G[7:0] & B[7:0]) is data format dependent. For the full signal mapping information please refer to the “IPU Sensor Interface Signal Mapping” chapter of the i.MX6 datasheet.

The table below summarizes the Parallel Camera interface signals

Table 16 Parallel Camera 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
IPU1_CSI0_DATA_EN	P1-59*	I	Parallel camera data enable input	Always
IPU1_CSI0_DATA00	P1-40*	I	Parallel camera data0	Always
IPU1_CSI0_DATA01	P1-42*	I	Parallel camera data1	Always
IPU1_CSI0_DATA02	P1-44*	I	Parallel camera data2	Always

Signal Name	Pin #	Type	Description	Availability
IPU1_CSI0_DATA03	P1-46*	I	Parallel camera data3	Always
IPU1_CSI0_DATA04	P1-39*	I	Parallel camera data4	not ('WAB' or 'WB')
IPU1_CSI0_DATA05	P1-41*	I	Parallel camera data5	not ('WAB' or 'WB')
IPU1_CSI0_DATA06	P2-64*	I	Parallel camera data6	Always
IPU1_CSI0_DATA07	P2-66*	I	Parallel camera data7	Always
IPU1_CSI0_DATA08	P2-68*	I	Parallel camera data8	not ('WAB' or 'WB')
IPU1_CSI0_DATA09	P2-70*	I	Parallel camera data9	not ('WAB' or 'WB')
IPU1_CSI0_DATA10	P2-72*	I	Parallel camera data10	Always
IPU1_CSI0_DATA11	P2-80*	I	Parallel camera data11	Always
IPU1_CSI0_DATA12	P2-82*	I	Parallel camera data12	not ('WAB' or 'WB')
IPU1_CSI0_DATA13	P2-84*	I	Parallel camera data13	not ('WAB' or 'WB')
IPU1_CSI0_DATA14	P1-48*	I	Parallel camera data14	not ('WAB' or 'WB')
IPU1_CSI0_DATA15	P1-45*	I	Parallel camera data15	not ('WAB' or 'WB')
IPU1_CSI0_DATA16	P1-47*	I	Parallel camera data16 (MUXED)	not ('WAB' or 'WB')
IPU1_CSI0_DATA17	P1-49*	I	Parallel camera data17 (MUXED)	not ('WAB' or 'WB')
IPU1_CSI0_DATA18	P1-33*	I	Parallel camera data18 (MUXED)	Always
IPU1_CSI0_DATA19	P1-35*	I	Parallel camera data19 (MUXED)	Always
IPU1_CSI0_HSYNC	P1-51*	I	Parallel camera HSYNC input	Always
IPU1_CSI0_PIXCLK	P1-57*	I	Parallel camera pixel clock input	Always
IPU1_CSI0_VSYNC	P1-53*	I	Parallel camera VSYNC input	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.3.4.2 MIPI camera interface MIPI-CSI

The MIPI camera interface accessible through the CL-SOM-iMX6 carrier board connectors is basically the receiving section of the i.MX6 integrated MIPI D-PHY block. Serial pixel data sourced from a compliant image sensor and sent over this interface, is de-serialized by the MIPI D-PHY receiver block and re-sent into the IPU trough the MIPI/CSI2 receiver and CSI2IPU bridge. The MIPI/CSI-2 receiver is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification.

Please refer to Figure 3 for a visual illustration of the pixel data path from CL-SOM-iMX6 carrier board interface into the IPUs through the MIPI camera interface.

The MIPI CSI-2 Receiver supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Supports up to 4 Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types

For additional details on MIPI-CSI and other relevant system blocks, please refer the “i.MX6 Reference Manual”. The table below summarizes the MIPI-CSI interface signals

Table 17 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI_CLK0M	P2-100	AI	D-PHY Negative D-Phy differential clock line Receiver input (also named CSI2_CLKN in i.MX6 reference manual)	Always
CSI_CLK0P	P2-102	AI	D-PHY Positive D-Phy differential clock line Receiver input (also named CSI2_CLKP in i.MX6 reference manual)	Always

Signal Name	Pin #	Type	Description	Availability
CSI_D0M	P2-93	AI	D-PHY Negative D-Phy differential data line Receiver input , Lane 0 (also named CSI2_DATAN0 in i.MX6 reference manual)	Always
CSI_D0P	P2-95	AI	D-PHY Positive D-Phy differential data line Receiver input , Lane 0 (also named CSI2_DATAP0 in i.MX6 reference manual)	Always
CSI_D1M	P1-118	AI	D-PHY Negative D-Phy differential data line Receiver input , Lane 1 (also named CSI2_DATAN1 in i.MX6 reference manual)	Always
CSI_D1P	P1-120	AI	D-PHY Positive D-Phy differential data line Receiver input , Lane 1 (also named CSI2_DATAP1 in i.MX6 reference manual)	Always
CSI_D2M	P1-121	AI	D-PHY Negative D-Phy differential data line Receiver input , Lane 2 (also named CSI2_DATAN2 in i.MX6 reference manual)	not 'C1000'
CSI_D2P	P1-123	AI	D-PHY Positive D-Phy differential data line Receiver input , Lane 2 (also named CSI2_DATAP2 in i.MX6 reference manual)	not 'C1000'
CSI_D3M	P1-111	AI	D-PHY Negative D-Phy differential data line Receiver input , Lane 3 (also named CSI2_DATAN3 in i.MX6 reference manual)	not 'C1000'
CSI_D3P	P1-113	AI	D-PHY Positive D-Phy differential data line Receiver input , Lane 3 (also named CSI2_DATAP3 in i.MX6 reference manual)	not 'C1000'

4.4 Audio Subsystem

The audio subsystem of CL-SOM-iMX6 consists of the following two groups of modules:

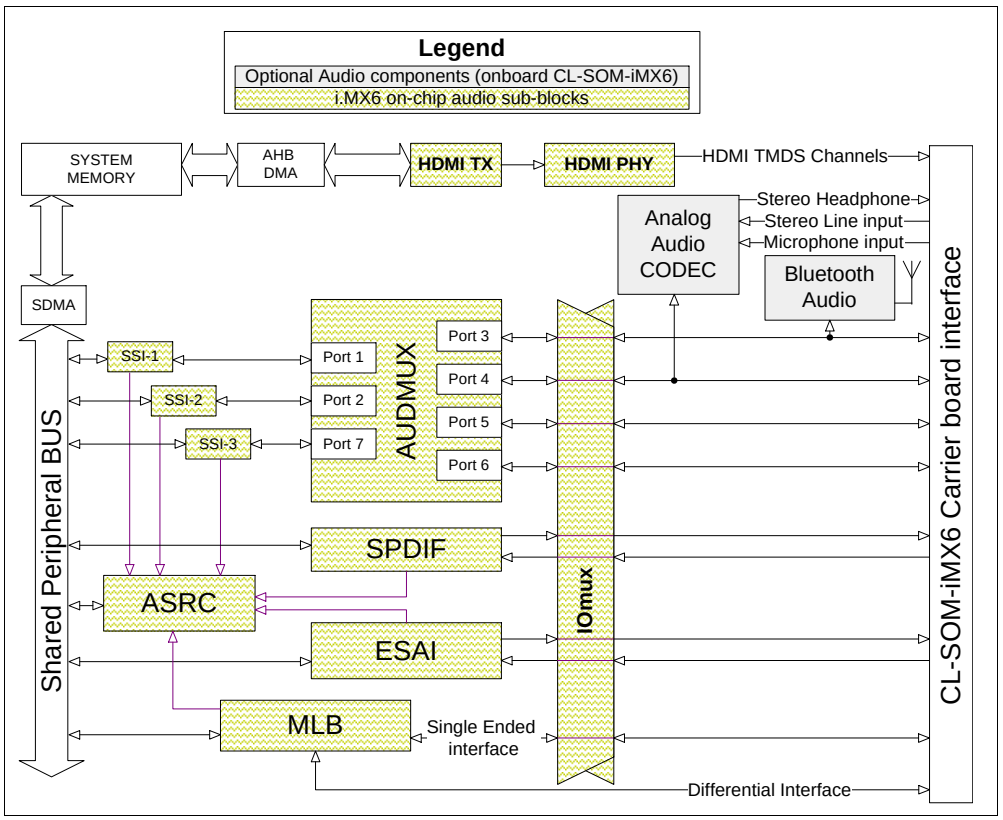
- Internal to the i.MX6 SoC:
- SSI-1, SSI-2, SSI-3
- AUDMUX
- ESAI
- SPDIF
- MediaLB
- HDMI
- External to the I.MX6 SoC (optional, on-board CL-SOM-iMX6):
- Analog Audio CODEC
- Bluetooth Digital Audio (for hands-free applications).

Audio data flows from/to the system memory through an i.MX6 internal bus called the "Shared Peripheral Bus" (see Figure 3). The high level blocks described in the sub-chapters below are designed to transfer audio data between various off-chip devices and the i.MX6 internal "Shared Peripheral BUS".

NOTE: A single special case where audio data path does not involve the "Shared Peripheral Bus" is the when the audio data flows from the system memory into the HDMI TX block, over the i.MX6 AXI bus. Please refer to chapter 4.6 of this document of additional details on HDMI.

A high level overview of the audio subsystem components is shown in Figure 4.

Figure 4 CL-SOM-iMX6 Audio subsystem architecture



4.4.1 Analog Audio CODEC

The CL-SOM-iMX6 analog audio functionality is implemented by interfacing the Wolfson WM8731 audio codec with i.MX6 AUDMUX port 4. The Wolfson WM8731 supports the following features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

The audio data path to the analog audio interface is illustrated in Figure 4.

Table 18 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted, (see Notes 1 and 2 below)			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVpp			45		
Programmable gain	1 kHz output		-73	0	6	dB
Programmable-gain step size	1 kHz			1		dB
Mute attenuation	1 kHz output, 0dB			80		dB
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2 below)	A-weighted, 0dB gain, Fsample = 48 kHz.		85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.			90		
Dynamic range, (see note 3 below)	A-weighted, −60-dB full-scale input		85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain			-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVpp			45		
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω		-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10	15		kΩ
	0 dB input gain		20	30		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2)	A-weighted, 0-dB gain			85		dB
Dynamic range, (see Note 3)	A-weighted, −60-dB full-scale input			85		dB
Total harmonic distortion,	0dB input, 0dB gain			-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVpp			45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.			34		dB

Parameter	Test conditions	Min	Typ	Max	Unit
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,		14		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance			10		kΩ
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

For additional details, please refer to the Wolfson WM8731 datasheet. The table below summarizes the Analog Audio interface signals

Table 19 Analog Audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
LHPOUT	P2-139	AO	Left channel headphone output	'A'
LLINEIN	P2-133	AI	Left channel line input	'A'
MICBIAS	P2-125	APO	Electret microphone bias supply	'A'
MICIN	P2-129	AI	Microphone input	'A'
RHPOUT	P2-137	AO	Headphones jack	'A'
RLINEIN	P2-131	AI	Line In jack	'A'

4.4.2 Digital Audio Interfaces

4.4.2.1 Sony/Philips Digital Interface (S/PDIF)

The CL-SOM-iMX6 features an S/PDIF interface allowing CL-SOM-iMX6 to receive and transmit digital audio data. The S/PDIF interface is implemented by means of the i.MX6 integrated S/PDIF transceiver.

The interface is compatible with the Tech 3250-E standard of the European Broadcasting Union, except clause 6.3.3 and the IEC60958-3 Ed2 for relevant topics.

For additional details, please refer to the "i.MX6 Reference Manual". The table below summarizes the SPDIF interface signals

Table 20 SPDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	P2-89*	I	External clock signal	Always
SPDIF_IN	P1-116*	I	Input line	Always
SPDIF_IN	P1-20*	I	Input line	Always
SPDIF_IN	P2-128*	I	Input line	Always
SPDIF_IN	P2-27*	I	Input line	Always
SPDIF_LOCK	P1-72*	O	Lock signal	Always
SPDIF_OUT	P1-32*	O	Output line signal	Always
SPDIF_OUT	P2-104*	O	Output line signal	Always
SPDIF_OUT	P2-121*	O	Output line signal	Always
SPDIF_SR_CLK	P1-61*	O	SR Lock signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.4.2.2 Extended Serial Audio Interface (ESAI)

The CL-SOM-iMX6 features an Enhanced Serial Audio Interface (ESAI), which provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers and DSPs. The ESAI consists of independent transmitter and receiver sections and supports the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Up to six transmitters and four receivers with TX2/RX3, TX3/RX2, TX4/RX1 and TX5/RX0 pins shared by transmitters 2 to 5 and receivers 0 to 3. TX0 and TX1 pins are used by transmitters 0 and 1 only.
- Programmable data interface modes such as I2S, LSB aligned, MSB aligned
- Programmable word length (8, 12, 16, 20 or 24bits)
- AC97 support
- 128-word Transmit FIFO shared by six transmitters
- 128-word Receive FIFO shared by four receivers

Figure 4 illustrates the ESAI integration with the CL-SOM-iMX6 audio sub-system. For additional details, please refer to the "i.MX6 Reference Manual". The table below summarizes the ESAI interface signals

Table 21 ESAI Interface Signals

Signal Name	Pin #	Type	Description	Availability
ESAI_RX_CLK	P2-71*	IO	RX serial bit clock	Always
ESAI_RX_FS	P2-77*	IO	RX frame sync signal	Always
ESAI_RX_HF_CLK	P2-128*	IO	RX high frequency clock	Always
ESAI_TX_CLK	P2-89*	IO	TX serial bit clock	Always
ESAI_TX_FS	P1-58*	IO	Frame sync for both the transmitters and the receivers in synchronous mode (SYN=1) or the transmitters only in asynchronous mode	Always
ESAI_TX_FS	P2-20*	IO	Frame sync for both the transmitters and the receivers in synchronous mode (SYN=1) or the transmitters only in asynchronous mode	Always
ESAI_TX_HF_CLK	P1-56*	IO	TX high frequency clock	Always
ESAI_TX_HF_CLK	P2-121*	IO	TX high frequency clock	Always
ESAI_TX0	P2-97*	IO	Transmit data 0	Always
ESAI_TX1	P2-119*	IO	Transmit data 1	Always
ESAI_TX2_RX3	P2-39*	IO	Transmit data 2 / Receive data 3	Always
ESAI_TX2_RX3	P2-53*	IO	Transmit data 2 / Receive data 3	Always
ESAI_TX3_RX2	P1-20*	IO	Transmit data 3 / Receive data 2	Always
ESAI_TX4_RX1	P1-72*	IO	Transmit data 4 / Receive data 1	Always
ESAI_TX5_RX0	P1-61*	IO	Transmit data 5 / Receive data 0	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.4.2.3 Synchronous Serial Interface (SSI) and Digital Audio Multiplexer (AUDMUX)

CL-SOM-iMX6 is equipped with three SSI ports. The SSI port is a full-duplex, serial port designed for communication with a variety of devices that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard. The following main features are supported:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots

- Gated Clock mode operation requiring no frame sync
- 2 sets of Transmit and Receive FIFOs. Each of the four FIFOs is 15x32 bits. The two sets of Tx/Rx FIFOs can be used in Network mode to provide 2 independent channels for transmission and reception
- Programmable data interface modes such as I2S, LSB, MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- Program options for frame sync and clock generation
- Programmable I2S modes (Master, Slave or Normal). 8 kHz up to 196 kHz audio sampling rate.
- AC97 support. 8 kHz up to 48 kHz frame rate

The SSI ports are accessible through the "Digital Audio multiplexer" (AUDMUX) block.

AUDMUX enables programmable synchronous data routing between the SSI ports and devices external to the i.MX6 SoC. The CL-SOM-iMX6 on-board analog audio codec and the bluetooth audio devices communicate with their SSI ports through AUDMUX ports 4 and 3 respectively (see Figure 4). AUDMUX supports the below listed features:

- Three internal ports
- Four external ports
- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx Frame sync and clock direction selection for host or peripheral
- Each host interface capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)

For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the AUDMUX interface signals

Table 22 AUDMUX port 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
AUD3_RXC	P1-39*	IO	Receive clock signal	not ('WAB' or 'WB')
AUD3_RXD	P1-49*	IO	Data receive signal	not ('WAB' or 'WB')
AUD3_RXFS	P1-41*	IO	Receive Frame sync signal	not ('WAB' or 'WB')
AUD3_TXC	P1-48*	IO	Transmit clock signal	not ('WAB' or 'WB')
AUD3_TXD	P1-45*	IO	Data transmit signal	not ('WAB' or 'WB')
AUD3_TXFS	P1-47*	IO	Transmit Frame sync signal	not ('WAB' or 'WB')

Table 23 AUDMUX port 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
AUD4_RXC	P1-99*	IO	Receive clock signal	Always
AUD4_RXC	P2-57*	IO	Receive clock signal	not 'A'
AUD4_RXD	P1-104*	IO	Data receive signal	Always
AUD4_RXD	P2-47*	IO	Data receive signal	not 'A'
AUD4_RXFS	P1-97*	IO	Receive Frame sync signal	Always
AUD4_RXFS	P2-59*	IO	Receive Frame sync signal	not 'A'
AUD4_TXC	P1-100*	IO	Transmit clock signal	Always
AUD4_TXC	P2-45*	IO	Transmit clock signal	not 'A'
AUD4_TXD	P1-101*	IO	Data transmit signal	Always
AUD4_TXD	P2-49*	IO	Data transmit signal	not 'A'
AUD4_TXFS	P1-102*	IO	Transmit Frame sync signal	Always
AUD4_TXFS	P2-51*	IO	Transmit Frame sync signal	not 'A'

Table 24 AUDMUX port 5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
AUD5_RXC	P1-73*	IO	Receive clock signal	Always
AUD5_RXC	P1-93*	IO	Receive clock signal	Always
AUD5_RXD	P1-66*	IO	Data receive signal	Always
AUD5_RXD	P1-99*	IO	Data receive signal	Always

Signal Name	Pin #	Type	Description	Availability
AUD5_RXFS	P1-65*	IO	Receive Frame sync signal	Always
AUD5_RXFS	P1-92*	IO	Receive Frame sync signal	Always
AUD5_TXC	P1-95*	IO	Transmit clock signal	Always
AUD5_TXD	P1-96*	IO	Data transmit signal	Always
AUD5_TXFS	P1-64*	IO	Transmit Frame sync signal	Always
AUD5_TXFS	P1-97*	IO	Transmit Frame sync signal	Always

Table 25 AUDMUX port 6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
AUD6_RXC	P1-83*	IO	Receive clock signal	Always
AUD6_RXD	P1-60*	IO	Data receive signal	Always
AUD6_RXFS	P1-82*	IO	Receive Frame sync signal	Always
AUD6_TXC	P1-105*	IO	Transmit clock signal	Always
AUD6_TXD	P1-109*	IO	Data transmit signal	Always
AUD6_TXFS	P1-107*	IO	Transmit Frame sync signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.5 Wireless

CL-SOM-iMX6 optional wireless communication capabilities are implemented with one of the following two assembly options:

- FCC Certified Single Band WLAN + Bluetooth are available with the “WB” ordering option of CL-SOM-iMX6. Please refer to section 4.5.1 for additional details.
- Dual Band WLAN + Bluetooth are available with the “WAB” ordering option of CL-SOM-iMX6. Please refer to 4.5.2 for additional details.

CL-SOM-iMX6 with the “WB” or the “WAB” option is equipped with a single U.FL high frequency connector allowing easy integration with external antennas:

- Primary WLAN/BT antenna connector J1 or J2. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality. J1 is available with the “WAB” ordering option while J2 is available with the “WB” ordering option of CL-SOM-iMX6.

Table 26 J1 or J2 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

4.5.1 Certified Single Band WLAN + Bluetooth

The optional single band WLAN + Bluetooth capabilities are based on the Murata LBEE5KL1DX module soldered onboard. LBEE5KL1DX is based on the Cypress (Broadcom) BCM4343W chipset enabling Single-Band Wi-Fi and Bluetooth functionality with CL-SOM-iMX6. LBEE5KL1DX supports the following features:

- FCC certified with chip antennas.
- Support of IEEE Std 802.11b, 802.11g and 802.11n.
- Bluetooth 4.1/EDR + BLE
- AP & STA dual mode network topologies support
- Power Class 1 (10dBm max) + BLE

When populated, LBEE5KL1DX is interfaced with the i.MX6 through the following interfaces:

- i.MX6 MMC/SD/SDIO1 interface is used for WLAN data.
- i.MX6 UART5 and AUDMUX port 3 interfaces are employed for Bluetooth and A2DP

data.

- J2 U.FL connector is available for external antenna connection.

Please refer to the i.MX6 and the Murata respective documentation for additional details.

NOTE: CL-SOM-iMX6 Certified Single Band WiFi functionality is available only with the 'WB' ordering option. Bluetooth Functionality is available with either 'WB' or 'WAB' ordering options

4.5.2 Dual Band WLAN + Bluetooth

The optional Dual band WLAN + Bluetooth capabilities are based on the Murata LBEH5HMZPC module soldered onboard. LBEH5HMZPC is based on the Cypress (Broadcom) BCM4339 chipset enabling Dual Band Wi-Fi® and Bluetooth functionality with CL-SOM-iMX6. LBEH5HMZPC supports the following features:

- Support of IEEE Std 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac.
- Dual Band support (5GHz & 2.4GHz bands).
- AP & STA dual mode network topologies support
- Advanced beamforming (802.11ac/n), Low-Density Parity Check (LDPC) code and Space-Time Block Code (STBC) support
- Wi-Fi Direct support
- Bluetooth v4.0+EDR + BLE

When populated, LBEH5HMZPC is interfaced with the i.MX6 through the following interfaces:

- i.MX6 MMC/SD/SDIO1 interface is used for WLAN data.
- i.MX6 UART5 and AUDMUX port 3 interfaces are employed for Bluetooth and A2DP data.
- J1 U.FL connector is available for external antenna connection.

Please refer to the i.MX6 and the Murata respective documentation for additional details.

NOTE: CL-SOM-iMX6 Dual Band 802.11a and 802.11ac capable WiFi functionality is available only with the 'WAB' ordering option. Bluetooth Functionality is available with either 'WB' or 'WAB' ordering options.

4.6 High-Definition Multimedia Interface (HDMI)

The HDMI interface available with CL-SOM-iMX6 is based on the "HDMI transmitter" & "HDMI 3D Tx PHY" integrated into the i.MX6 SoC. The "HDMI transmitter" combines video/display data from the IPU, Audio data from i.MX6 memory & control/status data from the ARM complex, into TMDS data & clock channels. The "HDMI 3D Tx PHY" transmits the combined data by means of 3 TMDS data pairs and a TMDS clock pair to the CL-SOM-iMX6 carrier board interface.

Figure 3 shows the video/display data path from the IPU to the CL-SOM-iMX6 carrier board interface through the HDMI transmitter & PHY. The HDMI audio data path is shown in Figure 4.

The HDMI 3D Tx PHY integrated into the i.MX6 SoC supports the following standards & features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a
- Support for up to 720p at 100Hz and 720i at 200Hz or 1080p at 60Hz and 1080i/720i at 120Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

For additional details, please refer to the "i.MX6 Reference Manual". The table below summarizes the HDMI interface signals

Table 27 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_CLKM	P2-16	AO	TMDS differential clock negative signal	Always
HDMI_CLKP	P2-18	AO	TMDS differential clock positive signal	Always
HDMI_D0M	P2-22	AO	TMDS differential data 0 negative signal	Always
HDMI_D0P	P2-24	AO	TMDS differential data 0 positive signal	Always
HDMI_D1M	P2-42	AO	TMDS differential data 1 negative signal	Always
HDMI_D1P	P2-44	AO	TMDS differential data 1 positive signal	Always
HDMI_D2M	P2-48	AO	TMDS differential data 2 negative signal	Always
HDMI_D2P	P2-50	AO	TMDS differential data 2 positive signal	Always
HDMI_HPD	P2-32	I	Hot Plug Detect signal, 5V tolerant.	Always
HDMI_TX_CEC_LINE	P2-6*	IO	Consumer Electronics Control signal	Always
HDMI_TX_DDC_SCL	P1-116*	IO	VESA Data Display Channel clock signal	Always
HDMI_TX_DDC_SDA	P1-125*	IO	VESA Data Display Channel data signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.7 MediaLB device interface

The Media Local Bus (MediaLB) is a standardized, inter-chip communication bus for "MOST" based devices. CL-SOM-iMX6 can act as a MediaLB device, utilizing the i.MX6 integrated MLB150 block which implements all the required functionality, including:

- Transmission of commands and data when functioning as the transmitting device associated with a channel address
- Reception of data and transmission of Rx status responses when functioning as the receiving device associated with a channel address
- MediaLB lock detection
- SystemChannel command handling

The MediaLB interface is accessible through the carrier board interface as a single ended interface (3 pins). The MediaLB audio path is illustrated in Figure 4.

For additional details, please refer to the "i.MX6 Reference Manual".

NOTE: The MediaLB device controller in not available by default. Please contact CompuLab for more information.

The table below summarizes the MediaLB interface signals

Table 28 MediaLB Interface Signals

Signal Name	Pin #	Type	Description	Availability
MLB_CLK	P2-39*	I	Single ended MediaLB bus clock (MUXED)	Contact Compulab
MLB_DATA	P1-58*	IO	Single ended MediaLB data (MUXED)	Contact Compulab
MLB_SIG	P2-20*	IO	Single ended MediaLB signaling information (MUXED)	Contact Compulab

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.8 Ethernet

CL-SOM-iMX6 incorporates a full-featured 10/100/1000 Ethernet interface, implemented with the i.MX6 integrated Ethernet MAC (ENET) coupled with the AR8033 RGMII Ethernet PHY from Atheros.

The CL-SOM-iMX6 Ethernet interface supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- IEEE 802.3u compliant Auto-Negotiation
- Integrated IEEE 1588 time stamping module (inside the MAC).
- Automatic channel swap (ACS)
- Full- and Half-duplex
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Activity and speed indicator LED controls

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

For additional details, please refer to the "i.MX6 Reference Manual". The table below summarizes the Ethernet interface signals

Table 29 Ethernet Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH_LED_ACT	P1-6^	AIO	Active High, activity LED driver. 2.5V signal	'E'
ETH_LINK-LED_10_100	P1-5^	AIO	Active High, 10/100Mbps link LED driver. 2.5V signal	'E'
ETH_LINK-LED_1000	P1-13^	AIO	Active High, 1Gbps link LED driver. 2.5V signal	'E'
ETH_MDI0N	P1-4	AIO	Negative part of 100ohm diff-pair 0	'E'
ETH_MDI0P	P1-2	AIO	Positive part of 100ohm diff-pair 0	'E'
ETH_MDI1N	P1-3	AIO	Negative part of 100ohm diff-pair 1	'E'
ETH_MDI1P	P1-1	AIO	Positive part of 100ohm diff-pair 1	'E'
ETH_MDI2N	P1-12	AIO	Negative part of 100ohm diff-pair 2	'E'
ETH_MDI2P	P1-10	AIO	Positive part of 100ohm diff-pair 2	'E'
ETH_MDI3N	P1-11	AIO	Negative part of 100ohm diff-pair 3	'E'
ETH_MDI3P	P1-9	AIO	Positive part of 100ohm diff-pair 3	'E'

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.9 USB 2.0

4.9.1 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the i.MX6 USB 2.0 OTG controller. The interface provides the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation in host mode
- Supports USB 2.0 High Speed (480 Mbps) and Full Speed (12 Mbps) operation in peripheral mode.
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints

The table below summarizes the USB2.0 OTG interface signals

Table 30 USB2.0 OTG Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_OTG_CHD_B	P1-80	IO	Charge detect signal	Always
USB_OTG_DN	P2-130	AIO	i.MX6 Native USB OTG port 1 DN signal	Always
USB_OTG_DP	P2-132	AIO	i.MX6 Native USB OTG port 1 DP signal	Always
USB_OTG_ID	P2-128*	I	USB OTD ID signal	Always
USB_OTG_ID	P2-71*	I	USB OTD ID signal	Always
USB_OTG_OC	P2-27*	I	OTG External input for VBUS overcurrent detection	Always
USB_OTG_OC	P2-85*	I	OTG External input for VBUS overcurrent detection	Always
USB_OTG_PWR	P2-104*	O	i.MX6 output to control OTG VBUS supply voltage	Always
USB_OTG_PWR	P2-87*	O	i.MX6 output to control OTG VBUS supply voltage	Always
USB_OTG_VBUS	P2-116	PI	VBUS input for i.MX6 Native USB OTG port	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

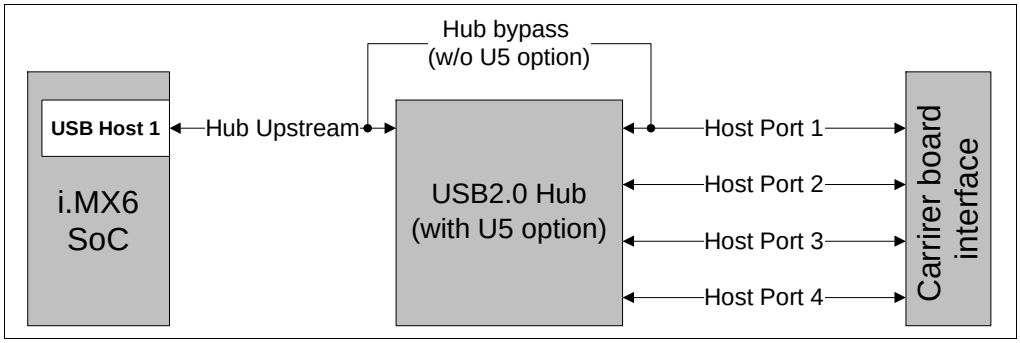
4.9.2 USB 2.0 Host

The CL-SOM-iMX6 high-speed USB interface is implemented with the i.MX6 high-speed USB host port 1. The interface supports the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation
- Complies with EHCI (high-speed host controller)

CL-SOM-iMX6 enables up to 4 USB Host ports by utilizing an optional on-board USB2.0 hub. The USB2.0 host ports mapping is shown in Figure 5.

Figure 5 USB2.0 Host ports



The tables below summarize the USB2.0 host interface signals

Table 31 USB2.0 host port1 (Native) Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_H1_DN	P1-130	AIO	i.MX6 Native USB host port 1 DN signal	not 'U5'
USB_H1_DP	P1-132	AIO	i.MX6 Native USB host port 1 DP signal	not 'U5'
USB_H1_OC	P1-46*	I	i.MX6 Host 1 External input for VBUS overcurrent detection	Always
USB_H1_PWR	P1-124*	O	i.MX6 output to control host VBUS supply voltage	not 'U5'
USB_H1_PWR	P1-44*	O	i.MX6 output to control host VBUS supply voltage	Always
USB_H1_VBUS	P1-140	PI	VBUS input for i.MX6 Native USB host port	not 'U5'

Table 32 USB2.0 host port1 (onboard Hub) Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB1_CPEN	P1-124	O	Active high output to control host VBUS supply voltage. High = VBUS enabled.	'U5'
USB1_DN	P1-130	AIO	Hub USB host port 1 DN signal	'U5'
USB1_DP	P1-132	AIO	Hub USB host port 1 DP signal	'U5'
USBHUBP1_NOVC	P1-106	I	Active low input, designed to inform SOM-iMX6 of an overcurrent condition on VBUS rail of USB Host port 1 (if detected by the VBUS power supply). Low = Overcurrent detected.	'U5'

Table 33 USB2.0 host port2 (onboard Hub) Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB2_CPEN	P1-128	O	Active high output to control host VBUS supply voltage. High = VBUS enabled.	'U5'
USB2_DN	P1-137	AIO	Hub USB host port 2 DN signal	'U5'
USB2_DP	P1-138	AIO	Hub USB host port 2 DP signal	'U5'
USBHUBP2_NOVC	P2-140	I	Active low input, designed to inform SOM-iMX6 of an overcurrent condition on VBUS rail of USB Host port 2 (if detected by the VBUS power supply). Low = Overcurrent detected.	'U5'

Table 34 USB2.0 host port3 (onboard Hub) Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB3_CPEN	P1-126	O	Active high output to control host VBUS supply voltage. High = VBUS enabled.	'U5'

Signal Name	Pin #	Type	Description	Availability
USB3_DN	P1-129	AIO	Hub USB host port 3 DN signal	'U5'
USB3_DP	P1-131	AIO	Hub USB host port 3 DP signal	'U5'
USBHUBP3_NOVC	P2-138	I	Active low input, designed to inform SOM-iMX6 of an overcurrent condition on VBUS rail of USB Host port 3 (if detected by the VBUS power supply). Low = Overcurrent detected.	'U5'

Table 35 USB2.0 host port4 (onboard Hub) Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB4_CPEN	P1-133	O	Active high output to control host VBUS supply voltage. High = VBUS enabled.	'U5'
USB4_DN	P1-135	AIO	Hub USB host port 4 DN signal	'U5'
USB4_DP	P1-136	AIO	Hub USB host port 4 DP signal	'U5'
USBHUBP4_NOVC	P2-136	I	Active low input, designed to inform SOM-iMX6 of an overcurrent condition on VBUS rail of USB Host port 4 (if detected by the VBUS power supply). Low = Overcurrent detected.	'U5'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.10 UARTs

Up to 5 UART ports are available with CL-SOM-iMX6. All the UART ports are derived from the i.MX6 SoC integrated UARTs and support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive
- DCE/DTE modes support

NOTE: UART signal direction in tables below it true only when i.MX6 UART controller operates in DCE mode. Please refer to "i.MX6 Reference Manual" for DTE mode signal directions.

NOTE: The UART5 interface is utilized by the bluetooth adapter available onboard CL-SOM-iMX6 (only boards with 'WB or 'WAB' ordering options). Using the UART5 interface with the carrier board precludes operation of the bluetooth adapter.

For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the UART interface signals

Table 36 UART1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	P2-54*	O	Clear to send	Always
UART1_DSR_B	P1-73*	IO	Data set ready	Always
UART1_DTR_B	P1-65*	IO	Data terminal ready	Always

Signal Name	Pin #	Type	Description	Availability
UART1_RTS_B	P2-56*	I	Request to send	Always
UART1_RX_DATA	P1-112*	I	Serial/infrared data receive	Always
UART1_RX_DATA	P1-41*	I	Serial/infrared data receive	not ('WAB' or 'WB')
UART1_TX_DATA	P1-114*	O	Serial/infrared data transmit	Always
UART1_TX_DATA	P1-39*	O	Serial/infrared data transmit	not ('WAB' or 'WB')

Table 37 UART2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS_B	P1-70*	O	Clear to send	not ('N4', 'N16' or 'N32')
UART2_CTS_B	P2-25*	O	Clear to send	Always
UART2_CTS_B	P2-78*	O	Clear to send	Always
UART2_RTS_B	P1-68*	I	Request to send	not ('N4', 'N16' or 'N32')
UART2_RTS_B	P2-76*	I	Request to send	Always
UART2_RX_DATA	P1-40*	I	Serial/infrared data receive	Always
UART2_RX_DATA	P1-61*	I	Serial/infrared data receive	Always
UART2_RX_DATA	P2-13*	I	Serial/infrared data receive	Always
UART2_TX_DATA	P1-42*	O	Serial/infrared data transmit	Always
UART2_TX_DATA	P1-72*	O	Serial/infrared data transmit	Always
UART2_TX_DATA	P2-41*	O	Serial/infrared data transmit	Always

Table 38 UART3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3_CTS_B	P1-46*	O	Clear to send	Always
UART3_CTS_B	P2-60*	O	Clear to send	Always
UART3_RTS_B	P1-44*	I	Request to send	Always
UART3_RX_DATA	P1-73*	I	Serial/infrared data receive	Always
UART3_TX_DATA	P1-65*	O	Serial/infrared data transmit	Always

Table 39 UART4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4_CTS_B	P2-80*	O	Clear to send	Always
UART4_RTS_B	P2-72*	I	Request to send	Always
UART4_RX_DATA	P2-66*	I	Serial/infrared data receive	Always
UART4_TX_DATA	P2-64*	O	Serial/infrared data transmit	Always

Table 40 UART5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART5_CTS_B	P2-84*	O	Clear to send	not ('WAB' or 'WB')
UART5_CTS_B	P2-87*	O	Clear to send	Always
UART5_RTS_B	P2-82*	I	Request to send	not ('WAB' or 'WB')
UART5_RTS_B	P2-85*	I	Request to send	Always
UART5_RX_DATA	P1-66*	I	Serial/infrared data receive	Always
UART5_RX_DATA	P2-70*	I	Serial/infrared data receive	not ('WAB' or 'WB')
UART5_TX_DATA	P1-64*	O	Serial/infrared data transmit	Always
UART5_TX_DATA	P2-68*	O	Serial/infrared data transmit	not ('WAB' or 'WB')

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.11 RS232

The CL-SOM-iMX6 incorporates a single RS232 port. The following features are supported:

- 32-entry FIFO for receiver and 32-entry FIFO for transmitter
- Programmable baud rate of up to 250 kbit/s
- 7 or 8 data bits per symbol.
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART-4 of the i.MX6 SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

NOTE: Using the RS-232 port precludes the use of UART-4 port.

The table below summarizes the RS232 interface signals

Table 41 RS232 Interface Signals

Signal Name	Pin #	Type	Description	Availability
RS232_RXD	P1-117	I	RS232 serial data in, RS-232 voltage levels	Always
RS232_TXD	P1-119	O	RS232 serial data out, RS-232 voltage levels	Always

4.12 MMC / SD / SDIO

The CL-SOM-iMX6 features 3 MMC / SD / SDIO host interfaces implemented with the i.MX6 integrated "Ultra Secured Digital Host Controller" (uSDHC). The following main features are supported by uSDHC:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.5.
- Conforms to the SD Host Controller Standard Specification version 3.0.
- Compatible with the SD Memory Card Specification version 3.0 and supports the "Extended Capacity SD Memory Card".
- Compatible with the SDIO Card Specification version 3.0.
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit
- 8-bit MMC modes (MMC-3 only).

Each MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

The MMC-1 controller interface controller interface supports up to 4-bit transfer modes. This interface is used for CL-SOM-iMX6 WLAN and Bluetooth functionality ("WB" product option). In case the "WB" option is not populated on-board CL-SOM-iMX6, MMC-1 is accessible through the carrier board interface.

The MMC-2 controller interface supports up to 4-bit transfer modes. This interface is only available at the carrier board interface whenever CL-SOM-iMX6 does not include the optional analog audio codec ("A" product option).

The MMC-3 controller interface supports up to 8-bit transfer modes. MMC-3 is always accessible through the carrier board interface. The MMC-3 interface is bootable, meaning CL-SOM-iMX6 can boot from an SD card over the MMC-3 interface.

For additional details, please refer to the "i.MX6 Reference Manual".

The tables below summarize the MMC/SD/SDIO interface signals

Table 42 MMC/SD/SDIO1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD1_CD_B	P2-71*	I	Active low card detection signal	Always
SD1_CLK	P2-73*	IO	Interface clock	not ('WAB' or 'WB')

Signal Name	Pin #	Type	Description	Availability
SD1_CMD	P2-75*	IO	Command signal	not ('WAB' or 'WB')
SD1_DATA0	P2-61*	IO	Card data bit 0	not ('WAB' or 'WB')
SD1_DATA1	P2-63*	IO	Card data bit 1	not ('WAB' or 'WB')
SD1_DATA2	P2-65*	IO	Card data bit 2	not ('WAB' or 'WB')
SD1_DATA3	P2-69*	IO	Card data bit 3	not ('WAB' or 'WB')
SD1_LCTL	P1-20*	O	An external LED control signal, designed to indicate that the SD interface is busy	Always
SD1_WP	P1-60*	I	Active low write protection signal	Always
SD1_WP	P2-77*	I	Active low write protection signal	Always

Table 43 MMC/SD/SDIO2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD2_CD_B	P1-56*	I	Active low card detection signal	Always
SD2_CLK	P2-59*	IO	Interface clock	not 'A'
SD2_CMD	P2-57*	IO	Command signal	not 'A'
SD2_DATA0	P2-47*	IO	Card data bit 0	not 'A'
SD2_DATA1	P2-51*	IO	Card data bit 1	not 'A'
SD2_DATA2	P2-49*	IO	Card data bit 2	not 'A'
SD2_DATA3	P2-45*	IO	Card data bit 3	not 'A'
SD2_WP	P1-58*	I	Active low write protection signal	Always

Table 44 MMC/SD/SDIO3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD3_CLK	P2-76*	IO	Interface clock	Always
SD3_CMD	P2-78*	IO	Command signal	Always
SD3_DATA0	P2-54*	IO	Card data bit 0	Always
SD3_DATA1	P2-56*	IO	Card data bit 1	Always
SD3_DATA2	P2-58*	IO	Card data bit 2	Always
SD3_DATA3	P2-60*	IO	Card data bit 3	Always
SD3_DATA4	P2-13*	IO	Card data bit 4	Always
SD3_DATA5	P2-41*	IO	Card data bit 5	Always
SD3_DATA6	P1-112*	IO	Card data bit 6	Always
SD3_DATA7	P1-114*	IO	Card data bit 7	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.13 Touch-Screen

CL-SOM-iMX6 features an optional on-board resistive touch-screen controller. The controller is communicating with the i.MX6 SoC over the SPI-1 interface. The interface supports 4-wire touch panels and is available through the CL-SOM-iMX6 carrier board interface.

The table below summarizes the Resistive Touch interface signals

Table 45 Resistive Touch Interface Signals

Signal Name	Pin #	Type	Description	Availability
TS_XN	P1-21	AIO	Touch screen X- (left)	'I'
TS_XP	P1-23	AIO	Touch screen X+ (right)	'I'
TS_YN	P1-27	AIO	Touch screen Y- (bottom)	'I'
TS_YP	P1-29	AIO	Touch screen Y+ (top)	'I'

4.14 Keypad

The CL-SOM-iMX6 CoM features a 7x7 matrix keypad interface derived from the keypad port (KPP) included with the i.MX6 SoC. The KPP supports the following features:

- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Supports a 2-point and 3-point contact key matrix

For additional details, please refer to the “i.MX6 Reference Manual”.

The table below summarizes the Keypad interface signals

Table 46 Keypad Interface Signals

Signal Name	Pin #	Type	Description	Availability
KEY_COL1	P1-64*	IO	Column input or output pin	Always
KEY_COL2	P2-5*	IO	Column input or output pin	Always
KEY_COL3	P1-116*	IO	Column input or output pin	Always
KEY_COL4	P2-85*	IO	Column input or output pin	Always
KEY_COL5	P1-124*	IO	Column input or output pin	not 'U5'
KEY_COL5	P1-32*	IO	Column input or output pin	Always
KEY_COL5	P1-48*	IO	Column input or output pin	not ('WAB' or 'WB')
KEY_COL5	P2-59*	IO	Column input or output pin	not 'A'
KEY_COL6	P1-47*	IO	Column input or output pin	not ('WAB' or 'WB')
KEY_COL6	P2-45*	IO	Column input or output pin	not 'A'
KEY_COL6	P2-77*	IO	Column input or output pin	Always
KEY_COL7	P1-33*	IO	Column input or output pin	Always
KEY_COL7	P1-56*	IO	Column input or output pin	Always
KEY_COL7	P2-51*	IO	Column input or output pin	not 'A'
KEY_ROW1	P1-66*	IO	Row input or output pin	Always
KEY_ROW2	P2-6*	IO	Row input or output pin	Always
KEY_ROW3	P1-125*	IO	Row input or output pin	Always
KEY_ROW4	P2-87*	IO	Row input or output pin	Always
KEY_ROW5	P1-45*	IO	Row input or output pin	not ('WAB' or 'WB')
KEY_ROW5	P2-57*	IO	Row input or output pin	not 'A'
KEY_ROW5	P2-71*	IO	Row input or output pin	Always
KEY_ROW6	P1-49*	IO	Row input or output pin	not ('WAB' or 'WB')
KEY_ROW6	P1-58*	IO	Row input or output pin	Always
KEY_ROW6	P2-49*	IO	Row input or output pin	not 'A'
KEY_ROW7	P1-35*	IO	Row input or output pin	Always
KEY_ROW7	P2-47*	IO	Row input or output pin	not 'A'
KEY_ROW7	P2-53*	IO	Row input or output pin	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.15 GPIO

CL-SOM-iMX6 provides up to 112 GPIO signals. The GPIO subsystem is derived from the i.MX6 integrated GPIO controller. i.MX6 GPIOs are divided into 8 blocks with up to 32 GPIOs in each block (a total of 8 x 32 = 256 GPIOs). The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the "i.MX6 Reference Manual".

NOTE: Not all GPIO signals supported by the i.MX6 SoC are available through the CL-SOM-iMX6 carrier board interface.

The table below summarizes the GPIO interface signals

Table 47 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1_IO00	P1-124*	IO	General purpose input/output	not 'U5'
GPIO1_IO01	P2-71*	IO	General purpose input/output	Always
GPIO1_IO02	P1-58*	IO	General purpose input/output	Always
GPIO1_IO04	P1-56*	IO	General purpose input/output	Always
GPIO1_IO05	P2-53*	IO	General purpose input/output	Always
GPIO1_IO07	P1-72*	IO	General purpose input/output	Always
GPIO1_IO08	P1-61*	IO	General purpose input/output	Always
GPIO1_IO09	P2-77*	IO	General purpose input/output	Always
GPIO1_IO10	P2-59*	IO	General purpose input/output	not 'A'
GPIO1_IO11	P2-57*	IO	General purpose input/output	not 'A'
GPIO1_IO12	P2-45*	IO	General purpose input/output	not 'A'
GPIO1_IO13	P2-49*	IO	General purpose input/output	not 'A'
GPIO1_IO14	P2-51*	IO	General purpose input/output	not 'A'
GPIO1_IO15	P2-47*	IO	General purpose input/output	not 'A'
GPIO1_IO16	P2-61*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO17	P2-63*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO18	P2-75*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO19	P2-65*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO20	P2-73*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO21	P2-69*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO1_IO24	P2-128*	IO	General purpose input/output	Always
GPIO1_IO25	P2-89*	IO	General purpose input/output	Always
GPIO1_IO26	P2-20*	IO	General purpose input/output	Always
GPIO1_IO27	P2-121*	IO	General purpose input/output	Always
GPIO1_IO29	P2-39*	IO	General purpose input/output	Always
GPIO2_IO09	P2-40*	IO	General purpose input/output	not ('N4', 'N16' or 'N32')
GPIO2_IO10	P2-29*	IO	General purpose input/output	not ('N4', 'N16' or 'N32')
GPIO2_IO13	P1-68*	IO	General purpose input/output	not ('N4', 'N16' or 'N32')
GPIO2_IO14	P1-70*	IO	General purpose input/output	not ('N4', 'N16' or 'N32')
GPIO2_IO23	P1-71*	IO	General purpose input/output	Always
GPIO2_IO24	P1-69*	IO	General purpose input/output	Always
GPIO2_IO25	P1-63*	IO	General purpose input/output	Always
GPIO3_IO21	P2-27*	IO	General purpose input/output	Always
GPIO3_IO22	P2-104*	IO	General purpose input/output	Always
GPIO3_IO24	P1-65*	IO	General purpose input/output	Always
GPIO3_IO25	P1-73*	IO	General purpose input/output	Always
GPIO3_IO26	P1-42*	IO	General purpose input/output	Always
GPIO3_IO27	P1-40*	IO	General purpose input/output	Always
GPIO3_IO28	P2-25*	IO	General purpose input/output	Always
GPIO3_IO30	P1-46*	IO	General purpose input/output	Always
GPIO3_IO31	P1-44*	IO	General purpose input/output	Always
GPIO4_IO05	P1-32*	IO	General purpose input/output	Always
GPIO4_IO08	P1-64*	IO	General purpose input/output	Always
GPIO4_IO09	P1-66*	IO	General purpose input/output	Always
GPIO4_IO10	P2-5*	IO	General purpose input/output	Always
GPIO4_IO11	P2-6*	IO	General purpose input/output	Always
GPIO4_IO12	P1-116*	IO	General purpose input/output	Always

Signal Name	Pin #	Type	Description	Availability
GPIO4_IO13	P1-125*	IO	General purpose input/output	Always
GPIO4_IO14	P2-85*	IO	General purpose input/output	Always
GPIO4_IO15	P2-87*	IO	General purpose input/output	Always
GPIO4_IO16	P1-108*	IO	General purpose input/output	Always
GPIO4_IO17	P1-105*	IO	General purpose input/output	Always
GPIO4_IO18	P1-109*	IO	General purpose input/output	Always
GPIO4_IO19	P1-107*	IO	General purpose input/output	Always
GPIO4_IO20	P1-60*	IO	General purpose input/output	Always
GPIO4_IO21	P1-75*	IO	General purpose input/output	Always
GPIO4_IO22	P1-76*	IO	General purpose input/output	Always
GPIO4_IO23	P1-77*	IO	General purpose input/output	Always
GPIO4_IO24	P1-78*	IO	General purpose input/output	Always
GPIO4_IO25	P1-81*	IO	General purpose input/output	Always
GPIO4_IO26	P1-82*	IO	General purpose input/output	Always
GPIO4_IO27	P1-83*	IO	General purpose input/output	Always
GPIO4_IO28	P1-84*	IO	General purpose input/output	Always
GPIO4_IO29	P1-85*	IO	General purpose input/output	Always
GPIO4_IO30	P1-87*	IO	General purpose input/output	Always
GPIO4_IO31	P1-88*	IO	General purpose input/output	Always
GPIO5_IO05	P1-89*	IO	General purpose input/output	Always
GPIO5_IO06	P1-90*	IO	General purpose input/output	Always
GPIO5_IO07	P1-92*	IO	General purpose input/output	Always
GPIO5_IO08	P1-93*	IO	General purpose input/output	Always
GPIO5_IO09	P1-94*	IO	General purpose input/output	Always
GPIO5_IO10	P1-95*	IO	General purpose input/output	Always
GPIO5_IO11	P1-96*	IO	General purpose input/output	Always
GPIO5_IO12	P1-97*	IO	General purpose input/output	Always
GPIO5_IO13	P1-99*	IO	General purpose input/output	Always
GPIO5_IO14	P1-100*	IO	General purpose input/output	Always
GPIO5_IO15	P1-101*	IO	General purpose input/output	Always
GPIO5_IO16	P1-102*	IO	General purpose input/output	Always
GPIO5_IO17	P1-104*	IO	General purpose input/output	Always
GPIO5_IO18	P1-57*	IO	General purpose input/output	Always
GPIO5_IO19	P1-51*	IO	General purpose input/output	Always
GPIO5_IO20	P1-59*	IO	General purpose input/output	Always
GPIO5_IO21	P1-53*	IO	General purpose input/output	Always
GPIO5_IO22	P1-48*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO23	P1-45*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO24	P1-47*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO25	P1-49*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO26	P1-33*	IO	General purpose input/output	Always
GPIO5_IO27	P1-35*	IO	General purpose input/output	Always
GPIO5_IO28	P1-39*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO29	P1-41*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO5_IO30	P2-64*	IO	General purpose input/output	Always
GPIO5_IO31	P2-66*	IO	General purpose input/output	Always
GPIO6_IO00	P2-68*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO6_IO01	P2-70*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO6_IO02	P2-72*	IO	General purpose input/output	Always
GPIO6_IO03	P2-80*	IO	General purpose input/output	Always
GPIO6_IO04	P2-82*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO6_IO05	P2-84*	IO	General purpose input/output	not ('WAB' or 'WB')
GPIO6_IO15	P2-97*	IO	General purpose input/output	Always
GPIO6_IO17	P1-114*	IO	General purpose input/output	Always
GPIO6_IO18	P1-112*	IO	General purpose input/output	Always
GPIO7_IO00	P2-41*	IO	General purpose input/output	Always
GPIO7_IO01	P2-13*	IO	General purpose input/output	Always
GPIO7_IO02	P2-78*	IO	General purpose input/output	Always
GPIO7_IO03	P2-76*	IO	General purpose input/output	Always
GPIO7_IO04	P2-54*	IO	General purpose input/output	Always
GPIO7_IO05	P2-56*	IO	General purpose input/output	Always
GPIO7_IO06	P2-58*	IO	General purpose input/output	Always
GPIO7_IO07	P2-60*	IO	General purpose input/output	Always
GPIO7_IO11	P1-20*	IO	General purpose input/output	Always
GPIO7_IO13	P2-119*	IO	General purpose input/output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.16 I²C

The CL-SOM-iMX6 features three general purpose I²C interfaces. The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

The I²C interfaces are implemented with the i.MX6 integrated I²C controller. For additional details, please refer to the "i.MX6 Reference Manual".

The tables below summarize the I2C interface signals

Table 48 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_SCL	P1-35*	IOD	I2C serial clock line	Always
I2C1_SCL	P2-27*	IOD	I2C serial clock line	Always
I2C1_SDA	P1-33*	IOD	I2C serial data line	Always
I2C1_SDA	P2-25*	IOD	I2C serial data line	Always

Table 49 I2C2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_SCL	P1-116*	IOD	I2C serial clock line	Always
I2C2_SDA	P1-125*	IOD	I2C serial data line	Always

Table 50 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	P2-53*	IOD	I2C serial clock line	Always
I2C3_SDA	P1-20*	IOD	I2C serial data line	Always

Table 51 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	P1-72*	IOD	I2C serial clock line (MUXED)	'C1000'
I2C4_SDA	P1-61*	IOD	I2C serial data line (MUXED)	'C1000'
I2C4_SDA	P2-39*	IOD	I2C serial data line (MUXED)	'C1000'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.17 SPI

CL-SOM-iMX6 features five Enhanced Configurable SPI ports. All CL-SOM-iMX6 SPI ports are derived from the i.MX6 SoC integrated ECSPI IPs. The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable Direct Memory Access (DMA) support

NOTE: Using the SPI1 interface with carrier board precludes access to onboard SPI flash described in chapter 3.3.2.

For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the SPI interface signals

Table 52 SPI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI1_MISO	P1-102*	IO	Master data in; slave data out	Always
ECSPI1_MISO	P1-47*	IO	Master data in; slave data out	not ('WAB' or 'WB')
ECSPI1_MISO	P1-64*	IO	Master data in; slave data out	Always
ECSPI1_MOSI	P1-101*	IO	Master data out; slave data in	Always
ECSPI1_MOSI	P1-45*	IO	Master data out; slave data in	not ('WAB' or 'WB')
ECSPI1_RDY	P1-32*	I	SPI data ready signal	Always
ECSPI1_SCLK	P1-100*	IO	SPI clock signal	Always
ECSPI1_SCLK	P1-48*	IO	SPI clock signal	not ('WAB' or 'WB')
ECSPI1_SS0	P1-104*	IO	Chip select signal	Always
ECSPI1_SS0	P1-49*	IO	Chip select signal	not ('WAB' or 'WB')
ECSPI1_SS0	P1-66*	IO	Chip select signal	Always
ECSPI1_SS1	P1-94*	IO	Chip select signal	Always
ECSPI1_SS1	P2-5*	IO	Chip select signal	Always
ECSPI1_SS2	P1-65*	IO	Chip select signal	Always
ECSPI1_SS2	P2-6*	IO	Chip select signal	Always
ECSPI1_SS3	P1-116*	IO	Chip select signal	Always
ECSPI1_SS3	P1-73*	IO	Chip select signal	Always

Table 53 SPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2_MISO	P1-39*	IO	Master data in; slave data out	not ('WAB' or 'WB')
ECSPI2_MISO	P1-63*	IO	Master data in; slave data out	Always
ECSPI2_MISO	P1-96*	IO	Master data in; slave data out	Always
ECSPI2_MOSI	P1-35*	IO	Master data out; slave data in	Always
ECSPI2_MOSI	P1-69*	IO	Master data out; slave data in	Always
ECSPI2_MOSI	P1-95*	IO	Master data out; slave data in	Always
ECSPI2_SCLK	P1-33*	IO	SPI clock signal	Always
ECSPI2_SCLK	P1-71*	IO	SPI clock signal	Always
ECSPI2_SCLK	P1-99*	IO	SPI clock signal	Always
ECSPI2_SS0	P1-41*	IO	Chip select signal	not ('WAB' or 'WB')
ECSPI2_SS0	P1-97*	IO	Chip select signal	Always
ECSPI2_SS1	P1-94*	IO	Chip select signal	Always
ECSPI2_SS2	P1-65*	IO	Chip select signal	Always
ECSPI2_SS3	P1-73*	IO	Chip select signal	Always

Table 54 SPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3_MISO	P1-77*	IO	Master data in; slave data out	Always
ECSPI3_MOSI	P1-76*	IO	Master data out; slave data in	Always
ECSPI3_RDY	P1-84*	I	SPI data ready signal	Always

Signal Name	Pin #	Type	Description	Availability
ECSPI3_SCLK	P1-75*	IO	SPI clock signal	Always
ECSPI3_SS0	P1-78*	IO	Chip select signal	Always
ECSPI3_SS1	P1-81*	IO	Chip select signal	Always
ECSPI3_SS2	P1-82*	IO	Chip select signal	Always
ECSPI3_SS3	P1-83*	IO	Chip select signal	Always

Table 55 SPI4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI4_MISO	P2-104*	IO	Master data in; slave data out	Always
ECSPI4_MOSI	P2-25*	IO	Master data out; slave data in	Always
ECSPI4_SCLK	P2-27*	IO	SPI clock signal	Always
ECSPI4_SS2	P1-65*	IO	Chip select signal	Always
ECSPI4_SS3	P1-73*	IO	Chip select signal	Always

Table 56 SPI5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI5_MISO	P2-47*	IO	Master data in; slave data out	not 'A'
ECSPI5_MISO	P2-61*	IO	Master data in; slave data out	not ('WAB' or 'WB')
ECSPI5_MOSI	P2-57*	IO	Master data out; slave data in	not 'A'
ECSPI5_MOSI	P2-75*	IO	Master data out; slave data in	not ('WAB' or 'WB')
ECSPI5_RDY	P1-72*	I	SPI data ready signal	Always
ECSPI5_SCLK	P2-59*	IO	SPI clock signal	not 'A'
ECSPI5_SCLK	P2-73*	IO	SPI clock signal	not ('WAB' or 'WB')
ECSPI5_SS0	P2-51*	IO	Chip select signal	not 'A'
ECSPI5_SS0	P2-63*	IO	Chip select signal	not ('WAB' or 'WB')
ECSPI5_SS1	P2-49*	IO	Chip select signal	not 'A'
ECSPI5_SS1	P2-65*	IO	Chip select signal	not ('WAB' or 'WB')
ECSPI5_SS2	P2-69*	IO	Chip select signal	not ('WAB' or 'WB')
ECSPI5_SS3	P2-45*	IO	Chip select signal	not 'A'

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.18 CAN

CL-SOM-iMX6 features two CAN bus interfaces. The CAN bus interfaces are implemented with the i.MX6 on chip "Flexible Controller Area Network" (FlexCAN) communication modules. FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

For additional details, please refer to of the "i.MX6 Reference Manual".

The tables below summarize the CAN bus interface signals

Table 57 CAN bus 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXCAN1_RX	P1-61*	I	FLEXCAN receive pin	Always
FLEXCAN1_RX	P2-6*	I	FLEXCAN receive pin	Always
FLEXCAN1_RX	P2-76*	I	FLEXCAN receive pin	Always
FLEXCAN1_TX	P1-72*	O	FLEXCAN transmit pin	Always
FLEXCAN1_TX	P2-5*	O	FLEXCAN transmit pin	Always
FLEXCAN1_TX	P2-78*	O	FLEXCAN transmit pin	Always

Table 58 CAN bus 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXCAN2_RX	P2-56*	I	FLEXCAN receive pin	Always
FLEXCAN2_RX	P2-87*	I	FLEXCAN receive pin	Always
FLEXCAN2_TX	P2-54*	O	FLEXCAN transmit pin	Always

Signal Name	Pin #	Type	Description	Availability
FLEXCAN2_TX	P2-85*	O	FLEXCAN transmit pin	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.19 General Purpose Timer (GPT)

CL-SOM-iMX6 features a general purpose timer (GPT). The GPT is capable of generating an event on CL-SOM-iMX6 carrier board interface and/or a system interrupt when the timer reaches a programmed value. Additional GPT functionality includes capturing the counter value in a register (this can be triggered by an event on the CL-SOM-iMX6 carrier board interface). The following main features are supported:

- One 32-bit up-counter with clock source selection, including external clock.
- 12-bit prescaler for division of input clock frequency.
- Two “Capture Event” trigger inputs (2 channels) with a programmable trigger edge.
- Three “Compare Event Occurred” outputs (3 channels) with programmable “active” state. A "forced compare" feature is also available.
- Interrupt generation at capture, compare, and rollover events.
- “Restart” or “free-run” operation modes support.

For additional details, please refer to the “i.MX6 Reference Manual”. The table below summarizes the GPT interface signals

Table 59 GPT Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT_CAPTURE1	P2-61*	I	Input pin for a capture event	not ('WAB' or 'WB')
GPT_CAPTURE2	P2-63*	I	Input pin for a capture event	not ('WAB' or 'WB')
GPT_CLK	P2-73*	I	Input pin for an option external clock to use with timer	not ('WAB' or 'WB')
GPT_COMPARE1	P2-75*	O	Output pin that indicates a "compare event" occurrence	not ('WAB' or 'WB')
GPT_COMPARE2	P2-65*	O	Output pin that indicates a "compare event" occurrence	not ('WAB' or 'WB')
GPT_COMPARE3	P2-69*	O	Output pin that indicates a "compare event" occurrence	not ('WAB' or 'WB')

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.20 Enhanced Periodic Interrupt Timer (EPIT)

CL-SOM-iMX6 is equipped with two “Enhanced Periodic Interrupt Timers” (EPIT) derived from the i.MX6 SoC capabilities. EPIT is a 32-bit set-and-forget timer that is capable of providing precise interrupts at regular intervals with minimal processor intervention. EPIT has the following key features:

- 32-bit down counter with clock source selection
- 12-bit prescaler for division of input clock frequency
- Interrupt generation when counter reaches the compare value
- A “Compare Event Occurred” output with programmable “active” state.
- “Set-and-Forget” or “free-running” operation modes support.

For additional details, please refer to the “i.MX6 Reference Manual”. The table below

summarizes the EPIT interface signals

Table 60 EPIT Interface Signals

Signal Name	Pin #	Type	Description	Availability
EPIT1_OUT	P1-124*	O	Output 1 for indicating the occurrence of an output compare event through a specified transition.	not 'U5'
EPIT1_OUT	P1-72*	O	Output 1 for indicating the occurrence of an output compare event through a specified transition.	Always
EPIT2_OUT	P1-61*	O	Output 2 for indicating the occurrence of an output compare event through a specified transition.	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.21 Pulse Width Modulation (PWM)

Four PWM output signals are available at the CL-SOM-iMX6 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Active high or active low configured output

For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the PWM interface signals

Table 61 PWM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	P1-85*	O	PWM1 output signal	Always
PWM1_OUT	P2-69*	O	PWM1 output signal	not ('WAB' or 'WB')
PWM1_OUT	P2-77*	O	PWM1 output signal	Always

Table 62 PWM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM2_OUT	P1-87*	O	PWM2 output signal	Always
PWM2_OUT	P2-65*	O	PWM2 output signal	not ('WAB' or 'WB')
PWM2_OUT	P2-71*	O	PWM2 output signal	Always

Table 63 PWM3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM3_OUT	P2-40*	O	PWM3 output signal	not ('N4', 'N16' or 'N32')
PWM3_OUT	P2-63*	O	PWM3 output signal	not ('WAB' or 'WB')

Table 64 PWM4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM4_OUT	P2-29*	O	PWM4 output signal	not ('N4', 'N16' or 'N32')
PWM4_OUT	P2-75*	O	PWM4 output signal	not ('WAB' or 'WB')

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.22 Watchdog timers (WDOG)

CL-SOM-iMX6 is equipped with two "Watchdog timers" (WDOG) derived from the i.MX6 SoC. The WDOG can be used to protect system from failures by providing a method of escaping from

unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a timeout, the WDOG will assert the internal system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. WDOG supports the following main features:

- A configurable timeout counter with periods from 0.5 seconds up to 128 seconds.
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout

For additional details, please refer to the "i.MX6 Reference Manual". The tables below summarize the Watchdog interface signals

Table 65 Watchdog1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
WDOG1_B	P1-85*	IO	This signal will power down the system	Always
WDOG1_B	P2-65*	IO	This signal will power down the system	not ('WAB' or 'WB')
WDOG1_B	P2-77*	IO	This signal will power down the system	Always
WDOG1_RESET_B_DEB	P2-65*	O	This signal is a reset source for the system	not ('WAB' or 'WB')

Table 66 Watchdog2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
WDOG2_B	P1-87*	IO	This signal will power down the system	Always
WDOG2_B	P2-69*	IO	This signal will power down the system	not ('WAB' or 'WB')
WDOG2_B	P2-71*	IO	This signal will power down the system	Always
WDOG2_RESET_B_DEB	P2-69*	O	This signal is a reset source for the system	not ('WAB' or 'WB')

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.23 Debug Interfaces

The CL-SOM-iMX6 exposes both of the i.MX6 Cortex-A9 core debug interfaces. The core supports debug through real-time trace via ARM CoreSight PTM, ETB and TPIU modules and static debug via JTAG.

4.23.1 JTAG

The CL-SOM-iMX6 JTAG interface is derived from the i.MX6 SoC integrated SJC module. The SJC module implements and manages the daisy-chained topology consisting of its' own TAP and those of the SDMA, and the ARM Debug Access Port (DAP). The SJC supports the following main features:

- IEEE P1149.1, 1149.6 (standard JTAG) interface to off-chip test and development equipment
- Debug-related control and status

For additional details, please refer to the SJC chapter of the "i.MX6 Reference Manual". The table below summarizes the JTAG interface signals

Table 67 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_DE_B	P1-20*	IO	i.MX6 debug request/acknowledge pin	Always
JTAG_MOD	P1-25	I	i.MX6 JTAG controller mode selection signal	Always
JTAG_TCK	P2-90	I	i.MX6 JTAG controller Test Clock (TCK) signal	Always
JTAG_TDI	P2-92	I	i.MX6 JTAG controller Test Data Input (TDI) signal	Always
JTAG_TDO	P2-94	O	i.MX6 JTAG controller Test Data Output (TDO) signal	Always
JTAG_TMS	P2-96	I	i.MX6 JTAG controller Test Mode Select (TMS) signal	Always
JTAG_TRSTB	P2-88	I	i.MX6 JTAG controller Test Reset (TRST) signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.23.2 Cortex-A9 Real Time Trace

The i.MX6 Cortex-A9 trace interface is accessible through the carrier board interface. The Cortex-A9 core platform supports static debug through logic internal to i.MX6. This includes the capability of real time trace via ARM CoreSight PTM, ETB and TPIU modules. The CTI and CTM modules allow cross-triggering of internal and external trigger sources.

For additional details, please refer to the ARM Cortex A9 MPCore Platform (ARM) chapter of the "i.MX6 Reference Manual". The table below summarizes the ARM CoreSight debug/Trace interface signals

Table 68 ARM CoreSight debug/Trace Interface Signals

Signal Name	Pin #	Type	Description	Availability
ARM_EVENTI	P2-53*	I	Input event signal	Always
ARM_EVENTO	P1-57*	O	Output event signal	Always
ARM_TRACE_CLK	P1-59*	O	Clock signal	Always
ARM_TRACE_CTL	P1-51*	O	Control signal	Always
ARM_TRACE00	P1-53*	O	Trace signal	Always
ARM_TRACE01	P1-48*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE02	P1-45*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE03	P1-47*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE04	P1-49*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE05	P1-33*	O	Trace signal	Always
ARM_TRACE06	P1-35*	O	Trace signal	Always
ARM_TRACE07	P1-39*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE08	P1-41*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE09	P2-64*	O	Trace signal	Always
ARM_TRACE10	P2-66*	O	Trace signal	Always
ARM_TRACE11	P2-68*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE12	P2-70*	O	Trace signal	not ('WAB' or 'WB')
ARM_TRACE13	P2-72*	O	Trace signal	Always
ARM_TRACE14	P2-80*	O	Trace signal	Always
ARM_TRACE15	P2-82*	O	Trace signal	not ('WAB' or 'WB')

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.24 General Purpose Clocks

CL-SOM-iMX6 is capable of driving/receiving general purpose clock signals to/from the carrier board through either single ended or differential signals.

The LVDS clock signals are input/output differential pairs compatible with the TIA/EIA-644 standard and capable of driving an up to 600MHz clock to the system. These signals can also be used as single ended clock inputs into the CL-SOM-iMX6. Any of the LVDS signals can be configured as follows:

- As inputs to feed external reference clocks to the i.MX6 on-chip PLLs and/or modules, for example as alternate reference clock for PCIe or/and SATA or video/audio interfaces.
- As outputs to be used as either a reference clock or as a functional clock for peripherals, for example an output of the PCIe master clock (root complex use).

For additional details, please refer to the "i.MX6 Reference Manual". The table below summarizes the General Purpose Clocks interface signals

Table 69 General Purpose Clocks Interface Signals

Signal Name	Pin #	Type	Description	Availability
CCM_CLKO1	P1-124*	O	Observability clock 1 output	not 'U5'
CCM_CLKO1	P1-32*	O	Observability clock 1 output	Always
CCM_CLKO1	P1-51*	O	Observability clock 1 output	Always
CCM_CLKO1	P2-53*	O	Observability clock 1 output	Always
CCM_CLKO2	P2-97*	O	Observability clock 2 output	Always
CLK1_N	P2-99	AIO	Negative side of LVDS clock 1 output. In case CLK1_P is used single ended as input, this signal must be tied to 1.25V.	Always
CLK1_P	P2-101	AIO	Positive side of LVDS clock 1 output. Can also be used as a single ended input	Always
CLK2_N	P1-52	AIO	Negative side of LVDS clock 2 output. In case CLK2_P is used single ended as input, this signal must be tied to 1.25V.	Always
CLK2_P	P1-54	AIO	Positive side of LVDS clock 2 output. Can also be used as a single ended input	Always
XTALOSC_REF_CLK_32K	P1-61*	O	32 KHz reference clock	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.25 External DMA Requests

CL-SOM-iMX6 provides two optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the i.MX6 internal SDMA controller. A logical channel can be configured to respond to an external synchronization request.

For additional details, please refer to the "Smart Direct Memory Access Controller" chapter of the "i.MX6 Reference Manual". The table below summarizes the SDMA interface signals

Table 70 SDMA Interface Signals

Signal Name	Pin #	Type	Description	Availability
SDMA_EXT_EVENT0	P1-95*	I	External DMA request 0	Always
SDMA_EXT_EVENT1	P1-96*	I	External DMA request 1	Always
SDMA_EXT_EVENT1	P2-119*	I	External DMA request 1	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

5 SYSTEM LOGIC

CL-SOM-iMX6 allows access to several system logic related signals through the carrier board interface connectors (P1 and P2). Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Management

5.1.1 Power Rails

The CL-SOM-iMX6 supports two power supply options:

- Regulated DC supply (4V Typical).
- Lithium-ion polymer battery

CL-SOM-iMX6 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board. The table below summarizes the power interface signals

Table 71 Power Interface Signals

Signal Name	Pin #	Type	Description	Availability
GND	P1-134	PI	Main Ground connection	Always
GND	P2-134	PI	Main Ground connection	Always
GND	P1-122	PI	Main Ground connection	Always
GND	P2-122	PI	Main Ground connection	Always
GND	P1-110	PI	Main Ground connection	Always
GND	P2-110	PI	Main Ground connection	Always
GND	P1-98	PI	Main Ground connection	Always
GND	P2-98	PI	Main Ground connection	Always
GND	P1-86	PI	Main Ground connection	Always
GND	P2-86	PI	Main Ground connection	Always
GND	P1-74	PI	Main Ground connection	Always
GND	P2-74	PI	Main Ground connection	Always
GND	P1-62	PI	Main Ground connection	Always
GND	P2-62	PI	Main Ground connection	Always
GND	P2-52	PI	Main Ground connection	Always
GND	P1-50	PI	Main Ground connection	Always
GND	P1-38	PI	Main Ground connection	Always
GND	P2-38	PI	Main Ground connection	Always
GND	P1-26	PI	Main Ground connection	Always
GND	P2-26	PI	Main Ground connection	Always
GND	P1-14	PI	Main Ground connection	Always
GND	P2-14	PI	Main Ground connection	Always
GND	P1-8	PI	Main Ground connection	Always
GND	P2-8	PI	Main Ground connection	Always
GND	P2-7	PI	Main Ground connection	Always
VCC_RTC	P1-37	PI	RTC back-up battery power input. Connect to an always on supply such as a 3V coin-cell lithium battery.	Always
VSYS	P1-139	PI	Main Power connection	Always
VSYS	P2-135	PI	Main Power connection	Always
VSYS	P1-127	PI	Main Power connection	Always
VSYS	P2-127	PI	Main Power connection	Always
VSYS	P1-115	PI	Main Power connection	Always
VSYS	P2-115	PI	Main Power connection	Always
VSYS	P1-103	PI	Main Power connection	Always
VSYS	P2-103	PI	Main Power connection	Always
VSYS	P1-91	PI	Main Power connection	Always
VSYS	P2-91	PI	Main Power connection	Always
VSYS	P1-79	PI	Main Power connection	Always
VSYS	P2-79	PI	Main Power connection	Always
VSYS	P1-67	PI	Main Power connection	Always
VSYS	P2-67	PI	Main Power connection	Always
VSYS	P1-55	PI	Main Power connection	Always
VSYS	P2-55	PI	Main Power connection	Always
VSYS	P1-43	PI	Main Power connection	Always
VSYS	P2-43	PI	Main Power connection	Always

Signal Name	Pin #	Type	Description	Availability
VSYS	P1-31	PI	Main Power connection	Always
VSYS	P2-31	PI	Main Power connection	Always
VSYS	P1-19	PI	Main Power connection	Always
VSYS	P2-19	PI	Main Power connection	Always
VSYS	P1-7	PI	Main Power connection	Always

5.1.2 Low Power Mode

To be added in a future revision of this document.

5.2 Reset

The SRC_POR_B signal is the main system reset input. Driving a logic zero for at least 1mS on the SRC_POR_B signal invokes a global reset that affects every module on CL-SOM-iMX6. For additional details, please refer to the "System Reset Controller" of the "i.MX6 Reference Manual". The table below summarizes the reset interface signals

Table 72 Reset Interface Signals

Signal Name	Pin #	Type	Description	Availability
SRC_POR_B	P2-33	I	i.MX6 SoC cold reset input. A logic low input resets all modules and logic in the SoC	Always

5.3 Boot Sequence

CL-SOM-iMX6 boot sequence defines which interface/media is used by CL-SOM-iMX6 to load and execute the initial software (such as U-boot). CL-SOM-iMX6 can load initial software from the following interfaces/media:

- The on-board primary boot device (SPI Flash with pre-flashed boot-loader).
- An external SD/MMC card using the MMC/SD/SDIO3 interface

CL-SOM-iMX6 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CL-SOM-iMX6:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows CL-SOM-iMX6 to boot from an external SD card, effectively bypassing the onboard SPI Flash.

The table below summarizes boot sequences and devices supported with CL-SOM-iMX6

Table 73 CL-SOM-iMX6 Boot sequences

sequence	ALT_BOOT	First	Second
Standard	Low or floating	Onboard SPI Flash	
Alternate	High	SD card on "MMC/SD/SDIO3" (4-bit mode)	Onboard SPI Flash

NOTE: If during an alternate boot sequence, the CL-SOM-iMX6 cannot load the initial software from the external SD card, CL-SOM-iMX6 will fall back and try to load the initial software from the onboard SPI flash.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system. The table below summarizes the alternative boot selection interface signals

Table 74 Alternative Boot selection Interface Signals

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P2-117	I;PD	Active high alternate boot sequence select input. leave floating or tie low for standard boot sequence	Always

5.4 System and Miscellaneous Signals

5.4.1 External regulator control

CL-SOM-iMX6 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX6 SoC. The logic that controls both signals draws its power from the VCC_RTC power rail, meaning that this power supply must always be present in order to use the external regulator control features.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that CL-SOM-iMX6 is in 'standby' or 'OFF' mode. The SNVS_PMIC_ON_REQ output indicates only 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

For additional details, please refer to the "System Reset Controller" chapter of the "i.MX6 Reference Manual". The table below summarizes the Power Control interface signals

Table 75 Power Control Interface Signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	P2-109	O	Notifies external power management IC to move from functional voltage to standby voltage	Always
SNVS_PMIC_ON_REQ	P2-37	O	Active high power-up request output from i.MX6 SoC. This signal is referenced to RTC supply voltage (3.0V by default)	Always
SRC_ONOFF	P2-35	I	CL-SOM-iMX6 supports the use of a button input signal to request power state changes: A short button press during OFF state, will result in transition to ON state. A short button press during ON state, will interrupt the CPU allowing customized SW response. A long (>5sec) press during ON state will result in transition to OFF state. NOTE: VCC_RTC must be valid in all states for this signal to behave as described.	Always

5.4.2 Flash Write-protection

The on-board SPI NOR flash is the default boot-loader storage as described in chapter 3.3.2. The FLASH_nWP signal can be used to prevent accidental corruption of the SPI Flash stored data.

NOTE: The Flash Write-protection signal below must be used in conjunction with SW to enable write protection. Using the Flash Write-protection signal alone will not enable write protection.

The table below summarizes the Flash Write protection interface signals

Table 76 Flash Write protection Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLASH_NWP	P2-46	PU33	Active low input enabling onboard EEPROM write protection and allowing SPI Flash write-protection.	Always

5.5 Signal Multiplexing Characteristics

Up to 112 of the CL-SOM-iMX6 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX6 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 10 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX6 pins are derived from the i.MX6 SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 77 Multifunctional Signals

Pin #	i.MX6 PAD	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Availability
P1-20	GPIO_16	ESAI_TX3_RX2	ENET_1588_EVENT2_IN	ENET_REF_CLK	SD1_LCTL	SPDIF_IN	GPIO7_IO11	I2C3_SDA	JTAG_DE_B			Always
P1-32	GPIO_19	KEY_COL5	ENET_1588_EVENT0_OUT	SPDIF_OUT	CCM_CLKO1	ECSPI1_RDY	GPIO4_IO05	ENET_TX_ER				Always
P1-33	CSI0_DAT8	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	I2C1_SDA	GPIO5_IO26		ARM_TRACE05			Always
P1-35	CSI0_DAT9	IPU1_CSI0_DATA09	EIM_DATA07	ECSPI2_MOSI	KEY_ROW7	I2C1_SCL	GPIO5_IO27		ARM_TRACE06			Always
P1-39	CSI0_DAT10	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	UART1_TX_DATA		GPIO5_IO28		ARM_TRACE07			not ('WAB' or 'WB')
P1-40	EIM_D27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00		UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23			Always
P1-40	EIM_D27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00	IPU2_CSI1_DATA13	UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23			not 'C1000'
P1-41	CSI0_DAT11	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	UART1_RX_DATA		GPIO5_IO29		ARM_TRACE08			not ('WAB' or 'WB')
P1-42	EIM_D26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01		UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22			Always
P1-42	EIM_D26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01	IPU2_CSI1_DATA14	UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22			not 'C1000'
P1-44	EIM_D31	EIM_DATA31	IPU1_DISP1_DATA20	IPU1_DI0_PIN12	IPU1_CSI0_DATA02	UART3_RTS_B	GPIO3_IO31	USB_H1_PWR				Always
P1-44	EIM_D31	EIM_DATA31	IPU1_DISP1_DATA20	IPU1_DI0_PIN12	IPU1_CSI0_DATA02	UART3_RTS_B	GPIO3_IO31	USB_H1_PWR			EIM_ACLK_FREERUN	'C1000'
P1-45	CSI0_DAT5	IPU1_CSI0_DATA05	EIM_DATA03	ECSPI1_MOSI	KEY_ROW5	AUD3_TXD	GPIO5_IO23		ARM_TRACE02			not ('WAB' or 'WB')
P1-46	EIM_D30	EIM_DATA30	IPU1_DISP1_DATA21	IPU1_DI0_PIN11	IPU1_CSI0_DATA03	UART3_CTS_B	GPIO3_IO30	USB_H1_OC				Always
P1-47	CSI0_DAT6	IPU1_CSI0_DATA06	EIM_DATA04	ECSPI1_MISO	KEY_COL6	AUD3_TXFS	GPIO5_IO24		ARM_TRACE03			not ('WAB' or 'WB')
P1-48	CSI0_DAT4	IPU1_CSI0_DATA04	EIM_DATA02	ECSPI1_SCLK	KEY_COL5	AUD3_TXC	GPIO5_IO22		ARM_TRACE01			not ('WAB' or 'WB')
P1-49	CSI0_DAT7	IPU1_CSI0_DATA07	EIM_DATA05	ECSPI1_SS0	KEY_ROW6	AUD3_RXD	GPIO5_IO25		ARM_TRACE04			not ('WAB' or 'WB')
P1-51	CSI0_MCLK	IPU1_CSI0_HSYNC			CCM_CLKO1		GPIO5_IO19		ARM_TRACE_CTL			Always
P1-53	CSI0_VSYNC	IPU1_CSI0_VSYNC	EIM_DATA01				GPIO5_IO21		ARM_TRACE00			Always
P1-56	GPIO_4	ESAI_TX_HF_CLK		KEY_COL7			GPIO1_IO04	SD2_CD_B				Always
P1-57	CSI0_PIXCLK	IPU1_CSI0_PIXCLK					GPIO5_IO18		ARM_EVENTO			Always
P1-58	GPIO_2	ESAI_TX_FS		KEY_ROW6			GPIO1_IO02	SD2_WP	MLB_DATA			Always
P1-59	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	EIM_DATA00				GPIO5_IO20		ARM_TRACE_CLK			Always
P1-60	DI0_PIN4	IPU1_DI0_PIN04	IPU2_DI0_PIN04	AUD6_RXD	SD1_WP		GPIO4_IO20					Always
P1-61	GPIO_8	ESAI_TX5_RX0	XTALOSC_REF_CLK_32K	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	USB_OTG_PWR_CTL_WAKE			Always
P1-61	GPIO_8	ESAI_TX5_RX0	XTALOSC_REF_CLK_32K	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	USB_OTG_PWR_CTL_WAKE	I2C4_SDA		'C1000'
P1-63	EIM_OE	EIM_OE	IPU1_DI1_PIN07	ECSPI2_MISO			GPIO2_IO25					Always
P1-64	KEY_COL1	ECSPI1_MISO	ENET_MDIO	AUD5_TXFS	KEY_COL1	UART5_TX_DATA	GPIO4_IO08	SD1_VSELECT				Always
P1-65	EIM_D24	EIM_DATA24	ECSPI4_SS2	UART3_TX_DATA	ECSPI1_SS2	ECSPI2_SS2	GPIO3_IO24	AUD5_RXFS	UART1_DTR_B			Always
P1-66	KEY_ROW1	ECSPI1_SS0	ENET_COL	AUD5_RXD	KEY_ROW1	UART5_RX_DATA	GPIO4_IO09	SD2_VSELECT				Always

Pin #	i.MX6 PAD	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Availability
P1-68	SD4_DAT5		SD4_DATA5	UART2_RTS_B			GPIO2_IO13					not ('N4', 'N16' or 'N32')
P1-69	EIM_CS1	EIM_CS1	IPU1_DI1_PIN06	ECSPI2_MOSI			GPIO2_IO24					Always
P1-70	SD4_DAT6		SD4_DATA6	UART2_CTS_B			GPIO2_IO14					not ('N4', 'N16' or 'N32')
P1-71	EIM_CS0	EIM_CS0	IPU1_DI1_PIN05	ECSPI2_SCLK			GPIO2_IO23					Always
P1-72	GPIO_7	ESAI_TX4_RX1	ECSPI5_RDY	EPIT1_OUT	FLEXCAN1_TX	UART2_TX_DATA	GPIO1_IO07	SPDIF_LOCK	USB_OTG_HOST_MODE			Always
P1-72	GPIO_7	ESAI_TX4_RX1	ECSPI5_RDY	EPIT1_OUT	FLEXCAN1_TX	UART2_TX_DATA	GPIO1_IO07	SPDIF_LOCK	USB_OTG_HOST_MODE	I2C4_SCL		'C1000'
P1-73	EIM_D25	EIM_DATA25	ECSPI4_SS3	UART3_RX_DATA	ECSPI1_SS3	ECSPI2_SS3	GPIO3_IO25	AUD5_RXC	UART1_DSR_B			Always
P1-75	DISP0_DAT0	IPU1_DISP0_DATA00	IPU2_DISP0_DATA00	ECSPI3_SCLK			GPIO4_IO21					not 'C1000'
P1-75	DISP0_DAT0	IPU1_DISP0_DATA00		ECSPI3_SCLK			GPIO4_IO21					Always
P1-76	DISP0_DAT1	IPU1_DISP0_DATA01	IPU2_DISP0_DATA01	ECSPI3_MOSI			GPIO4_IO22					not 'C1000'
P1-76	DISP0_DAT1	IPU1_DISP0_DATA01		ECSPI3_MOSI			GPIO4_IO22					Always
P1-77	DISP0_DAT2	IPU1_DISP0_DATA02	IPU2_DISP0_DATA02	ECSPI3_MISO			GPIO4_IO23					not 'C1000'
P1-77	DISP0_DAT2	IPU1_DISP0_DATA02		ECSPI3_MISO			GPIO4_IO23					Always
P1-78	DISP0_DAT3	IPU1_DISP0_DATA03	IPU2_DISP0_DATA03	ECSPI3_SS0			GPIO4_IO24					not 'C1000'
P1-78	DISP0_DAT3	IPU1_DISP0_DATA03		ECSPI3_SS0			GPIO4_IO24					Always
P1-81	DISP0_DAT4	IPU1_DISP0_DATA04	IPU2_DISP0_DATA04	ECSPI3_SS1			GPIO4_IO25					not 'C1000'
P1-81	DISP0_DAT4	IPU1_DISP0_DATA04		ECSPI3_SS1			GPIO4_IO25					Always
P1-82	DISP0_DAT5	IPU1_DISP0_DATA05	IPU2_DISP0_DATA05	ECSPI3_SS2	AUD6_RXFS		GPIO4_IO26					not 'C1000'
P1-82	DISP0_DAT5	IPU1_DISP0_DATA05		ECSPI3_SS2	AUD6_RXFS		GPIO4_IO26					Always
P1-83	DISP0_DAT6	IPU1_DISP0_DATA06	IPU2_DISP0_DATA06	ECSPI3_SS3	AUD6_RXC		GPIO4_IO27					not 'C1000'
P1-83	DISP0_DAT6	IPU1_DISP0_DATA06		ECSPI3_SS3	AUD6_RXC		GPIO4_IO27					Always
P1-84	DISP0_DAT7	IPU1_DISP0_DATA07	IPU2_DISP0_DATA07	ECSPI3_RDY			GPIO4_IO28					not 'C1000'
P1-84	DISP0_DAT7	IPU1_DISP0_DATA07		ECSPI3_RDY			GPIO4_IO28					Always
P1-85	DISP0_DAT8	IPU1_DISP0_DATA08	IPU2_DISP0_DATA08	PWM1_OUT	WDOG1_B		GPIO4_IO29					not 'C1000'
P1-85	DISP0_DAT8	IPU1_DISP0_DATA08		PWM1_OUT	WDOG1_B		GPIO4_IO29					Always
P1-87	DISP0_DAT9	IPU1_DISP0_DATA09	IPU2_DISP0_DATA09	PWM2_OUT	WDOG2_B		GPIO4_IO30					not 'C1000'
P1-87	DISP0_DAT9	IPU1_DISP0_DATA09		PWM2_OUT	WDOG2_B		GPIO4_IO30					Always
P1-88	DISP0_DAT10	IPU1_DISP0_DATA10	IPU2_DISP0_DATA10				GPIO4_IO31					not 'C1000'
P1-88	DISP0_DAT10	IPU1_DISP0_DATA10					GPIO4_IO31					Always
P1-89	DISP0_DAT11	IPU1_DISP0_DATA11	IPU2_DISP0_DATA11				GPIO5_IO05					not 'C1000'
P1-89	DISP0_DAT11	IPU1_DISP0_DATA11					GPIO5_IO05					Always
P1-90	DISP0_DAT12	IPU1_DISP0_DATA12	IPU2_DISP0_DATA12				GPIO5_IO06					not 'C1000'
P1-90	DISP0_DAT12	IPU1_DISP0_DATA12					GPIO5_IO06					Always
P1-92	DISP0_DAT13	IPU1_DISP0_DATA13	IPU2_DISP0_DATA13		AUD5_RXFS		GPIO5_IO07					not 'C1000'
P1-92	DISP0_DAT13	IPU1_DISP0_DATA13			AUD5_RXFS		GPIO5_IO07					Always
P1-93	DISP0_DAT14	IPU1_DISP0_DATA14	IPU2_DISP0_DATA14		AUD5_RXC		GPIO5_IO08					not 'C1000'
P1-93	DISP0_DAT14	IPU1_DISP0_DATA14			AUD5_RXC		GPIO5_IO08					Always
P1-94	DISP0_DAT15	IPU1_DISP0_DATA15	IPU2_DISP0_DATA15	ECSPI1_SS1	ECSPI2_SS1		GPIO5_IO09					not 'C1000'
P1-94	DISP0_DAT15	IPU1_DISP0_DATA15		ECSPI1_SS1	ECSPI2_SS1		GPIO5_IO09					Always
P1-95	DISP0_DAT16	IPU1_DISP0_DATA16	IPU2_DISP0_DATA16	ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10					not 'C1000'
P1-95	DISP0_DAT16	IPU1_DISP0_DATA16		ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10					Always
P1-96	DISP0_DAT17	IPU1_DISP0_DATA17	IPU2_DISP0_DATA17	ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11					not 'C1000'
P1-96	DISP0_DAT17	IPU1_DISP0_DATA17		ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11					Always
P1-97	DISP0_DAT18	IPU1_DISP0_DATA18	IPU2_DISP0_DATA18	ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2			not 'C1000'
P1-97	DISP0_DAT18	IPU1_DISP0_DATA18		ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2			Always
P1-99	DISP0_DAT19	IPU1_DISP0_DATA19	IPU2_DISP0_DATA19	ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3			not 'C1000'
P1-99	DISP0_DAT19	IPU1_DISP0_DATA19		ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3			Always
P1-100	DISP0_DAT20	IPU1_DISP0_DATA20	IPU2_DISP0_DATA20	ECSPI1_SCLK	AUD4_TXC		GPIO5_IO14					not 'C1000'
P1-100	DISP0_DAT20	IPU1_DISP0_DATA20		ECSPI1_SCLK	AUD4_TXC		GPIO5_IO14					Always
P1-101	DISP0_DAT21	IPU1_DISP0_DATA21	IPU2_DISP0_DATA21	ECSPI1_MOSI	AUD4_TXD		GPIO5_IO15					not 'C1000'
P1-101	DISP0_DAT21	IPU1_DISP0_DATA21		ECSPI1_MOSI	AUD4_TXD		GPIO5_IO15					Always
P1-102	DISP0_DAT22	IPU1_DISP0_DATA22	IPU2_DISP0_DATA22	ECSPI1_MISO	AUD4_TXFS		GPIO5_IO16					not 'C1000'
P1-102	DISP0_DAT22	IPU1_DISP0_DATA22		ECSPI1_MISO	AUD4_TXFS		GPIO5_IO16					Always
P1-104	DISP0_DAT23	IPU1_DISP0_DATA23	IPU2_DISP0_DATA23	ECSPI1_SS0	AUD4_RXD		GPIO5_IO17					not 'C1000'
P1-104	DISP0_DAT23	IPU1_DISP0_DATA23		ECSPI1_SS0	AUD4_RXD		GPIO5_IO17					Always
P1-105	DI0_PIN15	IPU1_DI0_PIN15	IPU2_DI0_PIN15	AUD6_TXC			GPIO4_IO17					Always
P1-107	DI0_PIN3	IPU1_DI0_PIN03	IPU2_DI0_PIN03	AUD6_TXFS			GPIO4_IO19					Always
P1-108	DI0_DISP_CLK	IPU1_DI0_DISP_CLK	IPU2_DI0_DISP_CLK				GPIO4_IO16					Always
P1-109	DI0_PIN2	IPU1_DI0_PIN02	IPU2_DI0_PIN02	AUD6_TXD			GPIO4_IO18					Always
P1-112	SD3_DAT6	SD3_DATA6	UART1_RX_DATA				GPIO6_IO18					Always
P1-114	SD3_DAT7	SD3_DATA7	UART1_TX_DATA				GPIO6_IO17					Always
P1-116	KEY_COL3	ECSPI1_SS3	ENET_CRS	HDMI_TX_DDC_SCL	KEY_COL3	I2C2_SCL	GPIO4_IO12	SPDIF_IN				Always
P1-124	GPIO_0	CCM_CLKO1		KEY_COL5	ASRC_EXT_CLK	EPIT1_OUT	GPIO1_IO00	USB_H1_PWR	SNVS_VIO_5			not 'U5'
P1-125	KEY_ROW3	XTALOSC_OSC32K_32K_OUT	ASRC_EXT_CLK	HDMI_TX_DDC_SDA	KEY_ROW3	I2C2_SDA	GPIO4_IO13	SD1_VSELECT				Always
P2-5	KEY_COL2	ECSPI1_SS1	ENET_RX_DATA2	FLEXCAN1_TX	KEY_COL2	ENET_MDC	GPIO4_IO10	USB_H1_PWR_CTL_WAKE				Always
P2-6	KEY_ROW2	ECSPI1_SS2	ENET_TX_DATA2	FLEXCAN1_RX	KEY_ROW2	SD2_VSELECT	GPIO4_IO11	HDMI_TX_CEC_LINE				Always

Pin #	i.MX6 PAD	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Availability
P2-13	SD3_DAT4	SD3_DATA4	UART2_RX_DATA				GPIO7_IO01					Always
P2-20	ENET_RXD1	MLB_SIG	ENET_RX_DATA1	ESAI_TX_FS		ENET_1588_EVENT3_OUT	GPIO1_IO26					Always
P2-25	EIM_D28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI		UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13			Always
P2-25	EIM_D28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI	IPU2_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13			not 'C1000'
P2-27	EIM_D21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17		USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN			Always
P2-27	EIM_D21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN			not 'C1000'
P2-29	SD4_DAT2		SD4_DATA2	PWM4_OUT			GPIO2_IO10					not ('N4', 'N16' or 'N32')
P2-39	ENET_TXD1	MLB_CLK	ENET_TX_DATA1	ESAI_TX2_RX3		ENET_1588_EVENT0_IN	GPIO1_IO29					Always
P2-39	ENET_TXD1	MLB_CLK	ENET_TX_DATA1	ESAI_TX2_RX3		ENET_1588_EVENT0_IN	GPIO1_IO29				I2C4_SDA	'C1000'
P2-40	SD4_DAT1		SD4_DATA1	PWM3_OUT			GPIO2_IO09					not ('N4', 'N16' or 'N32')
P2-41	SD3_DAT5	SD3_DATA5	UART2_TX_DATA				GPIO7_IO00					Always
P2-45	SD2_DAT3	SD2_DATA3	ECSPI5_SS3	KEY_COL6	AUD4_TXC		GPIO1_IO12					not 'A'
P2-47	SD2_DAT0	SD2_DATA0	ECSPI5_MISO		AUD4_RXD	KEY_ROW7	GPIO1_IO15	DCIC2_OUT				not 'A'
P2-49	SD2_DAT2	SD2_DATA2	ECSPI5_SS1	EIM_CS3	AUD4_TXD	KEY_ROW6	GPIO1_IO13					not 'A'
P2-51	SD2_DAT1	SD2_DATA1	ECSPI5_SS0	EIM_CS2	AUD4_TXFS	KEY_COL7	GPIO1_IO14					not 'A'
P2-53	GPIO_5	ESAI_TX2_RX3		KEY_ROW7	CCM_CLKO1		GPIO1_IO05	I2C3_SCL	ARM_EVENTI			Always
P2-54	SD3_DAT0	SD3_DATA0	UART1_CTS_B	FLEXCAN2_TX			GPIO7_IO04					Always
P2-56	SD3_DAT1	SD3_DATA1	UART1_RTS_B	FLEXCAN2_RX			GPIO7_IO05					Always
P2-57	SD2_CMD	SD2_CMD	ECSPI5_MOSI	KEY_ROW5	AUD4_RXC		GPIO1_IO11					not 'A'
P2-58	SD3_DAT2	SD3_DATA2					GPIO7_IO06					Always
P2-59	SD2_CLK	SD2_CLK	ECSPI5_SCLK	KEY_COL5	AUD4_RXFS		GPIO1_IO10					not 'A'
P2-60	SD3_DAT3	SD3_DATA3	UART3_CTS_B				GPIO7_IO07					Always
P2-61	SD1_DAT0	SD1_DATA0	ECSPI5_MISO		GPT_CAPTURE1		GPIO1_IO16					not ('WAB' or 'WB')
P2-63	SD1_DAT1	SD1_DATA1	ECSPI5_SS0	PWM3_OUT	GPT_CAPTURE2		GPIO1_IO17					not ('WAB' or 'WB')
P2-64	CSI0_DAT12	IPU1_CSI0_DATA12	EIM_DATA08		UART4_TX_DATA		GPIO5_IO30		ARM_TRACE09			Always
P2-65	SD1_DAT2	SD1_DATA2	ECSPI5_SS1	GPT_COMPARE2	PWM2_OUT	WDOG1_B	GPIO1_IO19	WDOG1_RESET_B_DEB				not ('WAB' or 'WB')
P2-66	CSI0_DAT13	IPU1_CSI0_DATA13	EIM_DATA09		UART4_RX_DATA		GPIO5_IO31		ARM_TRACE10			Always
P2-68	CSI0_DAT14	IPU1_CSI0_DATA14	EIM_DATA10		UART5_TX_DATA		GPIO6_IO00		ARM_TRACE11			not ('WAB' or 'WB')
P2-69	SD1_DAT3	SD1_DATA3	ECSPI5_SS2	GPT_COMPARE3	PWM1_OUT	WDOG2_B	GPIO1_IO21	WDOG2_RESET_B_DEB				not ('WAB' or 'WB')
P2-70	CSI0_DAT15	IPU1_CSI0_DATA15	EIM_DATA11		UART5_RX_DATA		GPIO6_IO01		ARM_TRACE12			not ('WAB' or 'WB')
P2-71	GPIO_1	ESAI_RX_CLK	WDOG2_B	KEY_ROW5	USB_OTG_ID	PWM2_OUT	GPIO1_IO01	SD1_CD_B				Always
P2-72	CSI0_DAT16	IPU1_CSI0_DATA16	EIM_DATA12		UART4_RTS_B		GPIO6_IO02		ARM_TRACE13			Always
P2-73	SD1_CLK	SD1_CLK	ECSPI5_SCLK	XTALOSC_OSC32K_32K_OUT	GPT_CLK		GPIO1_IO20					not ('WAB' or 'WB')
P2-75	SD1_CMD	SD1_CMD	ECSPI5_MOSI	PWM4_OUT	GPT_COMPARE1		GPIO1_IO18					not ('WAB' or 'WB')
P2-76	SD3_CLK	SD3_CLK	UART2_RTS_B	FLEXCAN1_RX			GPIO7_IO03					Always
P2-77	GPIO_9	ESAI_RX_FS	WDOG1_B	KEY_COL6	CCM_REF_EN_B	PWM1_OUT	GPIO1_IO09	SD1_WP				Always
P2-78	SD3_CMD	SD3_CMD	UART2_CTS_B	FLEXCAN1_TX			GPIO7_IO02					Always
P2-80	CSI0_DAT17	IPU1_CSI0_DATA17	EIM_DATA13		UART4_CTS_B		GPIO6_IO03		ARM_TRACE14			Always
P2-82	CSI0_DAT18	IPU1_CSI0_DATA18	EIM_DATA14		UART5_RTS_B		GPIO6_IO04		ARM_TRACE15			not ('WAB' or 'WB')
P2-84	CSI0_DAT19	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		GPIO6_IO05					not ('WAB' or 'WB')
P2-85	KEY_COL4	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	GPIO4_IO14					Always
P2-87	KEY_ROW4	FLEXCAN2_RX	IPU1_SISG5	USB_OTG_PWR	KEY_ROW4	UART5_CTS_B	GPIO4_IO15					Always
P2-89	ENET_CRS_DV		ENET_RX_EN	ESAI_TX_CLK	SPDIF_EXT_CLK		GPIO1_IO25					Always
P2-97	NANDF_CS2	NAND_CE2_B	IPU1_SISG0	ESAI_TX0	EIM_CRE	CCM_CLKO2	GPIO6_IO15	IPU2_SISG0				not 'C1000'
P2-97	NANDF_CS2	NAND_CE2_B	IPU1_SISG0	ESAI_TX0	EIM_CRE	CCM_CLKO2	GPIO6_IO15					Always
P2-104	EIM_D22	EIM_DATA22	ECSPI4_MISO	IPU1_DI0_PIN01		USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT				Always
P2-104	EIM_D22	EIM_DATA22	ECSPI4_MISO	IPU1_DI0_PIN01	IPU2_CSI1_DATA10	USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT				not 'C1000'
P2-119	GPIO_18	ESAI_TX1	ENET_RX_CLK	SD3_VSELECT	SDMA_EXT_EVENT1	ASRC_EXT_CLK	GPIO7_IO13	SNVS_VIO_5_CTL				Always
P2-121	ENET_RXD0	XTALOSC_OSC32K_32K_OUT	ENET_RX_DATA0	ESAI_TX_HF_CLK	SPDIF_OUT		GPIO1_IO27					Always
P2-128	ENET_RX_ER	USB_OTG_ID	ENET_RX_ER	ESAI_RX_HF_CLK	SPDIF_IN	ENET_1588_EVENT2_OUT	GPIO1_IO24					Always

5.6 RTC

The CL-SOM-iMX6 RTC is implemented with the Ambiq Micro AM1805 RTC circuit. The RTC provides time and calendar information. Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. The backup battery should be connected to the VCC_RTC power input.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

5.7 LED

The CL-SOM-iMX6 features a single general purpose green LED controlled by GPIO2_31 signal of the i.MX6. The LED is ON when GPIO2_31 is logic High.

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX6 CoM/SoM carrier board interface uses the CAMI connector. The SoM pinout is detailed in the table below

6.1 Connector Pinout

Table 78 Connector P1

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-1	ETH_MDI1P	4.7	P1-2	ETH_MDI0P	4.7
P1-3	ETH_MDI1N	4.7	P1-4	ETH_MDI0N	4.7
P1-5	ETH_LINK-LED_10_100	4.7	P1-6	ETH_LED_ACT	4.7
P1-7	VSYS	5.1	P1-8	GND	5.1
P1-9	ETH_MDI3P	4.7	P1-10	ETH_MDI2P	4.7
P1-11	ETH_MDI3N	4.7	P1-12	ETH_MDI2N	4.7
P1-13	ETH_LINK-LED_1000	4.7	P1-14	GND	5.1
P1-15	LVDS0_CLK_N	4.3.1.1	P1-16	LVDS0_TX0_N	4.3.1.1
P1-17	LVDS0_CLK_P	4.3.1.1	P1-18	LVDS0_TX0_P	4.3.1.1
P1-19	VSYS	5.1	P1-20	SPDIF_IN ESAI_TX3_RX2 SD1_LCTL GPIO7_IO11 I2C3_SDA JTAG_DE_B	4.4.2 4.4.2.1 4.11 4.14 4.15 4.23
P1-21	TS_XN	4.12	P1-22	LVDS0_TX1_N	4.3.1.1
P1-23	TS_XP	4.12	P1-24	LVDS0_TX1_P	4.3.1.1
P1-25	JTAG_MOD	4.23	P1-26	GND	5.1
P1-27	TS_YN	4.12	P1-28	LVDS0_TX2_N	4.3.1.1
P1-29	TS_YP	4.12	P1-30	LVDS0_TX2_P	4.3.1.1
P1-31	VSYS	5.1	P1-32	SPDIF_OUT KEY_COL5 GPIO4_IO05 ECSPI1_RDY CCM_CLKO1	4.4.2 4.13 4.14 4.16 4.23.2
P1-33	IPU1_CSI0_DATA18 KEY_COL7 GPIO5_IO26 I2C1_SDA ECSPI2_SCLK ARM_TRACE05	4.3.4 4.13 4.14 4.15 4.16 4.23.1	P1-34	LVDS0_TX3_N	4.3.1.1
P1-35	IPU1_CSI0_DATA19 KEY_ROW7 GPIO5_IO27 I2C1_SCL ECSPI2_MOSI ARM_TRACE06	4.3.4 4.13 4.14 4.15 4.16 4.23.1	P1-36	LVDS0_TX3_P	4.3.1.1
P1-37	VCC_RTC	5.1	P1-38	GND	5.1
P1-39	IPU1_CSI0_DATA04 AUD3_RXC UART1_TX_DATA GPIO5_IO28 ECSPI2_MISO ARM_TRACE07	4.3.4 4.4.2.2 4.9.2 4.14 4.16 4.23.1	P1-40	IPU1_DI1_PIN13 IPU1_DISP1_DATA23 IPU1_SISG3 IPU1_CSI0_DATA00 UART2_RX_DATA GPIO3_IO27	4.3.1 4.3.1 4.3.2 4.3.4 4.9.2 4.14
P1-41	IPU1_CSI0_DATA05 AUD3_RXFS UART1_RX_DATA GPIO5_IO29 ECSPI2_SS0 ARM_TRACE08	4.3.4 4.4.2.2 4.9.2 4.14 4.16 4.23.1	P1-42	IPU1_DISP1_DATA22 IPU1_SISG2 IPU1_CSI0_DATA01 UART2_TX_DATA GPIO3_IO26	4.3.1 4.3.2 4.3.4 4.9.2 4.14
P1-43	VSYS	5.1	P1-44	IPU1_DISP1_DATA20 IPU1_CSI0_DATA02 USB_H1_PWR UART3_RTS_B GPIO3_IO31	4.3.1 4.3.4 4.9.1 4.9.2 4.14

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-45	IPU1_CSI0_DATA15 AUD3_TXD KEY_ROW5 GPIO5_IO23 ECSPI1_MOSI ARM_TRACE02	4.3.4 4.4.2.2 4.13 4.14 4.16 4.23.1	P1-46	IPU1_DISP1_DATA21 IPU1_CSI0_DATA03 USB_H1_OC UART3_CTS_B GPIO3_IO30	4.3.1 4.3.4 4.9.1 4.9.2 4.14
P1-47	IPU1_CSI0_DATA16 AUD3_TXFS KEY_COL6 GPIO5_IO24 ECSPI1_MISO ARM_TRACE03	4.3.4 4.4.2.2 4.13 4.14 4.16 4.23.1	P1-48	IPU1_CSI0_DATA14 AUD3_TXC KEY_COL5 GPIO5_IO22 ECSPI1_SCLK ARM_TRACE01	4.3.4 4.4.2.2 4.13 4.14 4.16 4.23.1
P1-49	IPU1_CSI0_DATA17 AUD3_RXD KEY_ROW6 GPIO5_IO25 ECSPI1_SS0 ARM_TRACE04	4.3.4 4.4.2.2 4.13 4.14 4.16 4.23.1	P1-50	GND	5.1
P1-51	IPU1_CSI0_HSYNC GPIO5_IO19 ARM_TRACE_CTL CCM_CLKO1	4.3.4 4.14 4.23.1 4.23.2	P1-52	CLK2_N	4.23.2
P1-53	IPU1_CSI0_VSYNC GPIO5_IO21 ARM_TRACE00	4.3.4 4.14 4.23.1	P1-54	CLK2_P	4.23.2
P1-55	VSYS	5.1	P1-56	ESAI_TX_HF_CLK SD2_CD_B KEY_COL7 GPIO1_IO04	4.4.2.1 4.11 4.13 4.14
P1-57	IPU1_CSI0_PIXCLK GPIO5_IO18 ARM_EVENTO	4.3.4 4.14 4.23.1	P1-58	ESAI_TX_FS MLB_DATA SD2_WP KEY_ROW6 GPIO1_IO02	4.4.2.1 4.6 4.11 4.13 4.14
P1-59	IPU1_CSI0_DATA_EN GPIO5_IO20 ARM_TRACE_CLK	4.3.4 4.14 4.23.1	P1-60	IPU1_DI0_PIN04 IPU2_DI0_PIN04 AUD6_RXD SD1_WP GPIO4_IO20	4.3.1 4.3.1 4.4.2.2 4.11 4.14
P1-61	SPDIF_SR_CLK ESAI_TX5_RX0 UART2_RX_DATA GPIO1_IO08 I2C4_SDA FLEXCAN1_RX EPIT2_OUT XTALOSC_REF_CLK_32K	4.4.2 4.4.2.1 4.9.2 4.14 4.15 4.17 4.19 4.23.2	P1-62	GND	5.1
P1-63	IPU1_DI1_PIN07 GPIO2_IO25 ECSPI2_MISO	4.3.1 4.14 4.16	P1-64	AUD5_TXFS UART5_TX_DATA KEY_COL1 GPIO4_IO08 ECSPI1_MISO	4.4.2.2 4.9.2 4.13 4.14 4.16
P1-65	AUD5_RXFS UART1_DTR_B UART3_TX_DATA GPIO3_IO24 ECSPI1_SS2 ECSPI2_SS2 ECSPI4_SS2	4.4.2.2 4.9.2 4.9.2 4.14 4.16 4.16 4.16	P1-66	AUD5_RXD UART5_RX_DATA KEY_ROW1 GPIO4_IO09 ECSPI1_SS0	4.4.2.2 4.9.2 4.13 4.14 4.16
P1-67	VSYS	5.1	P1-68	UART2_RTS_B GPIO2_IO13	4.9.2 4.14
P1-69	IPU1_DI1_PIN06 GPIO2_IO24 ECSPI2_MOSI	4.3.1 4.14 4.16	P1-70	UART2_CTS_B GPIO2_IO14	4.9.2 4.14
P1-71	IPU1_DI1_PIN05 GPIO2_IO23 ECSPI2_SCLK	4.3.1 4.14 4.16	P1-72	SPDIF_LOCK ESAI_TX4_RX1 UART2_TX_DATA GPIO1_IO07 I2C4_SCL ECSPI5_RDY FLEXCAN1_TX EPIT1_OUT	4.4.2 4.4.2.1 4.9.2 4.14 4.15 4.16 4.17 4.19

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-73	AUD5_RXC UART1_DSR_B UART3_RX_DATA GPIO3_IO25 ECSPI1_SS3 ECSPI2_SS3 ECSPI4_SS3	4.4.2.2 4.9.2 4.9.2 4.14 4.16 4.16 4.16	P1-74	GND	5.1
P1-75	IPU1_DISP0_DATA00 IPU2_DISP0_DATA00 GPIO4_IO21 ECSPI3_SCLK	4.3.1 4.3.1 4.14 4.16	P1-76	IPU1_DISP0_DATA01 IPU2_DISP0_DATA01 GPIO4_IO22 ECSPI3_MOSI	4.3.1 4.3.1 4.14 4.16
P1-77	IPU1_DISP0_DATA02 IPU2_DISP0_DATA02 GPIO4_IO23 ECSPI3_MISO	4.3.1 4.3.1 4.14 4.16	P1-78	IPU1_DISP0_DATA03 IPU2_DISP0_DATA03 GPIO4_IO24 ECSPI3_SS0	4.3.1 4.3.1 4.14 4.16
P1-79	VSYS	5.1	P1-80	USB_OTG_CHD_B	4.9
P1-81	IPU1_DISP0_DATA04 IPU2_DISP0_DATA04 GPIO4_IO25 ECSPI3_SS1	4.3.1 4.3.1 4.14 4.16	P1-82	IPU1_DISP0_DATA05 IPU2_DISP0_DATA05 AUD6_RXFS GPIO4_IO26 ECSPI3_SS2	4.3.1 4.3.1 4.4.2.2 4.14 4.16
P1-83	IPU1_DISP0_DATA06 IPU2_DISP0_DATA06 AUD6_RXC GPIO4_IO27 ECSPI3_SS3	4.3.1 4.3.1 4.4.2.2 4.14 4.16	P1-84	IPU1_DISP0_DATA07 IPU2_DISP0_DATA07 GPIO4_IO28 ECSPI3_RDY	4.3.1 4.3.1 4.14 4.16
P1-85	IPU1_DISP0_DATA08 IPU2_DISP0_DATA08 GPIO4_IO29 PWM1_OUT WDOG1_B	4.3.1 4.3.1 4.14 4.20 4.21	P1-86	GND	5.1
P1-87	IPU1_DISP0_DATA09 IPU2_DISP0_DATA09 GPIO4_IO30 PWM2_OUT WDOG2_B	4.3.1 4.3.1 4.14 4.20 4.21	P1-88	IPU1_DISP0_DATA10 IPU2_DISP0_DATA10 GPIO4_IO31	4.3.1 4.3.1 4.14
P1-89	IPU1_DISP0_DATA11 IPU2_DISP0_DATA11 GPIO5_IO05	4.3.1 4.3.1 4.14	P1-90	IPU1_DISP0_DATA12 IPU2_DISP0_DATA12 GPIO5_IO06	4.3.1 4.3.1 4.14
P1-91	VSYS	5.1	P1-92	IPU1_DISP0_DATA13 IPU2_DISP0_DATA13 AUD5_RXFS GPIO5_IO07	4.3.1 4.3.1 4.4.2.2 4.14
P1-93	IPU1_DISP0_DATA14 IPU2_DISP0_DATA14 AUD5_RXC GPIO5_IO08	4.3.1 4.3.1 4.4.2.2 4.14	P1-94	IPU1_DISP0_DATA15 IPU2_DISP0_DATA15 GPIO5_IO09 ECSPI1_SS1 ECSPI2_SS1	4.3.1 4.3.1 4.14 4.16 4.16
P1-95	IPU1_DISP0_DATA16 IPU2_DISP0_DATA16 AUD5_TXC GPIO5_IO10 ECSPI2_MOSI SDMA_EXT_EVENT0	4.3.1 4.3.1 4.4.2.2 4.14 4.16 4.24	P1-96	IPU1_DISP0_DATA17 IPU2_DISP0_DATA17 AUD5_TXD GPIO5_IO11 ECSPI2_MISO SDMA_EXT_EVENT1	4.3.1 4.3.1 4.4.2.2 4.14 4.16 4.24
P1-97	IPU1_DISP0_DATA18 IPU2_DISP0_DATA18 AUD4_RXFS AUD5_TXFS GPIO5_IO12 ECSPI2_SS0	4.3.1 4.3.1 4.4.2.2 4.4.2.2 4.14 4.16	P1-98	GND	5.1
P1-99	IPU1_DISP0_DATA19 IPU2_DISP0_DATA19 AUD4_RXC AUD5_RXD GPIO5_IO13 ECSPI2_SCLK	4.3.1 4.3.1 4.4.2.2 4.4.2.2 4.14 4.16	P1-100	IPU1_DISP0_DATA20 IPU2_DISP0_DATA20 AUD4_TXC GPIO5_IO14 ECSPI1_SCLK	4.3.1 4.3.1 4.4.2.2 4.14 4.16
P1-101	IPU1_DISP0_DATA21 IPU2_DISP0_DATA21 AUD4_TXD GPIO5_IO15 ECSPI1_MOSI	4.3.1 4.3.1 4.4.2.2 4.14 4.16	P1-102	IPU1_DISP0_DATA22 IPU2_DISP0_DATA22 AUD4_TXFS GPIO5_IO16 ECSPI1_MISO	4.3.1 4.3.1 4.4.2.2 4.14 4.16

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-103	VSYS	5.1	P1-104	IPU1_DISP0_DATA23 IPU2_DISP0_DATA23 AUD4_RXD GPIO5_IO17 ECSPI1_SS0	4.3.1 4.3.1 4.4.2.2 4.14 4.16
P1-105	IPU1_DI0_PIN15 IPU2_DI0_PIN15 AUD6_TXC GPIO4_IO17	4.3.1 4.3.1 4.4.2.2 4.14	P1-106	USBHUBP1_NOVC	4.9.1
P1-107	IPU1_DI0_PIN03 IPU2_DI0_PIN03 AUD6_TXFS GPIO4_IO19	4.3.1 4.3.1 4.4.2.2 4.14	P1-108	IPU1_DI0_DISP_CLK IPU2_DI0_DISP_CLK GPIO4_IO16	4.3.1 4.3.1 4.14
P1-109	IPU1_DI0_PIN02 IPU2_DI0_PIN02 AUD6_TXD GPIO4_IO18	4.3.1 4.3.1 4.4.2.2 4.14	P1-110	GND	5.1
P1-111	CSI_D3M	4.3.4.1	P1-112	UART1_RX_DATA SD3_DATA6 GPIO6_IO18	4.9.2 4.11 4.14
P1-113	CSI_D3P	4.3.4.1	P1-114	UART1_TX_DATA SD3_DATA7 GPIO6_IO17	4.9.2 4.11 4.14
P1-115	VSYS	5.1	P1-116	SPDIF_IN HDMI_TX_DDC_SCL KEY_COL3 GPIO4_IO12 I2C2_SCL ECSPI1_SS3	4.4.2 4.5.1 4.13 4.14 4.15 4.16
P1-117	RS232_RXD	4.10	P1-118	CSI_D1M	4.3.4.1
P1-119	RS232_TXD	4.10	P1-120	CSI_D1P	4.3.4.1
P1-121	CSI_D2M	4.3.4.1	P1-122	GND	5.1
P1-123	CSI_D2P	4.3.4.1	P1-124	USB_H1_PWR USB1_CPEN KEY_COL5 GPIO1_IO00 EPIT1_OUT CCM_CLKO1	4.9.1 4.9.1 4.13 4.14 4.19 4.23.2
P1-125	HDMI_TX_DDC_SDA KEY_ROW3 GPIO4_IO13 I2C2_SDA	4.5.1 4.13 4.14 4.15	P1-126	USB3_CPEN	4.9.1
P1-127	VSYS	5.1	P1-128	USB2_CPEN	4.9.1
P1-129	USB3_DN	4.9.1	P1-130	USB_H1_DN USB1_DN	4.9.1 4.9.1
P1-131	USB3_DP	4.9.1	P1-132	USB_H1_DP USB1_DP	4.9.1 4.9.1
P1-133	USB4_CPEN	4.9.1	P1-134	GND	5.1
P1-135	USB4_DN	4.9.1	P1-136	USB4_DP	4.9.1
P1-137	USB2_DN	4.9.1	P1-138	USB2_DP	4.9.1
P1-139	VSYS	5.1	P1-140	USB_H1_VBUS	4.9.1

Table 79 Connector P2

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-1	N.C.		P2-2	N.C.	
P2-3	N.C.		P2-4	N.C.	
P2-5	KEY_COL2 GPIO4_IO10 ECSPI1_SS1 FLEXCAN1_TX	4.13 4.14 4.16 4.17	P2-6	HDMI_TX_CEC_LINE KEY_ROW2 GPIO4_IO11 ECSPI1_SS2 FLEXCAN1_RX	4.5.1 4.13 4.14 4.16 4.17
P2-7	GND	5.1	P2-8	GND	5.1
P2-9	LVDS1_CLK_N	4.3.1.1	P2-10	N.C.	
P2-11	LVDS1_CLK_P	4.3.1.1	P2-12	N.C.	
P2-13	UART2_RX_DATA SD3_DATA4 GPIO7_IO01	4.9.2 4.11 4.14	P2-14	GND	5.1
P2-15	LVDS1_TX2_N	4.3.1.1	P2-16	HDMI_CLKM	4.5.1
P2-17	LVDS1_TX2_P	4.3.1.1	P2-18	HDMI_CLKP	4.5.1

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-19	VSYS	5.1	P2-20	ESAI_TX_FS MLB_SIG GPIO1_IO26	4.4.2.1 4.6 4.14
P2-21	LVDS1_TX3_N	4.3.1.1	P2-22	HDMI_D0M	4.5.1
P2-23	LVDS1_TX3_P	4.3.1.1	P2-24	HDMI_D0P	4.5.1
P2-25	IPU1_DI0_PIN13 UART2_CTS_B GPIO3_IO28 I2C1_SDA ECSPI4_MOSI	4.3.1 4.9.2 4.14 4.15 4.16	P2-26	GND	5.1
P2-27	IPU1_DI0_PIN17 SPDIF_IN USB_OTG_OC GPIO3_IO21 I2C1_SCL ECSPI4_SCLK	4.3.1 4.4.2 4.9 4.14 4.15 4.16	P2-28	LVDS1_TX0_N	4.3.1.1
P2-29	GPIO2_IO10 PWM4_OUT	4.14 4.20	P2-30	LVDS1_TX0_P	4.3.1.1
P2-31	VSYS	5.1	P2-32	HDMI_HPD	4.5.1
P2-33	SRC_POR_B	5.1.2	P2-34	LVDS1_TX1_N	4.3.1.1
P2-35	SRC_ONOFF	5.4	P2-36	LVDS1_TX1_P	4.3.1.1
P2-37	SNVS_PMIC_ON_REQ	5.4	P2-38	GND	5.1
P2-39	ESAI_TX2_RX3 MLB_CLK GPIO1_IO29 I2C4_SDA	4.4.2.1 4.6 4.14 4.15	P2-40	GPIO2_IO09 PWM3_OUT	4.14 4.20
P2-41	UART2_TX_DATA SD3_DATA5 GPIO7_IO00	4.9.2 4.11 4.14	P2-42	HDMI_D1M	4.5.1
P2-43	VSYS	5.1	P2-44	HDMI_D1P	4.5.1
P2-45	AUD4_TXC SD2_DATA3 KEY_COL6 GPIO1_IO12 ECSPI5_SS3	4.4.2.2 4.11 4.13 4.14 4.16	P2-46	FLASH_NWP	5.4.1
P2-47	DCIC2_OUT AUD4_RXD SD2_DATA0 KEY_ROW7 GPIO1_IO15 ECSPI5_MISO	4.3.1.4 4.4.2.2 4.11 4.13 4.14 4.16	P2-48	HDMI_D2M	4.5.1
P2-49	AUD4_TXD SD2_DATA2 KEY_ROW6 GPIO1_IO13 ECSPI5_SS1	4.4.2.2 4.11 4.13 4.14 4.16	P2-50	HDMI_D2P	4.5.1
P2-51	AUD4_TXFS SD2_DATA1 KEY_COL7 GPIO1_IO14 ECSPI5_SS0	4.4.2.2 4.11 4.13 4.14 4.16	P2-52	GND	5.1
P2-53	ESAI_TX2_RX3 KEY_ROW7 GPIO1_IO05 I2C3_SCL ARM_EVENTI CCM_CLKO1	4.4.2.1 4.13 4.14 4.15 4.23.1 4.23.2	P2-54	UART1_CTS_B SD3_DATA0 GPIO7_IO04 FLEXCAN2_TX	4.9.2 4.11 4.14 4.17
P2-55	VSYS	5.1	P2-56	UART1_RTS_B SD3_DATA1 GPIO7_IO05 FLEXCAN2_RX	4.9.2 4.11 4.14 4.17
P2-57	AUD4_RXC SD2_CMD KEY_ROW5 GPIO1_IO11 ECSPI5_MOSI	4.4.2.2 4.11 4.13 4.14 4.16	P2-58	SD3_DATA2 GPIO7_IO06	4.11 4.14
P2-59	AUD4_RXFS SD2_CLK KEY_COL5 GPIO1_IO10 ECSPI5_SCLK	4.4.2.2 4.11 4.13 4.14 4.16	P2-60	UART3_CTS_B SD3_DATA3 GPIO7_IO07	4.9.2 4.11 4.14

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-61	SD1_DATA0 GPIO1_IO16 ECSPI5_MISO GPT_CAPTURE1	4.11 4.14 4.16 4.18	P2-62	GND	5.1
P2-63	SD1_DATA1 GPIO1_IO17 ECSPI5_SS0 GPT_CAPTURE2 PWM3_OUT	4.11 4.14 4.16 4.18 4.20	P2-64	IPU1_CSI0_DATA06 UART4_TX_DATA GPIO5_IO30 ARM_TRACE09	4.3.4 4.9.2 4.14 4.23.1
P2-65	SD1_DATA2 GPIO1_IO19 ECSPI5_SS1 GPT_COMPARE2 PWM2_OUT WDOG1_B WDOG1_RESET_B_DEB	4.11 4.14 4.16 4.18 4.20 4.21 4.21	P2-66	IPU1_CSI0_DATA07 UART4_RX_DATA GPIO5_IO31 ARM_TRACE10	4.3.4 4.9.2 4.14 4.23.1
P2-67	VSYS	5.1	P2-68	IPU1_CSI0_DATA08 UART5_TX_DATA GPIO6_IO00 ARM_TRACE11	4.3.4 4.9.2 4.14 4.23.1
P2-69	SD1_DATA3 GPIO1_IO21 ECSPI5_SS2 GPT_COMPARE3 PWM1_OUT WDOG2_B WDOG2_RESET_B_DEB	4.11 4.14 4.16 4.18 4.20 4.21 4.21	P2-70	IPU1_CSI0_DATA09 UART5_RX_DATA GPIO6_IO01 ARM_TRACE12	4.3.4 4.9.2 4.14 4.23.1
P2-71	ESAI_RX_CLK USB_OTG_ID SD1_CD_B KEY_ROW5 GPIO1_IO01 PWM2_OUT WDOG2_B	4.4.2.1 4.9 4.11 4.13 4.14 4.20 4.21	P2-72	IPU1_CSI0_DATA10 UART4_RTS_B GPIO6_IO02 ARM_TRACE13	4.3.4 4.9.2 4.14 4.23.1
P2-73	SD1_CLK GPIO1_IO20 ECSPI5_SCLK GPT_CLK	4.11 4.14 4.16 4.18	P2-74	GND	5.1
P2-75	SD1_CMD GPIO1_IO18 ECSPI5_MOSI GPT_COMPARE1 PWM4_OUT	4.11 4.14 4.16 4.18 4.20	P2-76	UART2_RTS_B SD3_CLK GPIO7_IO03 FLEXCAN1_RX	4.9.2 4.11 4.14 4.17
P2-77	ESAI_RX_FS SD1_WP KEY_COL6 GPIO1_IO09 PWM1_OUT WDOG1_B	4.4.2.1 4.11 4.13 4.14 4.20 4.21	P2-78	UART2_CTS_B SD3_CMD GPIO7_IO02 FLEXCAN1_TX	4.9.2 4.11 4.14 4.17
P2-79	VSYS	5.1	P2-80	IPU1_CSI0_DATA11 UART4_CTS_B GPIO6_IO03 ARM_TRACE14	4.3.4 4.9.2 4.14 4.23.1
P2-81	DSI_CLK0M	4.3.1.2	P2-82	IPU1_CSI0_DATA12 UART5_RTS_B GPIO6_IO04 ARM_TRACE15	4.3.4 4.9.2 4.14 4.23.1
P2-83	DSI_CLK0P	4.3.1.2	P2-84	IPU1_CSI0_DATA13 UART5_CTS_B GPIO6_IO05	4.3.4 4.9.2 4.14
P2-85	IPU1_SISG4 USB_OTG_OC UART5_RTS_B KEY_COL4 GPIO4_IO14 FLEXCAN2_TX	4.3.2 4.9 4.9.2 4.13 4.14 4.17	P2-86	GND	5.1
P2-87	IPU1_SISG5 USB_OTG_PWR UART5_CTS_B KEY_ROW4 GPIO4_IO15 FLEXCAN2_RX	4.3.2 4.9 4.9.2 4.13 4.14 4.17	P2-88	JTAG_TRSTB	4.23

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-89	SPDIF_EXT_CLK ESAI_TX_CLK GPIO1_IO25	4.4.2 4.4.2.1 4.14	P2-90	JTAG_TCK	4.23
P2-91	VSYS	5.1	P2-92	JTAG_TDI	4.23
P2-93	CSI_D0M	4.3.4.1	P2-94	JTAG_TDO	4.23
P2-95	CSI_D0P	4.3.4.1	P2-96	JTAG_TMS	4.23
P2-97	IPU1_SISG0 IPU2_SISG0 ESAI_TX0 GPIO6_IO15 CCM_CLKO2	4.3.2 4.3.2 4.4.2.1 4.14 4.23.2	P2-98	GND	5.1
P2-99	CLK1_N	4.23.2	P2-100	CSI_CLK0M	4.3.4.1
P2-101	CLK1_P	4.23.2	P2-102	CSI_CLK0P	4.3.4.1
P2-103	VSYS	5.1	P2-104	IPU1_DI0_PIN01 SPDIF_OUT USB_OTG_PWR GPIO3_IO22 ECSPI4_MISO	4.3.1 4.4.2 4.9 4.14 4.16
P2-105	DSI_D0M	4.3.1.2	P2-106	PCIE_RXM	4
P2-107	DSI_D0P	4.3.1.2	P2-108	PCIE_RXP	4
P2-109	PMIC_STBY_REQ	5.4	P2-110	GND	5.1
P2-111	DSI_D1M	4.3.1.2	P2-112	PCIE_TXM	4
P2-113	DSI_D1P	4.3.1.2	P2-114	PCIE_TXP	4
P2-115	VSYS	5.1	P2-116	USB_OTG_VBUS	4.9
P2-117	ALT_BOOT	5.2	P2-118	SATA_RXN	4.1
P2-119	ESAI_TX1 GPIO7_IO13 SDMA_EXT_EVENT1	4.4.2.1 4.14 4.24	P2-120	SATA_RXP	4.1
P2-121	SPDIF_OUT ESAI_TX_HF_CLK GPIO1_IO27	4.4.2 4.4.2.1 4.14	P2-122	GND	5.1
P2-123	SSD_NACT	4.1	P2-124	SATA_TXN	4.1
P2-125	MICBIAS	4.4	P2-126	SATA_TXP	4.1
P2-127	VSYS	5.1	P2-128	SPDIF_IN ESAI_RX_HF_CLK USB_OTG_ID GPIO1_IO24	4.4.2 4.4.2.1 4.9 4.14
P2-129	MICIN	4.4	P2-130	USB_OTG_DN	4.9
P2-131	RLINEIN	4.4	P2-132	USB_OTG_DP	4.9
P2-133	LLINEIN	4.4	P2-134	GND	5.1
P2-135	VSYS	5.1	P2-136	USBHUBP4_NOVC	4.9.1
P2-137	RHPOUT	4.4	P2-138	USBHUBP3_NOVC	4.9.1
P2-139	LHPOUT	4.4	P2-140	USBHUBP2_NOVC	4.9.1

6.2 Mating Connectors

Table 80 Connector type

CL-SOM-iMX6 connector			Carrier board (mating) connector P/N	
Ref.	Mfg.	P/N	Mfg.	P/N
P1, P2	AMP	1-5353183-0	AMP	1-5353190-0

Mating connectors and standoffs are available from CompuLab at:
http://compulab.co.il/support/cables-connectors-accessories/

The CompuLab P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 6 CL-SOM-iMX6 Top

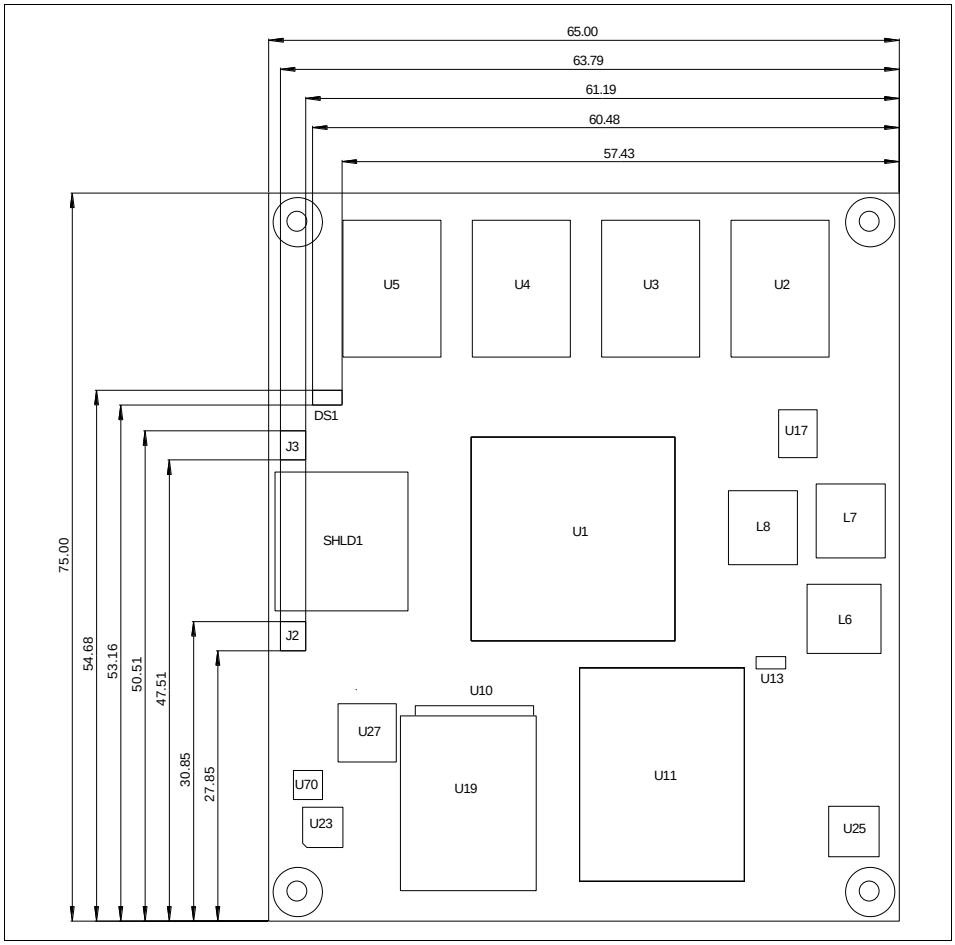
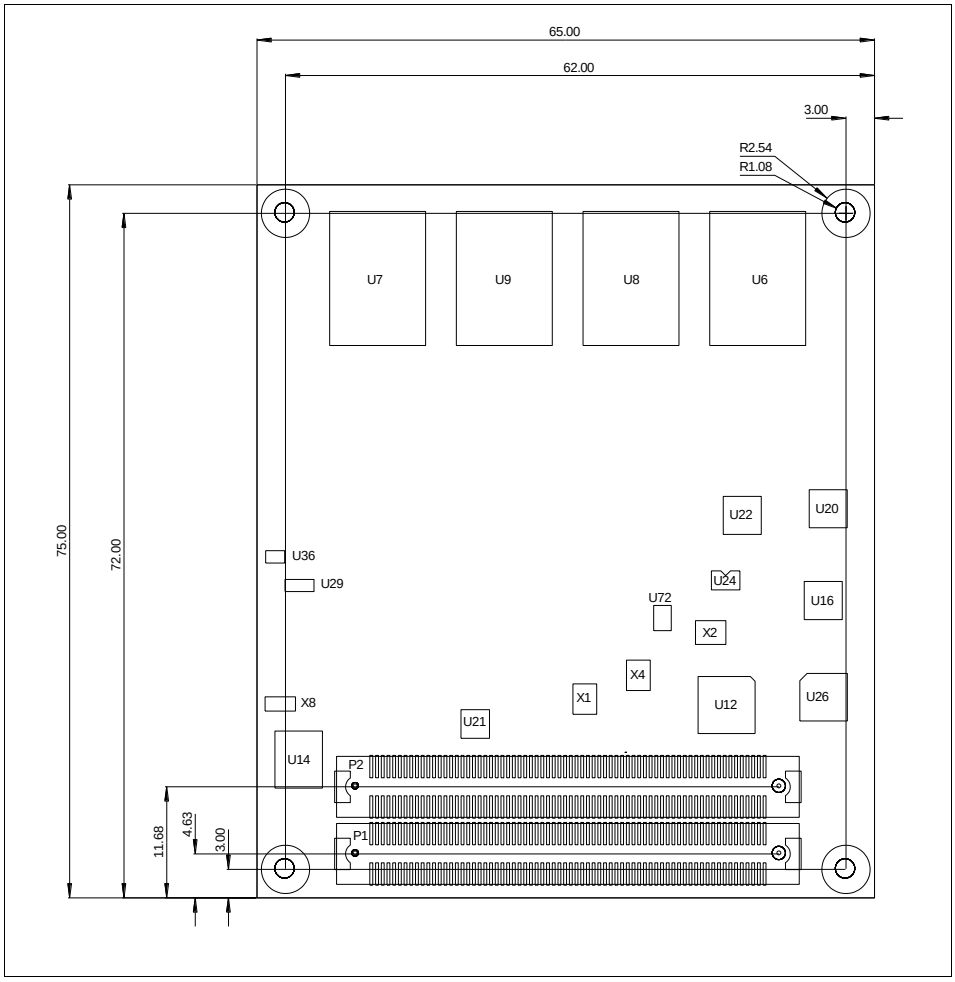


Figure 7 CL-SOM-iMX6 bottom



1. All dimensions are in millimeters.

2. Height of all components is < 3.5mm.

3. Carrier Board connectors provide 4mm board-to-board clearance.

4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format at http://www.compulab.co.il/products/computer-on-modules/cl-som-imx6-nxp-freescale-i-mx-6-system-on-module/#devres

6.4 Heat Spreader and Cooling Solutions

CL-SOM-iMX6 is available with a dedicated heat-spreader assembly. The CL-SOM-iMX6 heat-spreader is intended to act as a thermal interface and should be used in conjunction with a heat-sink or another external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is within the CL-SOM-iMX6 operating temperature limits. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

Documentation and CAD drawings for the CL-SOM-iMX6 heat-are provided at http://www.compulab.co.il/products/computer-on-modules/cl-som-imx6-nxp-freescale-i-mx-6-system-on-module/#devres

NOTE: Heat-Spreader is only available with the 'H' ordering option.

6.5 Standoffs/Spacers

The CL-SOM-iMX6 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 81 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 82 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)		0		5.0	V
Backup battery supply voltage (VCC_RTC)		2.8		3.3	V
USB VBUS		4.4		5.25	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 83 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	With 'WAB' option	3.4		4.45	V
	With 'WB' option	3.4		5.5	V
	Without 'WB'/'WAB' options	3.3		5.5	V
Backup battery supply voltage (VCC_RTC)		2.8	3.0	3.3	V
USB VBUS		4.4		5.25	V

7.3 DC Electrical Characteristics

Table 84 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{IH}		2.31		3.3	V
V_{IL}		0		0.99	V
V_{OH}		3.15			V
V_{OL}				0.15	V
RS232					
TX Voltage Swing		-5.5		5.5	V
RX Voltage Swing		-25		25	V

NOTE: For LVDS, PCIe, HDMI and MIPI electrical characteristics, please refer to the i.MX6 datasheet.

7.4 ESD Performance

Table 85 ESD Performance

Interface	ESD Performance
RS232	15kV using Human Body Model (HBM)
Multifunctional pins	2kV using Human Body Model (HBM) / 0.5kV using Charge Device Model (CDM)
USB Host ports (with U5 option)	4kV using Human Body Model (HBM)

7.5 Operating Temperature Ranges

The CL-SOM-iMX6 is available with three options of operating temperature range.

Table 86 CL-SOM-iMX6 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CL-SOM-iMX6 operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-iMX6.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CL-SOM-iMX6 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CL-SOM-iMX6.
- Refer to the SB-FX6 (rev1v2 or higher) carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX6, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-FX6 (rev1v2 or higher) carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of “Qualified Magnetics” contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 87 Qualified Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-FX6 (rev1v2 or higher) reference design schematics