CM-X300 CoM

Reference Guide Rev 1.31

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CompuLab

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Revision Information

Date	Description
September 01, 2008	Preliminary release
October 29, 2008	CM-X300 rev 1.1 release
November 30, 2008	Added section 3.3.19, PWM Controller.
December 01, 2008	Added section 3.3.8.1, Limitations of Display Controller Capabilities.
December 14, 2008	Added section 3.3.4.2, Implementing Magnetics
March 17, 2009	CM-X300 Revision 1.2 introduced Block Diagram (Figure 1) updated Section 2.2 CM-X300 Features updated Section 3.3.8.1 Limitations of Display Controller Capabilities updated with the PXA300 block diagram Section 3.3.18 Synchronous Serial Port (SSP) updated: SSP3 port added. Antenna disconnection instructions added to the sections 3.3.2 Wireless LAN and 3.3.3 Bluetooth Section 3.3.7 Keypad updated.
June 16, 2009	Note about LB-CS0 usage added CAMI connectors pin functions updated (keypad) Active power consumption data updated in the features table (1.5W max) Standby power consumption data updated in the features table (50mW) Added the chapter 6, Power Consumption, on page 52
October 12, 2009	PWM1 output added.
November 15, 2009	GPIO pins DC characteristics added
November 22, 2009	Formatting errors fixed
December 20, 2009	CIF GPIO info added
February 02, 2010	USB chapter revised
February 16, 2010	Standoff info updated
March 02, 2010	Note about CIF availability added GPIO80..82 usage note added FFUART availability on C624M note added PWM1-OUT/GPIO18 pull-up/down note added
May 26, 2010	USB2 port functionality in C624M configuration updated GPIO availability table updated
Dec 20, 2010	Battery option “B” added to table 4 Updated tables 5, 39 and 40. Updated chapter 3.3.15

Please check for a newer revision of this manual at CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic form version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-X300 Embedded PC Module, which are listed under Related Documents in this section.

Additional chapters are as follows:

2. Overview

3. Functional Description

1.2 CM-X300 Part Number Legend

Please refer to the CompuLab Website's prices section for information about decoding the CM-X300 part number: http://compulab.co.il/x300/html/x300-cm-price.htm.

1.3 Terminology

Table 1 Acronyms

Term	Description
CAMI	CompuLab's Aggregated Module Interface. A standardized module connector interface allowing interchangeability with other CM brand modules.
CoM	Computer-on-Modules are full-featured single board computers designed for mezzanine attachment to custom application through miniature high-density connectors

1.4 Related Documents

For additional information not covered in this manual, refer to the documents listed in Table 2.

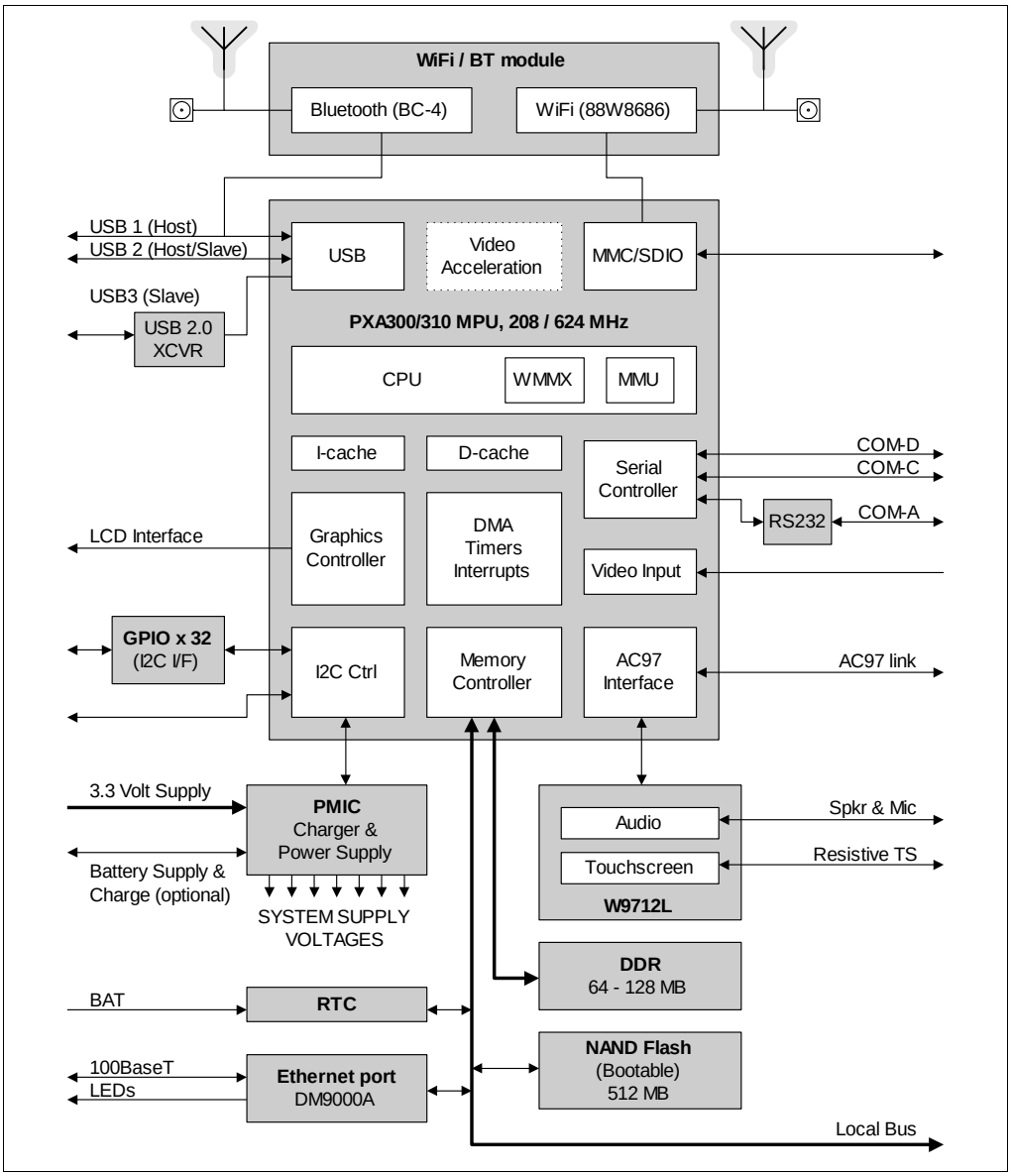
Table 2 Related Documents

Document	Location
X300 Products Developer Resources	http://compulab.co.il/x300/html/x300-developer.py
Universal Serial Bus Specification, Revision 2.0	
On-The-Go Supplement to Universal Serial Bus Specification, Revision 2.0	
Pullup/Pulldown Resistors Engineering Change Notice to the USB 2.0 Specification	
MultiMediaCard System Specification Version 3.3.1	
SD Memory Card Specification Version 1.10	
SDIO Card Specification Version 1.0	

2 OVERVIEW

2.1 Block Diagram

Figure 1 CM-X300 Block Diagram



2.2 CM-X300 Features

The "Option" column specifies the configuration code required to have the particular feature.
"+" means that the feature is always available.

Table 3 CPU, Memory and Busses

Feature	Specifications	Option
CPU	Intel XScale PXA300/310, 208 / 624 MHz, WMMX2, 2*128K internal SRAM 32 KB I-cache and 32 KB D-cache, WB, 128 MB address space DMA and Interrupt controllers, Timers	C
RAM	64 - 128 MB, DDR, 208 MHz, 16-bit	D
NAND Flash Disk	512 Mbytes, bootable.	N
External local bus	16-bit, variable rate up to 52 MHz, 3.3V tolerance	+
AC97 bus	AC97 / AMC97 Rev 2.1 compliant	+

Table 4 Peripherals

Feature	Specifications	Option
Graphics Controller	8/16 bit color, TFT / STN, frame buffer in CPU SRAM or system DDR Resolution: up to 800 x 480 x 16 without restrictions, and up to 1024 x 1024 with some restrictions about overlays, BPP and pixel clock.	+
Hardware accelleration	Supports up to D1 decode and encode performance for codecs including H.264, MPEG-4, H.263, MPEG-2, RealVideo and Microsoft WMV9. Hardware scaling, rotation and other raster graphics operations. * *Implemented by selecting PXA310 CPU option*	C624M
Video Input Port	Direct camera sensor support, max resolution 2560 x 2048, pixel clock up to 52MHz	+
USB	Host/Slave (OTG) port, 12 Mbps, 23-endpoints (in slave mode), OHCI v1.0 Host port (shared with Bluetooth, therefore not available with "W" option) USB 2.0 HS client port	+ ~~W~~ +
Serial Ports (UARTs)	Up to 3 UART ports, 16550 compatible, max 921 kbps COM-A - RS232, Rx / Tx COM-C - TTL, full modem controls COM-D - TTL, partial modem controls	 + + +
Synchronous Serial Port (SSP)	One SSP port, 13mbps, supports SSP, SPI, I^2S protocols.	+
General Purpose I/O	42 dedicated lines (32 I^2C-controlled + 10 memory-mapped) plus additional lines shared with other functions. Can also be used as interrupt inputs.	+
Keyboard & mouse	USB, keypad or redirection from COM port	+
Ethernet	Davicom DM9000A MAC & PHY, 10/100BaseT, Activity LED's	E
Audio codec	Wolfson W9712L, AC97 interface, mono microphone input, stereo line input and 25 mW output for active speakers	AT
Touchscreen ctrl.	A part of the W9712L codec chip. Supports resistive touch panels.	AT
RTC	Real Time Clock, powered by external lithium battery	+

WiFi Interface	Implements 802.11b/g wireless connectivity standard Supports Node to Access Point and Multi-Node (w/o access point) methods of connection. (Cannot act as Access Point) Marvell 88W8686 802.11b/g chipset. On-board ceramic chip antenna and connector for external antenna.	W
Bluetooth	Bluetooth V2.0+EDR system. CSR BlueCore4-ROM chipset, 2.4GHz band, up to 3Mbps. On-board ceramic chip antenna and connector for external antenna. Bluetooth and WiFi interface are always assembled together, and therefore are specified by the same assembling option.	W
Battery support	No battery support – operating voltage is 3.3V + 10% / -3%. Board is assembled with PMIC suitable for the specified operating voltage range. Battery support – operating range is 3.4V to 4.5V. Board is assembled with PMIC dedicated for battery operation.	+ B

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Without “B” option - 3.3V +10% / -3% With “B” option -3.4 to 4.7V (from battery or external regulator)
Active power consumption	0.18 – 1.5 W, depending on configuration and CPU speed
Standby/Sleep consumption	50 mW
Dimensions	66 x 44 x 7 mm
Weight	25 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0º to 70º C Extended: -20º to 70º C Industrial: -40º to 85º C
Storage temperature	-40º to 85º C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 FUNCTIONAL DESCRIPTION

3.1 Board Layout

3.1.1 Top Side Components

Figure 2 shows top side of CM-X300. The relevant top side components are listed in Table 6.

Figure 2 CM-X300 Top View Diagram

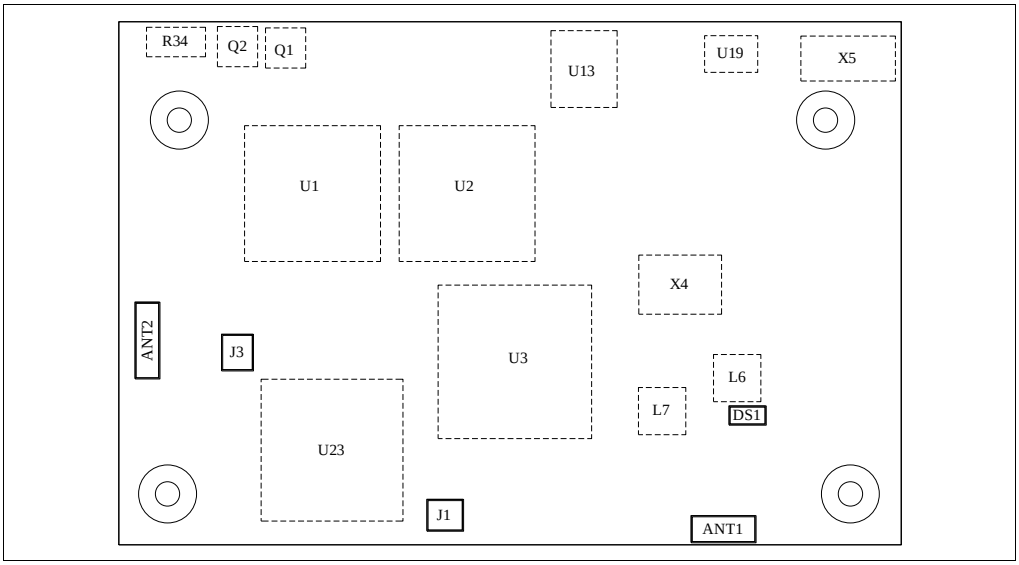


Table 6 Top Side Components

Reference	Function
J1	Bluetooth external antenna connector
J3	Wi-Fi external antenna connector
ANT1	Bluetooth antenna
ANT2	Wi-Fi antenna
DS1	Debug LED

3.1.2 Bottom Side Components

Figure 3 shows bottom side of CM-X300. The bottom side components are listed in Table 7.

Figure 3 CM-X300 Bottom View Diagram

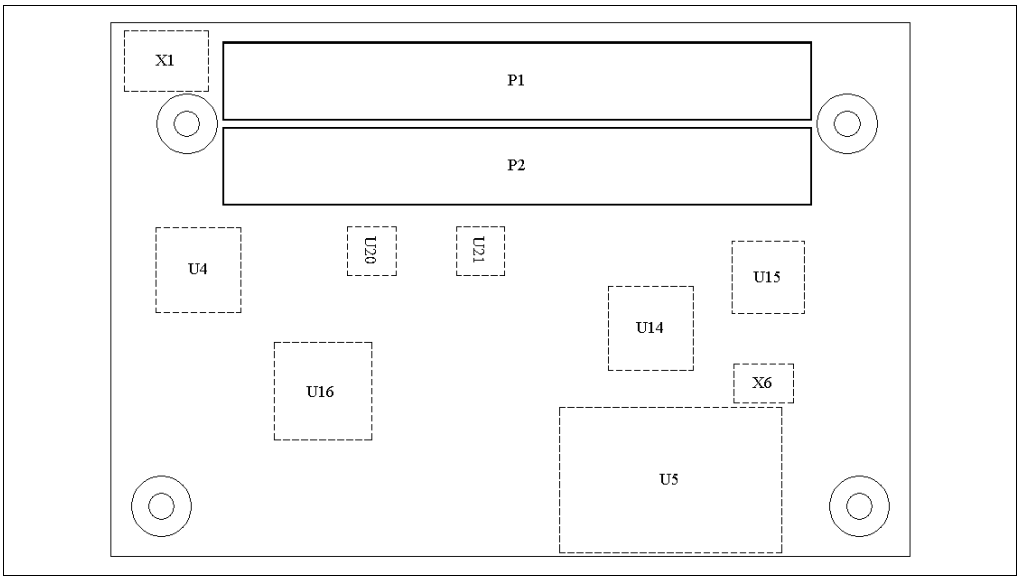


Table 7 Bottom Side Components

Reference	Function
P1	CAMI connector A
P2	CAMI connector B

3.2 Connectors Pinout

3.2.1 Interface Connectors

CAMI signal names, as described in the CAMI Specification as of February 4, 2004, are listed in the tables below. Signal descriptions may be found in the CM-X270 User's Manual. CAMI names are provided for easy comparison with previous modules.

3.2.1.1 Connector A

Table 8 Connector A (P1) pinout

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P1-01	ETH1-TDP	LAN Port, page 22	ETH1-TDP
P1-02	ETH1-RDN	LAN Port, page 22	ETH1-RDN
P1-03	ETH1-TDN	LAN Port, page 22	ETH1-TDN
P1-04	ETH1-RDP	LAN Port, page 22	ETH1-RDP
P1-05	ETH1-SPEED#	LAN Port, page 22	ETH1-LINK100#
P1-06	ETH1-LINK-ACT#	LAN Port, page 22	ETH1-LINK10#
P1-07	VCHRG	Power, page 39	VCORE
P1-08	GND	Power, page 39	GND
P1-09	WP1#	System Signals, page 39	WP1#
P1-10	N.C.	No Connect	ETH1-ACT#
P1-11	RST-IN#	System Signals, page 39	RST-IN#
P1-12	N.C.	No Connect	SPARE
P1-13	KP_MKOUT0 GPIO121	Keypad, page 27 CPU GPIO, page 34	GPIO0
P1-14	GND	Power, page 39	GND
P1-15	KP_MKOUT2 GPIO123	Keypad, page 27 CPU GPIO, page 34	GPIO2

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P1-16	KP_MKOUT1 GPOP122	Keypad, page 27 CPU GPIO, page 34	GPIO1
P1-17	EXTWAKE#	System Signals, page 39	PME#
P1-18	KP_MKOUT3 GPIO124	Keypad, page 27 CPU GPIO, page 34	GPIO3
P1-19	VCHRG	Power, page 39	VCORE
P1-20	VCC-RTC	Power, page 39	VCC-RTC
P1-21	ONKEY#	System Signals, page 39	SUSP-IN
P1-22	COM-A-RX#	Console UART, page 25	COM-A-RX
P1-23	N.C.	No Connect	COM-B-RX
P1-24	COM-A-TX#	Console UART, page 25	COM-A-TX
P1-25	N.C.	No Connect	COM-B-TX
P1-26	GND	Power, page 39	GND
P1-27	COM-D-RX GPIO112	Partial-Function UART, page 26 CPU GPIO, page 34	COM-D-RX
P1-28	COM-C-RX GPIO30	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-RX
P1-29	COM-D-TX GPIO113	Partial-Function UART, page 26 CPU GPIO, page 34	COM-D-TX
P1-30	COM-C-TX GPIO31	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-TX
P1-31	VBAT	Power, page 39	VCC3-3
P1-32	COM-C-DCD# GPIO33	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-DCD#
P1-33	N.C.	No Connect	COM-D-DCD#
P1-34	COM-C-DTR# GPIO36	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-DTR#
P1-35	N.C.	No Connect	COM-D-DTR#
P1-36	COM-C-DSR# GPIO34	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-DSR#
P1-37	N.C.	No Connect	COM-D-DSR#
P1-38	GND	Power, page 39	GND
P1-39	COM-D-CTS# GPIO114	Partial-Function UART, page 26 CPU GPIO, page 34	COM-D-CTS#
P1-40	COM-C-CTS# GPIO32	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-CTS#
P1-41	COM-D-RTS# GPIO111	Partial-Function UART, page 26 CPU GPIO, page 34	COM-D-RTS#
P1-42	COM-C-RTS# GPIO37	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-RTS#
P1-43	VCHRG	Power, page 39	VCORE
P1-44	COM-C-RIN# GPIO35	Full-Function UART, page 25 CPU GPIO, page 34	COM-C-RIN#
P1-45	N.C.	No Connect	COM-D-RIN#
P1-46	DF_CLE_nOE	Local Bus, page 26	IDE-RD#
P1-47	LB-CS0#	Local Bus, page 26	IDE-CS0#
P1-48	DF_ALE_nWE	Local Bus, page 26	IDE-WR#
P1-49	PWM2-OUT GPIO19	PWM Controller, page 41 CPU GPIO, page 34	IDE-IRQ
P1-50	GND	Power, page 39	GND
P1-51	PWM1-OUT GPIO18	PWM Controller, page 41 CPU GPIO, page 34	LB-IRQ0
P1-52	LB-CS1#	Local Bus, page 26	LB/IDE-CS1#
P1-53	TS-XP	Touch Panel Interface, page 38	TS-XP
P1-54	N.C.	No Connect	LB-IRQ1
P1-55	VCHRG	Power, page 39	VCORE
P1-56	BOOTENA#	System Signals, page 39	DEBUG1
P1-57	TS-YP	Touch Panel Interface, page 38	TS-YP
P1-58	N.C.	No Connect	DEBUG0
P1-59	N.C.	No Connect	SSI-DIN

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P1-60	I2C-DATA	I2C Bus, page 40	SSI-DOUT
P1-61	I2C-CLK	I2C Bus, page 40	SSI-CLK
P1-62	GND	Power, page 39	GND
P1-63	DF-A1	Local Bus, page 26	LB-A1
P1-64	DF-A0	Local Bus, page 26	LB-A0
P1-65	DF-A3	Local Bus, page 26	LB-A3
P1-66	DF-A2	Local Bus, page 26	LB-A2
P1-67	VBAT	Power, page 39	VCC3-3
P1-68	N.C.	No Connect	LB-A4
P1-69	GPIO80	CPU GPIO, page 34 (C624 only)	LB-A5
P1-70	DF-CS0#	Local Bus, page 26	LB-A6
P1-71	GPIO81	CPU GPIO, page 34 (C624 only)	LB-A7
P1-72	DF-CS1#	Local Bus, page 26	LB-A8
P1-73	GPIO82	CPU GPIO, page 34 (C624 only)	LB-A9
P1-74	GND	Power, page 39	GND
P1-75	GPIO83	CPU GPIO, page 34	LB-A11
P1-76	LB-RDY	Local Bus, page 26	LB-A10
P1-77	GPIO84	CPU GPIO, page 34	LB-A13
P1-78	LB-BE0#	Local Bus, page 26	LB-A12
P1-79	VCHRG	Power, page 39	VCORE
P1-80	LB-BE1#	Local Bus, page 26	LB-A14
P1-81	GPIO85/ SSPSCLK/ KP_DKIN0	CPU GPIO, page 34 Synchronous Serial Port (SSP), page 40 Keypad, page 27	LB-A15
P1-82	LB-LLA#	Local Bus, page 26	LB-A16
P1-83	GPIO86/ SSPSFRM/ KP_DKIN1	CPU GPIO, page 34 Synchronous Serial Port (SSP), page 40 Keypad, page 27	LB-A17
P1-84	LB-LUA#	Local Bus, page 26	LB-A18
P1-85	GPIO87/ SSPTXD/ KP_DKIN2	CPU GPIO, page 34 Synchronous Serial Port (SSP), page 40 Keypad, page 27	LB-A19
P1-86	GND	Power, page 39	GND
P1-87	GPIO88/ SSPTXD/ KP_DKIN3	CPU GPIO, page 34 Synchronous Serial Port (SSP), page 40 Keypad, page 27	LB-A21
P1-88	DF-RB#	Local Bus, page 26	LB-A20
P1-89	GPIO89	CPU GPIO, page 34	LB-A23
P1-90	DF-RE#	Local Bus, page 26	LB-A22
P1-91	VCHRG	Power, page 39	VCORE
P1-92	DF-WE#	Local Bus, page 26	LB-A24
P1-93	GPIO90	CPU GPIO, page 34	LB-A25
P1-94	DF-IO0	Local Bus, page 26	LB-D0
P1-95	DF-IO1	Local Bus, page 26	LB-D1
P1-96	DF-IO2	Local Bus, page 26	LB-D2
P1-97	DF-IO3	Local Bus, page 26	LB-D3
P1-98	GND	Power, page 39	GND
P1-99	DF-IO5	Local Bus, page 26	LB-D5
P1-100	DF-IO4	Local Bus, page 26	LB-D4
P1-101	DF-IO7	Local Bus, page 26	LB-D7
P1-102	DF-IO6	Local Bus, page 26	LB-D6
P1-103	VBAT	Power, page 39	VCC3-3
P1-104	DF-IO8	Local Bus, page 26	LB-D8
P1-105	DF-IO9	Local Bus, page 26	LB-D9
P1-106	DF-IO10	Local Bus, page 26	LB-D10
P1-107	DF-IO11	Local Bus, page 26	LB-D11
P1-108	DF-IO12	Local Bus, page 26	LB-D12
P1-109	DF-IO13	Local Bus, page 26	LB-D13
P1-110	GND	Power, page 39	GND

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P1-111	DF-IO15	Local Bus, page 26	LB-D15
P1-112	DF-IO14	Local Bus, page 26	LB-D14
P1-113	N.C.	No Connect	LB-IORDY
P1-114	N.C.	No Connect	LB-IOCS16#
P1-115	VCHRG	Power, page 39	VCORE
P1-116	N.C.	No Connect	LB-RD#
P1-117	N.C.	No Connect	PCM-MEMR#
P1-118	N.C.	No Connect	LB-WR#
P1-119	N.C.	No Connect	PCM-IOR#
P1-120	N.C.	No Connect	PCM-MEMW#
P1-121	N.C.	No Connect	PCM-IOW#
P1-122	GND	Power, page 39	GND
P1-123	KP_MKIN4 GPIO119	Keypad, page 27 CPU GPIO, page 34	PCM-WAIT#
P1-124	KP_MKIN3 GPIO118	Keypad, page 27 CPU GPIO, page 34	PCM-CE1#
P1-125	KP_MKOUT5 GPIO4_2	Keypad, page 27 CPU GPIO, page 34	PCM-RST#
P1-126	KP_MKOUT4 GPIO125	Keypad, page 27 CPU GPIO, page 34	PCM-CDA#
P1-127	VCHRG	Power, page 39	VCORE
P1-128	KP_MKIN0 GPIO115	Keypad, page 27 CPU GPIO, page 34	PCM-INTRDYA
P1-129	KP_MKIN6 GPIO2_2	Keypad, page 27 CPU GPIO, page 34	PCM-REG#
P1-130	KP_MKIN5 GPIO120	Keypad, page 27 CPU GPIO, page 34	PCM-WE#
P1-131	N.C.	No Connect	PCM-CE2#
P1-132	KP_MKIN7 GPIO3_2	Keypad, page 27 CPU GPIO, page 34	PCM-SKTSEL
P1-133	LB-CS2#	Local Bus, page 26	LB-CS0#
P1-134	GND	Power, page 39	GND
P1-135	LB-CS3# nXCVREN	Local Bus, page 26	LB-CS1#
P1-136	USBD-P	USB3 Interface, page 32	USB3-P
P1-137	RST-OUT#	System Signals, page 39	RST-OUT#
P1-138	USBD-N	USB3 Interface, page 32	USB3-N
P1-139	VBAT	Power, page 39	VCC3-3
P1-140	N.C.	No Connect	VCC5

3.2.1.2 Connector B

Table 9 Connector B (P2) pinout

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P2-01	N.C.	No Connect	PCI-REQ0#
P2-02	GND	Power, page 39	GND
P2-03	N.C.	No Connect	PCI-GNT0#
P2-04	EXT_TBAT	System Signals, page 39	SPARE
P2-05	N.C.	No Connect	PCI-GNT1#
P2-06	N.C.	No Connect	PCI-INTA#
P2-07	VBAT	Power, page 39	VCC3-3
P2-08	N.C.	No Connect	PCI-INTB#
P2-09	MMC_DAT1	MMC/SD/SDIO Controller, page 33	LPC-LAD1
P2-10	MMC_DAT0	MMC/SD/SDIO Controller, page 33	LPC-LAD0
P2-11	MMC_DAT3	MMC/SD/SDIO Controller, page 33	LPC-LAD3
P2-12	MMC_DAT2	MMC/SD/SDIO Controller, page 33	LPC-LAD2

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P2-13	MMC_CMD1	MMC/SD/SDIO Controller, page 33	LPC-SERIRQ
P2-14	GND	Power, page 39	GND
P2-15	MMC_CMD0	MMC/SD/SDIO Controller, page 33	LPC-LFRAME#
P2-16	MMC_CLK	MMC/SD/SDIO Controller, page 33	PCI-CLK0
P2-17	N.C.	No Connect	LPC-LDRQ#
P2-18	N.C.	No Connect	PCI-REQ1#
P2-19	VCHRG	Power, page 39	VCORE
P2-20	I2C_GPIO0_0	I2C Operated GPIO, page 34	PCI-AD0
P2-21	I2C_GPIO0_2	I2C Operated GPIO, page 34	PCI-AD2
P2-22	I2C_GPIO0_1	I2C Operated GPIO, page 34	PCI-AD1
P2-23	I2C_GPIO0_4	I2C Operated GPIO, page 34	PCI-AD4
P2-24	I2C_GPIO0_3	I2C Operated GPIO, page 34	PCI-AD3
P2-25	I2C_GPIO0_5	I2C Operated GPIO, page 34	PCI-AD5
P2-26	GND	Power, page 39	GND
P2-27	I2C_GPIO0_7	I2C Operated GPIO, page 34	PCI-AD7
P2-28	I2C_GPIO0_6	I2C Operated GPIO, page 34	PCI-AD6
P2-29	I2C_GPIO1_0	I2C Operated GPIO, page 34	PCI-AD8
P2-30	N.C.	No Connect	PCI-CBE0#
P2-31	VCHRG	Power, page 39	VCORE
P2-32	I2C_GPIO1_1	I2C Operated GPIO, page 34	PCI-AD9
P2-33	I2C_GPIO1_3	I2C Operated GPIO, page 34	PCI-AD11
P2-34	I2C_GPIO1_2	I2C Operated GPIO, page 34	PCI-AD10
P2-35	I2C_GPIO1_5	I2C Operated GPIO, page 34	PCI-AD13
P2-36	I2C_GPIO1_4	I2C Operated GPIO, page 34	PCI-AD12
P2-37	I2C_GPIO1_6	I2C Operated GPIO, page 34	PCI-AD14
P2-38	GND	Power, page 39	GND
P2-39	N.C.	No Connect	PCI-CBE1#
P2-40	I2C_GPIO1_7	I2C Operated GPIO, page 34	PCI-AD15
P2-41	N.C.	No Connect	PCI-SERR#
P2-42	N.C.	No Connect	PCI-PAR
P2-43	VBAT	Power, page 39	VCC3-3
P2-44	N.C.	No Connect	PCI-PERR#
P2-45	N.C.	No Connect	PCI-DEVSEL#
P2-46	N.C.	No Connect	PCI-STOP#
P2-47	N.C.	No Connect	PCI-IRDY#
P2-48	N.C.	No Connect	PCI-TRDY#
P2-49	N.C.	No Connect	PCI-FRAME#
P2-50	GND	Power, page 39	GND
P2-51	I2C_GPIO2_0	I2C Operated GPIO, page 34	PCI-AD16
P2-52	N.C.	No Connect	PCI-CBE2#
P2-53	I2C_GPIO2_2	I2C Operated GPIO, page 34	PCI-AD18
P2-54	I2C_GPIO2_1	I2C Operated GPIO, page 34	PCI-AD17
P2-55	VCHRG	Power, page 39	VCORE
P2-56	I2C_GPIO2_3	I2C Operated GPIO, page 34	PCI-AD19
P2-57	I2C_GPIO2_5	I2C Operated GPIO, page 34	PCI-AD21
P2-58	I2C_GPIO2_4	I2C Operated GPIO, page 34	PCI-AD20
P2-59	I2C_GPIO2_7	I2C Operated GPIO, page 34	PCI-AD23
P2-60	I2C_GPIO2_6	I2C Operated GPIO, page 34	PCI-AD22
P2-61	N.C.	No Connect	PCI-CBE3#
P2-62	GND	Power, page 39	GND
P2-63	I2C_GPIO3_1	I2C Operated GPIO, page 34	PCI-AD25
P2-64	I2C_GPIO3_0	I2C Operated GPIO, page 34	PCI-AD24
P2-65	I2C_GPIO3_3	I2C Operated GPIO, page 34	PCI-AD27
P2-66	I2C_GPIO3_2	I2C Operated GPIO, page 34	PCI-AD26
P2-67	VCHRG	Power, page 39	VCORE
P2-68	I2C_GPIO3_4	I2C Operated GPIO, page 34	PCI-AD28
P2-69	I2C_GPIO3_6	I2C Operated GPIO, page 34	PCI-AD30

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P2-70	I2C_GPIO3_5	I2C Operated GPIO, page 34	PCI-AD29
P2-71	TS-XM	Touch Panel Interface, page 38	TS-XM
P2-72	I2C_GPIO3_7	I2C Operated GPIO, page 34	PCI-AD31
P2-73	TS-YM	Touch Panel Interface, page 38	TS-YM
P2-74	GND	Power, page 39	GND
P2-75	CIF_DD2 GPIO41	Camera Interface, page 37 CPU GPIO, page 34	PP-PD2
P2-76	CIF_DD3 GPIO42	Camera Interface, page 37 CPU GPIO, page 34	PP-PD3
P2-77	CIF_DD1 GPIO40	Camera Interface, page 37 CPU GPIO, page 34	PP-PD1
P2-78	CIF_DD4 GPIO43	Camera Interface, page 37 CPU GPIO, page 34	PP-PD4
P2-79	VBAT	Power, page 39	VCC3-3
P2-80	CIF_DD5 GPIO44	Camera Interface, page 37 CPU GPIO, page 34	PP-PD5
P2-81	CIF_DD0 GPIO39	Camera Interface, page 37 CPU GPIO, page 34	PP-PD0
P2-82	CIF_DD6 GPIO45	Camera Interface, page 37 CPU GPIO, page 34	PP-PD6
P2-83	CIF_DD9 GPIO48	Camera Interface, page 37 CPU GPIO, page 34	PP-STROBE#
P2-84	CIF_DD7 GPIO46	Camera Interface, page 37 CPU GPIO, page 34	PP-PD7
P2-85	CIF_DD8 GPIO47	Camera Interface, page 37 CPU GPIO, page 34	PP-ALF#
P2-86	GND	Power, page 39	GND
P2-87	CIF_FV GPIO52	Camera Interface, page 37 CPU GPIO, page 34	PP-ERROR#
P2-88	CIF_MCLK GPIO49	Camera Interface, page 37 CPU GPIO, page 34	PP-ACK#
P2-89	SYS_EN	System Signals, page 39	PP-INIT#
P2-90	CIF_LV GPIO51	Camera Interface, page 37 CPU GPIO, page 34	PP-BUSY
P2-91	VCHRG	Power, page 39	VCORE
P2-92	N.C.	No Connect	PP-PE
P2-93	CIF_PCLK GPIO50	Camera Interface, page 37 CPU GPIO, page 34	PP-SLCTIN#
P2-94	N.C.	No Connect	PP-SLCT
P2-95	LCD-B1	LCD Interface, page 28	LCD-B1
P2-96	LCD-LP	LCD Interface, page 28	LCD-LP
P2-97	LCD-B2	LCD Interface, page 28	LCD-B2
P2-98	GND	Power, page 39	GND
P2-99	LCD-B4	LCD Interface, page 28	LCD-B4
P2-100	LCD-B3	LCD Interface, page 28	LCD-B3
P2-101	LCD-G0	LCD Interface, page 28	LCD-G0
P2-102	LCD-B5	LCD Interface, page 28	LCD-B5
P2-103	VCHRG	Power, page 39	VCORE
P2-104	LCD-G1	LCD Interface, page 28	LCD-G1
P2-105	LCD-G3	LCD Interface, page 28	LCD-G3
P2-106	LCD-G2	LCD Interface, page 28	LCD-G2
P2-107	LCD-G5	LCD Interface, page 28	LCD-G5
P2-108	LCD-G4	LCD Interface, page 28	LCD-G4
P2-109	LCD-R1	LCD Interface, page 28	LCD-R1
P2-110	GND	Power, page 39	GND
P2-111	LCD-FRM	LCD Interface, page 28	LCD-FRM
P2-112	LCD-SCK	LCD Interface, page 28	LCD-SCK
P2-113	LCD-R2	LCD Interface, page 28	LCD-R2

Conn-Pin	CM-X300 Signal Name	Reference	CAMI Signal Name
P2-114	LCD-DE	LCD Interface, page 28	LCD-DE-M
P2-115	VCHRG	Power, page 39	VCORE
P2-116	LCD-R3	LCD Interface, page 28	LCD-R3
P2-117	LCD-R5	LCD Interface, page 28	LCD-R5
P2-118	LCD-R4	LCD Interface, page 28	LCD-R4
P2-119	N.C.	No Connect	PS2-KDAT
P2-120	N.C.	No Connect	PS2-KCLK
P2-121	SSPTXD3	Synchronous Serial Port (SSP), page 40	IRDA-TX
P2-122	GND	Power, page 39	GND
P2-123	SSPRXD3	Synchronous Serial Port (SSP), page 40	IRDA-RX
P2-124	SSPSFRM3	Synchronous Serial Port (SSP), page 40	PS2-MDAT [USB5-P]
P2-125	KP_MKIN2 GPIO117	Keypad, page 27 CPU GPIO, page 34	PCM-CDB#
P2-126	SSPSCLK3	Synchronous Serial Port (SSP), page 40	PS2-MCLK [USB5-N]
P2-127	VCHRG	Power, page 39	VCORE
P2-128	KP_MKIN1 GPIO116	Keypad, page 27 CPU GPIO, page 34	PCM-INTRDYB
P2-129	AUD-SPDIF/ AC97_RST#	Audio Subsystem, page 38	AUD-SPDIF [AC97-RST#]
P2-130	AUD-INR/ AC97_SDOUT	Audio Subsystem, page 38	AUD-INR [AC97-SDOUT]
P2-131	AUD-OUTL/ AC97_SDIN	Audio Subsystem, page 38	AUD-OUTL [AC97-SDIN1]
P2-132	AUD-INL-MIC/ AC97_BITCLK	Audio Subsystem, page 38	AUD-INL-MIC [AC97-BITCLK]
P2-133	USB-OTG-ID	USB2 Interface, page 32	USB-OVC#
P2-134	GND	Power, page 39	GND
P2-135	VBAT	Power, page 39	VCC3-3
P2-136	AUD-OUTR/ AC97_SYNC	Audio Subsystem, page 38	AUD-OUTR [AC97-SYNC]
P2-137	USB-OTG-P	USB2 Interface, page 32	USB2-P
P2-138	USBH-P	USB1 Interface, page 32	USB1-P
P2-139	USB-OTG-N	USB2 Interface, page 32	USB2-N
P2-140	USBH-N	USB1 Interface, page 32	USB1-N

3.3 Application Information

3.3.1 Debug LED (DS1)

Debug LED is controlled by the CPU's GPIO79 pin. The LED will turn ON when GPIO79 is defined as output and its logic state is low.

- To define GPIO79 pad's GPIO function, bits 0..2 of the pad control register (MFPR) at 0x40E104D0 must be set to '0'
- To define GPIO79 as an output, set bit 15 of GPDR2 at 0x40E00014
- To assert GPIO79 high, set bit 15 of GPSR2 at 0x40E00020
- To assert GPIO79 low, set bit 15 of GPCR2 at 0x40E0002C

Note: all register accesses should be read-modify-write only!

3.3.2 Wireless LAN

The CM-X300 features a Marvell 88W8686 802.11b/g wireless LAN solution. The 88W8686 communicates with the CPU via the MMC2 interface in SDIO mode.

3.3.2.1 Wireless LAN Specifications

The CM-X300's wireless LAN's 802.11b RF specifications are listed in Table 10; 802.11g specs in Table 11.

Table 10 802.11b RF System Specifications

Parameter	Test Condition	Typical Value	Units
Transmit Power Output		15	dBm
Receive Sensitivity	1 Mbps, 8% PER	-90	dBm
	2 Mbps, 8% PER	-90	dBm
	5.5 Mbps, 8% PER	-90	dBm
	11 Mbps, 8% PER	-88	dBm
Maximum Receive Level	PER<8%	IEEE Compliant	dBm
Transmit Frequency Offset	Low, Middle, High Channels	±10	PPM
Spectral Mask	Max. TX Power	-40@fc±11MHz	dBc
		-60@fc±22MHz	
Error Vector Magnitude	Max. TX Power @ 11Mbps	-36	dB
Carrier Suppression	Max. TX Power	-25	dBc
Adjacent Channel Rejection	Desired channel is 3dB above sensitivity, 11Mbps, PER<8%	48	dBc

Table 11 802.11g RF System Specifications

Parameter	Test Condition	Typical Value	Units
Transmit Power Output		15	dBm
Receive Sensitivity	6 Mbps, 10% PER	-90	dBm
	9 Mbps, 10% PER	-88	dBm
	12 Mbps, 10% PER	-88	dBm
	18 Mbps, 10% PER	-87	dBm
	24 Mbps, 10% PER	-83	dBm
	36 Mbps, 10% PER	-80	dBm
	48 Mbps, 10% PER	-75	dBm
	54 Mbps, 10% PER	-74	dBm
Maximum Receive Level	PER<10%	IEEE Compliant	dBm
Transmit Frequency Offset	Low, Middle, High Channels	±10	PPM
Spectral Mask	Max. TX Power	-30@fc±11MHz	dBc
		-40@fc±20MHz	
		-50@fc±30MHz	
Error Vector Magnitude	Max. TX Power @ 11Mbps	-29	dB
Carrier Suppression	Max. TX Power	-25	dBc
Adjacent Channel Rejection	Desired channel is 3dB above sensitivity, 11Mbps, PER<8%	15	dBc

3.3.2.2 WLAN Antenna Configuration

The CM-X300 provides two possible WLAN antenna configurations. By default, an onboard WLAN antenna ANT2 is assembled. There is also a U.FL socket, J3, for connecting an external 2.4GHz antenna. See the CM-X300 Top View Diagram on page 13. For the best performance, the onboard antenna should be disconnected if an external antenna is in use. This may be accomplished by disassembling the serial 0R resistor R60.

3.3.3 Bluetooth

The CM-X300 features a CRS BC04-ROM Bluetooth solution. The BC04-ROM communicates with the CPU by means of the CPU's USB Full-Speed Host interface via the USB Host Controller. Therefore, on CM-X300 module configurations with the 'W' option the USB host interface (USB1) is not available on the CAMI.

3.3.3.1 Wireless LAN Specifications

CM-X300's Bluetooth RF specifications are listed in Table 12.

Table 12 Bluetooth RF System Specifications

Parameter	Test Condition	Typical Value	Units
Transmit Power Output		3	dBm
Receive Sensitivity	1 Mbps, 0.1% BER	-84	dBm
	2 Mbps, 0.1% BER	-87	dBm
	3 Mbps, 0.1% BER	-80	dBm
Initial Carrier Frequency Tolerance		5	kHz
Drift Rate		10	kHz
Drift (single slot packet)		10	kHz
Drift (five slot packet)		13	kHz
Carrier Frequency Drift Rate, DH5		13	kHz
Δf1avg Maximum Modulation		165	kHz
Δf2max Minimum Modulation		168	kHz
Δf2 avg /Δf1 avg		1.02	
20dB Bandwidth		654	kHz

3.3.3.2 Bluetooth Antenna Configuration

CM-X300 provides two possible Bluetooth antenna configurations. By default, an onboard WLAN antenna ANT1 is assembled. There is also a U.FL socket J1 for connecting an external 2.4GHz antenna. See the CM-X300 Top View Diagram on page 13. For the best performance, the onboard antenna should be disconnected if an external antenna is in use. This may be accomplished by disassembling the serial 0R resistor R61.

3.3.4 LAN Port

The LAN port (configuration option 'E') is implemented with a Davicom DM9000A ethernet controller. This is an ETH1 port on the CAMI. LAN port signals are listed in Table 13.

Table 13 LAN port signals

CM-X300 Signal Name	Type	Description
{ETH1-TDP, ETH1-TDN}	A	Transmit Differential Pair. The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with the isolation transformer.
{ETH1-RDP, ETH1-RDN}	A	Receive Differential Pair. The receive differential pair receives the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with an isolation transformer.
ETH1-LINK-ACT#	O	In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY. In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only.
ETH1-SPEED#	O	Its low output indicates that the internal PHY is operated in 100M/S, or it is floating for the 10M mode of the internal PHY.

3.3.4.1 Accessing DM9000A

The drivers for the Ethernet controller are provided in all SW support packages. The following description is for system-level programmers only.

There are two addressing ports for accessing DM9000A through the host interface. One port is the INDEX port and the other is the DATA port. In the CM-X300 the INDEX port is at the address 0x08000010 and the DATA port is at the address 0x08000014. The contents of the INDEX port are the register address of the DATA port. Before accessing any register, the address of the register must be saved in the INDEX port.

3.3.4.2 Implementing Magnetics

Refer to Table 14 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 14 are electrical equivalents, but may be not pin-to-pin compatible.

Table 14 Recommended Magnetic Modules

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012, H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05, PH163112 , YCL 0303, PH163539 *(Auto MDIX)
MAGCOM	HS9001 , HS9016
Halo	TG22-3506ND, TD22-3506G1, TG22-S010ND, TG22-S012ND, TG110-S050N2
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37, NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01, S558-5999-W2
Valor	ST6114, ST6118
Macronics	HS2123, HS2213
Bothhand	TS6121C,16ST8515,16ST1086

Figure 4 below shows an implementation example for use of a magnetic embedded in the RJ-45 socket with integrated LEDs. Both center taps of the magnetic should be connected to a 2.5V DC supply. Small LDO may be used for this purpose. Refer to Figure 5 for a voltage source implementation example. Decouple 2.5V voltage with at least one large and one small capacitors (10uF and 0.1uF respectively).

Figure 4 Magnetic Interconnect Schematic

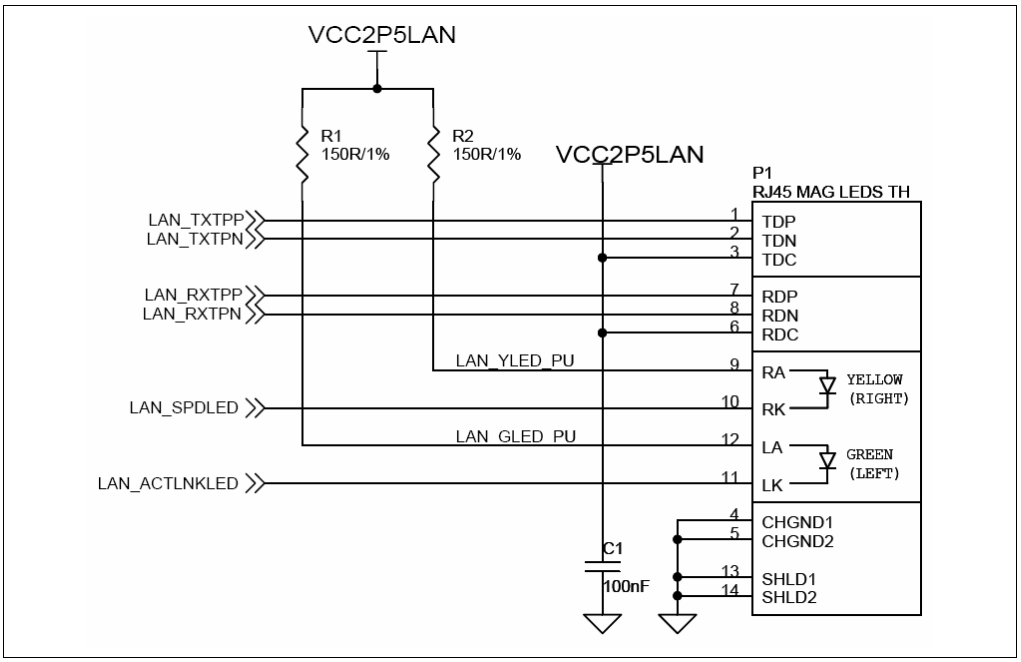
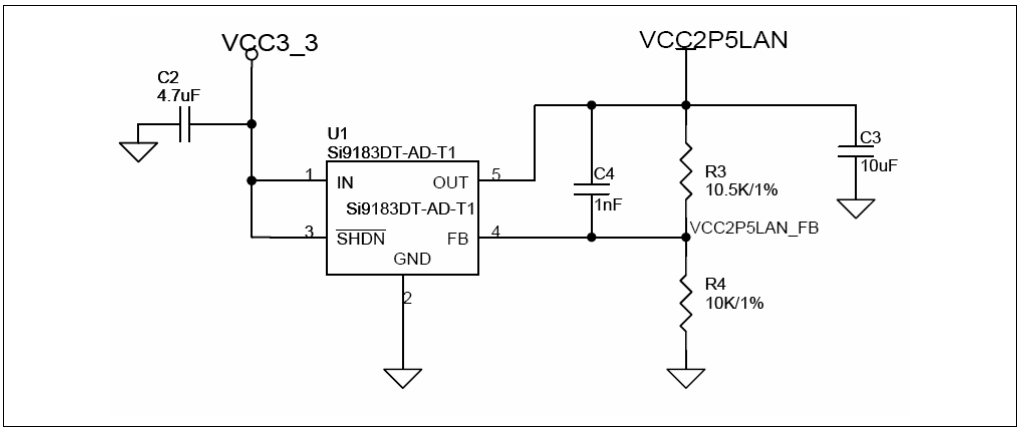


Figure 5 DC Source for Magnetic Center Taps



3.3.5 Serial Ports

CM-X300 incorporates 3 UARTs: one full function UART, one RX-TX only (console) UART and one partial-function UART. All three UARTs share the same feature list, baud rates and use the same programming model.

The UARTs share the following features:

- Functionally compatible with 16550A and 16750
- Ability to add or delete standard asynchronous communications bits (start, stop, and parity) in the serial data
- Independently controlled transmit, receive, line status, and data-set interrupts
- Modem control functions (nCTS and nRTS on two of the three UARTs. The full-function UART additionally has nDSR, nDTR, nRI, and nDCD signals)
- Auto-flow capability controls data I/O without generating interrupts:
  - nRTS (output) controlled by UART Receive FIFO
  - nCTS (input) from modem controls UART transmitter
- Programmable serial interface:

- 7- or 8-bit characters
- Even, odd, or no parity detection
- 1 stop-bit generation
- Baud-rate generation of 9.6K to 3.6M bps for all UARTs
- False start-bit detection

- 64-byte Transmit FIFO
- 64-byte Receive FIFO
- Complete status-reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include:
  - Loopback controls for communications link fault isolation
  - Break, parity, and framing-error simulation
- Fully prioritized interrupt system controls
- Separate DMA requests for transmit and receive data services
- Serial infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) specification

3.3.5.1 Full-Function UART

This is the CPU's UART1. The interface is routed to the CAMI COM-C serial port and uses TTL-levels signaling. The port's pin descriptions are listed in Table 15.

Note: In module configuration C624M (PXA310 processor) these pins are re-defined for use with the USB interface and not available on CAMI.

Table 15 Full-Function UART Signals

CM-X300 Signal Name	Type	Description
COM-C-RX	I	Serial Data In: receives the serial data from the external serial device or DCE into the internal serial port controller.
COM-C-TX	O	Serial Data Out: transmits the serial data from the internal serial port controller to the external serial device or DCE.
COM-C-CTS#	I	Clear To Send: is sent back to the serial port to indicate that the external data carrier equipment (DCE) is ready to accept data.
COM-C-RTS#	O	Request To Send: indicates to the external DCE that the internal serial port controller is ready to send data.
COM-C-DSR#	I	Data Set Ready: indicates that the external DCE is ready to establish a communication link with the serial port controller.
COM-C-DTR#	O	Data Terminal Ready: indicates to the external DCE that the serial port controller is ready to communicate.
COM-C-DCD#	I	Data Carrier Detect: is sent back to the serial port from data carrier equipment when it detects a carrier signal from a communications target.
COM-C-RIN#	I	Ring Indicate: is used by an external modem to inform the serial port that a ring signal has been detected. A change in state on this signal by the external modem can be configured to cause a modem status interrupt.

3.3.5.2 Console UART

This is the CPU's UART3. The interface is routed to the CAMI COM-A serial port and uses RS-232-levels signaling. The port's pin descriptions are listed in Table 16.

Table 16 Console UART Signals

CM-X300 Signal Name	Type	Description
COM-A-RX#	I	Serial Data In: receives the serial data from the external serial device or DCE into the internal serial port controller.

COM-A-TX#	O	Serial Data Out: transmits the serial data from the internal serial port controller to the external serial device or DCE.

3.3.5.3 Partial-Function UART

This is the CPU's UART2. The interface is routed to the CAMI COM-D serial port and uses TTL-levels signaling. The port's pin descriptions are listed in Table 17.

Table 17 Partial-Function UART Signals

CM-X300 Signal Name	Type	Description
COM-D-RX	I	Serial Data In: receives the serial data from the external serial device or DCE into the internal serial port controller.
COM-D-TX	O	Serial Data Out: transmits the serial data from the internal serial port controller to the external serial device or DCE.
COM-D-CTS#	I	Clear To Send: is sent back to the serial port to indicate that the external data carrier equipment (DCE) is ready to accept data.
COM-D-RTS#	O	Request To Send: indicates to the external DCE that the internal serial port controller is ready to send data.

3.3.6 Local Bus

The CM-X300's local bus is the unbuffered CPU's Data Flash Interface (DFI). The DFI is shared between the NAND Flash Controller (NFC) and Static Memory Controller (SMC).

The NAND Flash Controller (NFC) supports large- and small-block, 8-bit and 16-bit NAND flash devices.

The Static Memory Controller (SMC) maintains multiple static-memory types, such as synchronous and asynchronous flash devices, SRAM and SRAM-like variable-latency IO devices (VLIO).

3.3.6.1 Local Bus Signal Description

The Static Memory Controller (SMC) signals are listed in Table 18. The NAND Flash Controller (NFC) signals are listed in Table 19.

Note that some signals are shared between the two controllers.

Table 18 Local Bus Signals (SMC)

CM-X300 Signal Name	Type	Description
DF-IO[15:0]	I/O	Bidirectional data/address bus
DF_CLE_nOE	O	Output enable
DF_ALE_nWE	O	Write enable
LB-CS[3:0]# nXCVREN	O	Chip selects. LB-CS3 may be configured as nXCVREN (External transceiver enable) signal. It is asserted along with the Output Enable (DF_CLE_nOE) during read accesses and one DF_SLCK cycle before the Write Enable (DF_ALE_nWE) during write accesses. 0 = Enable transceiver 1 = Disable transceiver
LB-LUA#	O	Latch upper address. Used to latch the high-order address bits during the upper address cycle.
LB-LLA#	O	Latch lower address. Used to latch the low-order address bits during the lower address cycle.
DF-A[3:0]	O	Low-order address bits. Used as the lowest four address bits during an asynchronous burst transfer of the values in the lower address cycle on the DF-IO[15:0]

LB-BE[1:0]#	O	Data byte enable. nBE0 corresponds to DF-IO[7:0] nBE1 corresponds to DF-IO[15:8] 0 = Do not mask out corresponding byte 1 = Mask out corresponding byte
LB-RDY	I	Variable-Latency I/O Ready signal for inserting wait states. 0 = Wait 1 = VLIO is ready

Table 19 Local Bus Signals (NFC)

CM-X300 Signal Name	Type	Description
DF-IO[15:0]	I/O	Bidirectional data/address bus
DF-CS[1:0]#	O	Chip selects
DF_CLE_nOE	O	Command latch enable
DF_ALE_nWE	O	Address latch enable
DF-RE#	O	Read enable
DF-WE#	O	Write enable
DF-RB#	I	Ready/Busy_n (Low when Busy)

3.3.6.2 Static Memory Controller Address Map

The SMC has four separate partitions that are shown in Table 20.

Note: LB-CS0 is used internally as a chip select for the onboard Ethernet controller and cannot be used externally on modules with “E” option.

Table 20 SMC Address Map

Chip Select	Address Range
LB-CS0	0x0000_0000–0x0FFF_FFFF (256 Mbyte)
LB-CS1	0x3000_0000–0x3FFF_FFFF (256 Mbyte)
LB-CS2	0x1000_0000–0x13FF_FFFF (64 Mbyte)
LB-CS3	0x1400_0000–0x17FF_FFFF (64 Mbyte)

3.3.6.3 Local Bus Operation

For information about local bus AC characteristics refer to the Marvell PXA3xx (88AP3xx) Processor Family EMPI document, section 7.2.

For information related to operation of the Data Flash Interface representing the local bus in the CM-X300, refer to the Marvell® PXA3xx (88AP3xx) Processor Family Developers Manual Vol. II: Memory Controller Configuration Developers Manual, sections 2 and 3.

3.3.7 Keypad

The CM-X300’s keypad controller manages up to 8x6 matrix keys, up to eight direct keys, and up to two rotary encoders, which can implement scroll keys, jog-dials, and thumbwheels. The keypad controller provides an interface to two styles of keypads simultaneously through the matrix and direct keypad interface. The controller manages both manual and automatic scans.

Stable keypad activity that lasts longer than the debounce interval generates an interrupt. A manual matrix scan can then be conducted to assert the scan lines sequentially. The row readings for each column are read as they are scanned. If the “ignore-multiple-keypress” policy is chosen, only one interrupt is generated for a debounced keypress. For example, if three keys are pressed and held, only one interrupt is generated after the first key is pressed and held. The column-scan signals are automatically asserted in sequence by the automatic scan logic in the keypad controller, and the row readings are stored in the automatic scan registers. Automatic scans can be initiated by either of the following methods:

- If there is stable keypad activity for a period greater than the specified key debounce interval while the automatic-scan-on-activity is enabled, completion of the scan generates an interrupt.
- If the automatic-scan is enabled, user software determines when to initiate an automatic scan. This option does not generate an interrupt.

Table 21 Keypad Signals

CM-X300 Signal Name	Type	Description
KP_MKOUT[5:0]	O	Matrix Key Column-Scan Outputs The keypad controller sends column-scan output signals to the columns of the matrix keypad to detect any key(s) that are pressed. If an automatic scan is occurring, these column-scan output signals are driven by the automatic scan logic. At other times, they are driven by the settings of bits MS5 through MS0 in the CPU's Keypad Interface Control (KPC) register.
KP_MKIN[7:0]	I	Matrix Key Inputs (Returns) The input signals from the matrix keypad (matrix-keypad row readings).
KP_DKIN[3:0] (shared with GPIO88…85)	I	Direct Key Inputs Signals from the direct keys and the rotary-encoder sensor. KP_DKIN<1:0> are either input signals for direct keys 1 and 0 or input sensor signals for rotary encoder A (if enabled). KP_DKIN<3:2> are either input signals for direct keys 3 and 2 or input-sensor signals for rotary encoder B (if enabled).

Note: direct keys and rotary encoder inputs are shared with the Matrix Key Column-Scan Outputs and other signals and may be made available through software.

3.3.8 LCD Interface

Features of the LCD controller are as follows:

- Display modes
  - Single display modules
  - Passive panels: 24-bit-per-pixel color displays (no monochrome support)
  - Active panels: 8-, or 16 bit-per-pixel single-scan color displays without an internal frame buffer
  - Smart panels: Up to 24-bit-per-pixel single-scan color displays with an internal frame buffer
- Display sizes (both portrait and landscape formats):
  - 176 x 208
  - 176 x 220
  - 240 x 240
  - 320 x 240 (QVGA)
  - 320 x 320
  - 640 x 480 (VGA)
  - 800 x 480

  The following display sizes are supported, but may have restrictions with overlays enabled, BPP setting, and pixel clock frequency:
  - 800 x 600
  - 1024 x 768
  - 1024 x 1024
- 64-entry (by 24 bits) output FIFO
- Three 256-entry by 25-bit internal color-palette RAMs (one for each overlay and base), programmable for automatic loading at the beginning of each frame
- Command data RAM (16 x 9 bits) to hold command data
- Pixel depths of 8, 16, 18 and 24 bpp RGB, and 19 and 25 bpp RGBT formats

Table 22 LCD Signals

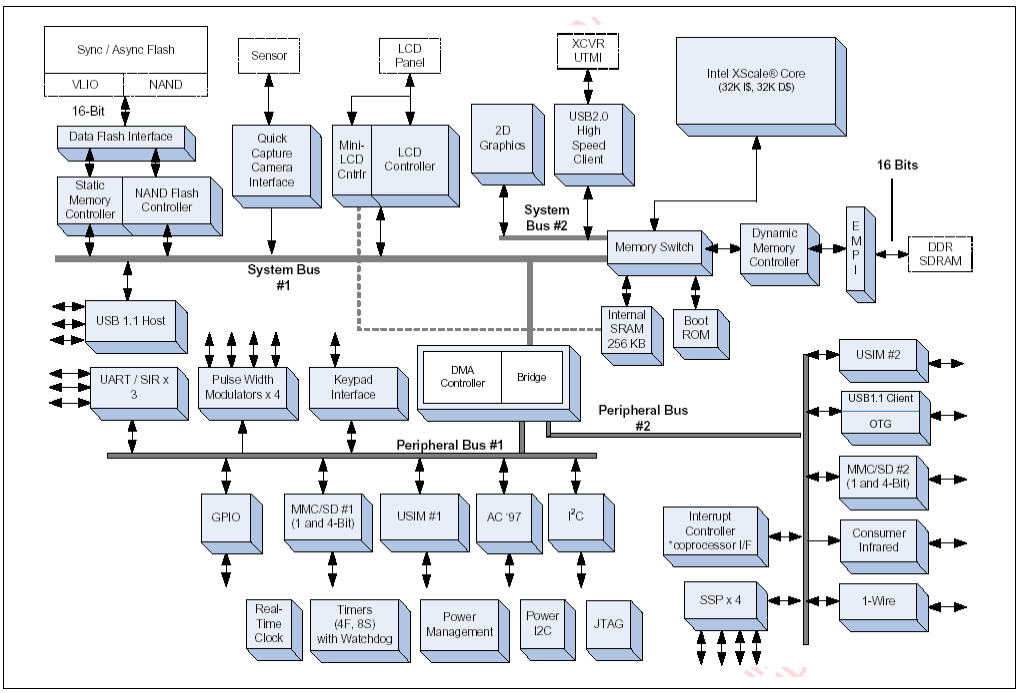
CM-X300 Signal Name	Type	Description
LCD-R[5:1]	O	Red channel data for TFT panels. Bit 0 of the panel's red channel should be connected to GND.
LCD-G[5:0]	O	Green channel data for TFT panels.
LCD-B[5:1]	O	Blue channel data for TFT panels. Bit 0 of the panel's blue channel should be connected to GND.
LCD-LP	O	HSYNC for TFT panels.
LCD-FRM	O	VSYNC for TFT panels.
LCD-SCK	O	Pixel clock.
LCD-DE	O	

3.3.8.1 Limitations of Display Controller Capabilities

The LCD controller provides a variety of programmable options including display type, resolution, frame buffer, pixel depth, overlays, hardware cursor, and output data formatting. Although all programmable combinations are possible, the available selection of displays dictates which combinations of these programmable options are practical. The type of external memory system used limits the bandwidth of the LCD DMA controller, which, in turn, limits the resolution and type of screen that can be controlled. Use information below to determine the maximum bandwidth of the internal bus that the LCD can use without negatively affecting all other functions.

The equations in this section provide a way to estimate the LCD bandwidth needed to drive an LCD panel with the PXA3xx processor. LCD bandwidth can affect overall system performance by reducing the available system memory bus bandwidth. The CM-X300's memory bus clock frequency is 130 MHz, data rate 260 MT/s. The LCD controller shares the System Bus #1 with other devices (see Figure 6 below)

Figure 6 PXA300 Processor Block Diagram



The LCD controller can be programmed with timing values that control the refresh rate and the needed LCD bandwidth for a specific LCD panel. The total needed memory bus bandwidth can be defined as the LCD bandwidth plus the system memory bus bandwidth used by any other running processes in the processor. When the total memory bus

bandwidth needed exceeds the total available memory bus bandwidth, visible video artifacts may be seen on the LCD panel.

$$\text{Total Needed Memory Bus Bandwidth} = \text{LCD Bandwidth} + \text{System Memory Bus Bandwidth}$$

The number of pixel clocks to send one line of pixels is calculated using the following equation:

$$\frac{\text{PixelClocks}}{\text{Line}} = (\text{HSW}+1)+(\text{BLW}+1)+(\text{PPL}+1)+(\text{ELW}+1)$$

Or:

$$\frac{\text{PixelClocks}}{\text{Line}} = \text{HSW}+\text{BLW}+\text{PPL}+\text{ELW}+4$$

where:

- HSW = Horizontal Sync Width
- BLW = Beginning of Line Width
- PPL = Pixels Per Line (Frame width -1)
- ELW = End of Line width

The number of line clocks (HSYNC clocks) needed to send one frame is calculated using the following equation:

$$\frac{\text{LineClocks}}{\text{Frame}} = (\text{VSW}+1)+\text{BFW}+(\text{LPP}+1)+\text{EFW}$$

Or:

$$\frac{\text{LineClocks}}{\text{Frame}} = \text{VSW}+\text{BFW}+\text{LPP}+\text{EFW}+2$$

where:

- VSW = Vertical Sync Width
- BFW = Beginning of Frame Width
- LPP = Lines Per Page (Frame height – 1)
- EFW = End of Frame Width

The number of pixel clocks to send one frame is calculated using the following equation:

$$\frac{\text{PixelClocks}}{\text{Frame}} = \frac{\text{LineClocks}}{\text{Frame}} \times \frac{\text{PixelClocks}}{\text{Line}}$$

substituting:

$$\frac{\text{PixelClocks}}{\text{Frame}} = (\text{VSW}+\text{BFW}+\text{LPP}+\text{EFW}+2)\times(\text{HSW}+\text{BLW}+\text{ELW}+\text{PPL}+4)$$

Because LPP = Height – 1 and PPL = Width – 1, the following equation applies:

$$\frac{\text{PixelClocks}}{\text{Frame}} = (\text{VSW}+\text{BFW}+\text{Height}+\text{EFW}+1)\times(\text{HSW}+\text{BLW}+\text{ELW}+\text{Width}+3)$$

The refresh rate, which is the number of frames per second that the LCD controller is fetching from memory and sending to the LCD panel, can be calculated using the following equation:

$$\text{Refresh Rate} = \frac{\text{Pixel Clock Frequency}}{\left(\frac{\text{Pixel Clocks}}{\text{Frame}}\right)}$$

Pixel clock frequency is a parameter of the chosen resolution and frames per second, as well as of the LCD-specific parameters, such as pixel clock wait states at the beginning and end of each line, the number of line clocks inserted in the beginning and end of each frame. Here's an example of some common video modes and their corresponding pixel clocks: http://www.engr.udayton.edu/faculty/jloomis/altera/DE2/vga.html

The LCD data rate required for each plane to support the LCD panel selected for the system is calculated using this formula:

$$\text{Data Rate} = \left(\frac{\text{Length} \times \text{Width} \times \text{Refresh Rate} \times \text{Bits per Pixel}}{8} \right) bps$$

The bits per pixel is the number of bits used in the memory to store each pixel. Memory organization for pixel depth of 16bpp uses 2 bytes of data per pixel. With overlays enabled, pixel depth is reduced to 15bpp still using 2 bytes.

The number of 4-beat burst operations (8 bytes/beat) that are generated by the LCD DMA controller is as follows:

$$\text{LCD DMA burst Count} = \left(\frac{\text{Data Rate}}{32} \right) \text{Burst/sec}$$

The time consumed by the LCD refresh operation is then calculated by:

$$\text{LCD refresh time} = (\text{LCD DMA burst count} \times \text{Pdma}) / \text{second}$$

The value of Pdma is the period in microseconds of LCD DMA four-beat burst, including SDRAM precharge time. The time remaining within each second after deducting the LCD refresh time is the time available for instruction and data fetches, hardware accesses, and memory refresh operations. Use caution when setting system parameters, such as core frequency, system frequency, memory frequency, and bus arbiter settings to ensure that LCD FIFOs do not underrun due to bus latencies caused by other internal and external peripherals. This caution applies especially for interrupt and polled modes that require a longer time to service.

Benchmarking a real system remains the best way to estimate the LCD subsystem's performance.

3.3.9 USB

3.3.9.1 USB Controllers

The CM-X300 features three USB controllers.

The USB device controller (UDC) is USB 1.1-compliant and supports all standard device requests issued by any certified USB host controller. This is a full-speed compliant device (does not support low-speed operation). This controller's interface is the CAMI USB2 Interface (only in C624 configurations).

The Universal Serial Bus 2.0 Device Controller (U2DC) supports both high-speed and full-speed modes. The C624 configuration modules feature the industry standard Universal Transceiver Macrocell Interface (UTMI), Version 1.05 transceiver for interfacing USB devices. The transceiver's interface is routed to the CAMI USB3 Interface. In the C624M modules a ULPI transceiver is used instead, connected to the CAMI USB2 Interface.

The Open Host Controller Interface (OHCI) Rev 1.0a-compatible USB host controller supports both high-speed and full-speed modes. The available interfaces for the host controller are the CAMI USB2 Interfacein C624 only non-W configuration modules and the CAMI USB1 Interface in non-W configurations.

For a full description of the USB protocol and its operation, refer to the documents listed in Table 2 and to Related Documents on page 9.

3.3.9.2 USB Interfaces Routing

Table 23 below describes USB interfaces routing differences between C624 and C624M module configurations.

Table 23 USB Interfaces

CAMI USB Interface	CM-X300-C625	CM-X300-C625M
USB1	USB Host Controller (differential port1 IF on PXA300)	USB Host Controller (single ended port 3 IF on PXA310)
USB2	USB Host Controller or USB Device Controller (OTG diff port 2 IF on PXA300)	USB2.0 Device Controller or USB Host Controller (ULPI IF on PXA310)
USB3	USB 2.0 Device Controller (UTMI IF) on PXA300	None

3.3.9.3 USB1 Interface

The USB1 CAMI interface is routed to the PXA300's differential USB port 1 or to the PXA310's single ended USB port 3 (by means of the onboard transmitter). In both cases this interface is controlled by the CPU's USB host controller. The module's integrated Bluetooth uses this port; therefore it's not available with "W" option.

Table 24 USB1 CAMI Port Signals

CM-X300 Signal Name	Type	Description
{USBH-P, USBH-N}	I/O	USB Full Speed Host Data Differential pair that connects to the USB host controller.

3.3.9.4 USB2 Interface

This interface has different functionality in modules with PXA300 and PXA310 processor.

In the C624 modules (PXA300) this interface provides USB1.1 host/device and OTG functionality and is routed to the PXA300's differential OTG USB port 2.

In the C624M modules (PXA310) this interface provides USB2.0 device or USB1.1 host functionality and is routed to the PXA300's ULPI interface by means of an onboard ULPI transmitter.

Table 25 USB2 CAMI Port Signals

CM-X300 Signal Name	Type	Description
{USB-OTG-P, USB-OTG-N}	I/O	USB Full Speed Host/Device/OTG and USB 2.0 Device Data Differential pair that connects to either the USB host controller, the USB device controller or USB 2.0 Device controller. On-The-Go functionality is available on this port.
USB-OTG-ID	I	Provides the OTG ID configuration.

3.3.9.5 USB3 Interface

This interface is available only on the C624 (PXA300) modules. It provides USB 2.0 high-speed device functionality and is routed to the UTMI interface of PXA300 by means of an onboard UTMI transmitter.

Table 26 USB3 CAMI Port Signals

CM-X300 Signal Name	Type	Description
{USBD-P, USBD-N}	I/O	USB 2.0 Device Data Differential pair that connects to the USB 2.0 device controller.

3.3.10 MMC/SD/SDIO Controller

The Multimedia Card (MMC) and Secure Digital (SD/SDIO) controller (MMC/SD/SDIO controller) provides a software-accessible hardware link between the processor and the MMC stack (a set of memory cards). The MMC/SD/SDIO controller supports Multimedia Card, Secure Digital, and Secure Digital I/O communication protocols.

- The MMC module manages the MMC system, which is low-cost data storage and communications system. The MMC module is based on the standards outlined in the Multimedia Card System Specification Version 3.3.1. The SD module manages one SD or SDIO card based on the standards outlined in the SD Memory Card Specification Version 1.10 and SDIO Card Specification Version 1.0.

The MMC/SD/SDIO controller manages the translation protocol from a standard MMC bus or from a serial peripheral interface (SPI) bus to the MMC stack. Software must select either the MMC/SD/SDIO mode or SPI mode to establish the communication protocol for the MMC/SD/SDIO controller.

3.3.10.1 MMC/SD/SDIO Controller Features

- A response FIFO (MMC_RES)
- Two transmit FIFOs (MMC_TXFIFO1 and MMC_TXFIFO2)
- Two receive FIFOs (MMC_RXFIFO1 and MMC_RXFIFO2)
- Two operating modes:
  - MMC/SD/SDIO mode for MMC, SD, and SDIO communication protocols.
  - SPI mode for the SPI communications protocol.
- One-bit and 4-bit data transfers for MMC, SD, and SDIO communication protocols
- Data transfer clock up to 26 MHz
- Based on FIFO status, turn clock on and off to prevent overflows and under-runs
- Support for all valid MMC and SD/SDIO protocol data-transfer modes
- Interrupt-based application interface to control software interaction
- Stream data transfers of 10 bytes or more
- Multiple MMC cards for the MMC communications protocol
- Only one SD or SDIO port can be used for SD or SDIO communications protocol at one time.
- Up to two MMC or SD/SDIO cards when the SPI communications protocol is used. Mixed card types are supported only by the SPI communications protocol.

3.3.10.2 MMC/SD/SDIO Controller Interface Signals

Table 27 MMC and SD/SDIO Mode Signals

CM-X300 Signal Name	Type	Description
MMC_CLK	O	Bus clock
MMC_CMD0	I/O	Command and responses
MMC_CMD1	I/O	Command and responses
MMC_DAT[3:0]	I/O	Read and write data

Table 28 SPI Mode Signals

CM-X300 Signal Name	Type	Description
MMC_CLK	O	SPI clock
MMC_CMD0	O	Output for command and write data
MMC_CMD1	O	Output for command and write data
MMC_DAT0	I	Input for response token and read data
MMC_DAT1	I	Signals an interrupt condition to the controller
MMC_DAT2	O	CS0 chip select
MMC_DAT3	O	CS1 chip select

3.3.11 GPIO

3.3.11.1 I²C Operated GPIOs

The CM-X300 features 32 I²C-operated GPIO lines implemented using two I²C GPIO extender IC's – Catalyst CAT9555 or compatible.

Table 29 GPIO Extenders

IC	Signals Controlled	CAT9555 I²C Address
A	I2C_GPIO0_[7:0] I2C_GPIO1_[7:0]	0b0100100x
B	I2C_GPIO2_[7:0] I2C_GPIO3_[7:0]	0b0100101x

Note: 'X' denotes R/W# bit.

Table 30 I²C Operated GPIO Signals

CM-X300 Signal Name	Type	Description
I2C_GPIO0_[7:0] I2C_GPIO1_[7:0] I2C_GPIO2_[7:0] I2C_GPIO3_[7:0]	I/O	5V-tolerant GPIO

Table 31 I²C Operated GPIO DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	$V_{CC\ typ}$ = 3.2V	-0.5	–	0.3 x V_{CC}	V
V_{IH}	High level input voltage	$V_{CC\ typ}$ = 3.2V	0.7 x V_{CC}	–	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.5V V_{OL} = 0.7V	8 10	8 to 20 10 to 24	–	mA
V_{OH}	High level output voltage	I_{OH} = -10 mA	2.5	–	–	V
I_{IH}	Input leakage current	$V_I = V_{CC}$	–	–	1	uA
I_{IL}	Input leakage current	$V_I = V_{SS}$	–	–	-100	uA

3.3.11.2 CPU GPIO

The General-Purpose I/O (GPIO) provides 11 general-purpose input/output GPIO ports for use in generating and capturing application-specific input and output. All ports are brought out of the processor through alternate function multiplexing. More ports may be made available when certain interfaces are not required by an application.

When programmed as an input, a GPIO port can also serve as an interrupt source. At the assertion of all resets, all ports are configured as inputs and remain inputs until they are configured either by the boot process or by user software.

The direction of the GPIO ports is controlled by writing to the CPU's GPIO Pin Direction register (GPDR2). When the GPIO pin is programmed as an output, the port is set by writing to the GPIO Pin Output Set Register (GPSR2) and cleared by writing to the GPIO Pin Output Clear Register (GPCR2). The Set and Clear registers can be written regardless of whether the port is configured as an input or an output. The programmed output state takes effect when the port is reconfigured as an output.

When the GPIO pin is programmed as an input, it can be configured to detect a rising edge, falling edge, or both through the GPIO Rising-Edge Detect Enable Register (GRER2) and the GPIO Falling-Edge Detect Enable Register (GFER2). The state of the edge-detect can be read through the GPIO Edge Detect Status Register (GEDR2). These edge-detects can be programmed to generate interrupts.

The value of each GPIO port is read through the GPIO Pin-Level Register (GPLR2). This register can be read at any time and can confirm the port state for both input and output configurations.

Note: GPIO18 is used internally by the u-boot when booting the module. It should not be pulled-up or down by values lower than 100K on the baseboard.

Table 32 CPU GPIO Signals

CM-X300 Signal Name	Type	Description
GPIO[90:80]	I/O	Dedicated GPIO (GPIO80..82 are available in C624 modules only. In the C624M modules using these GPIO lines will interfere with USB host function)
GPIO[52:39]	I/O	Camera interface GPIO (shared with CIF pins). These GPIO's are available for GPIO use only in C624M modules. These signals are routed to CAMI in C624 modules, too, but cannot be used as GPIO as they serve as UTMI USB transmitter's interface onboard.
GPIO[37:30]	I/O	FFUART GPIO (shared with FFUART pins). Available only in C624 modules. These pins are used for ULPI transmitter interface in C624M modules and are not available on CAMI.
GPIO[125:115]	I/O	Keypad GPIO (shared with keypad pins)
GPIO[114:111]	I/O	BTUART GPIO (shared with BTUART function pins)
GPIO[88:85]	I/O	SSP1 GPIO (shared with SSP1 pins)

Each of the 32-bit registers described maps its bits [31:0] to the GPIO pins [95:64]. Software should not modify any bits except [26:16] mapped accordingly to the CPU GPIO signals [90:80] available on the CAMI.

Table 33 CPU GPIO Registers

Name	Address	Description
GPLR2	0x40E0_0008	GPIO Pin-Level Register 2. Shows the current value of a particular port (regardless of the programmed port direction): 0 = Port state is low 1 = Port state is high
GPDR2	0x40E0_0014	GPIO Pin Direction Register 2. If a direction bit is set, the GPIO pin is an output. If it is cleared, it is an input. A pair of set/clear registers (GSDR2 and GCDR2) is also provided to enable the setting and clearing of individual bits of the GPDR2 register. 0 = Port configured as an input 1 = Port configured as an output
GPSR2	0x40E0_0020	GPIO Pin Output Set Register 2. An output port is set by writing a 1 to its corresponding bit in the GPSR2 (write-only register; reads return unpredictable values). 0 = Port level unaffected. 1 = If the port is configured as an output, set the port level logic high

Name	Address	Description
GPCR2	0x40E0_002C	GPIO Pin Output Clear Register 2. An output port is cleared when a 1 is written to the corresponding bit within the GPCR2 (write-only register; reads return unpredictable values). 0 = Port level unaffected. 1 = If the port is configured as an output, clear the port level logic low.
GRER2	0x40E0_0038	GPIO Rising-Edge Detect-Enable Register 2. GRER2 bit is set to cause a GEDR2 status bit to be set when the port transitions from Logic Level low to Logic Level high. 0 = Disable rising-edge detect enable. 1 = Set the corresponding GEDR status bit when a rising edge is detected on the GPIO port.
GFER2	0x40E0_0044	GPIO Falling-Edge Detect-Enable Register 2. GFER2 bit is set to cause a GEDR2 status bit to be set when the port transitions from Logic Level high to Logic Level low. 0 = No falling-edge detect enable. 1 = Set the corresponding GEDR status bit when a falling edge is detected on the GPIO port.
GEDR2	0x40E0_0050	GPIO Edge Detect Status Register 2 . When an edge-detect occurs on a port that matches the type of edge programmed in the GRER2 and/or GFER2 registers, the corresponding status bit is set in GEDR2. When a GEDR2 bit is set, the CPU must clear it. GEDR2 status bits are cleared by writing a 1 to them. Writing a 0 has no effect. Each edge-detect that sets the corresponding GEDR2 status bit for GPIO pins can trigger an interrupt request. 0 = No edge detect on the port as specified in GRER2 and/or GFER2. 1 = Edge detect on the port as specified in GRER2 and/or GFER2.
GSDR2	0x40E0_0408	GPIO Pin Bit-Wise Set Direction Register 2 . If a direction bit is set, the corresponding bit in GPDR2 is set and the GPIO function is configured as an output. If it is cleared, no change in the GPIO functionality or the GPDR2 register occurs. 0 = GPDR2 bit not affected. 1 = GPDR2 bit is set and GPIO function is set to OUTPUT.
GCDR2	0x40E0_0428	GPIO Pin Bit-Wise Clear Direction Register 2 . If a direction bit is set, the corresponding bit in GPDR2 is cleared and the GPIO function is configured as an input. If it is cleared, no change in the GPIO functionality or the GPDR2 register occurs. 0 = GPDR2 bit is not affected. 1 = GPDR2 bit is cleared and a GPIO function is set to INPUT.
GSRER2	0x40E0_0448	GPIO Bit-Wise Set Rising-Edge Register 2. If a bit is set, the corresponding bit in GRER2 is set and the GPIO function is configured to cause a GEDR2 status bit to be set when the port transitions from Logic Level zero (0) to Logic Level one (1). If the bit is cleared, no change in the GPIO functionality or GRERx occurs 0 = GRER2 bit not affected. 1 = GRER2 bit is set.
GCRER2	0x40E0_0468	GPIO Bit-wise Clear Rising-Edge Detect-Enable Register 2. If a bit is set, the corresponding bit in GRER2 is cleared and the GPIO function is configured to *not* cause a GEDR2 status bit to be set when the port transitions from Logic Level zero (0) to Logic Level one (1). If the bit is cleared, no change in the GPIO functionality or the GRER2 register occurs 0 = GRER2 bit not affected. 1 = GRER2 bit is cleared
GSFER2	0x40E0_0488	GPIO Bit-Wise Set Falling-Edge Register 2. If a bit is set, the corresponding bit in GFER2 is set and the GPIO function is configured to cause a GEDR2 status bit to be set when the port transitions from logic-level one (1) to logic-level zero (0). If the bit is cleared, no change in the GPIO functionality or the GFER2 register occurs 0 = GFER2 bit not affected 1 = GFER2 bit is set
GCFER2	0x40E0_04A8	GPIO Bit-wise Clear Falling-Edge Detect-Enable Register 2. If a bit is set, the corresponding bit in GFER2 is cleared and the GPIO function is configured to not cause a GEDR2 status bit to be set when the port transitions from logic-level one (1) to logic-level zero (0) If the bit is cleared, no change occurs in the GPIO functionality or the GFER2 register. 0 = GFER2 bit not affected 1 = GFER2 bit is cleared

Table 34 CPU GPIO DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	$V_{CC\ typ}$ = 3.2V	-0.3	–	0.2 x V_{CC}	V
V_{IH}	High level input voltage	$V_{CC\ typ}$ = 3.2V	0.8 x V_{CC}	–	V_{CC} + 0.3	V
V_{OH}	High level output voltage	I_{OH} = -1.5 to -18 mA	0.9 x V_{CC}	–	V_{CC}	V
V_{OL}	Low level output voltage	I_{OH} = -1.25 to -15 mA	V_{SS}	–	0.1 x V_{CC}	V
R_{PULLUP}, $R_{PULLDOWN}$	Pull-up and pull-down resistance		20	45	100	kOhm

3.3.12 Camera Interface

The CM-X300 camera interface is represented by the CPU's Quick Capture Interface. It connects the processor and a compatible external image-capture module, which consists of a sensor providing RAW image data, a sensor with a minimal level of integrated processing on RGB or YCbCr image data, or the combination of a sensor with more sophisticated image-processing capability.

Note: The Camera Interface is available only in CM-X300 modules with PXA310 processor (C624M configuration).

The Quick Capture Interface operates in three modes:

- Preprocessed Still-Image/Video Capture mode. Supports image sensors and camera modules that provide some level of preprocessing. The image data is in YCbCr 4:2:2 color space. The image data is captured through various interface options, optionally scaled and/or bit sliced, and then formatted and packed before it is presented to system memory resources.
- RAW Still-Image Capture mode. Captures and formats image data to be processed using algorithms targeting display or print quality. The image data is in the four element Bayer pattern of RGGB color space. The data is captured through the various interface options, optionally corrected for dead pixels, companded, black-level clamped, and then packed before it is presented to memory resources.
- RAW Video-Image Capture mode. Offers the digital viewfinder function and the video-clip capture function at a CIF, QCIF, SIF, or QSIF resolution. The sensor provides image data in the RAW RGGB color. The integrated pixel processing chain supports the conversion to RGB 8:8:8 and YCbCr 4:2:2 (and YCbCr 4:2:0 for PXA31x processor) color space through several functional units, which include:
  - Spatial scaling unit (SSU)
  - Pixel substitution unit (PSU)
  - Companding/black-level clamp/gamma correction unit (CGU)
  - Color synthesis unit (CSU)
  - Color management unit (color space conversion and correction) (CMU)

Table 35 Camera Interface Signals

CM-X300 Signal Name	Type	Description
CIF_DD[9:0]	I	Data lines to transmit 8 or 10 bits of data at a time. These pins may be defined as GPIO[48..39] in a camera-less application.
CIF_MCLK	O	Programmable clock output used by the image sensor. This pin may be defined as GPIO49 in a camera-less application.
CIF_PCLK	I	Pixel clock used by the Quick Capture Interface to clock the pixel data into the input FIFO. This pin may be defined as GPIO50 in a camera-less application.

CM-X300 Signal Name	Type	Description
CIF_FV	I/O	Frame start or alternate synchronization signal used by the sensor to signal frame readout or as an external vertical sync. For CIF_PCLK speeds > 26 MHz, the sensor CIF_FSYNC signal must not be active until at least 2 pixel clocks after the last valid data of a frame. This pin may be defined as GPIO52 in a camera-less application.
CIF_LV	I/O	Line start or alternate synchronization signal used by the sensor to signal line readout or as an external horizontal sync. For CIF_PCLK speeds > 26 MHz, the sensor CIF_HSYNC signal must not be active until at least 2 pixel clocks after the last valid data of a line. This pin may be defined as GPIO51 in a camera-less application.

3.3.13 Audio Subsystem

3.3.13.1 Audio I/O

The CM-X300 audio subsystem uses the Wolfson WM9715L as an AC'97 Rev 2.2 compatible stereo codec. Its analog audio interfaces include stereo line output which may also drive a 400mW speaker or 45mW headphone, mono microphone input and stereo line input.

Table 36 Audio I/O Signals

CM-X300 Signal Name	Type	Description
AUD-SPDIF	O	SPDIF Digital Audio Output
AUD-INL-MIC	AI	Left Line Input and Microphone Input
AUD-INR	AI	Right Line Input
AUD-OUTL	AO	Left Output (Speaker, Line or Headphone)
AUD-OUTR	AO	Right Output (Speaker, Line or Headphone)

3.3.13.2 AC'97 Bus

The AC'97 bus is available on the same CAMI connector pins as the audio I/O signals, when the "AT" option is not engaged.

Table 37 AC'97 Bus Signals

CM-X300 Signal Name	Type	Description
AUD-SPDIF/ AC97_RST#	O	Asynchronous, active-low CODEC reset. The CODEC registers arereset when AC97_RST is asserted
AUD-INR/ AC97_SDOUT	O	Serial audio output data to CODEC, for digital-to-analog conversion
AUD-OUTL/ AC97_SDIN	I	Serial audio input data, from primary CODEC
AUD-INL-MIC/ AC97_BITCLK	I	12.288 MHz bit-rate clock
AUD-OUTR/ AC97_SYNC	O	48-kHz frame indicator and synchronizer

3.3.14 Touch Panel Interface

The CM-X300 features a resistive touchpanel interface. It has a 12-bit resolution and supports 4-wire panels only.

Table 38 Touch Panel Interface Signals

CM-X300 Signal Name	Type	Description
TS-XP	AI	X+ (Right)
TS-YP	AI	Y+ (Top)
TS-XM	AI	X- (Left)
TS-YM	AI	Y- (Bottom)

3.3.15 Power

The CM-X300 connects to power sources through the dedicated pins on the CAMI connectors listed in the Table 39 below.

Table 39 Power Signals

CM-X300 Signal Name	Type	Description
GND	P	Ground (common wire)
VBAT	P	Battery/DC supply voltage
VCHRG	P	Charger voltage
VCC-RTC	P	RTC backup supply voltage

The main supply voltage for CM-X300 should be connected to VBAT pins on the CAMI.

When an external regulator is used for VBAT (CM-X300 without the "B" option) VCHRG pins can be left unconnected.

If a battery is used for VBAT (CM-X300 with the "B" option) VCHRG pins should be connected to an external DC Charger. Battery charge current is drawn from the VCHRG input.

The operating conditions for the charger and the battery are listed below.

Table 40 Battery and Charger Operating Conditions

Parameter	Description
VBAT voltage	**With "B" option:** VBAT should be in 3.4V to 4.5V voltage range. CM-X300 will not boot until VBAT is within this range. If the battery is completely drained (below 3.2V), then pre-charge mode is started when a charger has been detected. The current flow into the battery will be 40mA nominal. If within 60 min. the VBAT reached 3.2V, CM-X300 will be powered on, otherwise the pre-charge mode will be disabled. If VBAT reaches 4.7V (for example, when battery suddenly disconnects while charger is connected and powered), CM-X300 will be turned off immediately. **Without "B" option:** VBAT should be 3.3V for normal operation. When battery is not required by design, external regulator voltage should not fall below 3.2V.
VCHRG voltage	4.6 to 10.0 V
Battery type	The internal battery charger supports the following battery chemistries: • Single-Cell Li-Ion at 4.1V • Single-Cell Li-Ion at 4.2V • Li-Polymer Pack
VCC-RTC voltage	1.5 to 5.0 V Typical supply current 390 nA @ 3.0 V

3.3.16 System Signals

The CM-X300's system signals are listed in Table 41.

Table 41 System Signals

CM-X300 Signal Name	Type	Description
WP1#	I	Hardware write protect for the the entire onboard Data Flash. Prevents all program/erase operations. Pulled up to 3.3V internally. Connect to GND to write-protect.
RST-IN#	I/OD	Reset input to CPU and power-on reset output. Pulled up to 3.3V
EXTWAKE#	I	Processor's wakeup signal. Pulled down to GND. Pull to 3.3V to generate wakeup event.
ONKEY#	I	Connects to ON/OFF button. Pull to GND to switch the Power Management IC ON or OFF. Tying this line to GND for 5 s or more generates a hard reset.
IRQ	I	Processor's interrupt request. Connects to the pin GPIO19.
BOOTENA#	I	May be used to disable internal Data Flash. Normally pulled to GND. Pull to 3.3V to disable.
RST-OUT#	OD	Active low output, indicated reset state of the CPU's Services Power Management Unit
SYS_EN	O	System Enable for System Peripheral Power Supply. This output, when deactivated, signals that the system is entering S3/D4/C4 mode
EXT_TBAT	I	Should be connected to the battery's internal NTC resistor to make its temperature measurement by the charger function possible.

3.3.17 I²C Bus

Table 42 I²C Signals

CM-X300 Signal Name	Type	Description
I2C-CLK	O	I²C bus clock
I2C-DATA	I/O	I²C bus bidirectional data

3.3.18 Synchronous Serial Port (SSP)

The CM-X300 features two synchronous serial ports (SSP). These are the PXA3xx ports SSP1 and SSP3. PXA3xx port SSP1 is available as an alternate function on pins GPIO[85:88]. Port SSP3 is routed to CAMI connector B.

Table 43 SSP1 Port Signals

CM-X300 Signal Name	Type	Description
SSPSCLK	I/O	Synchronous Serial Protocol Serial Clock. Shared with pin GPIO85. Controls the timing of a serial transfer. SSPSCLK can be generated internally (master mode) or taken from an external source (slave mode)
SSPSFRM	I/O	Synchronous Serial Protocol Serial Frame Indicator. Shared with pin GPIO86. Indicates the beginning and the end of a serialized data sample. The SSPSFRM can be generated internally (master mode) or taken from an external source (slave mode).
SSPTXD	O	Synchronous Serial Protocol Transmit Data. Shared with pin GPIO87. Serial data out.
SSPRXD	I	Synchronous Serial Protocol Receive Data. Shared with pin GPIO88. Serial data in.

Table 44 SSP3 Port Signals

CM-X300 Signal Name	Type	Description
SSPSCLK3	I/O	Synchronous Serial Protocol Serial Clock. Controls the timing of a serial transfer. SSPSCLK can be generated internally (master mode) or taken from an external source (slave mode)
SSPSFRM3	I/O	Synchronous Serial Protocol Serial Frame Indicator. Indicates the beginning and the end of a serialized data sample. The SSPSFRM can be generated internally (master mode) or taken from an external source (slave mode).

CM-X300 Signal Name	Type	Description
SSPTXD3	O	Synchronous Serial Protocol Transmit Data. Serial data out.
SSPRXD3	I	Synchronous Serial Protocol Receive Data.Serial data in.

3.3.18.1 SSP Features

The SSP port features are:

- Directly supports Texas Instruments* Synchronous Serial (SSP) and Motorola* Serial Peripheral Interface (SPI).
- The Inter-IC Sound (I^2S) protocol is supported by programming the Programmable Serial Protocol (PSP). PSP format is only supported for emulation of the I^2S protocol.
- Data sample sizes can be set to 8, 16, 18 or 32 bits
- One FIFO for transmit data (TXFIFO) and a 2nd, independent, FIFO for receive data (RXFIFO). For non-packed data mode, the two FIFOs are each 16 rows deep x 32 bits wide for a total of 16 samples.
- FIFO packed mode allows double depth FIFOs if the samples are 8 bits or 16 bits wide. For packed data mode, both FIFOs are 32 locations deep x 16 bits wide for a total of 32 samples.
- Master mode and slave mode operation supported
- A maximum serial bit-rate supported of 13 Mbps.
- Receive-without-transmit operation
- Network mode with up to eight time slots for PSP formats, and independent transmit/receive in any/all/none of the time slots.

3.3.18.2 Turning the SSP Port On

In order to enable SSP function on pins GPIO[85:88], their alternate functions should be modified in the corresponding configuration registers. A binary value ‘001’ must be written into the bits [2:0] of the multi-function pin registers (MFPR) at addresses 0x40E104E8, 0x40E104EC, 0x40E104F0, 0x40E104F4 using a read-modify write access.

3.3.19 PWM Controller

The PWM function enables the control of leading- and falling-edge timing of two output channels. The edge timing can be set up to run indefinitely or adjusted on the fly to adapt to variable requirements. Power-saving modes include the ability to stop the internal clock source (PSCLK_PWM) used to source the PWM and drive the PWM_OUT signals to a steady high or low state.

The frequency range supporting a 50% duty cycle varies from 198.4 Hz to 6.5 MHz. Other duty-cycle options depend on the choice of preferred frequency.

Table 45 PWM Signals

CM-X300 Signal Name	Type	Description
PWM1-OUT	I/O	Pulse-width modulated signal, output of the CPU’s PWM1 controller. This pin is used internally by the u-boot when booting the module. It should not be pulled-up or down by values lower than 100K on the baseboard.
PWM2-OUT	I/O	Pulse-width modulated signal, output of the CPU’s PWM2 controller

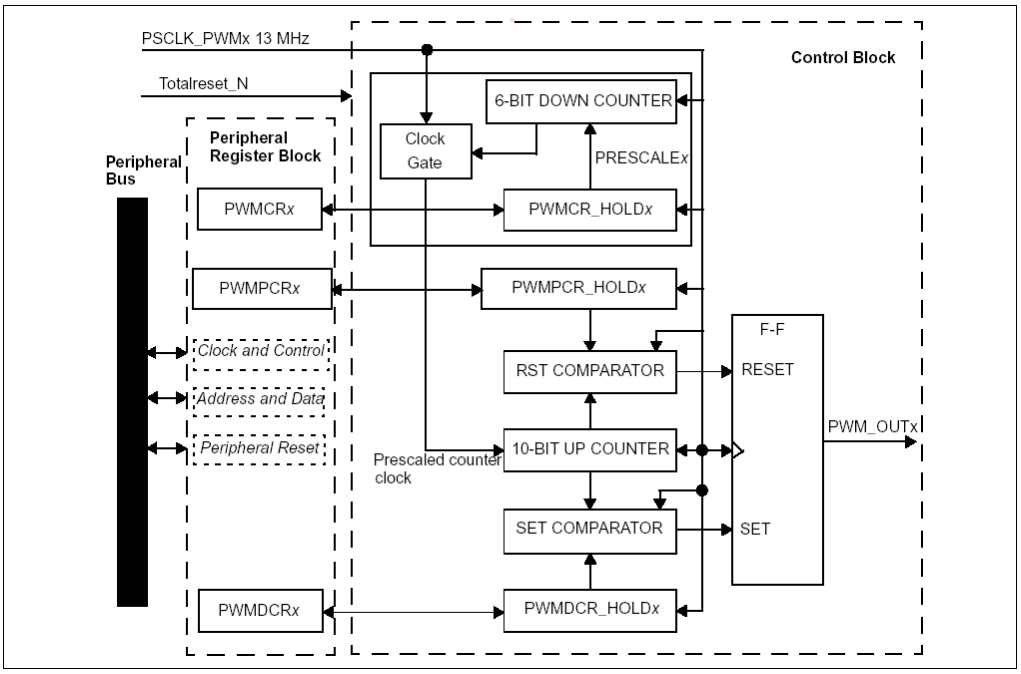
3.3.19.1 PWM Features

- Four pulse-width modulated signal channels
- Enhanced period controlled through 6-bit clock divider and 10-bit period counter
- 10-bit pulse control

3.3.19.2 PWM Operation

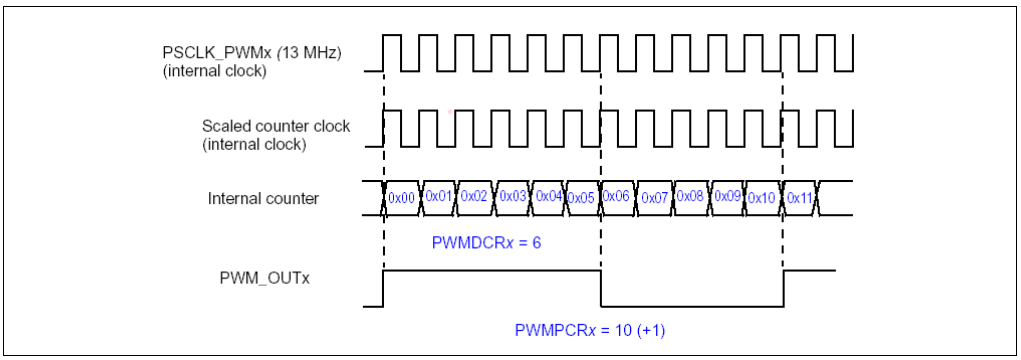
Figure 7 shows the block diagram for the PWM control logic.

Figure 7 PWM Block Diagram



To program the PWM controller, determine the period and pulse-width values. The period value is based on two registers, PWMPCR2 and PWMCR2.

Figure 8 Basic PWM Waveform

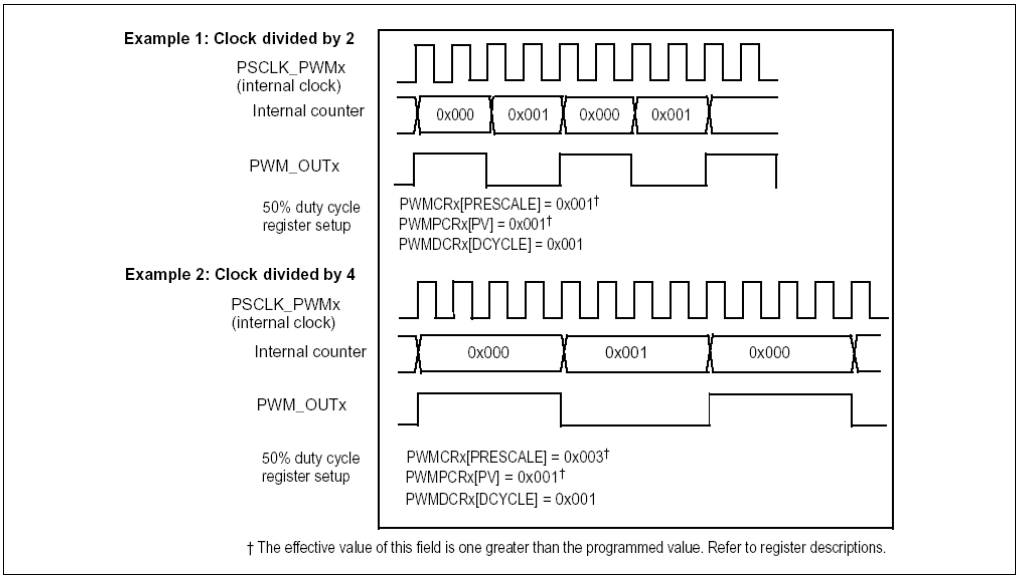


The output waveform in Figure 8 is derived by writing the PWMPCRx register with a value of 10(0x00A) and writing the PWMDCRx register with 0x06.

Pulse-width modulated signals, once programmed, output a specified waveform until the value in any associated register is altered. The time from the register change until the associated signal change depends on PWMPCRx[PV]:

- For PWMPCRx[PV] values 0x005 and larger—After a register value is altered, the PWM_OUTx signal changes when the previously programmed waveform cycle is complete.
- For PWMPCRx[PV] values less than 0x005—After a register value is altered, the PWM_OUTx signal changes after two waveform cycles

Figure 9 Effect of PWMCR2 Settings



Programming PWMCRx[PRESCALE] configures the prescaled counter clock. Two timing examples are provided in Figure 9. Both examples have the PWMDCRx and PWMPCRx registers set with the same 50% duty cycle setting. The first example shows the effect on the scaled counter clock effectively being divided by two with a setting of 0x01, while the second example shows the scaled counter clock being divided by four with a setting of 0x03. See Section 3.3.19.4 for more information regarding the calculation of waveform values.

3.3.19.3 PWM Reset Sequence

During system reset, the PWMCRx and PWMDCRx registers are reset to 0x0 and the PWMPCRx register is set to 0x004. Reset places the PWMx_OUT channel in a steady low state. The PWMx_OUT channel remains reset to 0x0 until the PWMDCRx register is programed with a non-zero value. Therefore,system reset results in no pulse-width modulated signal.

3.3.19.4 Programming Considerations

The PWM uses three registers to configure the output of the PWMx signal: PWMCRx, PWMDCRx, and PWMPCRx.

PWM timing is based on the input clock to the PWMx controller, PSCLK_PWMx, which is fixed at 13 MHz. This signal is divided by (PWMCRx[PRESCALE] + 1) to generate the scaled counter clock. The 6-bit PRESCALE field allows the input clock to be divided by values between 1 (PRESCALE = 0) and 64 (PRESCALE = 63). The scaled counter clock is further divided by contents of the PWMDCRx and PWMPCRx registers to generate the duty cycle and period of the PWMx signal.

- Use the following equation to calculate the frequency of the scaled counter clock: Scaled counter clock frequency = 13 MHz / (PWMCRx[PRESCALE] + 1)

- Use the following equation to calculate the cycle time of the scaled counter clock:
  Scaled counter clock cycle time = 76.9 ns x (PWMCRx[PRESCALE] + 1)

Both the period and the duty cycle of the PWM are based on the scaled counter clock cycle time. The PWMx_OUT signal is asserted for the number of scaled counter clock cycles equal to PWMDCRx[DCYCLE].

- To calculate the duty cycle time of the PWM,use the following equation:
  Duty cycle time = Scaled counter clock cycle time x PWMDCRx[DCYCLE]
- which also equals:
  Duty cycle time = 76.9nS x (PWMCRx[PRESCALE] + 1) x PWMDCRx[DCYCLE]

The PWM Period Control register (PWMPCRx) determines the number of scaled counter clock cycles each PWM period contains. The actual number of clocks is the value of PWMPCRx[PV] plus one. When the RST comparator equals (PWMPCRx[PV]+1), the comparators and the flip-flop are reset, and the values of the PWMDCR_HOLDx, PWMCR_HOLDx, and PWMPCR_HOLDx registers are loaded from the control block.

- Use the following equation to calculate the period of the PWM:
  PWM period = Scaled Counter Clock period x (PWMPCRx[PV] + 1)
- which also equals:
  PWM cycle time = 76.9nS x (PWMCRx[PRESCALE]+1) x (PWMPCRx[PV] + 1)
- Calculate values based on the necessary PWM cycle time and duty cycle with the following equations:
  Choose a PWMCRx[PRESCALE] value that is appropriate for all your PWM outputs.
  PWMPCRx[PV] = PWM cycle time / (76.0nS X (PWMCRx[PRESCALE] + 1)) – 1
  Duty cycle time = PWM cycle time * Duty Cycle%
  PWMDCRx[DCYCLE] = Duty cycle time / (76.0nS X (PWMCRx[PRESCALE] + 1))

For example, to create a 60% duty cycle 500 kHz signal, set PWMCRx[PRESCALE] to 0, PWMPCRx[PV] to 26 (0x1A), and PWMDCRx[DCYCLE] to 16 (0x10).

Note: To produce a toggle of the signal, the value of the PWMPCRx[PV]must be equal to or greater than PWMDCRx[DCYCLE]. If PWMPCRx[PV] is less than PWMDCRx[DCYCLE], the PWMx_OUT signal remains high. If PWMDCRx[DCYCLE] equals zero, the signal remains low.

The PWMDCRx[FD] bit determines if PWMx_OUT is always asserted. When this bit is set, PWMx_OUT remains high until PWMDCRx[FD] is cleared.

3.3.19.5 PWM Register Summary

The PWM contains three registers that control the clock, the period, and the duty cycle timing of the PWMx_OUT.

Table 46 PWM Registers

Address	Description
0x40C0_0000	PWM 1 Control Register (PWMCR1)
0x40C0_0004	PWM 1 Duty Cycle Register (PWMDCR1)
0x40C0_0008	PWM 1 Period Control Register (PWMPCR1)
0x40B0_0010	PWM 2 Control Register (PWMCR2)
0x40B0_0014	PWM 2 Duty Cycle Register (PWMDCR2)
0x40B0_0018	PWM 2 Period Control Register (PWMPCR2)

3.3.19.6 PWM Control Register (PWMCRx)

The PWM Control register (PWMCRx), defined in Table 47, configures the behavioral characteristics of the PWM shutdown response and the divisor for the input clocks to the PWM control unit that configures the frequency of the scaled counter clock.

This is a read/write register. Ignore reads from reserved bits. Write 0b0 to reserved bits.

Table 47 PWM Control Register

Bits	Access	Name	Description
31:7	–	–	Reserved
6	R/W	SD	Pulse Width Modulator Shutdown Mode: 0 = Graceful shutdown of PWMx when the PXA3xx processor family stops the clocks to the PWM. 1 = Abrupt shutdown of PWMx when the PXA3xx processor family stops the clocks to the PWM.
5:0	R/W	PRESCALE	The scaled counter clock frequency is: PSCLK_PWMx / (PRESCALEx + 1)

3.3.19.7 PWM Duty Cycle Register (PWMDCRx)

The PWMx Duty Cycle register (PWMDCRx), defined in Table 48, configures the duty cycle of the PWMx_OUT signal.

PWMDCRx[DCYCLE] specifies the number of scaled counter clocks that PWMx_OUT is asserted during each cycle of the PWMx_OUT. Refer to Section 3.3.19.4 for details on calculating the value of PWMDCRx[DCYCLE].

If PWMDCRx[FD] is set, PWMx_OUT remains high until PWMDCRx[FD] is cleared. This results in a duty cycle of 100%. Typically, PWMDCRx[FD] is cleared and the duty cycle of PWMx_OUT is a function of PWMDCRx[DCYCLE].

This is a read/write register. Ignore reads from reserved bits. Write 0b0 to reserved bits.

Table 48 PWM Duty Cycle Register

Bits	Access	Name	Description
31:11	–	–	Reserved
10	R/W	FD	Full Duty Cycle: 0 = PWMx_OUT is determined by DCYCLE value. 1 = PWMx_OUT is continuously asserted.
9:0	R/W	DCYCLE	Duty Cycle of PWMx_OUT: 0 = PWMx_OUT is continuously de-asserted. 1 = PWMx_OUT is high for the number of 13-MHz clock periods equal to PWMDCRx[DCYCLE] x (PWMCRx[PRESCALE]+1), If FD is set, DCYCLE has no effect on the output of PWM

3.3.19.8 PWM Period Control Register (PWMPCRx)

The Period Control registers (PWMPCRx), defined in This is a read/write register. Ignore reads from reserved bits. Write 0b0 to reserved bits.

Table 49, configures the cycle time of the PWMx_OUT signal.

PWMPCRx[PV] specifies the number of scaled counter clocks (plus one) in each cycle of the PWMx_OUT. Refer to Section 3.3.19.4 for details on calculating the value of PWMPCRx[PV].

If this register is cleared the PWMx_OUT signal maintains in a high state.

This is a read/write register. Ignore reads from reserved bits. Write 0b0 to reserved bits.

Table 49 PWM Period Control Register

Bits	Access	Name	Description
31:10	–	–	Reserved
9:0	R/W	PV	Period Value: The value of scaled clock cycles per cycle of PWMx_OUT plus one. If all zeros are written to this register the signal remains high.

4 BASEBOARD INTERFACE

4.1 CAMI Connectors

The CM-X300 connects to the external world through P1, P2 – 0.6 mm pitch 140-pin connectors.

4.1.1 Connectors Type and Layout

Table 50 CAMI Connectors

Reference	Mfg.	CM-X300 connector P/N	Baseboard (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab, see [prices] >> [accessories] links in the CompuLab's website. CompuLab's p/n name for AMP/Tyco 1-5353190-0 connector is "CON140".

4.1.2 Standoffs

CM-X300 has four mounting holes for standoffs. Standoff is implemented by two parts: screw and spacer.

Table 51 Standoff Part List

Part	Description	Manufacturer and P/N
Screw	M2, Pan head, Philips, 3.5mm +- 0.1mm Length, stainless Steel, Nickel or Zinc plating	Acton InoxPro BF22102003 Federal Screw Works DF1402003 WORLD BRIDGE MACHINARY 380J52020
Spacer	Spacer, M2, L = 4.14mm, Brass, Tin coating	World Bridge Machinery M2, L = 4.14mm

4.2 Mechanical drawings

Figure 10 CM-X300 Top View

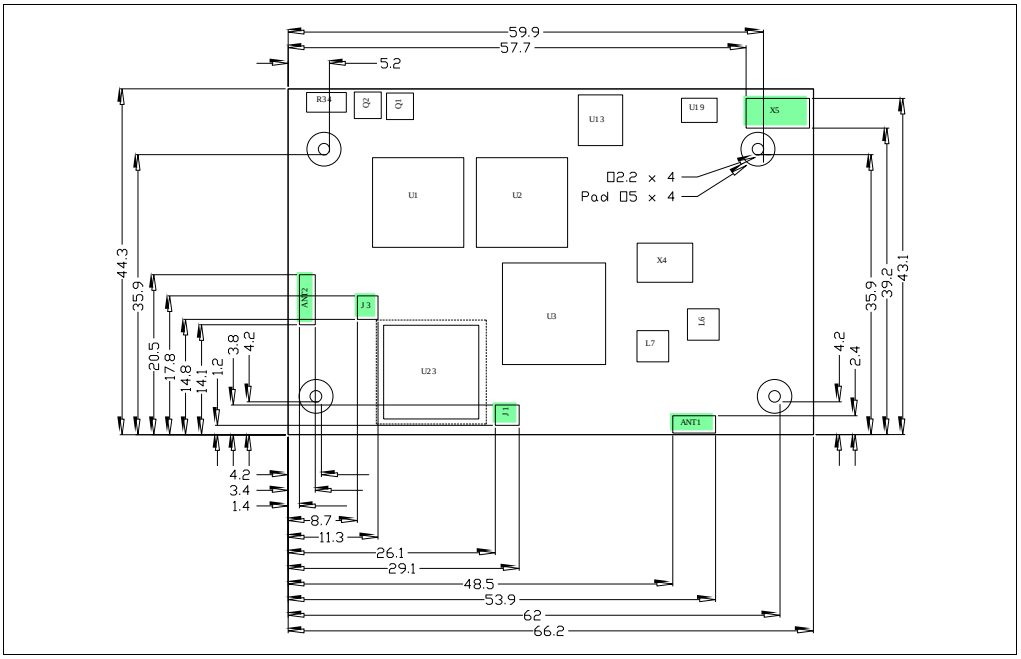
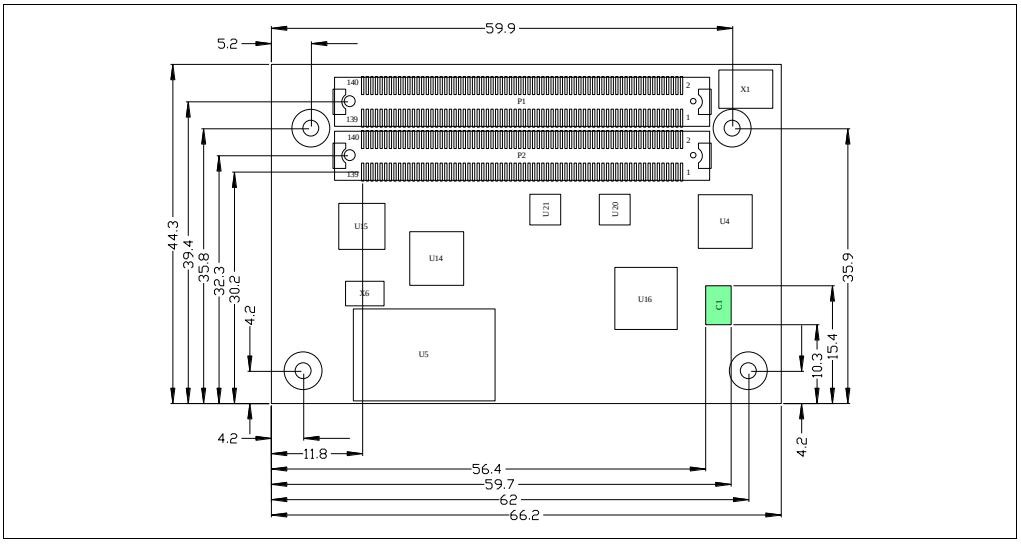


Figure 11 CM-X300 Bottom (X-Ray view – as aeen from the top side)



1. All dimensions are in millimeters
2. Height of all components except X5 and C1 is <2mm
3. The height of X5 is 2.5mm typ., of C1 is 2.0mm typ.
4. C1 is non-isolated, do not place components under C1 on the carrier board
5. CAMI connectors provide 4mm board-to-board clearance
6. Board thickness is 1.2mm

Mechanical drawings are available in DXF format from the CompuLab's website, following [Developer] >> [CM-X300] >> [CM-X300 - Dimensions and Connectors Location] links.

4.3 Baseboard Design Guidelines

Assure that all power pins are connected as specified in “Power” section of this manual. GND must be implemented by plane, rather than traces.

It is recommended to put several 100 nF and 10/100 uF capacitors between VBAT/VCHRG and GND near the mating connectors.

It is recommended to connect 3 out of the 4 standoff holes of the baseboard to GND, in order to improve EMC. The top right hole of the baseboard should be isolated, for compatibility with future CAMI modules (referring to module's orientation drawings).

Except of power connection, no other connection is mandatory for CM-X300 operation. All powerup electronics and all required pullups/pulldowns are found on the module.

If for some reason you decide to place external pullup or pulldown resistor on certain signal (for example - on GPIO's), check the documentation of that signal as provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.

You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:

- Ethernet and USB signals must be routed in differential pairs and by controlled impedance trace.
- Audio input must be decoupled from possible sources of baseboard noise.
- Local bus signals must be buffered in most cases.

Be careful when placing component under the CM-X300 module. CAMI connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-X300. In general, maximum allowable height for components placed under the CM-X300 is 2mm.

See the SB-X300 baseboard reference design schematics.

4.4 Baseboard Troubleshooting

Using grease solvent and soft brush, clean contacts of mating connectors of both module and baseboard. Remainders of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.

Using oscilloscope, check voltage levels and quality of VBAT and VCHRG power supplies. It should be as specified in “power” section. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of mating connector.

Using oscilloscope verify that GND pins of mating connector are indeed at zero voltage level, and there is no ground bouncing. Module must be plugged in during the test.

Create "minimum system" - only power, mating connectors, the module, and serial interface.

Check if the system starts properly. In system larger than minimum, the possible sources of disturbance could be:

- Devices improperly driving local bus
- External pullup/pulldown resistors overriding module’s on-board values, or any other components creating the same "overriding" effect.
- Bad power supply.

In order to avoid possible sources of disturbance, it is strongly recommended to start with minimal system and then add/activate off-board devices one by one.

Check for existence of soldering shorts between pins of mating connectors. Even if signals are not used on the baseboard, shorting them on the connectors can disable module's operation. Initial check can be performed using microscope. However, if microscope inspection finds nothing, it is advised to check using X-ray, because often solder bridges are deeply beneath the connector's body. Note that solder shorts are the most frequent factor disabling module's start.

Check possible signals shorting due to errors of baseboard PCB design or assembling.

Improper function of customer baseboard can accidentally delete bootup code from CM-X300, or even damage module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's SB-X300 baseboard.

It is recommended to assemble more that one baseboard for prototyping, in order to allow quick sorting out of problems related to specific board assembly.

5 OPERATING TEMPERATURE RANGES

The CM-X300 is available with three options of operating temperature range.

Table 52 CM-X300 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20^{o} to 70^{o} C	Every card undergoes short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every card is extensively tested for both lower and upper limits and at several midpoints.

6 POWER CONSUMPTION

Typical power consumption has been measured on module inserted into SB-X300 carrier board with no peripherials connected and 3.05V power source connected to the VBAT rail. Measurements do not include power drawn by the SB-X300 base board.

Table 53 CM-X300 Power Consumption (BT and Wi-Fi enabled)

Parameter	Value, mA	Note
I_{max}	470	Absolute maximum on CPU 100% load
I_{idle}	350	OS idle state average value
I_{susp}	16.5	Suspend mode typical value

In the following table the values are for the SW package which does not enable Bluetooth and Wireless Ethernet power supply.

Table 54 CM-X300 Power Consumption (BT and Wi-Fi disabled)

Parameter	Value, mA	Note
I_{max}	345	Absolute maximum on CPU 100% load
I_{idle}	185	OS idle state average value
I_{susp}	16.5	Suspend mode typical value