CM-T3530 CoM

Reference Guide

CompuLab

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Table 1   Revision Notes

Date	Description
November 2009	• First release
September 2010	• Fixed CM-T3530 block diagram on page 8 • Fixed signal function marking in the "Signal multiplexing" table on pages 32-33 • CM-T35 renamed into CM-T3530 • Fixed RS232 baud rate value • Fixed ADC_IN signal numbering • Fixed P1-42 and P2-42 description in the "GPIO availability" table on page 25 and in the "Signal multiplexing" table on pages 32-33
February 2011	• Removed USB host ports OHCI compliance • Added USB host ports low-speed and full-speed support note on page 18

Please check for a newer revision of this manual at CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1   INTRODUCTION

1.1   About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-T3530 Computer-on-Module.

1.2   CM-T3530 Part Number Legend

Please refer to the CompuLab website 'Prices' section to decode the CM-T3530 part number: http://www.compulab.co.il/t3530/html/t3530-cm-price.htm.

1.3   Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2   Related Documents

Document	Location
CM-T3530 Product Developer Resources	http://www.compulab.co.il/
OMAP35x Technical Reference Manual	http://www.ti.com/
TPS65930 Technical Reference Manual	http://www.ti.com/

2 OVERVIEW

2.1 Highlights

- Cortex-A8 OMAP3503 or OMAP3530 CPU, up to 720 MHz
- Up to 256 Mbyte mobile DDR
- Up to 512 Mbyte Flash Disk, including filesystem protection
- WLAN / WiFi 802.11b/g Interface
- Graphics controller supporting STN and TFT panels with 1400 x 1050 max resolution
- H.264, H.263, MPEG-4, MPEG-2, JPEG, WMV9 and additional video codecs implemented by IVA2.2 Subsystem using TMS320C64x+ DSP core @ 520 MHz
- PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support
- General purpose bus
- SDIO / MMC interface
- Camera Interface port
- Sound codec with speaker and microphone support
- Touchscreen Controller
- USB Slave / Host / OTG ports
- Serial ports, GPIO
- 100 Mbps Ethernet port
- Very low standby and active power consumption
- Tiny size: 66 x 44 x 7 mm
- Interchangeable with other modules via CAMI connectors
- SB-T35 - turns the CM-T3530 module into a tiny single board computer

The CM-T3530 is a small Computer-on-Module board designed to serve as a building block in embedded applications. The CM-T3530 has all the components required to run operating systems such as Linux and Windows CE. Ready packages for these operating systems are available from CompuLab.

The small size and low power consumption of the CM-T3530 allows its integration into hand-held and mobile devices, while its low price makes it an ideal selection for cost-sensitive applications. The CM-T3530 delivers a price / performance ratio significantly better than that of any other platform.

CM-T3530 is based on Texas Instruments OMAP3530 processor which combines two CPU cores in single package - an advanced Cortex-A8 ARM CPU for running operating system and application code, and TMS32064x DSP for dedicated video processing. Low voltage Mobile DDR enables very low power consumption in regular operation and in standby. For embedded applications, the CM-T3530 provides a general purpose local bus, 100Mbit Ethernet, serial ports, I/O lines and other essential functions, while integrated WiFi interface implement industry standard wireless connectivity.

The standardized CAMI ("CompuLab's Aggregated Module Interface") connectors of the CM-T3530 module allow interchangeability with other Computer-On-Module's available from CompuLab, enabling the flexibility required in a dynamic market where application requirements can change rapidly.

2.2   Block Diagram

Figure 1   CM-T3530 Block Diagram
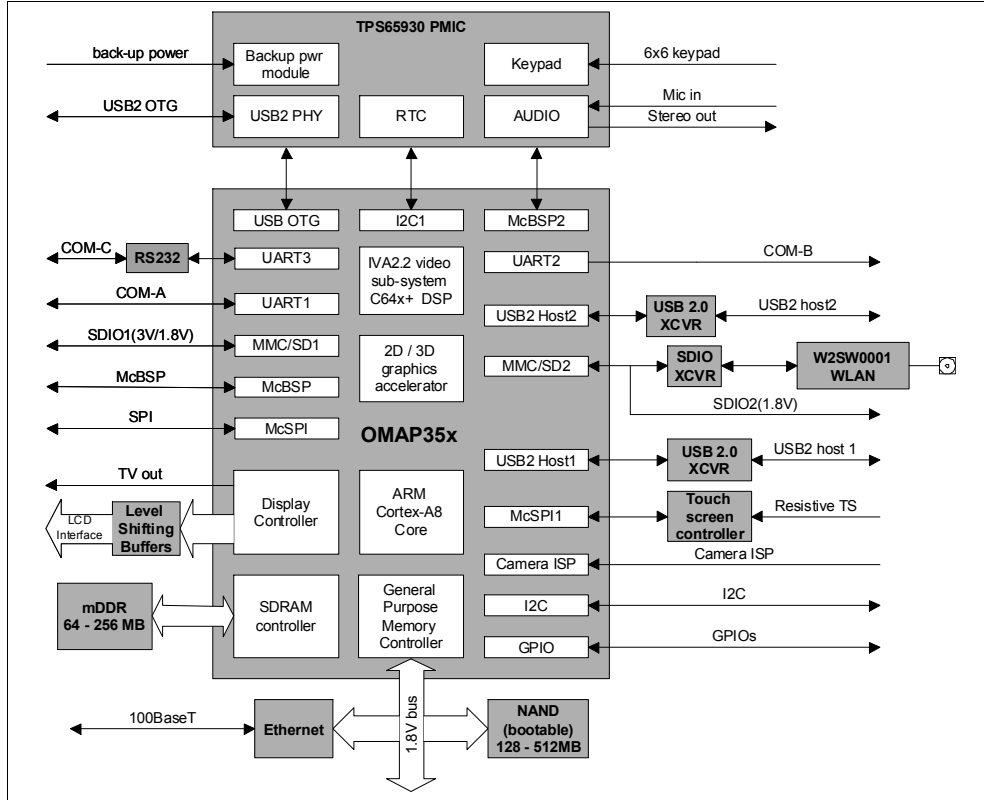
2.3   CM-T3530 Features

The "Option" column specifies the configuration code required to have the particular feature.
"+" means that the feature is always available.

Table 3   CPU, Memory and Busses

Feature	Specifications	Option
CPU	Texas Instruments OMAP3503 / OMAP3530 CPU 600 / 720 MHz, NEON™ SIMD Coprocessor L1 cache: 112 KB (DSP), 32 KB (ARM) L2 cache: 96 KB (DSP), 256 KB (ARM) DMA, Interrupt controllers, Timers	C
RAM	64 - 256 MB, Mobile DDR, 166 MHz, 32-bit	D
NAND Flash Disk	128 - 512 Mbytes, bootable	N
External local bus	16-bit, variable rate up to 133 MHz, 1.8V levels	+

Table 4   Peripherals

Feature	Specifications	Option
Graphics Controller	4/8/16/24 bit color, resolution up to 1400 x 1050, frame buffer in system DDR. Display types support : TFT (parallel RGB), STN, composite video - PAL / NTSC	+
Video acceleration	IVA2.2 Subsystem TMS320C64x+ DSP core running at rate up to 520 MHz. Supporting H.264, H.263, MPEG-4, MPEG-2, JPEG, WMV9 and additional codecs. Part of OMAP3530 CPU	C720M
2D / 3D graphics	PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support. Part of OMAP3530 CPU	C720M
Camera Interface	Direct camera sensor support, max resolution 4096 x 4096, pixel clock up to 130MHz. BT.601 / BT.656 Digital YCbCr 4:2:2 (8/16-Bit) interface.	+
USB	- Host / Slave (OTG) USB2 high-speed port, 480 Mbps - Additional two USB2 host ports, 480 Mbps, EHCI compliant	+ U
Serial Ports (UARTs)	3 UART ports, 16550 compatible: COM-A – 1.8V interface, partial modem controls, 3.6 Mbps COM-B – 1.8V interface, partial modem controls, 3.6 Mbps COM-C – RS232 interface, Rx / Tx only, 250 Kbps	+
General Purpose I/O	Up to 74 lines shared with other functions. Can also be used as interrupt inputs	+
Keyboard & mouse	USB, keypad or redirection from COM port	+
Ethernet	SMSC LAN9220 MAC & PHY, 10/100BaseT, Activity LED's	E
MMC / SD	MMC / SD / SDIO support including SDHC up to 32GB	+
Audio codec	I2S compliant audio codec, stereo output, differential mic input	+
Touchscreen ctrl.	TSC2046 touchscreen controller. Support 4-wire resistive panels	I
RTC	Real Time Clock, powered by external lithium battery	+
WiFi Interface	Implements 802.11b/g wireless connectivity standard Supports Node to Access Point and Multi-Node (w/o access point) methods of connection. (but cannot act as Access Point) Marvell 88W8686 802.11b/g chipset. On-board connector for external antenna.	W

Table 5   Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 3.8V or Lithium-ion polymer battery
Active power consumption	0.2 - 2 W, depending on configuration and CPU speed
Standby/Sleep consumption	20 - 100 mW, depending on configuration and mode
Dimensions	66 x 44 x 7 mm
Weight	16 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0º to 70º C Extended: -20º to 70º C Industrial: -40º to 85º C
Storage temperature	-40º to 85º C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)

Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 CORE SYSTEM COMPONENTS

3.1 OMAP35xx CPU

The OMAP35x family of high-performance application processors is based on the enhanced OMAP™ 3 architecture and is integrated on Texas Instruments' 65-nm process technology.

The architecture is designed to provide video, image, and graphics processing sufficient to support the following:

- Streaming video
- 2D/3D mobile gaming
- Video conferencing
- High-resolution still images
- Video capture in wireless terminals, multimedia-featured handsets, and high-performance personal digital assistants (PDA's).

This OMAP device includes power-management techniques required for high-performance mobile products.

The following subsystems are parts of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 microprocessor
- IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core
- SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects
- Camera image signal processor (ISP) supporting multiple formats and interfacing options to a wide variety of image sensors
- Display subsystem with multiple concurrent image manipulation support, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects that provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers a comprehensive power and clock-management scheme that enables high-performance, low-power operation and ultralow-power standby features. The device also supports SmartReflex™ adaptive voltage control.

Figure 2   OMAP35xx Block Diagram
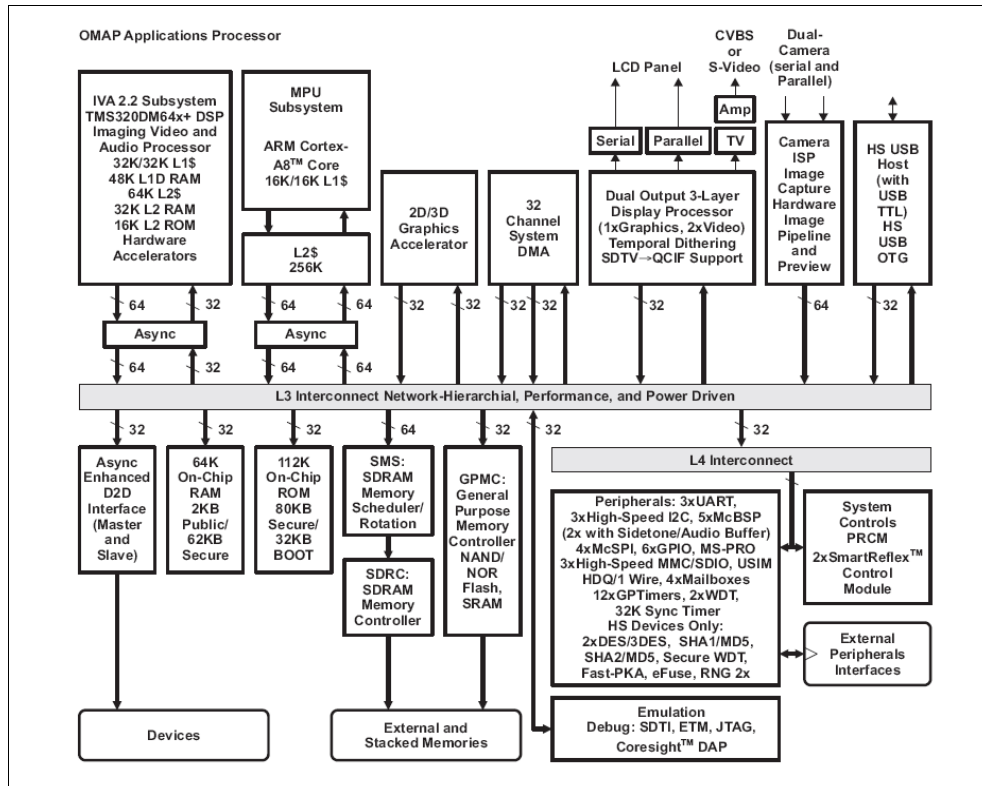
3.2   Multimedia System

3.2.1   IVA2.2 Subsystem

The OMAP35xx includes a high-performance imaging video and audio (IVA2.2) accelerator based on the Texas Instruments TMS320DMC64x+ VLIW DSP core.

For additional details, please refer to section 14 of the "OMAP35x Technical Reference Manual".

3.2.2   Multimedia Accelerator

The OMAP35xx 2D and 3D graphics accelerator (SGX) provides support for the following imaging and video features:

- 2D and 3D graphics and video codecs supported on common hardware
- Tile-based architecture
- An advanced shader feature set in excess of Microsoft VS3.0, PS3.0 and OGL2.0
- Industry standard API supports Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0 and OpenMax
- Fine-grained task switching, load balancing and power management
- Programmable high-quality image anti-aliasing
- Advanced geometry DMA driven operation for minimum CPU interaction
- Fully virtualized memory addressing for OS operation in a unified memory architecture
- Advanced and standard 2D operations (that is, vector graphics, BLT's, ROP's, etc.)
- Programmable video encode and decode support for H.264, H.263, MPEG4 (SP), WMV9 and JPEG

NOTE: Multimedia features are available only with the 'M' configuration option.

3.3   Memory

3.3.1   DRAM

The CM-T3530 board is assembled with 64, 128 or 256 Mbytes of mobile DDR. The DDR interface is 32-bits wide and runs with a 166 MHz clock.

3.3.2   NAND Flash

The CM-T3530 is assembled with 128 or 512 Mbytes of SLC NAND Flash.

The NAND Flash is the main non-volatile memory device of the CM-T3530, used for boot-loader, OS storage and flash disk implementation.

3.4   PMIC

The CM-T3530 features the TI TPS65930 companion chip for OMAP35xx power management and additional peripheral devices.

The TPS65930 is a power-management IC for OMAP™ and other mobile applications. The device includes power-management, a high-speed USB transceiver, LED drivers, an ADC, a real-time clock and embedded power control (EPC). In addition, the TPS65930 includes a full audio codec with two DAC's and two ADC's to implement dual voice channels, and a stereo downlink channel that can play all standard audio sample rates through a multiple format inter-integrated sound (I2S™) TDM interface.

The TPS65930 supports the power and peripheral requirements of the OMAP application processor. The power portion of the device contains three buck converters, two of which are controllable by a dedicated SmartReflex™ class-3 interface, multiple LDO regulators, an EPC to manage the power sequencing requirements of OMAP, an RTC and a backup module. The RTC can be powered by a backup battery when the main supply is not present, and the device includes a coin-cell charger to recharge the backup battery as needed.

4   PERIPHERAL INTERFACES

4.1   Local Bus

The CM-T3530 local bus is derived from the OMAP35xx general-purpose memory controller (GPMC) bus.

The GPMC is dedicated to interfacing with the following external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For additional details, please refer to section 11.1 of the "OMAP35x Technical Reference Manual".

NOTE: Local bus interface operates at 1.8V voltage levels.

Table 6   Local bus signals

Signal Name	Pin #	Type	Description
GPMC_A1	P1-71	O	Address bit 1
GPMC_A2	P1-70	O	Address bit 2
GPMC_A3	P1-73	O	Address bit 3
GPMC_A4	P1-72	O	Address bit 4
GPMC_A5	P1-75	O	Address bit 5
GPMC_A6	P1-76	O	Address bit 6
GPMC_A7	P1-77	O	Address bit 7
GPMC_A8	P1-78	O	Address bit 8
GPMC_A9	P1-81	O	Address bit 9
GPMC_A10	P1-80	O	Address bit 10
GPMC_D0	P1-94	IO	Data bit 0
GPMC_D1	P1-95	IO	Data bit 1
GPMC_D2	P1-96	IO	Data bit 2
GPMC_D3	P1-97	IO	Data bit 3
GPMC_D4	P1-100	IO	Data bit 4
GPMC_D5	P1-99	IO	Data bit 5
GPMC_D6	P1-102	IO	Data bit 6
GPMC_D7	P1-101	IO	Data bit 7
GPMC_D8	P1-104	IO	Data bit 8
GPMC_D9	P1-105	IO	Data bit 9
GPMC_D10	P1-106	IO	Data bit 10
GPMC_D11	P1-107	IO	Data bit 11
GPMC_D12	P1-108	IO	Data bit 12
GPMC_D13	P1-109	IO	Data bit 13
GPMC_D14	P1-112	IO	Data bit 14
GPMC_D15	P1-111	IO	Data bit 15
GPMC_nCS3	P1-92	O	Chip select bit 3
GPMC_nCS4	P1-93	O	Chip select bit 4
GPMC_nCS7	P1-85	O	Chip select bit 7
GPMC_IODIR		O	IO direction control for use with external transceivers
GPMC_CLK	P1-88	O	Clock
GPMC_nADV	P1-90	O	Address valid
GPMC_nOE	P1-89	O	Output enable
GPMC_nWE	P1-84	O	Write enable
GPMC_nBE0	P1-82	O	Lower byte enable

GPMC_nBE1	P1-87	O	Upper byte enable
GPMC_WAIT3	P1-83	I	External indication of wait

4.2   Display Interface

The CM-T3530 display subsystem is based on the display interface of the OMAP35xx.

The display subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on either a liquid-crystal display (LCD) panel or a TV set.

The display subsystem supports the following main features:

Display controller

- Programmable pixel display modes (1, 2, 4, 8, 12, 16 and 24 bits-per-pixel)
- Programmable panel size up to 2048 (lines) x 2048 (pixels)
- 256 x 24-bit entries palette in red, green and blue (RGB)
- Programmable pixel rate up to 75 MHz
- Four types of displays are supported: passive (STN) and active (TFT) colors, passive (STN) and active (TFT) monochromes
- Overlay support for graphics
- Programmable video re-sizer independent horizontal and vertical re-sampling
- Rotation of 90-, 180- and 270-degrees

Video encoder

- NTSC/PAL encoder outputs with the following standards:
  - NTSC-J, M
  - PAL-B, D, G, H, I
  - PAL-M
  - CGMS-A as described in the CEA-608-x standard
- Composite video (CVBS)
- Separate video (S-video)

For additional details, please refer to section 15 of the "OMAP35x Technical Reference Manual".

The LCD_VIO pin supplies power to the LCD interface, allowing configuring the operating voltage level of the LCD interface signals. The operating voltage can be set to 1.8V, 2.5V or 3.3V.

NOTE: The operating voltage level of the LCD interface is configured according to the LCD_VIO pin input voltage.

Table 7   Display interface signals

Signal Name	Pin #	Type	Description
			LCD interface
LCD_PCLK	P2-112	O	Pixel clock
LCD_HSYNC	P2-96	O	Horizontal synchronization
LCD_VSYNC	P2-111	O	Vertical synchronization
LCD_ACBIAS	P2-114	O	AC bias control (STN) or pixel data enable (TFT)
LCD_D0	P2-95	O	Pixel data bit 0
LCD_D1	P2-97	O	Pixel data bit 1
LCD_D2	P2-100	O	Pixel data bit 2
LCD_D3	P2-99	O	Pixel data bit 3
LCD_D4	P2-102	O	Pixel data bit 4

LCD_D5	P2-101	O	Pixel data bit 5
LCD_D6	P2-104	O	Pixel data bit 6
LCD_D7	P2-106	O	Pixel data bit 7
LCD_D8	P2-105	O	Pixel data bit 8
LCD_D9	P2-108	O	Pixel data bit 9
LCD_D10	P2-107	O	Pixel data bit 10
LCD_D11	P2-109	O	Pixel data bit 11
LCD_D12	P2-113	O	Pixel data bit 12
LCD_D13	P2-116	O	Pixel data bit 13
LCD_D14	P2-118	O	Pixel data bit 14
LCD_D15	P2-117	O	Pixel data bit 15
LCD_D16	P2-120	O	Pixel data bit 16
LCD_D17	P2-119	O	Pixel data bit 17
LCD_D18	P2-124	O	Pixel data bit 18
LCD_D19	P2-121	O	Pixel data bit 19
LCD_D20	P2-126	O	Pixel data bit 20
LCD_D21	P2-123	O	Pixel data bit 21
LCD_D22	P2-94	O	Pixel data bit 22
LCD_D23	P2-93	O	Pixel data bit 23
LCD_VIO	P2-16	P	Power supply input for LCD interface. Connect to 1.8V / 2.5V / 3.3V power rail. The power source must provide 150mA continuous current.
Video encoder			
TV_OUT1	P2-1	O	TV analog output composite
TV_OUT1	P2-3	O	TV analog output S-VIDEO

4.3   Ethernet

The CM-T3530 incorporates a single full-featured 10/100 Ethernet interface, implemented with the SMSC LAN9220 Ethernet controller.

The CM-T3530 Ethernet interface supports the following main features:

- Fully compliant with IEEE 802.3/802.3u standards
- 10BASE-T and 100BASE-TX
- Full- and Half-duplex
- HP Auto-MDIX
- Activity and speed indicator LED controls

Table 8   Ethernet interface signals

Signal Name	Pin #	Type	Description
CM_ETH_TXP	P1-1	AO	Transmit positive output
CM_ETH_TXN	P1-3	AO	Transmit negative output
CM_ETH_RXP	P1-4	AI	Receive positive input
CM_ETH_RXN	P1-2	AI	Receive negative input
CM_ETH_LED1	P1-6	OD	Activity indicator LED output. Active low.
CM_ETH_LED2	P1-5	OD	Speed indicator LED output. Active (100Mbs) low.

NOTE: For magnetics' selection recommendations, please refer to section 8.3 of this document.

4.4   USB 2.0

4.4.1   USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the OMAP35xx USB 2.0 OTG controller. The interface provides the following features:

- Supports USB 2.0 peripheral at High Speed (480 Mbps) and Full Speed (12 Mbps)

- Supports USB 2.0 host at High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps)

- Operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multipoint communications with other USB functions

- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the on-the-go (OTG) supplement (Revision 1.0a)

Table 9   USB 2.0 OTG interface signals

Signal Name	Pin #	Type	Description
USB0_DP	P1-136	AOI	USB OTG positive data
USB0_DN	P1-138	AOI	USB OTG negative data
USB0_ID	P1-137	AI	USB OTG ID
USB0_5V_OUT	P1-140	P	USB OTG VBUS power rail

4.4.2   USB 2.0 Host

The CM-T3530 high-speed USB interface is implemented with the OMAP35xx high-speed USB host subsystem. The interface provides the following features:

- Complies with the USB 2.0 standard for high-speed (480M bit/s) functions

- Complies with EHCI (high-speed host controller)

Two high-speed USB host ports are supported.

NOTE: The USB 2.0 host ports do not support low-speed and full-speed operation modes. External USB hub is recommended in order to enable these operation modes. Please refer to the SB-T35 design package for a comprehensive reference design.

NOTE: The USB 2.0 host ports are available only with the 'U' configuration option.

Table 10   USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description
			USB-1
USB1_DP	P2-138	AOI	USB host port 1 positive data
USB1_DN	P2-140	AOI	USB host port 1 negative data
USB1_CPEN	P2-6	AI	USB host port 1 external 5V supply enable. Active high.
USB1_VBUS	P2-8	AOI	USB host port 1 external 5V supply sense input.
			USB-2
USB2_DP	P2-137	AOI	USB host port 2 positive data
USB2_DN	P2-139	AOI	USB host port 2 negative data
USB2_CPEN	P2-9	AI	USB host port 2 external 5V supply enable. Active high.
USB2_VBUS	P2-11	AOI	USB host port 1 external 5V supply sense input.

4.5   WLAN

The CM-T3530 incorporates full-featured 802.11 b/g capabilities, implemented with the Wi2Wi W2SW0001 WLAN controller module. The W2SW0001 is a complete IEEE 802.11b/g solution based on the Marvell 88W8686 chipset.

Security features:

- WEP encryption (64 bit/128 bit)
- WPA TKIP security
- WPA2

The W2SW0001 is connected to the OMAP35xx SoC via the MMC-2 port.

Antenna Connection

The W2SW0001 requires a single 2.45GHz antenna. The antenna is connected via the onboard UFL high frequency connector J1. Any type of 2.45GHz WLAN antenna can be used. Please refer to section 6.3 for connector location.

Table 11   J1 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 12   802.11b RF system specifications

Parameter	Test Condition	Typical Value	Units
Transmit Power Output		15	dBm
Receive Sensitivity	1 Mbps, 8% PER	-87	dBm
	2 Mbps, 8% PER	-87	dBm
	5.5 Mbps, 8% PER	-87	dBm
	11 Mbps, 8% PER	-85	dBm
Maximum Receive Level	PER<8%	IEEE Compliant	dBm
Transmit Frequency Offset	Low, Middle, High Channels	±10	PPM
Spectral Mask	Max. TX Power	-40@fc±11MHz	dBc
		-60@fc±22MHz	
Error Vector Magnitude	Max. TX Power @ 11Mbps	-36	dB
Carrier Suppression	Max. TX Power	-25	dBc
Adjacent Channel Rejection	Desired channel is 3dB above sensitivity, 11Mbps, PER<8%	48	dBc

Table 13   802.11g RF system specifications

Parameter	Test Condition	Typical Value	Units
Transmit Power Output		15	dBm
Receive Sensitivity	6 Mbps, 10% PER	-86	dBm
	9 Mbps, 10% PER	-85	dBm
	12 Mbps, 10% PER	-85	dBm
	18 Mbps, 10% PER	-84	dBm
	24 Mbps, 10% PER	-80	dBm
	36 Mbps, 10% PER	-77	dBm
	48 Mbps, 10% PER	-73	dBm
	54 Mbps, 10% PER	-72	dBm
Maximum Receive Level	PER<10%	IEEE Compliant	dBm
Transmit Frequency Offset	Low, Middle, High Channels	±10	PPM
Spectral Mask	Max. TX Power	-30@fc±11MHz	dBc
		-40@fc±20MHz	
		-50@fc±30MHz	
Error Vector Magnitude	Max. TX Power @ 11Mbps	-29	dB
Carrier Suppression	Max. TX Power	-25	dBc
Adjacent Channel Rejection	Desired channel is 3dB above sensitivity, 11Mbps, PER<8%	15	dBc

4.6 Audio

The CM-T3530 audio subsystem is implemented with the audio codec of the TI TPS65930 companion chip. The audio subsystem supports the following features:

- External class-D amplifier pre-driver stereo output
- Differential microphone input
- Single-ended auxiliary input

Table 14   Audio signals

Signal Name	Pin #	Type	Description
AUDIO_OUT_R	P2-136	AO	Pre-driver output right for external class-D amplifier
AUDIO_OUT_L	P2-130	AO	Pre-driver output left for external class-D amplifier
AUDIO_IN	P2-128	AI	Auxiliary audio input
MIC_IN_P	P2-131	AI	Differential microphone positive input
MIC_IN_N	P2-133	AI	Differential microphone negative input
MIC_BIAS	P2-129	P	Microphone bias
AGND	P2-125 P2-132	P	Dedicated analog audio ground

4.7 UART's

The CM-T3530 incorporates two general purpose UART's. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 3.6M bit/s
- Configurable data format

NOTE: UART ports operate at 1.8V voltage levels.

NOTE: UART signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 15   UART signals

Signal Name	Pin #	Type	Description
UART-1			
UART1_TX	P1-24	O	UART1 serial data out
UART1_RX	P1-22	I	UART1 serial data in
UART1_CTS	P1-27	I	UART1 clear to send
UART1_RTS	P1-29	O	UART1 request to send
UART-2			
UART2_TX	P1-32	O	UART2 serial data out
UART2_RX	P1-34	I	UART2 serial data in
UART2_CTS	P1-33	I	UART2 clear to send
UART2_RTS	P1-35	O	UART2 request to send

4.8   RS232

The CM-T3530 incorporates a single RS232 port. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 250 kbit/s
- Configurable data format
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART3 of the OMAP35xx SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

Table 16   RS232 signals

Signal Name	Pin #	Type	Description
RS232_TXD	P1-30	O	RS232 serial data out
RS232_RXD	P1-28	I	RS232 serial data in

4.9   MMC / SD / SDIO

The CM-T3530 features two multimedia card high-speed/secure data/secure digital I/O (MMC / SD / SDIO) host interfaces. The following main features are supported:

- Full compliance with MMC command/response sets as defined in the Multimedia Card System Specification, v4.2. including high-capacity (size >2GB) cards HC MMC.
- Full compliance with SD command/response sets as defined in the SD Memory Card Specifications, v2.0. including high-capacity cards SDHC up to 32 GB.
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10
- Compliance with sets as defined in the SD Card Specification, Part A2, SD Host Controller Standard Specification, v1.00
- Full compliance with MMC bus testing procedure as defined in the Multimedia Card System Specification, v4.2
- Full compliance with CE-ATA command/response sets as defined in the CE-ATA Standard Specification

Each MMC/SD/SDIO host controller can support one MMC memory card, one SD memory card or one SDIO card. Other combinations (for example, two SD cards, one MMC card, and one SD card) are not supported through a single controller.

The first controller (MMC-1) integrates an internal transceiver that allows a direct connection to the MMC/SD/SDIO card (1.8 and 3V) without an external transceiver. The software-controlled VCC_MMC power output pin allows setting the proper operating voltage.

The second controller (MMC-2) allows connecting MMC/SD/SDIO (only 1.8V) cards or an external device that uses the MMC/SD/SDIO interface (a WLAN device for example). The second instance also supports an external transceiver and provides direction signals for data and command. Using an external transceiver device precludes 8-bit transfer mode.

For additional details, please refer to section 22 of the "OMAP35x Technical Reference Manual".

Certain MMC/SD/SDIO signals are multiplexed with signals used for other on-board functional modules. The following table summarizes availability of the MMC/SD/SDIO ports:

Table 17   MMC / SD / SDIO port availability

CM-T3530 port	OMAP35xx port	Availability
MMC-1	MMC-1	Always available.
MMC-2	MMC-2	Only available **without** 'W' option.

NOTE: MMC/SD/SDIO signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 18   MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description
MMC-1			
MMC1_CLK	P1-12	O	Output clock
MMC1_CMD	P1-13	IO	Command signal
MMC1_DAT0	P1-15	IO	Card data bit 0 / SPI serial input
MMC1_DAT1	P1-16	IO	Card data bit 1
MMC1_DAT2	P2-4	IO	Card data bit 2
MMC1_DAT3	P1-18	IO	Card data bit 3
MMC1_DAT4	P1-9	IO	Card data bit 4
MMC1_DAT5	P1-17	IO	Card data bit 5
MMC1_DAT6	P1-21	IO	Card data bit 6
MMC1_DAT7	P1-23	IO	Card data bit 7
MMC1_CD	P1-25	I	Card detection. Pulled-up to 1.8V.
VCC_MMC	P1-10	P	MMC1 dedicated LDO output. Configurable voltage (1.8V/3.3V)
MMC-2			
MMC2_CLK	P1-48	O	Output clock
MMC2_CMD	P1-41	IO	Command signal
MMC2_DAT0	P1-46	IO	Card data bit 0 / SPI serial input
MMC2_DAT1	P1-47	IO	Card data bit 1
MMC2_DAT2	P1-52	IO	Card data bit 2
MMC2_DAT3	P149	IO	Card data bit 3
MMC2_DAT4	P1-54	IO	Card data bit 4
MMC2_DAT5	P1-39	IO	Card data bit 5
MMC2_DAT6	P1-56	IO	Card data bit 6
MMC2_DAT7	P1-45	IO	Card data bit 7

4.10   Touch-Screen

The CM-T3530 features a resistive touch-screen interface. The interface supports 4-wire touch panels.

Table 19   Touch-screen signals

Signal Name	Pin #	Type	Description
TS_X+	P1-53	AI	Touch screen X+ (right)
TS_X-	P1-57	AI	Touch screen X- (left)
TS_Y+	P2-71	AI	Touch screen Y+ (top)
TS_Y-	P2-73	AI	Touch screen Y- (bottom)

4.11   Keypad

The CM-T3530 features a 6x6 matrix keypad interface derived from the keypad controller of the TI TPS65930 companion chip. The keypad controller implements a built-in scanning algorithm to decode hardware-based key presses and to reduce software overhead.

Figure 3   Keypad connection
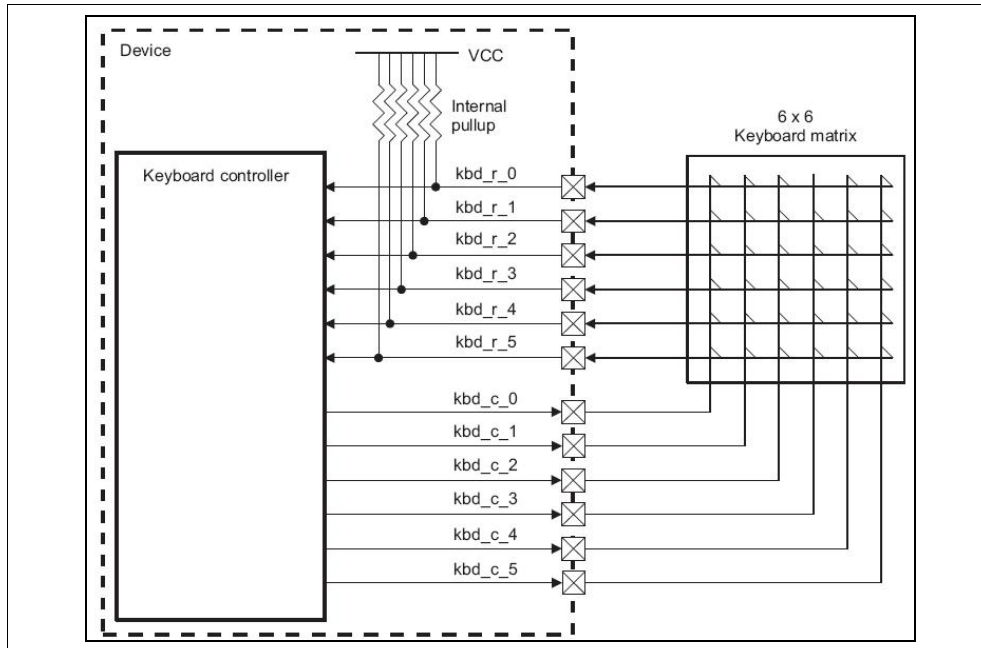
Table 20   Keypad signals

Signal Name	Pin #	Type	Description
KPD_R0	P2-48	I	Matrix key row input 0
KPD_R1	P2-52	I	Matrix key row input 1
KPD_R2	P2-54	I	Matrix key row input 2
KPD_R3	P2-56	I	Matrix key row input 3
KPD_R4	P2-68	I	Matrix key row input 4
KPD_R5	P2-60	I	Matrix key row input 5
KPD_C0	P2-53	OD	Matrix key column scan output 0
KPD_C1	P2-57	OD	Matrix key column scan output 1
KPD_C2	P2-59	OD	Matrix key column scan output 2
KPD_C3	P2-61	OD	Matrix key column scan output 3
KPD_C4	P2-63	OD	Matrix key column scan output 4
KPD_C5	P2-65	OD	Matrix key column scan output 5

4.12   GPIO

The CM-T3530 provides up to 74 GPIO signals. These signals can be configured for the following applications:

- Data input / output
- Keyboard interface with a debounce cell
- Interrupt generation
- Wake-up request

For additional details, please refer to section 24 of the "OMAP35x Technical Reference Manual".

NOTE: GPIO signals operate at 1.8V voltage levels.

NOTE: GPIO signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Most GPIO signals are multiplexed with signals used for other on-board functional modules. The following table summarizes the availability of the GPIO's:

Table 21   GPIO availability

CM-T3530 signal	OMAP35xx signal	Availability
P1-133	GPIO_10	Available with all configurations.
P2-18	GPIO_11	Available with all configurations. Muxed with JTAG.
P1-123	GPIO_12	Only available **without** 'U' option. Muxed with McBSP-5.
P1-125	GPIO_13	Only available **without** 'U' option.
P1-128	GPIO_14	Only available **without** 'U' option.
P1-119	GPIO_15	Only available **without** 'U' option.
P1-130	GPIO_16	Only available **without** 'U' option.
P1-120	GPIO_18	Only available **without** 'U' option. Muxed with McBSP-5.
P1-124	GPIO_19	Only available **without** 'U' option. Muxed with McBSP-5.
P1-126	GPIO_20	Only available **without** 'U' option. Muxed with McBSP-5.
P1-121	GPIO_21	Only available **without** 'U' option.
P1-117	GPIO_23	Only available **without** 'U' option.
P2-20	GPIO_31	Available with all configurations. Muxed with JTAG.
P1-92	GPIO_54	Available with all configurations. Muxed with local bus controls.
P1-93	GPIO_55	Available with all configurations. Muxed with local bus controls.
P1-85	GPIO_58	Available with all configurations. Muxed with local bus controls.
P1-88	GPIO_59	Available with all configurations. Muxed with local bus controls.
P1-87	GPIO_61	Available with all configurations. Muxed with local bus controls.
P1-83	GPIO_65	Available with all configurations. Muxed with local bus controls.
P2-80	GPIO_94	Available with all configurations. Muxed with camera interface.
P2-68	GPIO_95	Available with all configurations. Muxed with camera interface.
P2-72	GPIO_96	Available with all configurations. Muxed with camera interface.
P2-77	GPIO_97	Available with all configurations. Muxed with camera interface.
P2-78	GPIO_98	Available with all configurations. Muxed with camera interface.
P2-81	GPIO_99	Available with all configurations. Muxed with camera interface.
P2-82	GPIO_100	Available with all configurations. Muxed with camera interface.
P2-83	GPIO_101	Available with all configurations. Muxed with camera interface.
P2-84	GPIO_102	Available with all configurations. Muxed with camera interface.
P2-85	GPIO_103	Available with all configurations. Muxed with camera interface.
P2-88	GPIO_104	Available with all configurations. Muxed with camera interface.
P2-87	GPIO_105	Available with all configurations. Muxed with camera interface.
P2-90	GPIO_106	Available with all configurations. Muxed with camera interface.
P2-89	GPIO_107	Available with all configurations. Muxed with camera interface.
P2-92	GPIO_108	Available with all configurations. Muxed with camera interface.
P2-69	GPIO_109	Available with all configurations. Muxed with camera interface.
P2-66	GPIO_110	Available with all configurations. Muxed with camera interface.

CM-T3530 signal	OMAP35xx signal	Availability
P2-76	GPIO_111	Available with all configurations. Muxed with camera interface.
P2-75	GPIO_126	Available with all configurations. Muxed with camera interface.
P1-48	GPIO_130	Only available **without** 'W' option. Muxed with MMC-2, SPI-3.
P1-41	GPIO_131	Only available **without** 'W' option. Muxed with MMC-2, SPI-3.
P1-46	GPIO_132	Only available **without** 'W' option. Muxed with MMC-2, SPI-3.
P1-47	GPIO_133	Only available **without** 'W' option. Muxed with MMC-2.
P1-52	GPIO_134	Only available **without** 'W' option. Muxed with MMC-2, SPI-3.
P1-49	GPIO_135	Only available **without** 'W' option. Muxed with MMC-2, SPI-3.
P1-54	GPIO_136	Only available **without** 'W' option. Muxed with MMC-2.
P1-39	GPIO_137	Only available **without** 'W' option. Muxed with MMC-2.
P1-56	GPIO_138	Only available **without** 'W' option. Muxed with MMC-2.
P1-45	GPIO_139	Only available **without** 'W' option. Muxed with MMC-2.
P1-33	GPIO_140	Available with all configurations. Muxed with UART-2, McBSP-2.
P1-35	GPIO_141	Available with all configurations. Muxed with UART-2, McBSP-2.
P1-32	GPIO_142	Available with all configurations. Muxed with UART-2, McBSP-2.
P1-34	GPIO_143	Available with all configurations. Muxed with UART-2, McBSP-2.
P1-24	GPIO_148	Available with all configurations. Muxed with UART-1.
P1-29	GPIO_149	Available with all configurations. Muxed with UART-1.
P1-27	GPIO_150	Available with all configurations. Muxed with UART-1.
P1-22	GPIO_151	Available with all configurations. Muxed with UART-1.
P2-28	GPIO_156	Available with all configurations. Muxed with SPI-4, McBSP-1.
P2-30	GPIO_157	Available with all configurations. Muxed with McBSP-1.
P2-32	GPIO_158	Available with all configurations. Muxed with SPI-4, McBSP-1.
P2-34	GPIO_159	Available with all configurations. Muxed with SPI-4, McBSP-1.
P2-27	GPIO_161	Available with all configurations. Muxed with SPI-4, McBSP-1.
P2-29	GPIO_162	Available with all configurations. Muxed with McBSP-1.
P1-42	GPIO_164	Available with all configurations.
P2-70	GPIO_167	Available with all configurations. Muxed with camera interface.
P1-61	GPIO_168	Available with all configurations. Muxed with I2C-2.
P1-36	GPIO_170	Available with all configurations. Muxed with HDQ/1-Wire.
P2-45	GPIO_178	Only available **without** 'U' option. Muxed with SPI-2.
P2-39	GPIO_179	Only available **without** 'U' option. Muxed with SPI-2.
P2-49	GPIO_180	Only available **without** 'U' option. Muxed with SPI-2.
P2-47	GPIO_181	Only available **without** 'U' option. Muxed with SPI-2.
P2-37	GPIO_182	Only available **without** 'U' option. Muxed with SPI-2.
P1-60	GPIO_183	Available with all configurations. Muxed with I2C-2.
P1-63	GPIO_184	Available with all configurations. Muxed with I2C-3.
P1-64	GPIO_185	Available with all configurations. Muxed with I2C-3.

4.13   Camera Interface

The camera interface is implemented with the camera sub-system (ISP) of the OMAP35x SoC. The camera ISP provides the system interface and the processing capability to connect RAW image-sensor modules to the CM-T3530. For additional details, please refer to section 12 of the "OMAP35x Technical Reference Manual".

NOTE: The camera interface operates at 1.8V voltage levels.

Table 22   Camera interface signals

Signal Name	Pin #	Type	Description
CAM_PCLK	P2-77	I	Parallel interface pixel clock
CAM_HS	P2-80	IO	Line trigger input/output signal
CAM_VS	P2-68	IO	Frame trigger input/output signal
CAM_STROBE	P2-75	O	Flash strobe control signal
CAM_FLD	P2-78	IO	Field identification input/output signal
CAM_WEN	P2-70	I	External write-enable signal
CAM_XCLKA	P2-72	O	External clock for the image-sensor module
CAM_XCLKB	P2-76	O	External clock for the image-sensor module
CAM_D0	P2-81	I	Parallel input data line 0
CAM_D1	P2-82	I	Parallel input data line 1

CAM_D2	P2-83	I	Parallel input data line 2
CAM_D3	P2-84	I	Parallel input data line 3
CAM_D4	P2-85	I	Parallel input data line 4
CAM_D5	P2-88	I	Parallel input data line 5
CAM_D6	P2-87	I	Parallel input data line 6
CAM_D7	P2-90	I	Parallel input data line 7
CAM_D8	P2-89	I	Parallel input data line 8
CAM_D9	P2-92	I	Parallel input data line 9
CAM_D10	P2-69	I	Parallel input data line 10
CAM_D11	P2-66	I	Parallel input data line 11

4.14 I^2C

The CM-T3530 features two general purpose high speed I^2C interfaces. The following features are supported:

- Compliance with Philips I^2C specification version 2.1
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Support for HS mode for transfer up to 3.4M bits/s

The I^2C interfaces are implemented with the I^2C-2 and I^2C-3 controller modules of the OMAP35x SoC.

NOTE: I^2C interfaces operate at 1.8V voltage levels.

Table 23 I^2C signals

Signal Name	Pin #	Type	Description
I^2C-2			
I2C2_SDA	P1-60	IOD	I2C serial data line. Open drain buffer. Pulled up to 1.8V
I2C2_SCL	P1-61	IOD	I2C serial clock line. Open drain buffer. Pulled up to 1.8V
I^2C-3			
I2C3_SDA	P1-64	IOD	I2C serial data line. Open drain buffer. Pulled up to 1.8V
I2C3_SCL	P1-63	IOD	I2C serial clock line. Open drain buffer. Pulled up to 1.8V

4.15 SPI

CM-T3530 features three multi-channel serial port interfaces (SPI). The following main features are supported:

- Serial clock with programmable frequency, polarity and phase for each channel
- A wide selection of SPI word lengths ranging from 4 bits to 32 bits

Certain SPI signals are multiplexed with signals used for other on-board functional modules. The following table summarizes availability of the SPI ports:

Table 24 SPI port availability

CM-T3530 port	OMAP35xx port	Availability
SPI-2	SPI-2	Only available **without** 'U' option
SPI-3	SPI-3	Only available **without** 'W' option
SPI-4	SPI-4	Always available

NOTE: SPI interfaces operate at 1.8V voltage levels.

NOTE: SPI signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 25   SPI signals

Signal Name	Pin #	Type	Description
SPI-2			
SPI2_CLK	P2-45	IO	Serial clock
SPI2_CS0	P2-47	IO	Chip select 0
SPI2_CS1	P2-37	O	Chip select 1
SPI2_SIMO	P2-39	IO	Serial data master out
SPI2_SOMI	P2-49	IO	Serial data master input
SPI-3			
SPI3_CLK	P1-48	IO	Serial clock
SPI3_CS0	P1-49	IO	Chip select 0
SPI3_CS1	P1-52	O	Chip select 1
SPI3_SIMO	P1-41	IO	Serial data master out
SPI3_SOMI	P1-46	IO	Serial data master input
SPI-4			
SPI4_CLK	P2-28	IO	Serial clock
SPI4_CS0	P2-27	IO	Chip select 0
SPI4_SIMO	P2-32	IO	Serial data master out
SPI4_SOMI	P2-34	IO	Serial data master input

4.16   McBSP

The CM-T3530 features three multi-channel buffered serial port (McBSP) interfaces. The following main features are supported:

- L4 interconnect slave interface supporting:
  - 32-bit data bus width
  - 32-bit access supported
  - 16- /8-bit access not supported
  - 10-bit address bus width
  - Write non-posted transaction mode supported
- 128 x 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Interrupts configurable in legacy mode (2 requests) or PRCM compliant (1 request)
- Transmit and receive DMA requests triggered with programmable FIFO thresholds

For additional details, please refer to section 21 of the "OMAP35x Technical Reference Manual".

Certain McBSP signals are multiplexed with signals used for other on-board functional modules. The following table summarizes availability of the McBSP ports:

Table 26   McBSP port availability

CM-T3530 port	OMAP35xx port	Availability
McBSP-1	McBSP-1	Always available
McBSP-3	McBSP-3	Always available
McBSP-5	McBSP-5	Only available **without** 'U' option

NOTE: McBSP interfaces operate at 1.8V voltage levels.

NOTE: McBSP signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 27   McBSP signals

Signal Name	Pin #	Type	Description
McBSP-1			
McBSP1_DR	P2-34	I	Received serial data
McBSP1_CLKR	P2-28	IO	Receive Clock
McBSP1_FSR	P2-30	IO	Receive frame synchronization
McBSP1_DX	P2-32	IO	Transmitted serial data
McBSP1_CLKX	P2-29	IO	Transmit clock
McBSP1_FSX	P2-27	IO	Transmit frame synchronization
McBSP-3			
McBSP3_DR	P1-35	I	Received serial data
McBSP3_DX	P1-33	IO	Transmitted serial data
McBSP3_CLKX	P1-32	IO	Transmit clock
McBSP3_FSX	P1-34	IO	Transmit frame synchronization
McBSP-5			
McBSP5_DR	P1-120	I	Received serial data
McBSP5_DX	P1-126	IO	Transmitted serial data
McBSP5_CLKX	P1-123	IO	Transmit clock
McBSP5_FSX	P1-124	IO	Transmit frame synchronization

4.17   HDQ / 1-Wire

The HDQ/1-Wire interface implements the hardware protocol of the master functions of the Benchmark HDQ and the Dallas Semiconductor 1-Wire® protocols.

The following main features are supported:

- Benchmark HDQ protocol
- Dallas Semiconductor 1-Wire® protocol
- Power-down mode

NOTE: HDQ/1-Wire interface operates at 1.8V voltage levels.

Table 28   HDQ / 1-Wire signals

Signal Name	Pin #	Type	Description
HDQ_SIO	P1-36	IO	Serial data input/output

4.18   JTAG

The CM-T3530 JTAG interface is derived from the OMAP35xx SoC JTAG port.

The OMAP35x target debug interface uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI and TDO), a return clock (RTCK) to meet the clocking requirements of the ARM968 processor and the two instrumentations pins (EMU0 and EMU1).

For additional details, please refer to section 25.6 of the "OMAP35x Technical Reference Manual".

NOTE: The JTAG interface operates at 1.8V voltage levels.

Table 29 JTAG signals

Signal Name	Pin #	Type	Description
JTAG_TCK	P2-24	I	Test clock
JTAG_TDO	P2-17	O	Test data output
JTAG_TDI	P2-21	I	Test data input
JTAG_TMS	P2-23	IO	Test mode select
JTAG_nTRST	P2-25	I	Test logic reset
JTAG_RTCK	P2-22	O	Returned test clock
JTAG_EMU0	P2-18	IO	Channel 0 trigger
JTAG_EMU1	P2-20	IO	Channel 1 trigger

5 SYSTEM LOGIC

5.1 Power Management

5.1.1 Power Rails

The CM-T3530 supports two power supply options:

- Regulated DC 3.8V
- Lithium-ion polymer battery

The CM-T3530 does not feature an onboard Lithium-ion polymer battery charger. If required, such a charger must be implemented on the baseboard.

Table 30 Power signals

Signal Name	Type	Description
VCC_CM	P	Main power supply. Typical voltage – 3.8V.
BKBAT	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave unconnected if RTC back-up is not required.
GND	P	Common ground.

5.1.2 Low Power Mode

To be added in a future revision of this document.

5.2 Reset

CM-T3530 supports two reset signals: cold reset (nRST_IN) and warm reset (SYS_nRESWARM).

Cold reset is generated at power up by the TPS65930 companion chip to reset the full logic of the CM-T3530. Cold reset is a global reset that affects every module on the device. nRST_IN assertion also causes SYS_nRESWARM assertion.

Warm reset is also a global reset, but it does not affect all the modules on the device. Usually, the device does not require a complete reboot on a warm reset.

The nRST_IN signal should be used as the main system reset.

For additional details, please refer to section 4 of the "OMAP35x Technical Reference Manual".

Table 31 Reset signals

Signal Name	Pin #	Type	Description
nRST_IN	P1-11	IOD	Cold reset. Active low. Pulled up to 1.8V.
SYS_nRESWARM	P1-116	IOD	Warm reset. Active low. Pulled up to 1.8V.

5.3 Boot Options

The CM-T3530 supports two boot sequences providing the following boot options:

- Boot from onboard NAND flash
- Boot from external SD card connected to MMC-1 interface
- Boot from external PC host via USB OTG port
- Boot from external PC host via RS232 port

The boot sequence is selected with the BOOT_SOURCE signal. The standard boot sequence is designed for normal system operation with the onboard NAND flash acting as the boot media. The alternate boot sequence is mainly intended for system debug and production, but can also be used for normal operation with an SD memory device (connected to the MMC-1 interface) acting as the boot media.

For additional details, please refer to section 25 of the "OMAP35x Technical Reference Manual".

Table 32   Boot sequences

Boot sequence	BOOT_SOURCE signal input	First device	Second device	Third device	Forth device
Standard	Unconnected.	NAND	USB	RS232	MMC-1
Alternate	Pulled to 1.8V with 1k resistance.	USB	RS232	MMC-1	NAND

Table 33   Boot selection signals

Signal Name	Pin #	Type	Description
BOOT_SOURCE	P1-65	I	Boot selection. Pulled down with 8.2k. Leave disconnected for standard boot sequence.

5.4 System and Miscellaneous Signals

5.4.1 External DMA Requests

The CM-T3530 provides two optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the OMAP35x SDMA controller. A logical channel can be configured to respond to an external synchronization request.

For additional details, please refer to section 9 of the "OMAP35x Technical Reference Manual".

Table 34   System signals

Signal Name	Pin #	Type	Description
nDMAREQ0	P1-92	I	External OMAP35xx DMA request 0
nDMAREQ1	P1-93 P1-83	I	External OMAP35xx DMA request 1
RESERVED	P2-10	I	Reserved for future use. Leave unconnected.
RESERVED	P1-135	-	Reserved for future use. Leave unconnected.
RESERVED	P1-66	I	Reserved for debug and production. Leave unconnected.

5.4.2 LED Drivers

The CM-T3530 features two open-drain LED drivers capable of driving two arrays of parallel LED's. These outputs are derived from the TPS65930 LED driver block.

For additional details, please refer to section 7 of the "TPS65930 Technical Reference Manual".

5.4.3 ADC

The CM-T3530 features two general purpose ADC inputs implemented with the TPS65930 ADC block.

For additional details, please refer to section 8 of the "TPS65930 Technical Reference Manual".

Table 35   Miscellaneous signals

Signal Name	Pin #	Type	Description
ADC_IN0	P1-132	I	General purpose ADC input 0.
ADC_IN2	P1-131	I	General purpose ADC input 2.
PMIC_LED_A	P2-13	OD	LED driver A.
PMIC_LED_B	P2-15	OD	LED driver B.
SYS_CLKOUT1	P1-133	O	Configurable output clock1. Can output main oscillator clock (26MHz).

5.5 Signal Multiplexing Characteristics

OMAP35x pins can have up to eight alternate function modes. The table below provides a description of signal multiplexing. Function names marked with gray shading denote the default function intended in the CM-T3530 design.

Table 36   Signal multiplexing

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-22	uart1_rx	-	mcbsp1_clkr	mcspi4_clk	gpio_151	-	-	safe_mode
P1-24	uart1_tx	-	-	-	gpio_148	-	-	safe_mode
P1-27	uart1_cts	-	-	-	gpio_150	-	-	safe_mode
P1-29	uart1_rts	-	-	-	gpio_149	-	-	safe_mode
P1-32	mcbsp3_clkx	uart2_tx	-	-	gpio_142	-	-	safe_mode
P1-33	mcbsp3_dx	uart2_cts	-	-	gpio_140	-	-	safe_mode
P1-34	mcbsp3_fsx	uart2_rx	-	-	gpio_143	-	-	safe_mode
P1-35	mcbsp3_dr	uart2_rts	-	-	gpio_141	-	-	safe_mode
P1-36	hdq_sio	sys_altclk	i2c2_sccbe	i2c3_sccbe	gpio_170	-	-	safe_mode
P1-39	mmc2_dat5	mmc2_dir_dat1	cam_global_reset	mmc3_dat1	gpio_137	-	-	safe_mode
P1-41	mmc2_cmd	mcspi3_simo	-	-	gpio_131	-	-	safe_mode
P1-42	uart3_rts_sd	-	-	-	gpio_164	-	-	safe_mode
P1-45	mmc2_dat7	mmc2_clkin	-	mmc3_dat3	gpio_139	-	-	safe_mode
P1-46	mmc2_dat0	mcspi3_somi	-	-	gpio_132	-	-	safe_mode
P1-47	mmc2_dat1	-	-	-	gpio_133	-	-	safe_mode
P1-48	mmc2_clk	mcspi3_clk	-	-	gpio_130	-	-	safe_mode
P1-49	mmc2_dat3	mcspi3_cs0	-	-	gpio_135	-	-	safe_mode
P1-52	mmc2_dat2	mcspi3_cs1	-	-	gpio_134	-	-	safe_mode
P1-54	mmc2_dat4	mmc2_dir_dat0	-	mmc3_dat0	gpio_136	-	-	safe_mode
P1-56	mmc2_dat6	mmc2_dir_cmd	cam_shutter	mmc3_dat2	gpio_138	-	-	safe_mode
P1-60	i2c2_sda	-	-	-	gpio_183	-	-	safe_mode
P1-61	i2c2_scl	-	-	-	gpio_168	-	-	safe_mode
P1-63	i2c3_scl	-	-	-	gpio_184	-	-	safe_mode
P1-64	i2c3_sda	-	-	-	gpio_185	-	-	safe_mode
P1-83	gpmc_wait3	sys_ndmareq1	-	-	gpio_65	-	-	safe_mode
P1-85	gpmc_ncs7	gpmc_io_dir	mcbsp4_fsx	gpt8_pwm_evt	gpio_58	-	-	
P1-87	gpmc_nbe1	-	-	-	gpio_61	-	-	safe_mode
P1-88	gpmc_clk	-	-	-	gpio_59	-	-	safe_mode
P1-92	gpmc_ncs3	sys_ndmareq0	-	-	gpio_54	-	-	safe_mode
P1-93	gpmc_ncs4	sys_ndmareq1	mcbsp4_clkx	gpt9_pwm_evt	gpio_55	-	-	safe_mode
P1-117	etk_d9	sys_secure_indicator	mmc3_dat5	hsusb1_nxt	gpio_23	mm1_rxdm	hsusb1_tll_nxt	-

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-119	etk_d1	mcspi3_somi	-	hsusb1_data1	gpio_15	mm1_txse0	hsusb1_tll_data1	-
P1-120	etk_d4	mcbsp5_dr	mmc3_dat0	hsusb1_data4	gpio_18	-	hsusb1_tll_data4	-
P1-121	etk_d7	mcspi3_cs1	mmc3_dat7	hsusb1_data3	gpio_21	mm1_txen_n	hsusb1_tll_data3	-
P1-123	etk_clk	mcbsp5_clkx	mmc3_clk	hsusb1_stp	gpio_12	mm1_rxdp	hsusb1_tll_stp	-
P1-124	etk_d5	mcbsp5_fsx	mmc3_dat1	hsusb1_data5	gpio_19	-	hsusb1_tll_data5	-
P1-125	etk_ctl	-	mmc3_cmd	hsusb1_clk	gpio_13	-	hsusb1_tll_clk	-
P1-126	etk_d6	mcbsp5_dx	mmc3_dat2	hsusb1_data6	gpio_20	-	hsusb1_tll_data6	-
P1-128	etk_d0	mcspi3_simo	mmc3_dat4	hsusb1_data0	gpio_14	mm1_rxrcv	hsusb1_tll_data0	-
P1-130	etk_d2	mcspi3_cs0	-	hsusb1_data2	gpio_16	mm1_txdat	hsusb1_tll_data2	-
P1-133	sys_clkout1	-	-	-	gpio_10	-	-	safe_mode
P2-18	jtag_emu0	-	-	-	gpio_11	-	-	safe_mode
P2-20	jtag_emu1	-	-	-	gpio_31	-	-	safe_mode
P2-27	mcbsp1_fsx	mcspi4_cs0	mcbsp3_fsx	-	gpio_161	-	-	safe_mode
P2-28	mcbsp1_clkr	mcspi4_clk	-	-	gpio_156	-	-	safe_mode
P2-29	mcbsp1_clkx	-	mcbsp3_clkx	-	gpio_162	-	-	safe_mode
P2-30	mcbsp1_fsr	-	cam_global_reset	-	gpio_157	-	-	safe_mode
P2-32	mcbsp1_dx	mcspi4_simo	mcbsp3_dx	-	gpio_158	-	-	safe_mode
P2-34	mcbsp1_dr	mcspi4_somi	mcbsp3_dr	-	gpio_159	-	-	safe_mode
P2-37	mcspi2_cs1	gpt8_pwm_evt	hsusb2_tll_data3	hsusb2_data3	gpio_182	mm2_txen_n	-	safe_mode
P2-39	mcspi2_simo	gpt9_pwm_evt	hsusb2_tll_data4	hsusb2_data4	gpio_179	-	-	safe_mode
P2-45	mcspi2_clk	-	hsusb2_tll_data7	hsusb2_data7	gpio_178	-	-	safe_mode
P2-47	mcspi2_cs0	gpt11_pwm_evt	hsusb2_tll_data6	hsusb2_data6	gpio_181	-	-	safe_mode
P2-49	mcspi2_somi	gpt10_pwm_evt	hsusb2_tll_data5	hsusb2_data5	gpio_180	-	-	safe_mode
P2-66	cam_d11	-	-	-	gpio_110	-	-	safe_mode
P2-68	cam_vs	-	-	-	gpio_95	-	-	safe_mode
P2-69	cam_d10	-	-	-	gpio_109	-	-	safe_mode
P2-70	cam_wen	-	cam_shutter	-	gpio_167	-	-	safe_mode
P2-72	cam_xclka	-	-	-	gpio_96	-	-	safe_mode
P2-75	cam_strobe	-	-	-	gpio_126	-	-	safe_mode
P2-76	cam_xclkb	-	-	-	gpio_111	-	-	safe_mode
P2-77	cam_pclk	-	-	-	gpio_97	-	-	safe_mode
P2-78	cam_fld	-	cam_global_reset	-	gpio_98	-	-	safe_mode
P2-80	cam_hs	-	-	-	gpio_94	-	-	safe_mode
P2-81	cam_d0	-	-	-	gpio_99	-	-	safe_mode
P2-82	cam_d1	-	-	-	gpio_100	-	-	safe_mode
P2-83	cam_d2	-	-	-	gpio_101	-	-	safe_mode
P2-84	cam_d3	-	-	-	gpio_102	-	-	safe_mode
P2-85	cam_d4	-	-	-	gpio_103	-	-	safe_mode
P2-87	cam_d6	-	-	-	gpio_105	-	-	safe_mode
P2-88	cam_d5	-	-	-	gpio_104	-	-	safe_mode
P2-89	cam_d8	-	-	-	gpio_107	-	-	safe_mode
P2-90	cam_d7	-	-	-	gpio_106	-	-	safe_mode
P2-92	cam_d9	-	-	-	gpio_108	-	-	safe_mode

5.6 RTC

The CM-T3530 RTC is implemented with the internal RTC of the TI TPS65930 companion chip. The RTC provides time and calendar information, timed interrupt generation and alarm wake-up event functionality.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present. The backup battery should be connected to the BKBAT power input.

For additional details, please refer to section 3 of the "TPS65930 Technical Reference Manual".

5.7 LED

The CM-T3530 features a single general purpose green LED controlled by GPIO186 of the OMAP35xx SoC. The LED is ON when GPIO186 is set high.

6   BASEBOARD INTERFACE

The CM-T3530 connects to the baseboard through P1 and P2 - 0.6 mm pitch 140-pin connectors.

6.1   Connector Pinout

Table 37   Connector P1

Pin #	CM-T3530 Signal Name	Reference Section	Pin #	CM-T3530 Signal Name	Reference Section
P1-01	CM_ETH_TXP	4.3	P1-02	CM_ETH_RXN	4.3
P1-03	CM_ETH_TXN	4.3	P1-04	CM_ETH_RXP	4.3
P1-05	CM_ETH_LED2	4.3	P1-06	CM_ETH_LED1	4.3
P1-07	VCC_CM	5.1.1	P1-08	GND	5.1.1
P1-09	MMC1_DAT4	4.9	P1-10	VCC_MMC	4.9
P1-11	nRST_IN	5.2	P1-12	MMC1_CLK	4.9
P1-13	MMC1_CMD	4.9	P1-14	GND	5.1.1
P1-15	MMC1_DAT0	4.9	P1-16	MMC1_DAT1	4.9
P1-17	MMC1_DAT5	4.9	P1-18	MMC1_DAT3	4.9
P1-19	VCC_CM	5.1.1	P1-20	BKBAT	
P1-21	MMC1_DAT6	4.9	P1-22	UART1_RX GPIO151	4.7 4.12
P1-23	MMC1_DAT7	4.9	P1-24	UART1_TX GPIO148	4.7 4.12
P1-25	MMC1_CD	4.9	P1-26	GND	5.1.1
P1-27	UART1_CTS GPIO150	4.7 4.12	P1-28	RS232_RXD	4.8
P1-29	UART1_RTS GPIO149	4.7 4.12	P1-30	RS232_TXD	4.8
P1-31	VCC_CM	5.1.1	P1-32	McBSP3_CLKX UART2_TX GPIO142	4.16 4.7 4.12
P1-33	McBSP3_DX UART2_CTS GPIO140	4.16 4.7 4.12	P1-34	McBSP3_FSX UART2_RX GPIO143	4.16 4.7 4.12
P1-35	McBSP3_DR UART2_RTS GPIO141	4.16 4.7 4.12	P1-36	HDQ_SIO GPIO170	4.17 4.12
P1-37	N.C.		P1-38	GND	5.1.1
P1-39	MMC2_DAT5 GPIO137	4.9	P1-40	N.C.	
P1-41	MMC2_CMD SPI3_SIMO GPIO131	4.9 4.15 4.12	P1-42	GPIO164	4.12
P1-43	VCC_CM	5.1.1	P1-44	N.C.	
P1-45	MMC2_DAT7 GPIO139	4.9 4.12	P1-46	MMC2_DAT0 SPI3_SOMI GPIO132	4.9 4.15 4.12
P1-47	MMC2_DAT1 GPIO133	4.9 4.12	P1-48	MMC2_CLK SPI3_CLK GPIO130	4.9 4.15 4.12
P1-49	MMC2_DAT3 SPI3_CS0 GPIO135	4.9 4.15 4.12	P1-50	GND	5.1.1
P1-51	N.C.		P1-52	MMC2_DAT2 SPI3_CS1 GPIO134	4.9 4.15 4.12
P1-53	TS_X+	4.10	P1-54	MMC2_DAT4 GPIO136	4.9 4.12
P1-55	VCC_CM	5.1.1	P1-56	MMC2_DAT6 GPIO138	4.9 4.12
P1-57	TS_X-	4.10	P1-58	N.C.	
P1-59	N.C.		P1-60	I2C2_SDA GPIO183	4.14 4.12

Pin #	CM-T3530 Signal Name	Reference Section		Pin #	CM-T3530 Signal Name	Reference Section
P1-61	I2C2_SCL GPIO168	4.14 4.12		P1-62	GND	5.1.1
P1-63	I2C3_SCL GPIO184	4.14 4.12		P1-64	I2C3_SDA GPIO185	4.14 4.12
P1-65	BOOT_SOURCE	5.3		P1-66	RESERVED	5.4
P1-67	VCC_CM	5.1.1		P1-68	N.C.	
P1-69	N.C.			P1-70	GPMC_A2	4.1
P1-71	GPMC_A1	4.1		P1-72	GPMC_A4	4.1
P1-73	GPMC_A3	4.1		P1-74	GND	5.1.1
P1-75	GPMC_A5	4.1		P1-76	GPMC_A6	4.1
P1-77	GPMC_A7	4.1		P1-78	GPMC_A8	4.1
P1-79	VCC_CM	5.1.1		P1-80	GPMC_A10	4.1
P1-81	GPMC_A9	4.1		P1-82	GPMC_nBE0	4.1
P1-83	GPMC_WAIT3 nDMAREQ1 GPIO65	4.1 5.4 4.12		P1-84	GPMC_nWE	4.1
P1-85	GPMC_nCS7 GPMC_IODIR GPIO58	4.1 4.1 4.12		P1-86	GND	5.1.1
P1-87	GPMC_nBE1 GPIO61	4.1 4.12		P1-88	GPMC_CLK GPIO59	4.1 4.12
P1-89	GPMC_nOE	4.1		P1-90	GPMC_Nadv	4.1
P1-91	VCC_CM	5.1.1		P1-92	GPMC_nCS3 nDMAREQ0 GPIO54	4.1 5.4 4.12
P1-93	GPMC_nCS4 nDMAREQ1 GPIO55	4.1 5.4 4.12		P1-94	GPMC_D0	4.1
P1-95	GPMC_D1	4.1		P1-96	GPMC_D2	4.1
P1-97	GPMC_D3	4.1		P1-98	GND	5.1.1
P1-99	GPMC_D5	4.1		P1-100	GPMC_D4	4.1
P1-101	GPMC_D7	4.1		P1-102	GPMC_D6	4.1
P1-103	VCC_CM	5.1.1		P1-104	GPMC_D8	4.1
P1-105	GPMC_D9	4.1		P1-106	GPMC_D10	4.1
P1-107	GPMC_D11	4.1		P1-108	GPMC_D12	4.1
P1-109	GPMC_D13	4.1		P1-110	GND	5.1.1
P1-111	GPMC_D15	4.1		P1-112	GPMC_D14	4.1
P1-113	N.C.			P1-114	N.C.	
P1-115	VCC_CM	5.1.1		P1-116	SYS_nRESWARM	5.2
P1-117	GPIO23	4.12		P1-118	N.C.	
P1-119	GPIO15	4.12		P1-120	GPIO18	4.12
P1-121	GPIO21	4.12		P1-122	GND	5.1.1
P1-123	GPIO12	4.12		P1-124	GPIO19	4.12
P1-125	GPIO13	4.12		P1-126	GPIO20	4.12
P1-127	VCC_CM	5.1.1		P1-128	GPIO14	4.12
P1-129	N.C.			P1-130	GPIO16	4.12
P1-131	ADC_IN2	5.4		P1-132	ADC_IN0	5.4
P1-133	SYS_CLKOUT1	5.4		P1-134	GND	5.1.1
P1-135	RESERVED	5.4		P1-136	USB0_DP	4.4.1
P1-137	USB0_ID	4.4.1		P1-138	USB0_DN	4.4.1
P1-139	VCC_CM	5.1.1		P1-140	USB0_5V_OUT	4.4.1

Table 38   Connector P2

Pin #	CM-T3530 Signal Name	Reference Section		Pin #	CM-T3530 Signal Name	Reference Section
P2-01	TV_OUT1	4.2		P2-02	GND	5.1.1
P2-03	TV_OUT2	4.2		P2-04	MMC1_DAT2 GPIO124	4.9 4.12
P2-05	N.C.			P2-06	USB1_CPEN	4.4.2
P2-07	VCC_CM	5.1.1		P2-08	USB1_VBUS	4.4.2
P2-09	USB2_CPEN	4.4.2		P2-10	RESERVED	5.4
P2-11	USB2_VBUS	4.4.2		P2-12	EXT_REG_EN	
P2-13	PMIC_LED_A	5.4.2		P2-14	GND	5.1.1
P2-15	PMIC_LED_B	5.4.2		P2-16	LCD_VIO	4.2
P2-17	JTAG_TDO	4.18		P2-18	JTAG_EMU0	4.18
P2-19	VCC_CM	5.1.1		P2-20	JTAG_EMU1	4.18

Pin #	CM-T3530 Signal Name	Reference Section		Pin #	CM-T3530 Signal Name	Reference Section
P2-21	JTAG_TDI	4.18		P2-22	JTAG_RTCK	4.18
P2-23	JTAG_TMS	4.18		P2-24	JTAG_TCK	4.18
P2-25	JTAG_nTRST	4.18		P2-26	GND	5.1.1
P2-27	McBSP1_FSX SPI4_CS0 GPIO161	4.16 4.15 4.12		P2-28	McBSP1_CLKR SPI4_CLK GPIO156	4.16 4.15 4.12
P2-29	McBSP1_CLKX GPIO162	4.16 4.12		P2-30	McBSP1_FSR GPIO157	4.16 4.12
P2-31	VCC_CM	5.1.1		P2-32	McBSP1_DX SPI4_SIMO GPIO158	4.16 4.15 4.12
P2-33	N.C.			P2-34	McBSP1_DR SPI4_SOMI GPIO159	4.16 4.15 4.12
P2-35	N.C.			P2-36	N.C.	
P2-37	SPI2_CS1 GPIO182	4.15 4.12		P2-38	GND	5.1.1
P2-39	SPI2_SIMO GPIO179	4.15 4.12		P2-40	N.C.	
P2-41	N.C.			P2-42	N.C.	
P2-43	VCC_CM	5.1.1		P2-44	N.C.	
P2-45	SPI2_CLK GPIO178	4.15 4.12		P2-46	N.C.	
P2-47	SPI2_CS0 GPIO181	4.15 4.12		P2-48	KPD_R0	4.11
P2-49	SPI2_SOMI GPIO180	4.15 4.12		P2-50	GND	5.1.1
P2-51	N.C			P2-52	KPD_R1	4.11
P2-53	KPD_C0	4.11		P2-54	KPD_R2	4.11
P2-55	VCC_CM	5.1.1		P2-56	KPD_R3	4.11
P2-57	KPD_C1	4.11		P2-58	KPD_R4	4.11
P2-59	KPD_C2	4.11		P2-60	KPD_R5	4.11
P2-61	KPD_C3	4.11		P2-62	GND	5.1.1
P2-63	KPD_C4	4.11		P2-64	N.C.	
P2-65	KPD_C5	4.11		P2-66	CAM_D11 GPIO110	4.13 4.12
P2-67	VCC_CM	5.1.1		P2-68	CAM_VS GPIO95	4.13 4.12
P2-69	CAM_D10 GPIO109	4.13 4.12		P2-70	CAM_WEN GPIO167	4.13 4.12
P2-71	TS_Y+	4.10		P2-72	CAM_XCLKA GPIO96	4.13 4.12
P2-73	TS_Y-	4.10		P2-74	GND	5.1.1
P2-75	CAM_STROBE GPIO126	4.13 4.12		P2-76	CAM_XCLKB GPIO111	4.13 4.12
P2-77	CAM_PCLK GPIO97	4.13 4.12		P2-78	CAM_FLD GPIO98	4.13 4.12
P2-79	VCC_CM	5.1.1		P2-80	CAM_HS GPIO94	4.13 4.12
P2-81	CAM_D0 GPIO99	4.13 4.12		P2-82	CAM_D1 GPIO100	4.13 4.12
P2-83	CAM_D2 GPIO101	4.13 4.12		P2-84	CAM_D3 GPIO102	4.13 4.12
P2-85	CAM_D4 GPIO103	4.13 4.12		P2-86	GND	5.1.1
P2-87	CAM_D6 GPIO105	4.13 4.12		P2-88	CAM_D5 GPIO104	4.13 4.12
P2-89	CAM_D8 GPIO107	4.13 4.12		P2-90	CAM_D7 GPIO106	4.13 4.12
P2-91	VCC_CM	5.1.1		P2-92	CAM_D9 GPIO108	4.13 4.12
P2-93	LCD_D23	4.2		P2-94	LCD_D22	4.2
P2-95	LCD_D0	4.2		P2-96	LCD_HSYNC	4.2
P2-97	LCD_D1	4.2		P2-98	GND	5.1.1
P2-99	LCD_D3	4.2		P2-100	LCD_D2	4.2
P2-101	LCD_D5	4.2		P2-102	LCD_D4	4.2
P2-103	VCC_CM	5.1.1		P2-104	LCD_D6	4.2
P2-105	LCD_D8	4.2		P2-106	LCD_D7	4.2

Pin #	CM-T3530 Signal Name	Reference Section	Pin #	CM-T3530 Signal Name	Reference Section
P2-107	LCD_D10	4.2	P2-108	LCD_D9	4.2
P2-109	LCD_D11	4.2	P2-110	GND	5.1.1
P2-111	LCD_VSYNC	4.2	P2-112	LCD_PCLK	4.2
P2-113	LCD_D12	4.2	P2-114	LCD_ACBIAS	4.2
P2-115	VCC_CM	5.1.1	P2-116	LCD_D13	4.2
P2-117	LCD_D15	4.2	P2-118	LCD_D14	4.2
P2-119	LCD_D17	4.2	P2-120	LCD_D16	4.2
P2-121	LCD_D19	4.2	P2-122	GND	5.1.1
P2-123	LCD_D21	4.2	P2-124	LCD_D18	4.2
P2-125	AGND	4.6	P2-126	LCD_D20	4.2
P2-127	VCC_CM	5.1.1	P2-128	AUDIO_IN	4.6
P2-129	MIC_BIAS	4.6	P2-130	AUDIO_OUT_L	4.6
P2-131	MIC_IN_P	4.6	P2-132	AGND	4.6
P2-133	MIC_IN_N	4.6	P2-134	GND	5.1.1
P2-135	VCC_CM	5.1.1	P2-136	AUDIO_OUT_R	4.6
P2-137	USB2_DP	4.4.2	P2-138	USB1_DP	4.4.2
P2-139	USB2_DM	4.4.2	P2-140	USB1_DM	4.4.2

6.2   Connector Type

Table 39   Connector type

Part Reference	Mfg.	CM-T3530 connector P/N	Baseboard (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab, see [prices] >> [accessories] links at CompuLab's website.

CompuLab's P/N for the AMP 1-5353190-0 connector is "CON140".

6.3   Mechanical Drawings
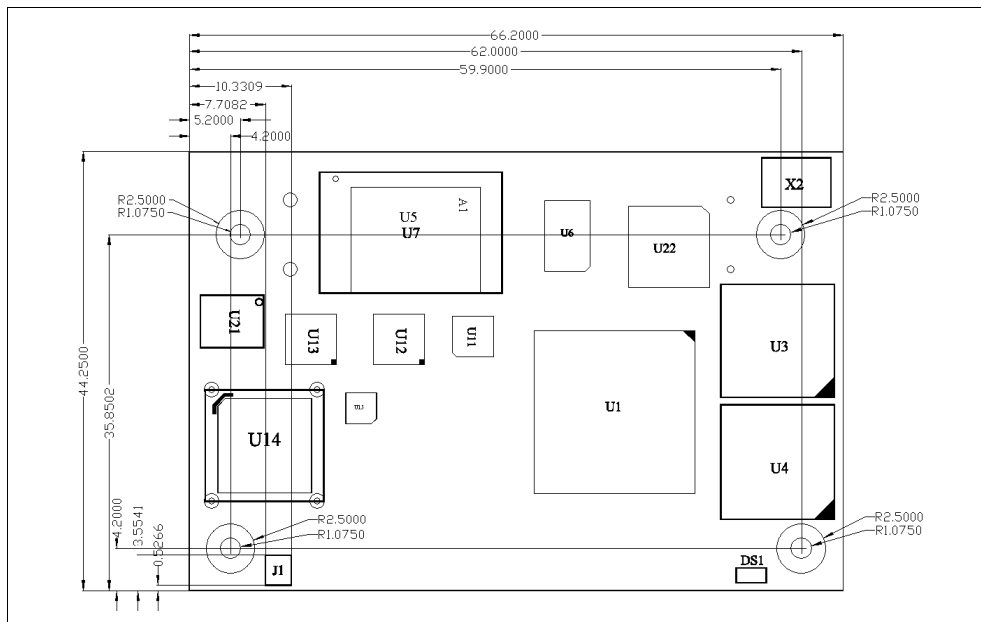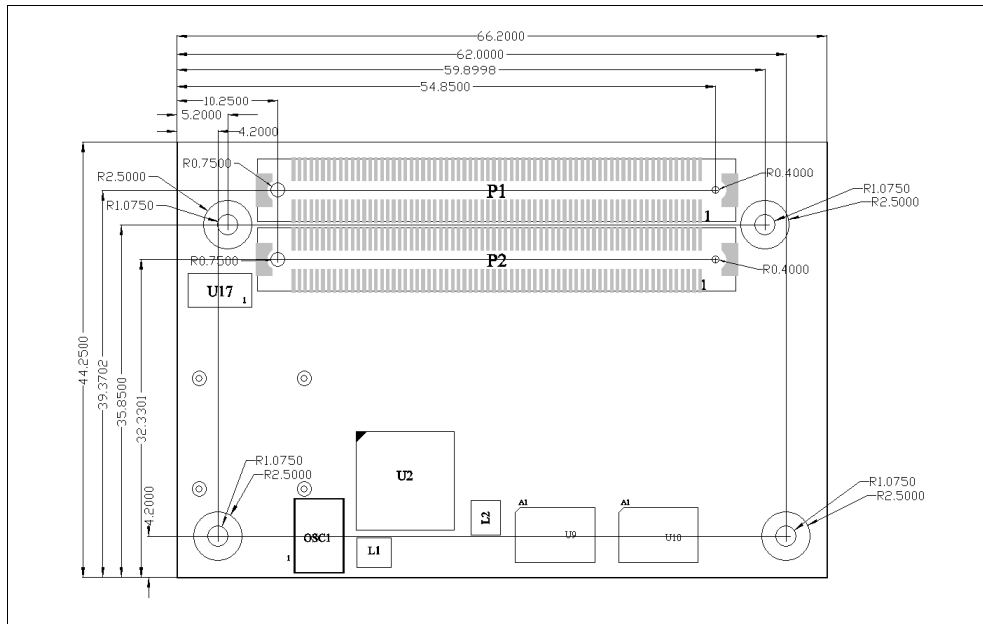
Figure 4   CM-T3530 top

Figure 5   CM-T3530 bottom (X-Ray view - as seen from top side)

1.   All dimensions are in millimeters.

2.   Height of all components is <2mm.

3.   Baseboard connectors provide 4mm board-to-board clearance.

4.   Board thickness is 1.6mm.

Mechanical drawings are available in DXF format from CompuLab's website, following [Developer] >> [CM-T3530] >> [CM-T3530 - Dimensions and Connectors Location] links.

6.4   Standoffs

The CM-T3530 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 40   Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7   OPERATIONAL CHARACTERISTICS

7.1   Absolute Maximum Ratings

Table 41   Absolute Maximum ratings

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	2.1		4.5	V
LCD interface power supply voltage (LCD_VIO)	-0.5		4.6	V

7.2   Recommended Operating Conditions

Table 42   Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	3.4	3.8	4.5	V
LCD interface power supply voltage (LCD_VIO)	TBD	3.3	3.6	V
RTC backup battery voltage (BKBAT)	1.8	3.2	3.3	V

7.3   DC Electrical Characteristics

Table 43   DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
MMC-1					
V_{IH}	VCC_MMC = 1.8V	1.17		2.1	V
	VCC_MMC = 3.0V	1.875		3.3	
V_{IL}	VCC_MMC = 1.8V	-0.3		0.63	V
	VCC_MMC = 3.0V	-0.3		0.75	
V_{OH}	VCC_MMC = 1.8V	1.6			V
	VCC_MMC = 3.0V	2.25			
V_{OL}	VCC_MMC = 1.8V			0.2	V
	VCC_MMC = 3.0V			0.375	
1.8V Digital I/O					
V_{IH}		1.17		2.1	V
V_{IL}		-0.3		0.63	V
V_{OH}		1.4			V
V_{OL}				0.4	V
LCD Interface					
V_{OH}	LCD_VIO = 3.3V	2.3			V
					V
V_{OL}	LCD_VIO = 3.3V			0.7	V
					V
I^2C (open drain with internal pull up to 1.8V)					
V_{IH}		1.26		2.3	V
V_{IL}		-0.5		0.54	V
V_{OH} (open drain with 3mA sink current)		0		0.36	V
JTAG					
V_{IH}		1.17		2.1	V
V_{IL}		-0.3		0.63	V
V_{OH}		1.6			V
V_{OL}				0.2	V

RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V

7.4　Power Output Characteristics

Table 44　Power Output Characteristics

Parameter	Min	Typ	Max	Unit
VCC_MMC				
Output voltage (programmable)	1.7945	1.85	1.9055	V
	2.7645	2.85	2.9355	V
	2.91	3.0	3.09	V
	3.0555	3.15	3.2445	V
Rated output current			220	mA
USB0_5V_OUT				
Output voltage		4.8		V
Rated output current		100		mA

7.5　Power Consumption

To be added in a future revision of this document.

7.6　ESD Performance

Table 45　ESD Performance

Interface	ESD Performance
USB OTG	±8 kV ESD using HBM
USB host	±8 kV ESD using HBM
RS232	±15 kV ESD using HBM

7.7　Operating Temperature Ranges

The CM-T3530 is available with three options of operating temperature range.

Table 46　CM-T3530 Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Baseboard Design Guidelines

- Ensure that all VCC_CM and GND power pins are connected.

- Major power rails - VCC_CM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system's signal quality, because the planes provide a current return path for all interface signals.

- It is recommended to put several 100nF and 10/100uF capacitors between VCC_CM and GND near the mating connectors.

- It is recommended to connect the standoff holes of the baseboard to GND, in order to improve EMC.

- Except for a power connection, no other connection is mandatory for CM-T3530 operation. All power-up circuitry and all required pullups/pulldowns are found on the module.

- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIO's), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.

- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet and USB signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
  - Local bus signals must be buffered in most cases.

- Be careful when placing components under the CM-T3530 module. The baseboard interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-T3530. Maximum allowable height for components placed under the CM-T3530 is 1.5mm.

- Refer to the SB-T35 baseboard reference design schematics.

8.2 Baseboard Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the baseboard. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.

- Using an oscilloscope, check the voltage levels and quality of the VCC_CM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.

- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.

- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

- Devices improperly driving the local bus
  - External pullup/pulldown resistors overriding the module's on-board values, or any other component creating the same "overriding" effect
  - Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.

- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the baseboard, shorting them on the connectors can disable the module's operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector's body. Note that solder shorts are the most frequent factor disabling a module's start.

- Check possible signal's shorting due to errors of baseboard PCB design or assembly.

- Improper functioning of a customer baseboard can accidentally delete boot-up code from the CM-T3530, or even damage the module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's SB-T35 baseboard.

- It is recommended to assemble more that one baseboard for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics' Implementation

8.3.1 Magnetics' Selection

Refer to the table below for compatible magnetics. Magnetics listed under the "Qualified" title have been tested in order to verify proper operation with the LAN9220 device. Magnetics in the "Suggested" category have been evaluated on the vendor-supplied datasheet level, but have not been tested. Designers should test and qualify all magnetics before using them in an application.

Table 47   Compatible Magnetics

| Vendor	P/N	Package
Qualified Magnetics		
UDE	RTA-1D4B8V1A	Integrated RJ45
Pulse	H1102	16-pin SOIC
Halo	TG110-RP55N5	16-pin SOIC
Halo	HFJ11-RP26E-L12RL	Integrated RJ45
Delta	RJSE1R5310A	Integrated RJ45
Suggested Magnetics		
Pulse	J0011D01B	Integrated RJ45
Bothhand	TS6121C	16-pin SOIC
Bothhand	LU1S041X-43	Integrated RJ45

8.3.2 Magnetics' Connection

The center tap connection on the CM-T3530 side for the transmit channel must be connected to a 3.3V analog power rail (can be created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. Decouple the 3.3V voltage with at least one large and one small capacitor (10uF and 0.1uF respectively). The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

The center tap connection on the CM-T3530 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 µF capacitor is required from the receive channel center tap of the magnetics to digital ground.

The figure below shows an implementation example with a magnetic embedded in the RJ-45 socket with integrated LED's.

Figure 6   Magnetics' connection example
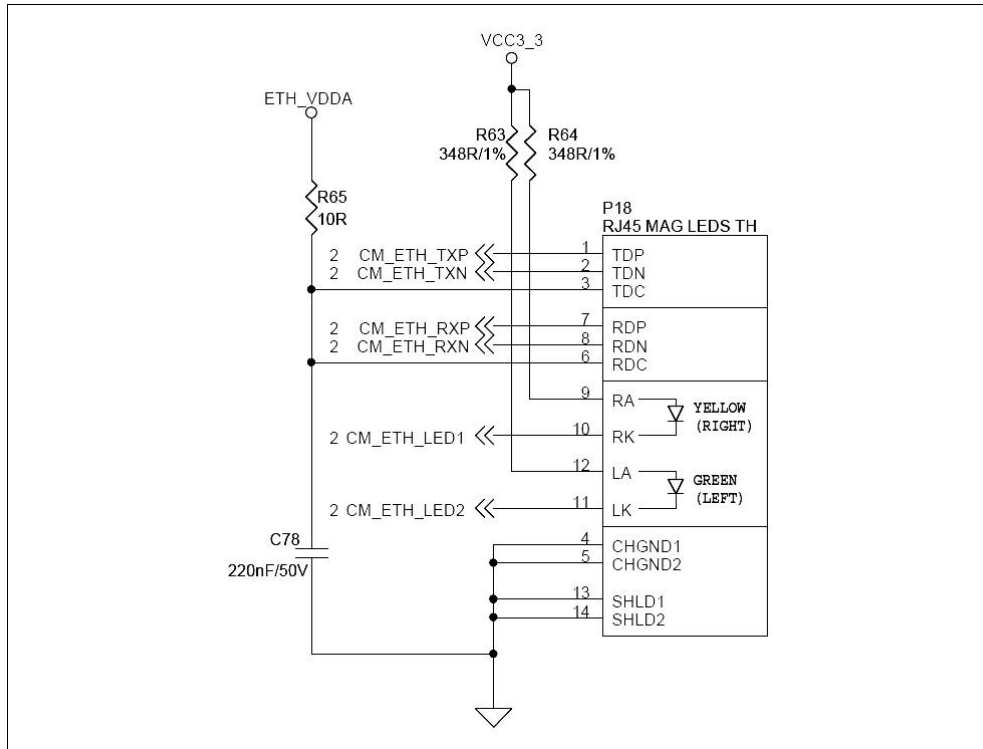
8.4   Battery Powered Design

The power management sub-system of the CM-T3530 is designed for direct operation with a Lithium ion Polymer battery. Battery charging and supervision functions must be implemented on the baseboard. Please refer to SB-T35 design package for a comprehensive reference design.