CM-X270
Computer-on-Module

Reference Guide

Table of Contents

1. Revision Notes

Date	Description
01-Oct-2005	▪ First release
08-Oct-2005	▪ Added baseboard design and troubleshooting guidelines
22-Feb-2006	▪ Updated peak current at VCC_3STBY power rail. ▪ Updated deep sleep PME. ▪ Fixed PCMCIA signal-to-GPIO mapping. ▪ Added a comment regarding PWM0 line availability. ▪ Updated IDE-CS0# mapping. ▪ Updated baseboard design and troubleshooting guidelines. ▪ Fixed A option audio codec p/n (CS4299->CS4202) ▪ Added comment regarding LB-A0 signal. ▪ Added comment regarding I2S usage. ▪ Fixed AC97 SDIN0/SDIN1 pin naming. ▪ Removed MMCLK from GPIO list ▪ Documented 24.576 MHz clock output (AC97_SYSCLK). ▪ Documented LB-DREQ0. ▪ Updated Linux serial port mapping. ▪ Updated CAMI pin routing : SSP/I2C, MG-LCD1_PWM, PXA-270 GPIO[86]/[87].
23-Apr-2006	▪ Added CM-X270L information. ▪ Added JTAG pads drawing for CM-X270W.
14-Jun-2006	▪ Fixed JTAG-TRST pulling to "up".
21-Jun-2006	▪ Added WiFi interface specifications
26-Jun-2006	▪ Updated Audio load driving specifications
27-Jun-2006	▪ Fixed CM-X270W drawing
03-Jul-2006	▪ Changed Write Protection (WP) pin specifications.
27-Jul-2006	▪ Added WLAN chapter ▪ Added NOR flash setup block comment ▪ Added REQ1/GNT1 pair comment ▪ Added GPIO29 to GPIO table ▪ Fixed GPCS to LB-CS in CS truth table
13-Sep-2006	▪ Removed unsupported SUSP-IN pin from documentation. Described alternative methods of entering the suspend/sleep mode. ▪ Removed rev 1.1 vs. 1.2 difference notes, as rev 1.1 cards are no longer shipped.
26-Sep-2006	▪ Improved mechanical drawings. ▪ Fixed 2700G VLIO CS address.
03-Oct-2006	▪ Clarified invariance of serial port assignment in X270W vs. X270L

	▪ Removed GPIO88 (was on P2-133) from available GPIO's list.
05-Nov-2006	▪ Added details about RTC supply ▪ Added table specifying GPIO's initial state and pullup
31-Jan-2007	▪ Modified LB timing and timing diagram and added clarifications ▪ Added reset timing diagram. ▪ Added WLAN power consumption info ▪ Added LCD B2 and R2 signals to the 2700G section. ▪ Added a comment regarding power rail stabilization time.
20-Mar-2007	▪ Fixed COM-C-DCD# CAMI routing on page 89.
16-Jul-2007	▪ Removed incorrect comments about 18-bit LCD support.
13-Aug-2007	▪ Datasheet (first pages) updated with information about Rev 2 features: GPRS and Bluetooth
23-Oct-2007	▪ Added GPRS and Bluetooth subsection. ▪ Updated power supply section. ▪ Added information regarding the new AC'97 CODEC. ▪ Updated CAMI connectors table for CM-X270W rev 2. ▪ Fixed IORDY signal on LB timing diagram. ▪ Added trigger type and pulse length for LB-IRQx ▪ Added a comment regarding bufferability of LB-IRQ0 ▪ Added a comment on using AC'97 inerface pins as GPIOs. ▪ Removed 2700G documentation, because this feature is no longer offered for new designs.
12-Dec-2007	▪ Removed mentioning of external PCI clock input
31-Mar-2008	▪ US and Canada GSM bands support note ▪ Added USB1 port availability note
24-Jun-2008	▪ Added Wi2Wi WLAN description for CM-X270L rev1.4

Please check for a newer revision of this manual in CompuLab's website - http://www.compulab.co.il, following [Products] >> [Developer] >> [CM-X270] links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

2. Overview

2.1. Highlights

- **Intel's XScale PXA270 CPU, up to 520 MHz, 32+32 KB cache, WMMX**
- **General purpose bus and optional PCI, LPC, AC97 busses**
- **16 - 128 Mbyte SDRAM**
- **128 / 512 Mbyte Flash Disk**
- **WiFi Interface**
- **GSM / GPRS modem**
- **Bluetooth interface**
- **Graphics controller integrated in PXA270 supporting STN and TFT panels up to 800 x 600 pixels**
- **Video Input Port**
- **PCMCIA controller**
- **Sound codec with speaker and microphone support**
- **Touchscreen Controller**
- **Slave and host USB ports**
- **Serial ports, GPIO, hard-disk interface**
- **10/100BaseT Ethernet port**
- **Very low standby and active power consumption**
- **Two size options: 66 x 44 mm (X270L) or 68 x 58 mm (X270W)**
- **Interchangeable with other modules via CAMI connectors**

** Note: some of above specified features are optional*

The CM-X270 is a small "Computer-On-Module" board designed to serve as a building block in embedded applications. The CM-X270 has all the components required to run operating systems such as Linux and Windows CE. Ready packages for these operating systems are available from CompuLab.

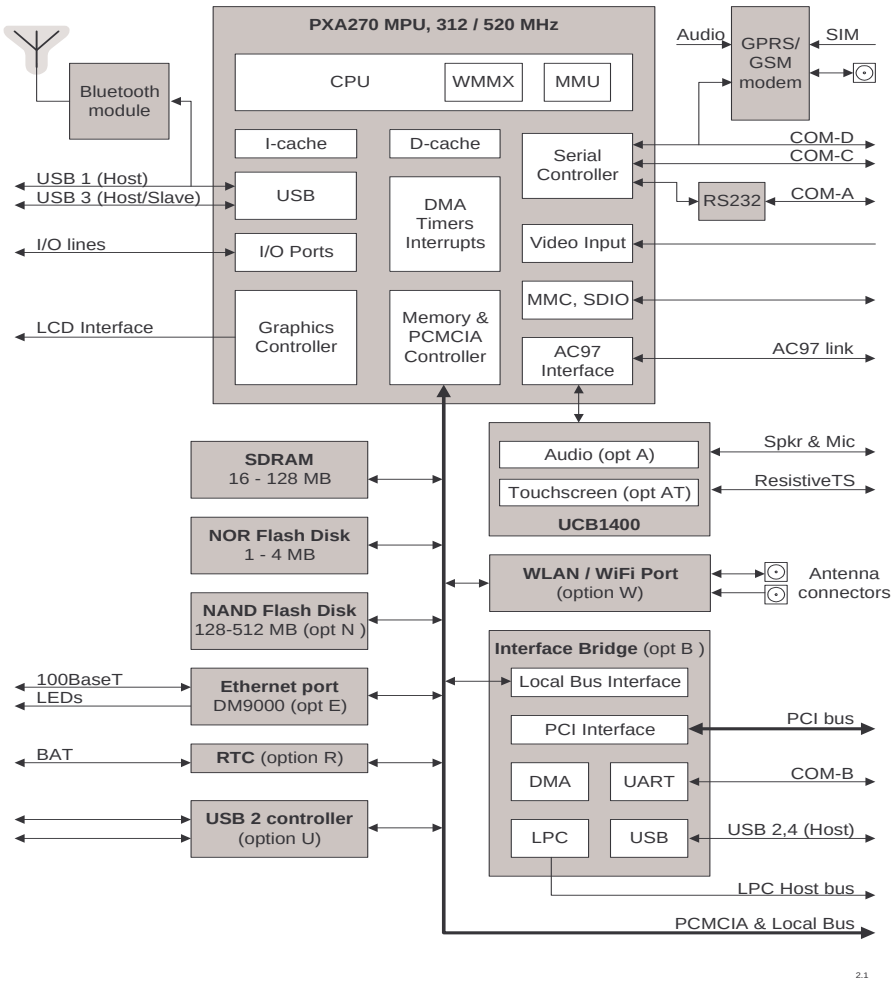
The small size of the CM-X270 allows its integration into hand-held and mobile applications, while its low price makes it an ideal selection for cost-sensitive applications. Based on Intel's XScale architecture, the CM-X270 delivers a price/performance ratio significantly better than that of any other platform.

The feature set of the CM-X270 module combines a 32-bit CPU, SDRAM, Flash Disk and vital computing peripherals. For embedded applications, the CM-X270 provides a 32-bit PCI bus, 100Mbit Ethernet, serial ports, general purpose I/O lines and many other essential functions.

An integrated WLAN (WiFi) interface implements 802.11 b/g industry standard wireless connectivity. The on-board GPRS modem enables data transmission to any arbitrary destination using public subscriber network infrastructure. Voice communication is also fully supported, practically implementing full featured cellular phone integrated into the CoM. The CM-X270 is the first and only CoM in the market implementing this advanced features.

The standardized CAMI ("CompuLab's Aggregated Module Interface") connectors of the CM-X270 module allow interchangeability with other Computer-On-Module's available from CompuLab, enabling the flexibility required in a dynamic market where application requirements can change rapidly.

2.2. Block Diagram



This manual covers both CM-X270W and CM-X270L product versions. Both versions have identical functionality and interface, except of certain cases which are explicitly specified in relevant sections.

2.3. Features

"Option" column specifies the configuration code required to have the particular feature.
"+" means that the feature is always available.

CPU, Memory and Buses

Feature	Specifications	Option
CPU	Intel XScale PXA270, 312 / 520 MHz, WMMX 32 KB I-cache and 32 KB D-cache, WB, 128 MB address space DMA and Interrupt controllers, Timers	+
DRAM	16 - 128 MB, SDRAM, 100 MHz, 32-bit	+
NOR Flash	1 - 4 Mbytes	+
NAND Flash Disk	128 - 512 Mbytes	N
External local bus	16-bit, variable rate up to 100 MHz, 3.3V tolerant	+
AC97 bus	AC97 / AMC97 Rev 2.1 compliant	+
PCI bus	32-bit, 2.1-compliant, 132 MB/s, arbiter for 4 masters, 5.0V tolerant	B
LPC bus	Host, 33 MHz, Intel LPC v1.0 compatible	B
JTAG Interface	Available	+

Peripherals

Feature	Specifications	Option
Graphics Controller	4/8/16 bit color, TFT / STN, resolution up to 800 x 600 x 16, frame buffer in system SDRAM	+
Video Input Port	Direct camera sensor support, max resolution 2048 x 2048. 30 fps @ 320x240, 15 fps @640x480	+
USB	One Host port, 12 Mbps, OHCI v1.1 One Host/Slave port, 12 Mbps, 24-endpoints, OHCI v1.1 Additional Host ports, 12 Mbps, OHCI v1.0 compliant (one port in X270L or two ports in X270W)	+ + B
Serial Ports (UARTs)	Up to 4 UART ports, 16550 compatible, 921 kbps COM-A - RS232, full modem COM-B - TTL, Rx/Tx COM-C - TTL, partial modem COM-D - TTL, Rx/Tx	 + B + +
General Purpose	About 50 lines shared with other functions. Can also be	+

I/O	used as interrupt inputs.	
Hard Disk Interface	IDE, PIO mode	+
Keyboard & mouse	USB or redirection from COM port	+
Ethernet	Davicom DM9000 MAC & PHY, 10/100BaseT, LED's	E
Audio codec	Crystal CS4202 or Phillips UCB1400, AC97 interface, mono microphone input, stereo line input and 25 mW output for active speakers	A
Touchscreen ctrl.	A part of the UCB1400 codec chip. Supports resistive touch panels.	AT
PCMCIA controller	Direct support for 1st slot, hooks for 2nd slot, 16 bit interface	+
RTC	Real Time Clock, powered by external lithium battery	R
WiFi Interface	802.11 b/g capabilities, Wi2Wi W2SW0001 controller module based on the Marvell's 88W8686 chipset. Up to 54 Mbps, 2.45 GHz band, single antenna support.	W
GPRS / GSM and cellular phone	Telit GE864 module. GSM 850, 900, DCS 1800 or PCS 1900 network communication services. GPRS Class 10, Voice, Circuit Switched Data transfer, Fax, Phone-book and SMS. On-board SIM card socket. Connector for external antenna. Available only in CM-X270W.	K
Bluetooth	Bluetooth V2.0+EDR system. CSR BlueCore4-ROM chipset, 2.4GHz band, up to 3Mbps. On-board ceramic chip antenna and connector for external antenna. Available only in CM-X270W.	J

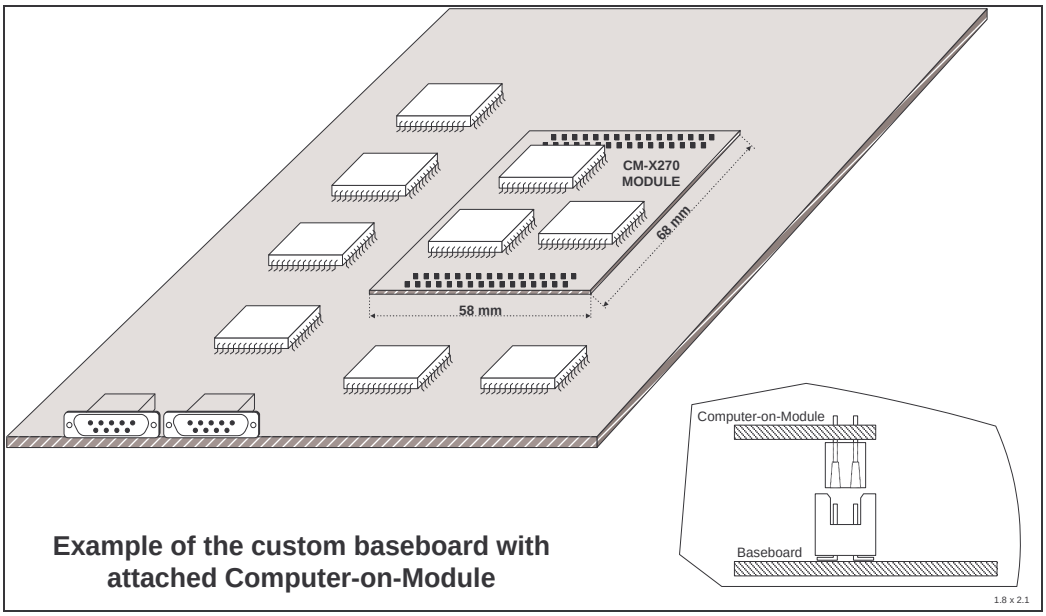
Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 3.3V or dual 3.3V / 5.0V (for "A" option)
Active power consumption	0.2 - 2 W, depending on configuration and speed
Standby/Sleep consumption	3 - 100 mW, depending on configuration and mode
Dimensions	66 x 44 mm (X270L) or 68 x 58 mm (X270W)
Weight	35 gram
MTBF	> 100,000 hours
Operation temperature (on case)	Commercial : 0^o to 70^o C
	Extended : -20^o to 70^o C
	Industrial : -40^o to 85^o C
Storage temperature	-40^o to 85^o C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)

Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	3 x 140 pin, 0.6 mm
Connector re-insertion	50 cycles

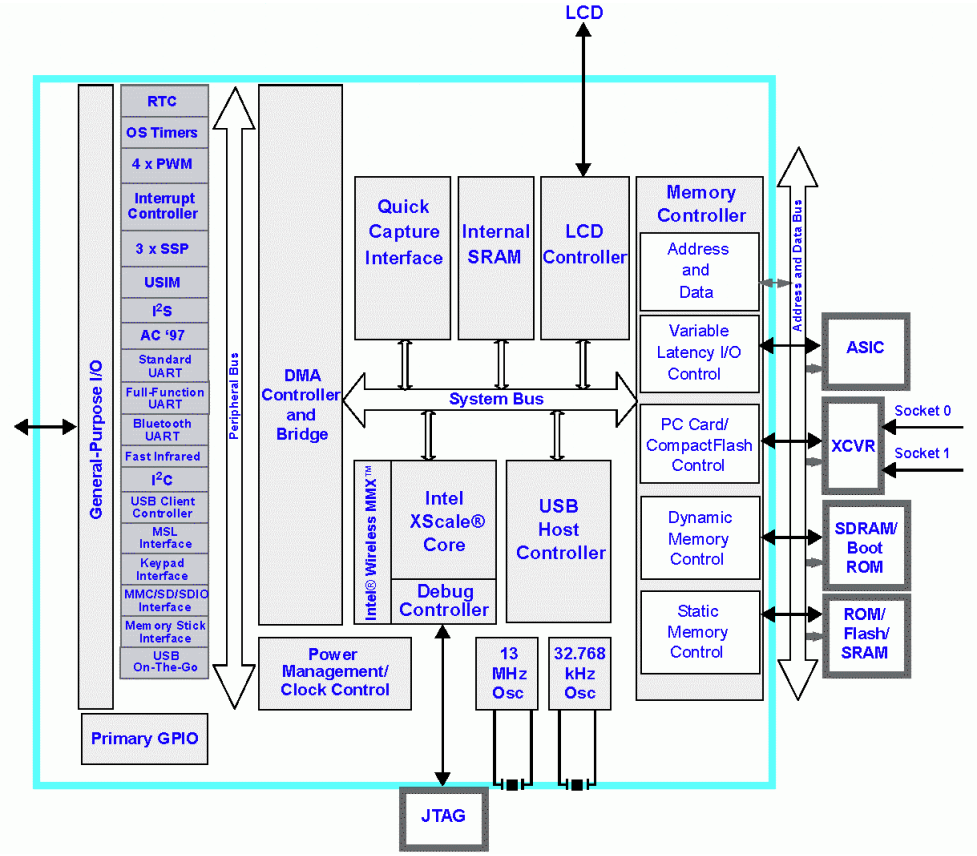
2.4. Computer-on-Module Concept

The CM-X270 is a miniature single board computer packed as a module. It contains a CPU, memory, flash disk and peripherals. All interface functions of the CM-X270 are routed through miniature high-density connectors, designed for piggyback attachment to a custom baseboard. Depending on application, custom baseboard adds more functions, and/or routes module's signals to interface connectors.



Example of the custom baseboard with attached Computer-on-Module

2.5. PXA270 Processor



XScale PXA270 Block Diagram

The PXA270 processor is an integrated system-on-a-chip microprocessor for high performance, low power portable handheld and handset devices. It incorporates Intel's XScale microarchitecture with on-the-fly frequency scaling and sophisticated power management to provide excellent MIPs/mW performance. The PXA270 processor is ARM Architecture Version 5TE instruction set compliant (excluding floating point instructions) and follows the ARM programmer's model.

An integrated LCD display controller provides support for displays up to 800 x 600 pixels, and permits 1-, 2-, 4-, and 8-bit grayscale and 8- or 16-bit color pixels. A 256 entry/512 byte palette RAM provides flexibility in color mapping.

A set of serial devices and general system resources provide computation and connectivity capabilities for a variety of applications. Intel XScale microarchitecture provides the following features:

- ARM Architecture Version 5TE ISA compliant
  - ARM Thumb Instruction Support
  - ARM DSP Enhanced Instructions
- Low power consumption and high performance
- Media Processing Technology
  - Enhanced 16-bit Multiply
  - 40-bit Accumulator
- 32-KByte Instruction Cache
- 32-KByte Data Cache
- Instruction and Data Memory Management Units
- Branch Target Buffer

The processor integrates XScale microarchitecture with the following peripheral set:

- Clock and Power Controllers
- DMA Controller
- LCD Controller
- Interrupt Controller
- AC97
- Universal Serial Bus (USB) Client
- I^2S
- I2C
- MultiMediaCard
- FIR Communication
- Synchronous Serial Protocol (SSP) Port
- General Purpose I/O pins
- UART's
- Real-Time Clock
- OS Timers
- Pulse Width Modulation
- USB Host and Slave controller
- Camera Interface

PXA270 has integrated coprocessor to accelerate multimedia applications. This coprocessor is characterized by a 64-bit single-instruction multiple-data (SIMD) architecture and compatibility with the integer functionality of the Intel's Wireless MMX™ technology and streaming SIMD extensions (SSE) instruction sets. Key features of this coprocessor include:

- 30 media-processing instructions

- 64-bit architecture up to eight-way SIMD
- 16 x 64-bit register file
- SIMD PSR flags with group-conditional execution support
- SIMD instruction support for sum of absolute differences (SAD) and multiply-accumulate (MAC) operations
- Instruction support for alignment and video operations
- Intel's MMX and SSE integer instruction compatibility
- Superset of existing media-processing instructions in the Intel XScale® core

PXA270 processor has on-chip memory. Key features of the internal memory module include:

- 256 Kbytes of on-chip RAM arranged as four banks of 64 Kbytes
- Bank-by-bank power management for reduced power consumption
- Support for byte writes

2.6. Memory

DRAM
The CM-X270 can be assembled with 16, 32, 64 or 128 Mbytes of Synchronous DRAM. The SDRAM interface is 32-bits wide and runs with a 100 MHz clock.

NOR Flash
The CM-X270 is assembled with 1, 2 or 4 Mbytes of linear (NOR) Flash ROM. The first 1MB is used for ARMMON (Bootloader) and O/S Kernel; the remainder is used for Flash Disk implementation. The setup block located in the NOR flash contains vital production information including bootloader configuration, PCB revision, manufacturing stamp, MAC addresses for Ethernet and WLAN.

NAND Flash
For applications requiring large, non-volatile on-board storage, the CM-X270 can be assembled with an additional NAND Flash. The NAND Flash is a block device - optimized for block read and write operations rather than for random access. It is used for implementation of a Flash Disk, regarded by the operating system as a regular disk drive. The NAND Flash is available in sizes of 32, 128 and 512 Mbytes. The CM-X270 is designed for upward compatibility with future NAND Flash devices of larger capacity.

Flash Write Protection

NAND flash can be write protected by applying "0" to WP# of CAMI connector. If WP# is left open or pulled up, write operations to flash are enabled. In CM-X270W WP# pin location is P3-100, in CM-X270L its location is P1-09.
NOR flash doesn't have write protection.

2.7. Flash Disk

One of the key advantages of CM-X270 architecture is its on-board flash disk, supported by all operating systems available for the CM-X270. The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts and it is built into the CM-X270 module. The Flash Disk is implemented by three parts:

- Flash memory component - NOR and optional NAND
- Interface logic
- Flash Disk Driver firmware

NOR vs. NAND tradeoffs

NOR and NAND are two different technologies of Flash components. NOR technology has capabilities and a price advantage in low capacities, up to 4 MBytes, while NAND technology is available and has a price advantage in higher capacities - from 32 to 512 MBytes today and more in the future. The CM-X270 card has one NOR and one optional NAND component on-board. Either NOR or NAND or both can be used as an on-board Flash Disk. A NOR Flash is mandatory for the CM-X270, because startup code - ARMMON/Bootloader and O/S kernel is located in it. If a Flash Disk is not required, or if only a small Flash Disk is required, only the NOR Flash is assembled on the card. If more than 3 MB's of Flash Disk is required, both NOR and NAND Flashes are assembled. In that case, the most cost effective selection is to use the minimum NOR size - 1MB, and to use NAND as the main flash disk storage.

Flash Disk Driver

The Flash Disk Driver emulates disk-like behavior using the Flash memory component. The driver's core code is operating system independent - the same code is used for all operating systems. However, since each operating system requires that the driver be integrated through a different interface, CompuLab provides a Flash Disk Driver kit per operating system. Driver code is also included in ARMMON, to provide Flash Disk service through ARMMON calls. The driver performs the following functions:

- Translation of sector read/write requests coming from the operating system to block access operations on physical media (Flash)
- Buffering and consolidation of sector write operations
- Mapping and swapping-out of bad blocks
- Error correction using ECC
- Anti-wearing
- Crash / power fail protection

Anti-wearing algorithm

The Flash Disk Driver ensures that block write operations will be distributed evenly across the physical media, regardless of the location (logical sector number) requested by the operating system. Even distribution ensures that all Flash blocks will be worn at the same (slow) rate and the Flash will continue operating for a long time without reliability degradation. The following example outlines expected reliability.

Flash actual data: Size - 32 MB. Guaranteed minimum of writes per block - 100,000.

Assuming that a specific application continuously writes to the Flash Disk, 300KB per minute then:

Guaranteed life time = [32MB * 100,000] / 300KB/min = 20 years

This simple example shows that the guaranteed period of reliable operation is well above any practical limit.

Reliability

The reliability issue concerns two different aspects: mechanical and functional.
Obviously, the mechanical reliability of the Flash Disk is far above that of its hard disk counterpart, as it doesn't have any moving parts and is securely soldered on-board.
In terms of functional reliability, the Flash Disk is similar to a standard, high-quality hard disk. Operating systems using the Flash Disk will perform with the same or better reliability level than that of its hard disk counterpart.

Fault Tolerance

Flash Disk Driver algorithms and data structures are designed for full recovery in the event of an operating system crash or unexpected power off. The Driver achieves fault tolerance through the following method:
When new data is stored and control information should be updated, the driver first copies the control information to a new location and alters it accordingly. When control information is finally updated, the driver switches between the old and new copies in a single step. Only then is the previous copy deleted.
If driver operation is aborted in the middle, due to power off for example, on the next start, the driver will use the last valid copy of control information and will remove the newer, incomplete copy.
The fault tolerance implemented by the Flash Disk Driver ensures that its operation will remain correct and consistent, i.e., it will continue emulating hard disk behavior. It doesn't however provide any remedy for an incorrect state of a file system, which may be caused by the operating system itself in the event of a crash. Problems like these are transparent to the Flash Disk Driver and should be handled on the operating system level. For example, Linux files can be protected against power failures by using an EXT3 file system with journaling.

Performance

	NOR	**NAND**
Read	400 KB/s	1000 KB/s
Write	20 KB/s	500 KB/s

The Flash Disk has an internal write buffer. The buffer’s contents are flushed into non-volatile media within 200 ms after write operation. Therefore, the requirement for a 200 ms delay should be taken into account when scheduling a system shutdown.

During write operations, the Flash Disk Driver performs atomic sequences which can last up to 15 uS. The Driver disables interrupts during this time. Users whose applications cannot tolerate a 15 uS lock should contact CompuLab's technical support for a review of available solutions.

2.8. Interface Bridge

The Interface Bridge is an advanced LocalBus-to-PCI companion chip that supports a PXA270 processor interface. The Interface Bridge provides a link from the host bus to the PCI bus and also provides a Shared Memory (SDRAM) Controller, Low Pin Count (LPC) Host Controller, Interrupt Controller, DMA Controller, Timers, USB Host Controller and Power Management.

Bridge Features

- **Shared SDRAM Controller**
  - Direct access to the entire SDRAM address space
  - Deep PCI to SDRAM buffers for burst transfer optimization
  - 96 MHz SDRAM bus operation
- **PCI Bus Controller**
  - 32-bit data bus interface
  - Supports PCI rev. 2.1 specification
  - Provides CPU to PCI buffers for burst transfer optimization
  - Built-in PCI bus arbiter supports up to four individual external bus master devices
  - Supports CLKRUN# signal function
  - 33 MHz PCI bus operation
- **Interrupt Controller**
  - One maskable interrupt to processor
- **Chaining DMA Controller**
  - Four independent DMA channels
  - Chaining and non-chaining modes
  - PCI memory space and I/O space addressing
  - Rotating and fixed priority modes
  - Supports transfers to unaligned address
- **Timers**
  - 4-channel 24-bit auto-reloaded timer with pre-scale 1, 1/16 or 1/256
  - Supports interrupt generation

- **Low Pin Count (LPC) Host Controller**
  - Compliant with Intel LPC Interface Specification Rev. 1.0
  - Supports the Serial IRQ Protocol
- **USB Host Controller**
  - Two USB ports
  - 12 Mbps or 1.5 Mbps speed
  - Supports power management and overcurrent protection
  - Fully compatible with USB specification version 1.1 and OHCI 1.0 register model
- **UART**
  - 16550 mode compatible, TXD and RXD signals only

A detailed description of the Bridge's functional blocks is provided in the "Peripherals and Functions" section.

3. Buses

3.1. Local Bus Interface

The CM-X270's Local Bus is derived from PXA270 processor’s memory interface bus. Processor’s signals are routed directly to CAMI connector, without buffering. Local Bus implements the access to various types of devices sharing the same interface lines. Interface lines function change dynamically per-cycle, according to the type of addressed device.

The external memory bus interface supports:

- RAM / ROM memories
- Variable Latency I/O
- PCMCIA expansion cards
- Compact Flash cards
- 16-bit (only) aligned access

Local Bus Signals

CAMI Signal Name	PXA270 Name	CAMI Pin Number	Type	Description
LB-A0	MA [0]	P1-64	Output	Used in some PCMCIA/CF accesses only. Other 8 bit aligned accesses are not supported.
LB-A1	MA [25:1]	P1-63	Output	**Local Bus Address.** LB-A [25:1] can address up to 64 MB range per chip select (LB-CSx). LB-A [25:1] specifies the address of 16-bit word. Note: 16-bit word alignment, as supported by PXA270 processor, doesn't impose significant restriction on accessing byte-wide devices. For accessing byte-wide device, address lines [X:0] of the device should be connected to LB-A [(X+1):1] respectively.
LB-A2		P1-66		
LB-A3		P1-65		
LB-A4		P1-68		
LB-A5		P1-69		
LB-A6		P1-70		
LB-A7		P1-71		
LB-A8		P1-72		
LB-A9		P1-73		
LB-A10		P1-76		
LB-A11		P1-75		
LB-A12		P1-78		
LB-A13		P1-77		
LB-A14		P1-80		
LB-A15		P1-81		
LB-A16		P1-82		
LB-A17		P1-83		
LB-A18		P1-84		
LB-A19		P1-85		
LB-A20		P1-88		
LB-A21		P1-87		
LB-A22		P1-90		
LB-A23		P1-89		
LB-A24		P1-92		
LB-A25		P1-93		
LB-D0	MD [15:0]	P1-94	I/O	**Local Bus Data**, 16-bit width.
LB-D1		P1-95		
LB-D2		P1-96		
LB-D3		P1-97		
LB-D4		P1-100		
LB-D5		P1-99		
LB-D6		P1-102		
LB-D7		P1-101		

LB-D8		P1-104		
LB-D9		P1-105		
LB-D10		P1-106		
LB-D11		P1-107		
LB-D12		P1-108		
LB-D13		P1-109		
LB-D14		P1-112		
LB-D15		P1-111		
LB-RD#	nOE	P1-116	Output	**Local Bus Read Control.** Should be connected to output enable of the accessed device.
LB-WE#	nPWE	P1-118	Output	**Local Bus Write Control.** Should be connected to write enable of the accessed device.
LB-IORDY	RDY	P1-113	Input	**Local Bus I/O Ready input.** Notifies the bus controller when an external device is ready to transfer data.
LB-CS0#	nCS3	P1-133	Output	**Local Bus Chip Selects.** For devices such as SRAM, ROM, Flash and peripherals. Generated by onboard logic using nCS3 and MA[25:22] lines. The appropriate addresses are listed in the memory mapping table at the end of the manual.
LB-CS1#		P1-135		
LB-CS2# *		P3-68		
LB-CS3# *		P3-70		
LB-DREQ0 *	GPIO[97]	P3-69	Input	Local bus DMA request
LB-IRQ0	GPIO[1]	P1-51	Input	Local bus interrupt signals. Edge triggered. Pulse width > 1us.
LB-IRQ1	GPIO[101]	P1-54		

* LB-CS2, LB-CS3 and LB-DREQ0 are available only in CM-X270W.

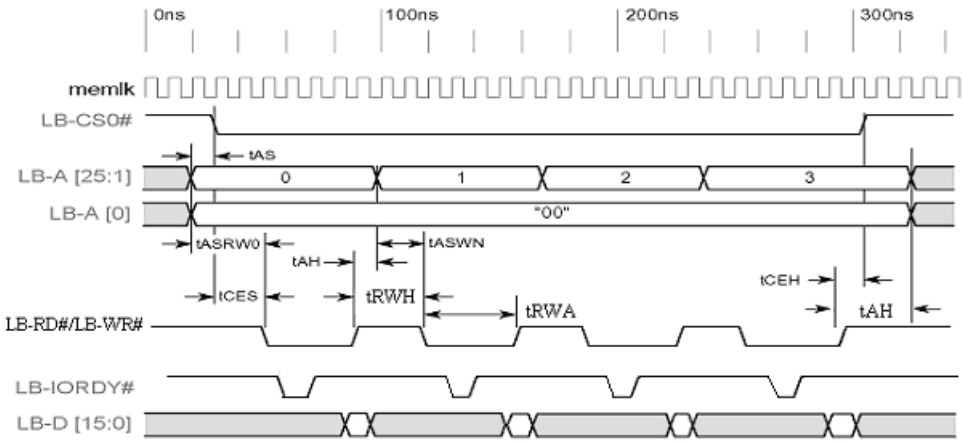
Local Bus Buffering

Local bus must be used very carefully, as bad routing, overloading or contention created by off-board circuitry will affect functionality of on-board components as well. As general rule, local bus should be buffered before any further routing or connection on the baseboard. Buffers should be located near the module's connectors. Buffers reference design is available in schematics of SB-X270 (simple) and ATX (more complicated) boards.

In simple baseboards, the designer can avoid buffers if baseboard trace length doesn't exceed 5 cm and the load is a single device having input capacitance below 20 pF.

Variable Latency I/O Interface

In reads and writes to VLIO, the processor samples the data-ready input - RDY (LB-IORDY#). When the internal RDY signal is high, the I/O device is ready for data transfer. If the RDY signal is low during LB-WR#/LB-RD# assertion, the assertion period is prolonged accordingly.
Data is latched on the rising edge of internal 200 MHz clock once the internal RDY signal is high and the minimum assertion time for LB-RD# has been reached. The chip select remains asserted for one clock cycle after the burst's final LB-RD# or LB-WR# deassertion. Refer to the figure below for Variable Latency I/O read timing and AC Specifications.



Symbol	Description	Delay (ns)
tAS	LB-A [25:0] setup to LB-CS#	15
tASRW0	LB-A [25:0] setup to LB-RD#/LB-WR#	25
tASRWN	LB-A [25:0] setup to LB-RD#/LB-WR# (next access)	MSC1[RDN3]+10
tAH	LB-A [25:0] hold after LB-RD#/LB-WR#	MSC1[RDN3]-10
tCES	LB-CS# setup to LB-RD#/LB-WR# asserted	10
tCEH	LB-CS# hold after LB-RD#/LB-WR# de-asserted	5
tDSW	LB-D [15:0] write data setup to LB-WR# de-asserted	MSC1[RDF3]*5+20
tDHW	LB-D [15:0] write data hold after LB-WR# de-asserted	MSC1[RRR3]*10-5
tDSR	LB-D [15:0] read data setup to LB-RD# de-asserted	20
tDHR	LB-D [15:0] read data hold after LB-RD# de-asserted	0
tRWA	LB-RD#/LB-WR# asserted	MSC1[RDF3]*5+5+waits
tRWH	LB-RD#/LB-WR# high time between beats of write data	MSC1[RDN3]*10
tCSH	LB-CS# de-asserted to LB-CS# asserted	MCS1[RRR3]*10+5
tRDYH	LB-IORDY hold after LB-RD#/LB-WR# de-asserted	0

- Encoding scheme for RDN and RDF:

ENCODED (Programmed) Value	DECODED (Actual) Value
0-11	0-11
12	15
13	20
14	26
15	30

- Minimum value for RDF is 3. Minimum value for RDN is 2.

In PXA270 processor, ‘nWE’ signal is used for accessing constant latency devices while ‘nPWE’ signal is used for accessing variable latency devices. In CM-X270, the ‘nPWE’ signal is routed out as local bus write enable. Therefore, the CS region for access of external devices must always be set to variable latency mode. There is no restriction in accessing constant latency devices in variable latency mode, and the RDY signal will always remain active in that case.

Use the memory interface configuration registers of the PXA270 processor to program the device access timings. The address map of the LB-CSx signals can be found in the end of this manual. Refer to section 6.5.3.1 in the PXA-270 developer manual for information about the MSC1 register. Note that all LB-CSx signals of the CM-X270 card are derived from PXA270's nCS3. If altering the values of the MSC1 register, remember that nCS3 should always be set to 16-bit width operation and VLIO mode.

The complete map of PXA270 memory space can be found on Fig. 28-2 in the PXA270 developer manual.

3.2. PCI Interface

The PCI interface is implemented by an Interface Bridge. On the PCI-bus side, it provides the following features:

- 32-bit data bus interface
- PCI rev. 2.1 specification support
- CPU to PCI buffers for burst transfer optimization
- A built-in PCI bus arbiter supports up to two individual external bus master devices
- 33 MHz PCI bus operation

On the processor bus side, it provides the following features:

- Direct access to the entire SDRAM address space
- Deep PCI to SDRAM buffers for burst transfer optimization
- Four independent DMA channels
- 96 MHz SDRAM bus operation

Master and Target Operation

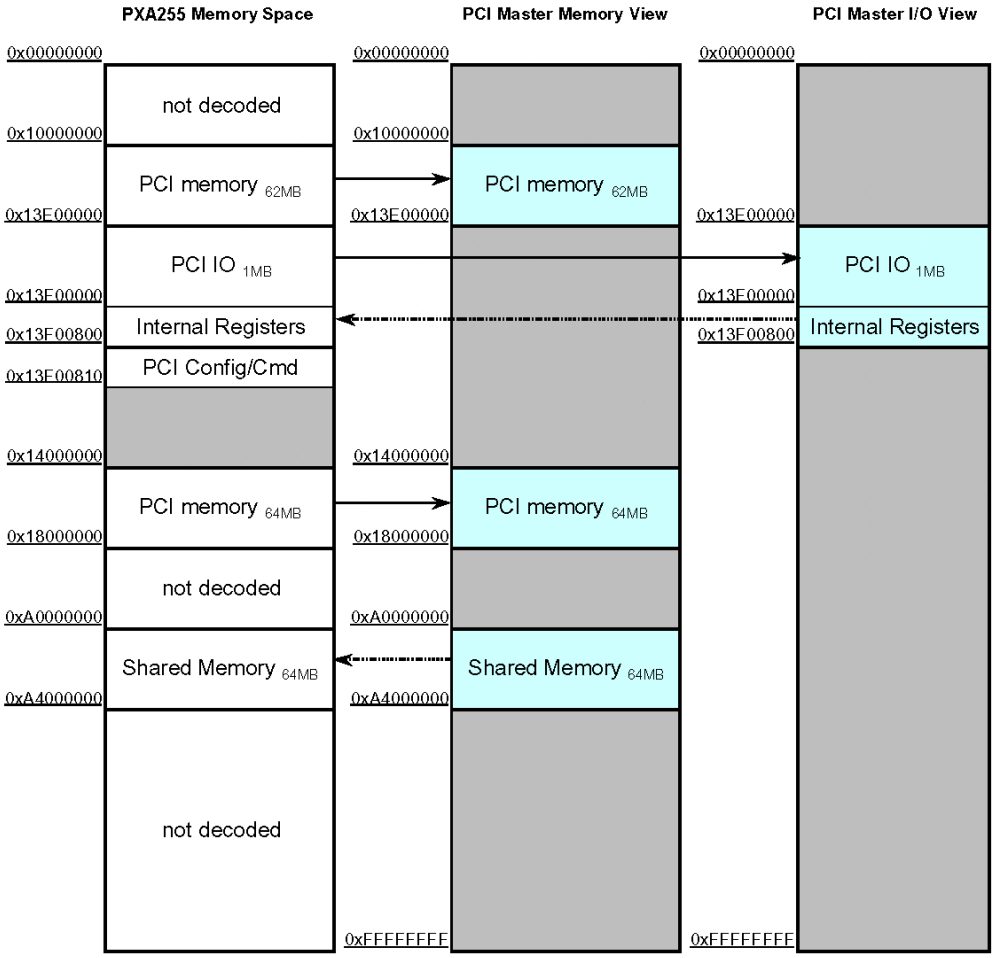
The CM-X270 includes an integrated PCI bus host bridge allowing the CM-X270 to interface with any PCI bus Revision 2.1-compliant master or target device.

(Note: the master is the device that initiates the PCI transfer. The slave, or target, is the device being addressed by the master for the data transfer.)

The PCI host bridge on the CM-X270 has the following functionality:

- **Master controller**—Allows the CPU to be a master on the PCI bus. The CPU can generate transactions to configure the PCI host bridge, as well as all external devices on the PCI bus. The CPU can also generate memory and I/O read and write transactions on the PCI bus.
- **Target controller**—Allows external PCI bus masters to access the CM-X270's on-board SDRAM.

The PCI bus is fully-compliant to the Revision 2.1 standard. Standard PCI slots can be connected to this bus. The arbiter in the core logic module provides support for four external bus masters. Arbiter signals are routed to an interface connector. For more PCI masters, the designer can use an external arbiter.



PCI to Memory Interface

The PCI interface supports PCI memory read/write transactions. The supported PCI commands are write, write and invalidate, read, read line and read multiple. The write and write and invalidate commands are treated the same. The read command is handled differently for read line and read multiple. If read prefetch is disabled, the read command will not prefetch, but read line and read multiple will prefetch in the current line (32 bytes alignment). The decoding speed is always medium decoding. Retry and disconnect with/without data are supported. The initial latency and subsequent latency timers are supported. To guarantee operation, CLKRUN# should not be asserted when the PCI bus is

non-idle, the write FIFO is not empty or when the read prefetch FIFO is not empty. PCI lock cycle (device lock) is also supported.

For PCI write transactions, data is posted to the write FIFO, then the data gathering mechanism will issue proper write commands to the SDRAM controller. All write cycles issued to the SDRAM controller are 32-byte aligned. The write FIFO is capable of containing 64 bytes. Once the FIFO is full, the PCI state machines will insert wait states until the FIFO is capable of receiving more data or will disconnect if the subsequent latency timer expires.

For PCI read transactions, if read prefetch is enabled, the prefetch mechanism will issue proper commands to prefetch data and queue it into the read FIFO. All read requests issued to the SDRAM controller are 32-byte aligned. At the end of a read transaction, the prefetch FIFO is flushed. If read data is not yet ready, wait states are inserted until the data is ready or until the latency timers expire to retry or disconnect the current read cycle. For data consistency, PCI read cycles will be delayed until the completion of all outstanding write cycles possibly posted to the write buffer.

PCI Clock System

The clock source is from an on-board oscillator. Normally the CM-X270 acts as a 'motherboard', providing clocks to all other parts of the application. The on-board clock source feeds all on-board PCI devices and also provides one clock output on the interface connector.

If a developer needs to synchronize with another PCI bus system, operated from different clock source PCI-to-PCI bridge can be used. Suitable bridges are available from HiNT, PLX and other manufacturers.

The PCI standard allows up to a 2ns clock skew. In order to minimize the initial skew value, the internal feedback path is designed with a 12 cm trace length - to create the initial delay. Feedback is provided to the clock generation block of the PCI bridge. The timing of all internal clock references is shifted accordingly. In other words, PCI signals are pre-compensated for an external clock trace length of 12 cm. The maximum allowed length of the external clock trace is:
12 cm (pre-compensated) + 30 cm (max propagation delay for a skew less than 2ns)

PCI Bus Signals

Signal	Pin Number	Type	Description
PCI-AD0	P2-20	B	**PCI Address Data Bus** is the PCI time-multiplexed PCI Address / PCI Data bus
PCI-AD1	P2-22	B	
PCI-AD2	P2-21	B	
PCI-AD3	P2-24	B	
PCI-AD4	P2-23	B	
PCI-AD5	P2-25	B	
PCI-AD6	P2-28	B	
PCI-AD7	P2-27	B	
PCI-AD8	P2-29	B	
PCI-AD9	P2-32	B	
PCI-AD10	P2-34	B	
PCI-AD11	P2-33	B	
PCI-AD12	P2-36	B	
PCI-AD13	P2-35	B	
PCI-AD14	P2-37	B	
PCI-AD15	P2-40	B	
PCI-AD16	P2-51	B	
PCI-AD17	P2-54	B	
PCI-AD18	P2-53	B	
PCI-AD19	P2-56	B	
PCI-AD20	P2-58	B	
PCI-AD21	P2-57	B	
PCI-AD22	P2-60	B	
PCI-AD23	P2-59	B	
PCI-AD24	P2-64	B	
PCI-AD25	P2-63	B	
PCI-AD26	P2-66	B	
PCI-AD27	P2-65	B	
PCI-AD28	P2-68	B	
PCI-AD29	P2-70	B	
PCI-AD30	P2-69	B	
PCI-AD31	P2-72	B	

PCI Bus Signals (continued)

Signal	Pin Number	Type	Description
PCI-CBE0#	P2-30	B	**Command or Byte-Enable Bus** functions: (1) as a time-multiplexed bus command that defines the type of transaction on the AD bus, or (2) as byte enables: CBE0 for AD7–AD0 CBE1 for AD15–AD8 CBE2 for AD23–AD16 CBE3 for AD31–AD24
PCI-CBE1#	P2-39	B	
PCI-CBE2#	P2-52	B	
PCI-CBE3#	P2-61	B	
PCI-DEVSEL#	P2-45	B	**Device Select** is asserted by the target when it has decoded its address as the target of the current transaction. This signal is pulled up on-board with an 8.2K resistor.
PCI-FRAME#	P2-49	B	**Frame** is driven by the transaction initiator to indicate the start and duration of the transaction. This signal is pulled up on-board with an 8.2K resistor.
PCI-GNT0#	P2-03	O	**Bus Grant(s)** are asserted by the CM-X270 to grant device(s) access to the bus. GNT2/3 are available only in CM-X270W
PCI-GNT1# **	P2-05	O	
PCI-GNT2#	P3-18	O	
PCI-GNT3#	P3-15	O	

PCI Bus Signals (continued)

Signal	Pin Number	Type	Description
PCI-INTA#	P2-06	I	**PCI Interrupt Requests** are asserted to request an interrupt. INTC/D are available only in CM-X270W
PCI-INTB#	P2-08	I	
PCI-INTC#	P3-20	I	
PCI-INTD#	P3-17	I	
PCI-IRDY#	P2-47	B	**Initiator Ready** is asserted by the current bus master to indicate that data is ready on the bus (write) or that the master is ready to accept data (read). This signal is pulled up on-board with an 8.2K resistor.
PCI-PAR	P2-42	B	**PCI Parity** is driven by the initiator or target to indicate parity on the AD31–AD0 and CBE3–CBE0 buses.
PCI-REQ0#	P2-01	I	**Bus Request(s)** are asserted by the master(s) to request access to the bus. REQ2/3 are available only in CM-X270W
PCI-REQ1# **	P2-18	I	
PCI-REQ2#	P3-22	I	
PCI-REQ3#	P3-13	I	
PCI-SERR#	P2-41	I	**System Error** is used for reporting address parity errors or any other system error where the result is fatal. This signal is pulled up on-board with an 8.2K resistor.
PCI-STOP#	P2-46	B	**Stop** is asserted by the target to request that the current bus transaction be stopped. This signal is pulled up on-board with an 8.2K resistor.
PCI-TRDY#	P2-48	B	**Target Ready** is asserted by the currently addressed target to indicate its ability to complete the current data phase of a transaction. This signal is pulled up on-board with an 8.2K resistor.
PCI-CLK0	P2-16	O	**PCI Bus Clock Output** is a 33-MHz clock for PCI bus devices. This signal is derived from an onboard 33MHz source. Clock edge position is internally compensated in order to reduce skew to a minimum.

** In CM-X270W, REQ1/GNT1 pair is different from other REQ/GNT. Its priority is higher that that of others, and even higher than of internal devices (PCI to local bus bridge and USB host). This can lead to run conditions in some cases. When possible, it is recommended to avoid using REQ1/GNT1 in CM-X270W.

Output drive and maximum load specifications are according to PCI bus Standard Rev-2.1.

PCI resource map

Device	IDSEL line	PCI dev. / func.	IRQ
Baseboard Ethernet chip	AD27	0x0F, func. 0	A
LPC bridge, GPIO control	AD12	0x1, func. 2	-
USB controller of Interface Bridge	AD12	0x1, func. 4	-

3.3. LPC - Low Pin Count Interface

The CM-X270 implements an LPC Interface and Controller as described in the LPC 1.0 specification. The Low Pin Count (LPC) Bridge function resides in PCI Device 1 function 2. The LPC bus provides a functional replacement for interfacing legacy ISA functions, such as the Super-I/O chip.

LPC Cycle Types
The bridge implements all of the cycle types described in the LPC Interface 1.0 specification. The table below shows the cycle types supported by the bridge.

LPC Cycle Types

Cycle Type	Comment
Memory Read	1 byte only
Memory Write	1 byte only
I/O Read	1 byte only. Controller breaks up 16 and 32-bit processor cycles into multiple 8-bit transfers.
I/O Write	1 byte only. Controller breaks up 16 and 32-bit processor cycles into multiple 8-bit transfers.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes.
Bus Master Write	Can be 1, 2, or 4 bytes.

I/O Cycles
For I/O cycle targeting registers specified in the controller's decode ranges, the controller performs I/O cycles as defined in the LPC specification. These are 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the controller breaks it up into multiple 8-bit transfers. If the cycle is not claimed by any peripheral (and is subsequently aborted), a

value of all 1's (FFh) is returned to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

Bus Master Cycles
The LPC interface supports Bus Master cycles and requests (using LDRQ#) as defined in the LPC specification. The controller has one LDRQ# input, and thus supports one separate bus master device. It uses the associated START fields for Bus Master 0.

LPC bus signals

Signal	Pin Number	Type	Description
LPC-LAD0	P2-10	I/O	LPC Multiplexed Command, Address, Data.
LPC-LAD1	P2-09	I/O	
LPC-LAD2	P2-12	I/O	
LPC-LAD3	P2-11	I/O	
LPC-LDRQ#	P2-17	I	LPC Serial DMA/Master Request Inputs
LPC-LFRAME#	P2-15	O	LPC Frame: Indicates the start of an LPC cycle, or an abort.
LPC-SERIRQ	P2-13	I	Serial Interrupt input

In addition to the above signals, an LPC device needs a PCI clock and the Reset (RST-OUT#) signal.

LPC Address Mapping

LPC access is mapped through 64K address region. Only I/O cycles on the LPC bus are supported. Physical address of the region is 0x13E00000 - 0x13E0FFFF.
Virtual mapping in Linux (kernel address space) is 0xe7E00000 - 0xe7E0FFFF.
The 16 least significant bits denote LPC addresses. For example the physical address 0x13E002F8 denotes address 0x2F8 on the LPC bus.

3.4. AC'97 Interface

The AC'97 Controller Unit (ACUNIT) of the PXA270 processor supports the AC'97 revision 2.0 features. The ACUNIT also supports the audio controller link (AC-link). The AC-link is a serial interface for transferring digital audio, modem, mic-in, CODEC register control, and status information.

The AC'97 CODEC sends the digitized audio samples that the ACUNIT stores in memory. For playback or synthesized audio production, the processor retrieves stored audio samples and sends them to the CODEC through the AC-link. The external digital-to-analog

converter (DAC) in the CODEC then converts the audio samples to an analog audio waveform.

Feature List

The processor's ACUNIT supports the following AC'97 features:

- Independent channels for stereo Pulse Code Modulated (PCM) In, Stereo PCM Out, modem-out, modem-in and mono mic-in All of the above channels support only 16-bit samples in hardware. Samples less than 16 bits are supported through software.
- Multiple sample rate AC'97 2.0 CODECs (48 kHz and below). The ACUNIT depends on the CODEC to control the varying rate.
- Read/write access to AC'97 registers
- Secondary CODEC support
- Three Receive FIFOs (32-bit, 16 entries)
- Two Transmit FIFOs (32-bit, 16 entries)

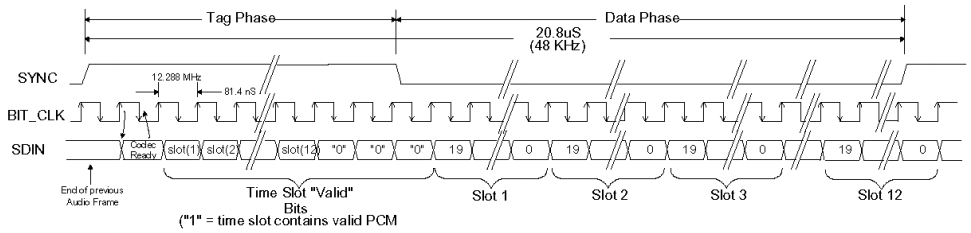
The processor's ACUNIT does not support these optional AC'97 features:

- Double-rate sampling (n+1 sample for PCM L, R & C)
- 18- and 20-bit sample lengths

AC-link Overview

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfers through individual frames transmitted in a serial fashion. Each frame is divided into twelve outgoing and twelve incoming data streams, or slots. The architecture of the AC-link allows a maximum of two codecs to be connected.

Figure 1 – AC-link waveforms



BIT_CLK is fixed at 12.288 MHz and is sourced by the primary codec - either on-board audio codec, or another codec off-board. It provides the necessary clocking to support twelve 20-bit time slots. AC-link serial data is transitioned on each rising edge of

BIT_CLK. The receiver of AC-link data samples each serial bit on the falling edge of BIT_CLK.

The AC97 controller via the AC_SYNC signal indicates synchronization of all AC-link data transactions. The primary codec drives the serial bit clock onto the AC-link, which the AC97 controller then qualifies with the AC_SYNC signal to construct data frames. AC_SYNC, fixed at 48 KHz, is derived by dividing down BIT_CLK. AC_SYNC remains high for a total duration of 16 BIT_CLK's at the beginning of each frame. The portion of the frame in which AC_SYNC is high is defined as the tag phase. The remainder of the frame, in which AC_SYNC is low, is defined as the data phase. Each data bit is sampled on the falling edge of BIT_CLK.

The AC97 controller has two SDIN pins: one - SDIN1 - is routed to interface connector and the other - SDIN0 - is permanently assigned for on-board codec.

AC97 link signals

Signal	Pin Number in X270W (X270L)	Type	Description
AC97-RST# [AUD-SPDIF]	P3-124 (P2-129)	O	**AC97 Reset:** Master H/W reset to external Codec(s)
AC97-SYNC [AUD-OUTR]	P3-125 (P2-136)	O	**AC97 Sync:** 48 KHz fixed rate sample sync to the Codec(s)
AC97-BITCLK [AUD-INL-MIC]	P3-120 (P2-132)	I	**AC97 Bit Clock:** 12.288 MHz serial data clock generated by the external Codec(s).
AC97-SDOUT [AUD-INR]	P3-123 (P2-130)	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). AC97-SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC97-SDIN1	P3-121	I	**AC97 Serial Data In 1:**Serial TDM data input from a Codec
AC97-SDIN0 [AUD-OUTL]	P3-119 (P2-131)	I	**AC97 Serial Data In 0:**Serial TDM data input from a Codec.
AC97_SYSCLK	P3-76	O	**24.576 MHz clock output** Available only in CM-X270W

In CM-X270W, AC97 signals are routed to 3rd connector, having dedicated pin assignments. The CM-X270L has only two connectors, therefore AC97 signals are sharing pins with Audio interface. Baseboard designer can connect 2nd and 3rd connector pins together to allow interchangeability between modules, assuming of course that on-board Audio chip is not assembled.

Note: if AC’97 pins are used as GPIOs, the AC’97 CODEC can not be operated at the same time.

I2S - Inter-Integrated-Circuit Sound Interface

I2S is a protocol for digital stereo audio. The I2S Controller (I2SC) functional block for the PXA270 processor controls the I2S link (I2SLINK), which is a low-power four-pin serial interface for stereo audio. The I2S interface and the Audio CODEC ‘97 (AC’97) interface may not be used at the same time.

The I2SC consists of buffers, status and control registers, serializer, and counters for transferring digitized audio between the processor system memory and an external I2S CODEC.

For playback of digitized audio or production of synthesized audio, the I2SC retrieves digitized audio samples from processor system memory and sends them to a CODEC through the I2SLINK. The external digital-to-analog converter in the CODEC then converts the audio samples into an analog audio waveform.

For recording of digitized audio, the I2SC receives digitized audio samples from a CODEC (through the I2SLINK) and stores them in processor system memory.

The I2Scontroller supports the normal-I2S and the MSB-Justified-I2S formats. Four pins connect the controller to an external CODEC:

- A bit-rate clock, which can use either an internal or an external source.
- A formatting or “Left/Right” control signal.
- Two serial audio pins, one input and one output.

The I2Sdata can be stored to and retrieved from system memory either by the DMA controller or by programmed I/O.

For I2S systems, additional pins are required to control the external CODEC. Some CODECs use an L3 control bus, which requires 3 signals — L3_CLK, L3_DATA, and L3_MODE — for writing bytes into the L3-bus register. The I2SC supports the L3 bus protocol via software control of the general-purpose I/O (GPIO) pins. The I2SC does not provide hardware control for the L3 bus protocol.

Two similar protocols exist for transmitting digitized stereo audio over a serial path: Normal-I2Sand MSB-Justified-I 2 S. Both work with a variety of clock rates, which can be obtained by dividing the PLL clock by a programmable divider, or from an external clock source.

I2S signals

Signal	Pin Number	Type	Description
BITCLK	P3-120 (P2-132)	I/O	BITCLK supplies the serial audio bit rate, which is the basis for the external CODEC bit-sampling logic. BITCLK is one-quarter the frequency of internal SYSCLK and is 64 times the audio sampling frequency. One bit of the serial audio data sample is transmitted or received each BITCLK period. A single serial audio sample comprises a “left” and “right” signal, each containing either 8, 16 or 32 bits
SYSCLK	P3-124 (P2-129)	O	All clocks in the I 2 S controller are based on the I2S_SYSCLK signal.I2S_SYSCLK generates a frequency between approximately 2 MHz and 12.2 MHz by dividing down the PLL clock with a programmable divisor. This frequency is always 256 times the audio sampling frequency. I2S_SYSCLK is driven out of the PXA27x processor only if I2S_BITCLK is configured as an output.
SYNC	P3-125 (P2-136)	O	SYNC is BITCLK divided by 64, resulting in an 8 kHz to 48 kHz signal. The state of SYNC is used to denote whether the current serial data samples are “Left” or “Right” channel data.
SDATA_IN	P3-119 (P2-131)	I	The SDATA_IN and SDATA_OUT data pins are used to send/receive the serial audio data to/from the CODEC.
SDATA_OUT	P3-123 (P2-130)	O	

I2S signals are sharing connector pins with AC97 interface.

Note: if onboard AC’97 CODEC is assembled, I2S interface cannot be used. As an alternative approach, external I2S CODECs can be connected on the SSP interface. Please refer to par. 8.4.11 in the PXA-270 CPU developer manual for more details.

3.5. SSP - Synchronous Serial Port Interface

The SSP is a synchronous serial interface that connects to a variety of external analog-to-digital (A/D) converters, telecommunication CODEC’s, and many other devices that use serial protocols for data transfer. The SSP provides support for the following protocols:

- Texas Instruments (TI) Synchronous Serial Protocol

- Motorola Serial Peripheral Interface (SPI) protocol
- National Semiconductor Microwire
- Programmable Serial Protocol (PSP)

The SSP operates as a full-duplex device for the TI Synchronous Serial Protocol, SPI, and PSP protocols and as a half-duplex device for the Microwire protocol. The FIFO's can be loaded or emptied by the CPU using programmed I/O or DMA burst transfers.

Features

- Supports the TI Synchronous Serial Protocol, the Motorola SPI protocol, National Semiconductor Microwire, and a Programmable Serial Protocol (PSP)
- Two independent transmit and receive FIFO's, each 16 samples deep by 32-bits wide
- Sample sizes from four to 32-bits
- Maximum bit rate of 13 Mbps in slave clocking mode (requires using DMA)
- Master-mode and slave-mode operation
- Receive-without-transmit operation

PXA270 processor has three independent SSP ports, named SSP1 – SSP3. Only the SSP1 port is routed to an CM-X270 connector. SSP pins share CIF (camera interface) functionality, thus either one of the interfaces can operate simultaneously.

SSP signals

Signal	Pin Number in X270W (X270L)	Type	Description
SSI-DIN [CIF-PCLK]	P3-88 (P1-59)	I	Serial input
SSI-DOUT [CIF-LV]	P3-78 (P2-90)	I/O	Serial output pin.
SSI-CLK [CIF-MCLK]	P3-108 (P2-88)	I/O	Serial clock
SSI-FRM [CIF-FV]	P3-93 (P2-87)	O	Gate signal for serial frame

3.6. I2C Bus Interface

The I2C is a serial bus with a two-pin interface. The data pin is used for input and output functions and the clock pin is used to control and reference the I2C bus. The I2C unit allows the processor to serve as a master and slave device that resides on the I2C bus.

The I2C unit enables the processor to communicate with I2C peripherals and microcontrollers for system management functions. The I2C bus requires a minimal amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

The I2C unit is a peripheral device that resides on the processor's internal bus. Data is transmitted to and received from the I2C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to *The I2C-Bus Specification* for complete details on I2C bus operation.

The I2C unit does not support hardware general call, 10-bit addressing, or CBUS compatibility.

I2C signals

Signal	Pin Number	Type	Description
SDA	P1-60	I/O	I2C data
SCL	P1-61	I/O	I2C clock

Functional Description

The I2C bus defines a serial protocol for passing information between agents on the I2C bus using a two pin interface that consists of a Serial Data/Address (SDA) line and a Serial Clock Line (SCL). Each device on the I2C bus is recognized by a unique 7-bit address and can operate as a transmitter or as a receiver in master or slave mode. The table below lists I2C operation modes.

I2C Device	Definition
Transmitter	Sends data to the I2C bus.
Receiver	Receives data from the I2C bus.
Master	Initiates a transfer, generates the clock signal, and terminates the transactions.
Slave	Device addressed by a master.
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	Ensures that only one master controls the bus when more than one simultaneously tries to do so. This ensures that messages are not corrupted.

The I2C bus allows for a multi-master system, which means that more than one device can initiate data transfers at the same time. To support this feature, the I2C bus arbitration relies on the wired-AND connection of all I2C interfaces to the I2C bus. Two masters can drive the bus simultaneously, provided they drive identical data. If a master tries to drive SDA high while another master drives SDA low, it loses the arbitration. The SCL line is a synchronized combination of clocks generated by the masters using the wired-AND connection to the SCL line.

I2C bus serial operation uses an open-drain wired-AND bus structure, which allows multiple devices to drive the bus lines and to communicate status about events such as arbitration, wait states, error conditions, etc. For example, when a master drives the clock (SCL) line during a data transfer, it transfers a bit on every instance that the clock is high. When the slave is unable to accept or drive data at the rate the master requests, the slave can hold the clock line low between the high states to insert a wait interval. The master's clock can only be altered by another master during arbitration or a slow slave peripheral that keeps the clock line low.

I2C transactions are either initiated by the processor as a master or received by the processor as a slave. Both conditions may result in reads, writes or both to the I2C bus.

Operational Blocks

The I2C unit is connected to the peripheral bus. The processor interrupt mechanism can be used to notify the CPU that there is activity on the I2C bus. Polling can be used instead of interrupts. The I2C unit consists of the two wire interface to the I2C bus, an 8-bit buffer for passing data to and from the processor, a set of control and status registers and a shift register for parallel/serial conversions.

The I2C unit initiates an interrupt to the processor when a buffer is full, a buffer is empty, the I2C unit slave address is detected, arbitration is lost or a bus error condition occurs. All interrupt conditions must be cleared explicitly by software.

The 8-bit I2C Data Buffer Register (IDBR) is loaded with a byte of data from the shift register interface to the I2C bus when receiving data and from the processor internal bus when writing data. The serial shift register is not user accessible.

The I2C Control Register (ICR) and the I2C Status Register (ISR) are located in the I2C memory-mapped address space.

The I2C unit supports fast mode operation of 400 Kbits/sec and a standard mode of 100 Kbits/sec.

I2C Bus Interface Modes

The I2C unit can accomplish a transfer in different operation modes. The following table summarizes the different modes.

Mode	Description
Master - Transmit	• I2C unit acts as a master. • Used for a write operation • I2C unit sends the data. • I2C unit is responsible for clocking. • Slave device in slave-receive mode
Master - Receive	• I2C unit acts as a master. • Used for a read operation • I2C unit receives the data. • I2C unit is responsible for clocking. • Slave device in slave-transmit mode
Slave - Transmit	• I2C unit acts as a slave. • Used for a master read operation • I2C unit sends the data. • Master device in master-receive mode
Slave - Receive (default)	• I2C unit acts as a slave. • Used for a master write operation • I2C unit receives the data. • Master device in master-transmit mode

While the I2C unit is idle, it defaults to slave-receive mode. This allows the interface to monitor the bus and receive any slave addresses intended for the processor.

When the I2C unit receives an address that matches the 7-bit address found in the I2C Slave Address Register (ISAR) or the general call address, the interface either remains in slave-receive mode or transitions to slave-transmit mode. The Read/Write bit (R/nW) determines which mode the interface enters. The R/nW bit is the least significant bit of the byte containing the slave address. If the R/nW bit is low, the master that initiated the transaction intends write data and the I2C unit remains in slave-receive mode. If the R/nW is high, the master that initiated the transaction intends to read data and the I2C unit transitions to slave-transmit mode.

When the I2C unit initiates a read or write on the I2C bus, it transitions from the default slave-receive mode to the master-transmit mode. If the transaction is a write, the I2C unit

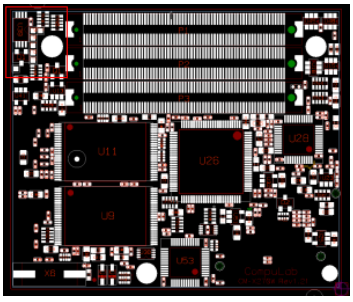
remains in master-transmit mode after the address transfer is completed. If the transaction is a read, the I2C unit transmits the start address, then transitions to master-receive mode.

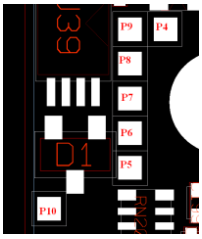
I2C signals - see previous SSP section.

3.7. JTAG Interface

JTAG interface allows access to processor and memory, mainly for purpose of code debugging. In CM-X270W, JTAG interface pins are available on 3rd CAMI connector and also as contact pads on PCB (only in CM-X270W rev 1.x).

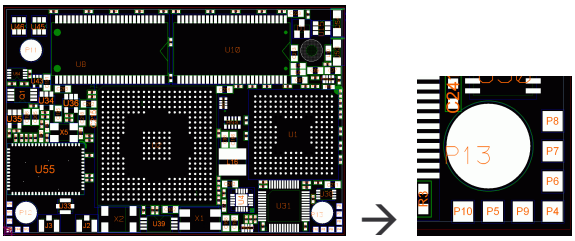
Signal	Pin	Type	Description
JTAG-TCK	P3-77	I	**Test Clock** is the input clock for the test access port.
JTAG-TDI	P3-83	I	**Test Data Input** is the serial input stream for input data. This pin has a weak internal pull-up resistor. It is sampled on the rising edge of TCK. If not driven, this input is sampled High internally.
JTAG-TDO	P3-85	O/TS	**Test Data Output** is the serial output stream for result data. It is in high-impedance state except when scanning is in progress.
JTAG-TMS	P3-81	I	**Test Mode Select** is an input for controlling the test access port. This pin has a weak internal pull-up resistor. If it is not driven, it is sampled High internally.
JTAG-TRST#	P3-87	I	**JTAG Reset** is the test access port (TAP) reset. This pin has a 8.2K internal pullup resistor.





VCC3 - P4
TRST# - P5 (optional)
TMS - P6
TDO - P7
TDI - P8
TCK - P9
GND - P10

In CM-X270L module, JTAG interface is available on PCB pads:



VCC3 - P4
TRST# - P5 (optional)
TMS - P6
TDO - P7
TDI - P8
TCK - P9
GND - P10

4. System Logic

This chapter describes the on-board hardware resources such as DMA's, Timers, Interrupt Controller and Real Time Clock used to manage system operation,.

4.1. Reset Options

Reset of processor can be initiated by one of the following options:

- RST-IN# - a nonmaskable hardware reset. It can be used at power up or when no system information requires preservation. Note that assertion on power up is not mandatory, as power up reset is generated on-board.
- Watchdog reset is asserted through the watchdog timer and resets the system except for the Clocks and Power Manager. This reset is used as a code monitor. If code fails to complete a specified sequence, the processor assumes a fatal system error has occurred and causes a watchdog reset.
- GPIO1 reset can be enabled through the GPIO alternate function registers. It is used as an alternative to hardware reset to preserve the memory controller registers and a few critical states in the Clocks, Power Manager and the Real Time Clock (RTC).

Reset Sequence

[RST-IN or powerup] >> [Processor] >> [All components & RST-OUT]

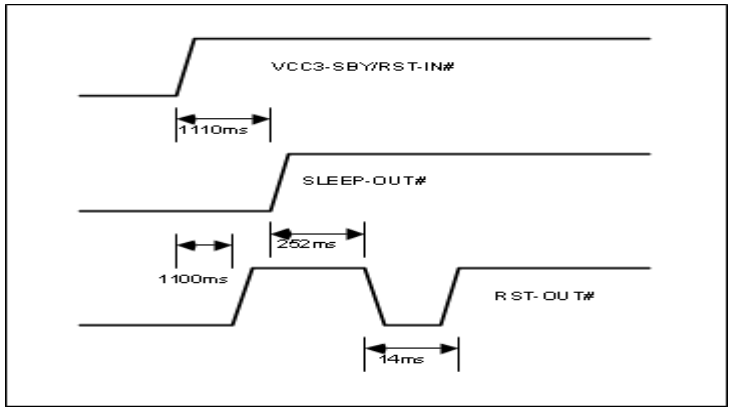
RST-OUT# will be asserted in the following conditions:

- RST-IN# assertion.
- During an ordered boot sequence (RST-OUT# is generated by the bootloader).

Reset/power rail control signals

CM-X270 Signal Name	CAMI Pin	Type	Description
RST-IN#	P1-11	In	Hardware Reset, initiates reset sequence for all on-board components, equivalent to power up reset. Active low. Pulled up on board by 8.2K resistor.
RST-OUT#	P1-137	Out	Indication from on-board reset logic that components are being reset. Active low.
SLEEP-OUT#	P3-95 (P2-89)	Out	Indication from on-board power manager to turn on main power rails.

Power ON/RST_IN# timings:



4.2. Power Supply & Management

Power Supply Considerations

The CM-X270 with all options other than "A" (but "AT" is okay) can operate with a single 3.3 Volt supply. In this case all supply pins, including those of 5V supply, should be connected to the 3.3V power net.

If "A" option included – the CM-X270 requires both 3.3V and 5V supply voltages for proper operation.

All VCORE power pins should also be connected to 3.3V net. The CM-X270 has an on-board 3.3V-to-VCORE high-efficiency switched converter, therefore the option of external VCORE supply is not required (and not supported) for CM-X270.

Power Net Description

Signal	Voltage	Description
VCC3-3 VCORE	3.3 V 3.6V with GPRS	Common 3.3 Volt power supply, for most functional blocks of the CM-X270. Maximum turn on ramp rate for cards without B option: 12mV/uS Maximum turn on ramp rate for cards with B option: 3.3mV/uS
VCC5	5.0 V	5.0 Volt power supply. Required only if "A" option assembled.
VCC3-SBY	3.3V 3.6V with GPRS	Standby supply, for deep sleep mode. In sleep mode designer can cut off all other supply voltages, leaving only Standby. It will retain SDRAM contents and required CPU state, in order to wakeup on request.
VCC-RTC	1.4 V to 3.3 V	Power for optional V3020 real time clock. This pin can be driven independently of all other power pins, from an external lithium battery. Its typical current consumption is below 0.4 uA.

Notes

- Except when otherwise specified, allowed tolerance on all power rails is ± 5%
- If any of above-mentioned supply functions are not used, respective supply pins must be connected to VCC3 power rail.
- Cards with GPRS option must be powered by 3.6V supply.

System & component consumption in mA

Description	Max Activity			Idle			Sleep, Power On			Sleep, Power Off		
	3v	5v	SB	3v	5v	SB	3v	5v	SB	3v	5v	SB
CM-X270 basic system	550	-	100	300	-	10	35	-	8	0	-	8
Interface Bridge	112	-	-	111	-	-	0	-	-	0	-	-
Ethernet	37	-	-	37	-	-	11	-	-	0	-	-
Audio codec ("A" option)	32	36	-	23	36	-	1	6	-	0	0	-

- All specified consumption values are typical. Momentary peak values can exceed typical values by factor of two.
- The measurements specificed in the above table were made on CM-X270W-D64-F4-C520-MG-N128-B-E-A-R configuration.
- CM-X270 basic system - with SDRAM, NOR, NAND and peripherals integrated into PXA270 chip.
- Maximum activity is achieved by ARMmon busy loop. Idle - under Linux. Sleep - entered from Linux or ARMmon.
- Idle mode: the processor core is not being clocked, but the rest of the system is fully operational. This mode is used during brief lulls in activity, when the external system must continue operation but the processor core is idle. Linux and Win CE operating system put the processor in Idle state when application is inactive.
- 3V - total consumption from VCC3/VCORE rails
- SB - consumption from Standby rail in CM-X270W. Mainly depends on SDRAM size: 8 mA for 64 MB, 14 mA for 128 MB.

Power Supply Pins

GND	P1-08, P1-14, P1-26, P1-38, P1-50, P1-62, P1-74, P1-86, P1-98, P1-110, P1-122, P1-134, P2-02, P2-14, P2-26, P2-38, P2-50, P2-62, P2-74, P2-86, P2-98, P2-110, P2-122, P2-134 P3-08, P3-14, P3-26, P3-38, P3-50, P3-62, P3-74, P3-86, P3-98, P3-110, P3-122, P3-134
VCC3	P1-67, P1-103, P1-139, P2-07, P2-43, P2-79, P2-135 P3-19, P3-55, P3-91, P3-127, P3-135
VCC5	P1-140, P3-131
VCORE	P1-07, P1-19, P1-43, P1-55, P1-79, P1-91, P1-115, P1-127, P2-19, P2-31, P2-55, P2-67, P2-91, P2-103, P2-115, P2-127 P3-07, P3-31, P3-43, P3-67, P3-79, P3-103, P3-115
VCC-RTC	P1-20
VCC3-STBY	P1-31 P3-102, P3-104, P3-106, P3-107, P3-109, P3-111

Sleep mode

Sleep Mode is the most power saving mode supported by the CM-X270. In sleep mode, the processor, interface bridge, Ethernet and all other peripherals are disabled. The system designer can cut off power supply to processor's core and peripherals. The system retains the SDRAM contents and the minimal register settings required to return to normal operation. Sleep mode is entered into by a software command. Developer can implement entering to sleep mode on external event (for example - using GPIO) by writing interrupt service routine which issues sleep command to the operating system.

Sleep mode is exited on a Power Management Event (PME). Possible sources of a PME are:

- Alarm timer. The alarm timer allows the application to periodically enter and exit sleep mode, in order to check the state of peripherals which are not able to generate a PME themselves.
- LB-IRQ0 pin on the CAMI connector - PXA-270 GPIO[1]
- PME# pin on the CAMI connector – PXA-270 GPIO[0]
  Note: PME# is buffered on CM-X270W rev 1.x and on CM-X270L rev 1.1, which creates conseptual problem: if 3.3V rail is not powered during sleep, PME# cannot be used. In this case use LB-IRQ0 as external wakeup source. In higher versions of mentioned cards this problem doesn't exsist and PME# can be used.

User can implement sleep mode exit on events from other sources, such as USB, serial ports or Ethernet by tying the source signal to PME# / LB-IRQ0 pin. However, in certain cases such connection of peripheral signal to PME# / LB-IRQ0 pin requires additional buffering or logic.

Processor exits sleep mode (i.e. begins executing code) in less than 1 ms after PME. But the actual time of system wake up depends on operating system drivers, functional blocks used on-board, and external peripherals connected. With slow-awaking peripherals, such as hard disk or USB device, exit from sleep can take several seconds.

While in sleep mode with all but standby power cut off, a fully populated CM-X270 board consumes 5-14 mA from a 3.3V source, depending on card's SDRAM size. Sleep mode support is built into the Linux and Win CE packages for CM-X270. Documented source code for power management is available with the CM-X270's Linux kernel package. On-board peripherals are getting hardware reset during sleep state, and RST-OUT# signal is driven low.

A dedicated signal SLEEP-OUT# (PXA-270 SYS_EN signal) is available on P3-95 (X270W) or P2-89 (X270L) and could be used to turn VCC3-3 & VCORE power rails on and off. If SLEEP-OUT# is used to control the power rails, they must be switched within 125ms from SLEEP-OUT# deassertion.

VCC3-STBY current consumption

Standby rail implementation is different in CM-X270W and CM-X270L.
In X270W standby power delivered through 6 pins of P3 and one pin of P1. These pins deliver power to SDRAM and parts of CPU in all modes, including active and sleep. During normal operation peak current can reach 800 mA. User must connect all Standby pins to 3.3V source.

The X270L doesn't have P3, therefore Standby power delivered to SDRAM only through single pin of P1. It is used only during Sleep mode, when current consumption is low. In normal operation the power to SDRAM delivered from VCC3-3 rail. Power source switching implemented on-board by FET.

4.3. Watchdog and Timers

Timers of the PXA270 processor

The operating-system timers block provides a set of timer channels that allows software to generate timed interrupts (or wake-up events). In the PXA270 processor, these interrupts are generated by two sets of timer channels. The first set, which provides one counter and four match registers, is clocked from a 3.25-MHz clock. The other set, which provides eight counters and eight match registers, can be clocked from either the 32.768-kHz timer clock, a 13-MHz clock, or an externally supplied clock, providing a wide range of timer resolutions.

The Operating System Count register (OSCR) is a free running up-counter. The OS timer also contains four 32-bit match registers (OSMR3, OSMR2, OSMR1, OSMR0). Developers can read and write to each register. When the value in the OSCR is equal to the value within any of the match registers, and the interrupt enable bit is set, the corresponding bit in the OSSR is set. These bits are also routed to the interrupt controller where they can be programmed to cause an interrupt. OSMR3 also serves as a watchdog match register that resets the processor when a match occurs provided that the OS Timer Watchdog Match Enable Register (OWER) is set. You must initialize the OSCR and OSMR and clear any set status bits before the interrupts are enabled within the CPU.

Developers can use the OSMR3 as a watchdog compare register. This function is enabled by setting OWER[0]. When a compare against this register occurs and the watchdog is enabled, reset is applied to the processor and most internal states are cleared. Internal reset is asserted for 256 processor clocks and then removed, allowing the processor to boot.

The following procedure is suggested when using OSMR3 as a watchdog – each time the operating system services the register:

1. The current value of the counter is read.
2. An offset is then added to the read value. This offset corresponds to the amount of time before the next time-out (care must be taken to account for counter wraparound).
3. The updated value is written back to OSMR3.

The OS code must repeat this procedure periodically before each match occurs. If a match occurs, the OS timer asserts a reset to the processor.

In addition to the OSCR0 and four match registers OSMR0–3,the processor provides eight additional timer channels (OSCR4–11) with a wider range of counter resolutions, interval and periodic timers, synchronization features, output waveform generation, and low-power mode operability.

Additional information on the OS timers block can be found in chap. 22 in the PXA-270 manual.

CM-X255 compatibility

The one Count register OSCR0 and four Match registers OSMR0–3 are identical to those in the PXA255 processor. The watchdog-reset functionality is also unchanged. However, the input clock that increments OSCR0 has changed. For the PXA25x processor, this clock was 3.6864 MHz. For the PXA270 processor, the clock frequency is 3.25 MHz. Software must recalculate any time periods that must be exact.

Timer of Interface Bridge

An additional timer is provided by the Interface Bridge chip. The Timer provides 4-channel 24-bit auto-reloaded counters with pre-scale 1, 1/16 or 1/256 and it supports interrupt generation.

4.4. Real-Time Clocks

The CM-X270 has two distinct Real-Time Clocks - one provided by the PXA270 CPU and the other implemented by the optional V3020 chip. The optional V3020 RTC allows the CM-X270 to perform timekeeping functions while rest of the card is unpowered.

RTC of the PXA270 processor

This section explains the RTC functions of the PXA270 CPU. It is called CPURTC through the rest of the section. The V3020 RTC is explained in subsequent sections.

The CPURTC provides five basic functions: Timer, Wristwatch, Stopwatch, Periodic, interrupt and Trimmer:

- Timer Section
  - User-programmable, free-running counter
  - User-programmable alarm register
  - Resolution of one second
- Wristwatch Section
  - User-programmable, free-running counter containing time of the day in terms of hours, minutes, seconds, day of week, week of month, day of month, month and year.
  - User-programmable alarm registers to generate alarms in terms of hours, minutes, seconds, day of week, week of month, day of month, month, and year.
  - Resolution of one second
- Stopwatch Section
  - Programmable counter register that contains the time elapsed between two events in terms of hours, minutes, seconds, and hundredths of a second.
  - Two user-programmable alarm registers to generate alarms in terms of hours, minutes, seconds, and hundredths of a second.
  - Resolution of one 100^{th} of a second
- Periodic Interrupt Section
  - Programmable alarm register to generate periodic interrupts at regular intervals
  - Resolution of one millisecond

Each section has one or more counter registers and one or more corresponding alarm registers. For example, the timer section has one counter register and one alarm register. First, the desired alarm set conditions are written to the alarm register. The corresponding alarm-enable bit in the CPURTC Status register (RTSR) is then set. If a counter has a count-enable bit, the corresponding count-enable bit must be set to enable the counter to start counting. The count-enable bits for the corresponding counter registers reside in the RTSR. The stopwatch and periodic-interrupt sections have count-enable bits, while the

timer and wristwatch sections consist of free-running counters without any count-enable bits.

When the data in the counter register and the alarm register are equal, the CPURTC controller signals the power manager, regardless of the state of the corresponding alarm-enable bit in the RTSR. The CPURTC controller then checks whether the corresponding alarm-enable bit in the RTSR has been set. If so, the corresponding alarm-detect bit in the RTSR is set, indicating an alarm has been detected. This information is forwarded to the interrupt controller. The corresponding alarm-detect bit in the RTSR is cleared by writing a one to it. This process is identical for all alarm-detection events.

Timer

The Timer section consists of a free-running counter, the RTC Counter register (RCNR), which starts incrementing after the deassertion of hardware reset or watchdog reset. The count value is incremented at each rising edge of the 1-Hz clock. This value of this counter can be altered by writing to it. The value of the counter is unaffected by transitions into and out of sleep or idle modes. The corresponding RTC Alarm register, RTAR, can be written with a value to be compared against the counter. On each rising edge of the 1-Hz clock, the counter is incremented and then compared to the value of RTAR. If the values match, and if the alarm-enable bit (RTSR[ALE]) is set, the corresponding alarm-detect bit (RTSR[AL]) is set.

Additional information about CPURTC can be found in chap. 21 of the PXA-270 manual.

The divider logic for generating the HZ clock is programmable. This lets to trim the counter to adjust for inherent inaccuracies in the crystal. The trimming mechanism allows adjusting the CPURTC to an accuracy of +/- 5 seconds per month.

All registers in the CPURTC, with the exception of RTTR, are reset by a hardware reset or a watchdog reset. The trim register, RTTR, is reset only by a hardware reset.

V3020 RTC

The major advantage of EM Microelectronics' V3020 RTC is that it can be powered from external source (such as lithium battery) while CM-X270 is turned off. The RTC integrated into PXA270 processor doesn't support this key feature.

To preserve its functionality V3020 RTC must be power from 1.4V to 5V source, supplying 0.4 uA (microampere) current.

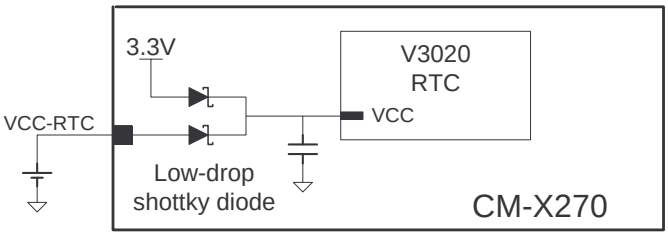
The real-time clock/calendar provides seconds, minutes, hours, day, date, month, year, and century information. A time/date programmable polled ALARM is included. The end-of-the-month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year up to the year 2100. The clock operates in either the 24hr or 12hr format with an AM/PM indicator.

Setting the time and date of V3020 RTC is supported through ARMmon, Linux and Win CE packages provided for CM-X270.

Interface

V3020 RTC uses single line serial I/O interface, implemented using standard R/W operations and MD[16] local bus data line at physical address 0x05400000 in the PXA-270 CPU memory space.

The RTC uses a dedicated lithium backup battery when the rest of the card is powered down. The battery should be connected to the VCC-RTC input of CAMI connector. The equivalent RTC supply circuit is shown in the figure below.



4.5. Interrupt Controller

The interrupt controller can receive interrupts from onboard peripherals or GPIO pins of the CPU. The list of the interrupts present in the PXA270 CPU along with their bit positions in the interrupt controller status registers can be found on page 25-5 (par 25.4.3) in the PXA270 manual.

In general, each GPIO line of the PXA270 CPU can be used as an external interrupt input. The selection of interrupt assignment is controlled by a number of mask and status registers, as described below and in the PXA270 Developers Manual.

GPIO pins interrupts are divided into three groups: GPIO0, GPIO1 and the rest of GPIO pins which are OR-ed and presented as one interrupt to the system.

GPIO[0] is assigned to be PME (power management event) signal of the system. Both PME# signal of the CAMI connector and PME output of the onboard Ethernet controller are OR-ed using onboard logic and connected to GPIO[0].

There are dedicated general purpose interrupt pins on the CAMI connector:
GPIO[1] is connected to the LB-IRQ0 signal of the CAMI.
GPIO[101] is connected to LB-IRQ1 pin of the CAMI.

Other interrupt (GPIO) lines are shared with alternate functions and are routed to connector locations according to the alternate function. If the designer wants to reserve the option of switching to another computer-on-module without redesigning his base board, only the above-mentioned lines should be used as interrupts.

Some of the GPIO pins are used as interrupts onboard the CM-X270 peripherals:

Peripheral name	**GPIO #**
DM9000 ethernet controller	10
UCB1400 (touchscreen subsystem)	96
IT8152 PCI bridge	22

4.6. DMA Controller of the PXA270 Processor

The PXA270 processor contains a direct-memory access (DMA) controller that transfers data to and from memory in response to requests generated by peripheral devices or companion chips. The peripheral devices and companion chips do not directly supply addresses and commands to the memory controller. Instead, the states required to manage a

data stream are maintained in 32 DMA channels, DMA[31:0], in the DMA controller. The DMA controller supports flow-through and fly-by transfers.

Features

- Memory-to-memory data transfers in flow-through mode.
- Data transfers for peripheral-bus peripherals (PBP). Supported types are PBP-to-memory and memory-to-PBP transfers, both in flow-through mode only.
- Data transfers for internal-bus peripherals (IBPs) such as the quick capture (video) interface. The only supported transfer types are IBP-to-memory and flow-through mode.
- 32 channels, 68 PBP requests, 3 IBP requests, and 3 external device requests. Allows any request to a channel to be pre-programmed.
- A priority mechanism to process active channels (four channels with outstanding DMA requests at any given time).
- Each of the 32 channels can operate for descriptor-fetch or no-descriptor-fetch transfers.
- Special descriptor modes (descriptor comparison and descriptor branching).
- Retrieval of trailing bytes in the receive peripheral-device buffers.
- Programmable data-burst sizes (8, 16, or 32 bytes) and programmable peripheral device data widths (byte, half word, or word)
- Up to (8 Kbytes –1) bytes of data transfer per descriptor. Larger transfers can be performed by chaining multiple descriptors.
- Flow-control bits to process requests from peripheral devices. Requests are not processed unless the flow-control bit is set.

In both WinCE and Linux there is a dynamic management of DMA channel assignment upon request from the drivers.

4.7. DMA Controller of the Interface Bridge

In addition to the DMAC of PXA270 processor, another DMA Controller is provided by the Interface Bridge chip. It is named Chaining DMA (CDMA). The CDMA controller is PCI function 1 in the Interface Bridge. The CDMA is able to support four independent DMA channels capable of transferring data between SDRAM and PCI devices. Each channel supports both chaining and non-chaining transfers. In addition, both PCI memory device address and PCI I/O device address are supported.

The Chaining DMA (CDMA) controller is capable of unaligned transfers: when bits 0 – 1 of the initial address in PCI space are not equal to bits 0 – 1 of the initial address in SDRAM space.

CDMA channels are not used by any CM-X270 / SB-X270 on-board devices and they are available for user hardware implementation.

CDMA Features

- Four independent DMA channels
- Chaining and non-chaining modes
- PCI memory space and I/O space addressing
- Rotating and fixed priority modes
- Supports transfers to unaligned addresses

5. Peripheral Interface

This chapter describes controllers and interfaces to peripheral functions such as GPIO, Ethernet, COM ports, PCMCIA and USB.

5.1. General Purpose I/O

CM-X270 has 80 GPIO pins, almost all of which are shared with alternate functions provided by the CPU. Each pin can be programmed as either an input or output. When programmed to be an input, a GPIO can also serve as an interrupt source. On power-up, most GPIO pins are configured by ARMMON to their alternate function; however, this can be changed by the user if the alternate function is not required.

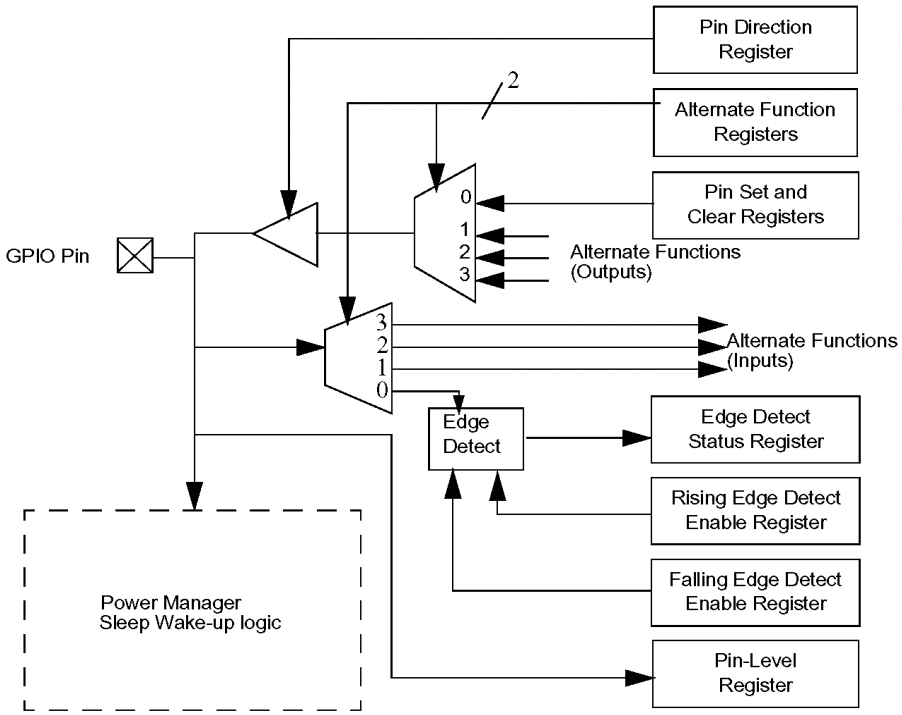
Use the GPIO Pin Direction Register (GPDR) to set the GPIO pins as outputs or inputs. When programmed as an output, the pin can be set high by writing to the GPIO Pin Output Set Register (GPSR) and cleared low by writing to the GPIO Pin Output Clear Register (GPCR). It is possible to write to the set and clear registers regardless of whether the pin is configured as an input or an output. If a pin is configured as an input, the programmed output state occurs when the pin is reconfigured as an output.

Validate each GPIO pin's state by reading the GPIO Pin Level Register (GPLR). You can read this register any time to confirm the state of a pin. In addition, use the GPIO Rising Edge Detect Enable Register (GRER) and GPIO Falling Edge Detect Enable Register (GFER) to detect either a rising edge or falling edge on a given GPIO pin. Use the GPIO Edge Detect Status register (GEDR) to read edge detect state. Developers can program these edge detects to generate interrupts

The following GPIO pins can be used as wakeup sources in standby and sleep mode:
GPIO # 113, 53, 40, 38, 35, 31, 15:9, 4:3, 1:0
Only GPIO # 1:0 can be used as wakeup source in deep-sleep mode.

Most GPIO pins can also serve an alternate function within the processor. These functions are hardwired into specific GPIO pins and their use is described in the following paragraphs. The figure below shows a block diagram of a single GPIO pin.

General-Purpose I/O Block Diagram



GPIO Alternate Functions

GPIO pins can have as many as six alternate functions that can be set to enable additional functionality within the processor. If a GPIO is used for an alternate function, then it cannot be used as a GPIO at the same time. The table below lists each GPIO pin and its corresponding alternate functions.

CAMI Pin X270W (X270L)	CPU GPIO	Alternate #1 In	Alternate #2 In	Alternate #3 In	Alternate #1 Out	Alternate #2 Out	Alternate #3 Out
P1-51	1						
P3-44 (P1-33)	12	EXT-SYNC[1]	CIF-DD[7]		CHOUT[1]	PWM-OUT[3]	48-MHz
P3-42	14	L-VSYNC	SSP-SFRM2			SSP-SFRM2	UCLK
P3-96 (P2-82)	17	KP-MKIN[6]	CIF-DD[6]			PWM-OUT[1]	
P3-40	19	SSP-SCLK2		FFRXD	SSP-SCLK2	L-CS	nURST
P3-108 (P2-88)	23		SSP-SCLK		CIF-MCLK	SSP-SCLK	
P3-93 (P2-87)	24	CIF-FV	SSP-SFRM		CIF-FV	SSP-SFRM	
P3-78 (P2-90)	25	CIF-LV			CIF-LV	SSPTXD	
P3-88 (P1-59)	26	SSPRXD	CIF-PCLK	FFCTS			
P3-80 (P2-81)	27	SSP-EXTCLK	SSP-SCLKEN	CIF-DD[0]	SSP-SYSCLK		FFRTS
P3-120 (P2-132)	28	AC97-BITCLK	I2S-BITCLK	SSPSFRM	I2S-BITCLK		SSP-SFRM
P3-119 (P2-131)	29	AC97_SDATA_IN_0	I2S_SDATA_IN	SSPSCLK	SSPRXD2		SSPSCLK
P3-123 (P2-130)	30				I2S-SDATA-OUT	AC97-SDATA-OUT	USB-P3-2
P3-125 (P2-136)	31				I2S-SYNC	AC97-SYNC	USB-P3-6
P1-22 (P1-28)	34	FFRXD	KP_MKIN <3>	SSPSCLK3	USB_P2_2		SSPSCLK3
P3-27	35	FFCTS	USB_P2_1	SSPSFRM		KP_MKO	SSPTXD3

(P1-40)				3		UT<6>	
P3-21 (P1-32)	36	FFDCD	SSPSCLK 2	KP_MKIN <7>	USB_P2_4	SSPSCLK 2	
P3-25 (P1-36)	37	FFDSR	SSPSFRM 2	KP_MKIN <3>	USB_P2_8	SSPSFRM 2	FFTXD
P1-30 (P1-44)	38	FFRI	KP_MKIN _4	USB_P2_3	SSPTXD3	SSPTXD2	PWM_OU T<1>
P1-24 (P1-30)	39	KP_MKIN <4>		SSPSFRM 3	USB_P2_6	FFTXD	SSPSFRM 3
P3-23 (P1-34)	40	SSPRXD2		USB_P2_5	KP_MKO UT<6>	FFDTR	SSPSCLK 3
P3-28 (P1-42)	41	FFRXD	USB_P2_7	SSPRXD3	KP_MKO UT<7>	FFRTS	
P1-28 (P1-22)	42	BTRXD	ICP-RXD				CIF-MCLK
P1-30 (P1-24)	43			CIF-FV	ICP-TXD	BTTXD	CIF-FV
P1-40 (P1-39)	44	BTCTS		CIF-LV			CIF-LV
P1-42 (P1-41)	45			CIF-PCLK	AC97-SYSCLK	BTRTS	SSP-SYSCLK3
P1-27 P2-123	46	ICP-RXD	STD-RXD			PWM-OUT[2]	
P1-29 P2-121	47	CIF-DD[0]			STD-TXD	ICP-TXD	PWM-OUT[3]
P1-117	48	CIF-DD[5]			BB-OB-DAT[1]	nPOE	
P1-119	50	CIF-DD[3]		SSP-SCLK2	BB-OB-DAT[2]	nPIOR	SSP-SCLK2
P1-121	51	CIF-DD[2]			BB-OB-DAT[3]	nPIOW	
P3-49 (P1-35)	52	CIF-DD[4]	SSP-SCLK3		BB-OB-CLK	SSP-SCLK3	
P1-125	53	FFRXD	USB-P2-3		BB-OB-STB	CIF-MCLK	SSP-SYSCLK
P1-131	54		BB-OB-WAIT	CIF-PCLK		nPCE[2]	
P1-129	55	CIF-DD[1]	BB-IB-DAT[1]			nPREG	
P1-123	56	nPWAIT	BB-IB-DAT[2]		USB-P3-4		
P1-114	57	nIOIS16	BB-IB-				SSPTXD

			DAT[3]				
P2-95	58		LDD[0]			LDD[0]	
P2-97	59		LDD[1]			LDD[1]	
P2-100	60		LDD[2]			LDD[2]	
P2-99	61		LDD[3]			LDD[3]	
P2-102	62		LDD[4]			LDD[4]	
P2-101	63		LDD[5]			LDD[5]	
P2-104	64		LDD[6]			LDD[6]	
P2-106	65		LDD[7]			LDD[7]	
P2-105	66		LDD[8]			LDD[8]	
P2-108	67		LDD[9]			LDD[9]	
P2-107	68		LDD[10]			LDD[10]	
P2-109	69		LDD[11]			LDD[11]	
P2-113	70		LDD[12]			LDD[12]	
P2-116	71		LDD[13]			LDD[13]	
P2-118	72		LDD[14]			LDD[14]	
P2-117	73		LDD[15]			LDD[15]	
P2-111	74					L-FCLK-RD	
P2-96	75					L-LCLK-A0	
P2-112	76					L-PCLK-WR	
P2-114	77					L-BIAS	
P2-128	81		CIF-DD[0]		SSPTXD3	BB-OB-DAT[0]	
P1-128	82	SSPRXD3	BB-IB-DAT[0]	CIF-DD[5]			FFDTR
P2-125	83	SSP-SFRM3	BB-IB-CLK	CIF-DD[4]	SSP-SFRM3	FFTXD	FFRTS
P1-126	84	SSPCLK3	BB-IB-STB	CIF-FV	SSPCLK3		CIF-FV
P1-124	85	FFRXD	DREQ[2]	CIF-LV	nPCE[1]	BB-IB-WAIT	CIF-LV
P3-45 (P2-92)	86	SSPRXD2	LDD[16]	USB-P3-5	PCE[1]	LDD[16]	
P3-56	87	nPCE[2]	LDD[17]	USB-P3-1	SSPTXD2	LDD[17]	SSP-SFRM2

P3-72	88	USBHPWR<1>	SSPRXD2	SSPFRM2			SSPFRM2
P3-92 (P2-78)	90	KP-MKIN[5]	USB-P3-5	CIF-DD[4]		nURST	
P3-94 (P2-80)	91	KP-MKIN[6]	USB-P3-1	CIF-DD[5]		UCLK	
P1-15	92	MM-DAT[0]			MM-DAT[0]	MSBS	
P3-58 (P1-37)	97	KP-DKIN[4]	DREQ[1]	KP-MKIN[3]		MBGNT	
P3-54 P3-121 (P2-93)	99	KP-DKIN[6]	AC97-SDATA-IN1	KP-MKIN[5]			FFTXD
P3-41 P1-49	100	KP-MKIN[0]	DREQ[2]	FFCTS			
P1-54 P3-39	101	KP-MKIN[1]					
P3-37	102	KP-MKIN[2]		FFRXD	nPCE[1]		
P3-52	103	CIF-DD[3]				KP-MKOUT0	
P3-48 P1-132	104	CIF-DD[2]			PSKTSEL	KP-MKOUT1	
P3-46 (P1-45)	105	CIF-DD[1]			nPCE[2]	KP-MKOUT2	
P3-47 (P2-83)	106	CIF-DD[9]				KP-MKOUT3	
P3-60 (P2-85)	107	CIF-DD[8]				KP-MKOUT4	
P3-89 (P2-84)	108	CIF-DD[7]			CHOUT[0]	KP-MKOUT5	
P1-16	109	MM-DAT[1]	MSSDIO		MM-DAT[1]	MSSDIO	
P2-4	110	MM-DAT[2]/ MM-CCS[0]			MM-DAT[2]/ MM-CCS[0]		
P1-18	111	MM-DAT[3]/ MM-CCS[1]			MM-DAT[3]/ MM-CCS[1]		
P1-13	112	MMCMD	nMSINS		MMCMD		

P3-124 (P2-129)	113			USB-P3-3	I2S-SYSCLK	AC97-RESET-n	
P3-82 (P2-77)	114	CIF-DD[1]			UEN	UVS0	
P3-90 (P2-76)	115	DREQ[0]	CIF-DD[3]	MBREQ	UEN	nUVS1	PWM-OUT[1]
P3-84 (P2-75)	116	CIF-DD[2]	AC97-SDATA-IN0	UDET	DVAL[0]	nUVS2	MBGNT
P1-61	117	SCL			SCL		
P1-60	118	SDA			SDA		

- Function names marked with gray shading denote the alternate functionality intended by CM-X270 design.
- Some GPIO's can be routed to several alternative pins of PXA270 processor, which means they will appear on several alternative pins of CAMI connectors.
- For CM-X270L GPIOs 28,29,30,31,113 are available only for modules without A/AT option.
- GPIO's 14,19,87,88,95,102 are used by WiFi interface and are not available when WiFi assembled.
- All GPIO's which are routed exclusively through P3 connector, are not available in X270L.

The below table specifies initial state of GPIO pins, as set by ARMmon and on-board pullup resistors :

CPU GPIO pin #	**ARMmon preset**			**On-board pullup**
	Direction	Function	Level (if set as GPIO)	
1	In	GPIO	L	100K
12	In	GPIO	L	-
14	In	GPIO	L	-
19	In	GPIO	L	-
23	In	GPIO	L	-
24	In	GPIO	L	-
25	In	GPIO	L	-
26	In	GPIO	L	-
27	In	GPIO	L	-
28	In	AC97_BITCLK	L	-
29	In	AC97_ SDATA_IN_0	L	-
30	Out	AC97_ SDATA_OUT	H	-

31	Out	AC97_SYNC	H	-
32	In	GPIO	L	-
34	In	FFRXD	L	-
35	In	FFCTS	L	-
36	In	FFDCD	L	-
37	In	FFDSR	L	-
38	In	FFRI	L	-
39	Out	FFTXD	L	-
40	Out	FFDTR	L	-
41	Out	FFRTS	L	-
42	In	BTRXD	L	-
43	Out	BTTXD	L	-
44	In	BTCTS	L	-
45	Out	BTRTS	L	-
46	In	ICP_RXD	L	-
47	In	ICP_TXD	L	-
48	Out	GPIO	H	-
49	Out	nPWE	H	-
50	Out	GPIO	H	-
51	Out	GPIO	H	-
52	In	GPIO	L	-
53	In	GPIO	L	-
54	Out	GPIO	H	8.2K
55	In	GPIO	L	-
56	In	GPIO	L	-
57	In	GPIO	L	-
58	Out	LDD<0>	L	-
59	Out	LDD<1>	L	-
60	Out	LDD<2>	L	-
61	Out	LDD<3>	L	-
62	Out	LDD<4>	L	-
63	Out	LDD<5>	L	-
64	Out	LDD<6>	L	-
65	Out	LDD<7>	L	-
66	Out	LDD<8>	L	-
67	Out	LDD<9>	L	-
68	Out	LDD<10>	L	-
69	Out	LDD<11>	L	-
70	Out	LDD<12>	L	-
71	Out	LDD<13>	L	-

72	Out	LDD<14>	L	-
73	Out	LDD<15>	L	-
74	Out	L_FCLK_RD	L	-
75	Out	L_LCLK_A0	L	-
76	Out	L_PCLK_WR	L	-
77	Out	L_BIAS	L	-
81	In	GPIO	L	-
82	In	GPIO	L	-
83	In	GPIO	L	-
84	In	GPIO	L	-
85	Out	GPIO	H	8.2K
86	In	GPIO	L	-
87	In	GPIO	L	-
88	In	GPIO	L	-
90	In	GPIO	L	-
91	In	GPIO	L	-
92	In	GPIO	L	100K
97	In	GPIO	L	-
98	Out	AC97_SYSCLK	L	-
99	In	GPIO	L	-
100	In	GPIO	L	-
101	In	GPIO	L	-
102	In	GPIO	L	-
103	In	GPIO	L	-
104	In	GPIO	L	-
105	In	GPIO	L	-
106	In	GPIO	L	-
107	In	GPIO	L	-
108	In	GPIO	L	-
109	In	GPIO	L	100K
110	In	GPIO	L	100K
111	In	GPIO	L	100K
112	In	GPIO	L	100K
113	Out	AC97_RESET_n	H	-
114	In	GPIO	L	-
115	In	GPIO	L	-
116	In	GPIO	L	-
117	In	GPIO	L	4.7K
118	In	GPIO	L	4.7K

5.2. Pulse Width Modulator

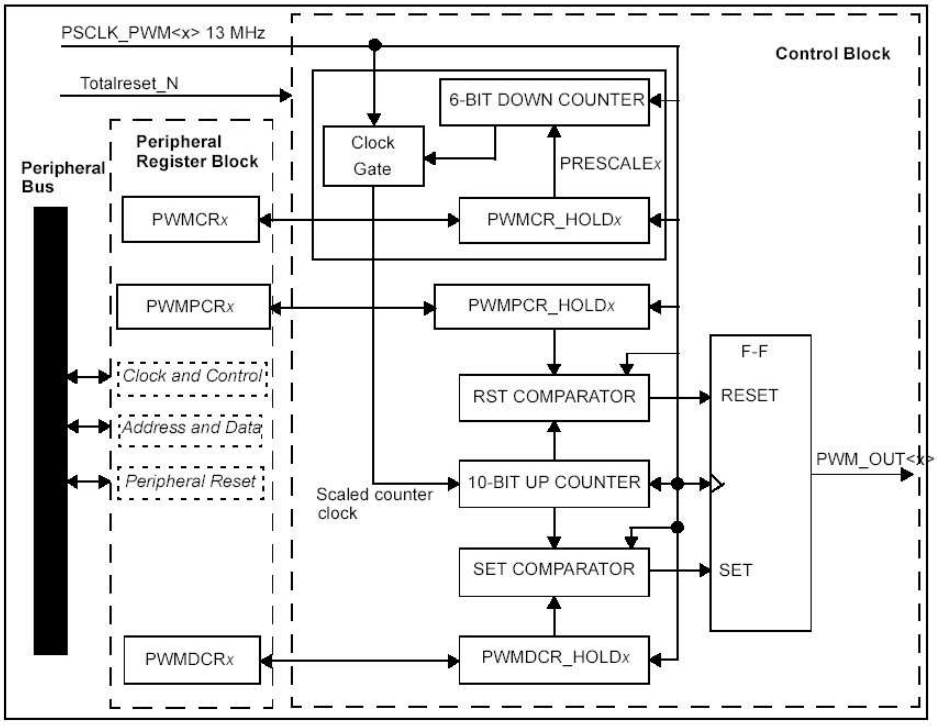
Use the Pulse Width Modulator (PWM) to generate up to four signals to be output from the processor. The signals are based on the 13 MHz clock and must be a minimum of two clock cycles wide. These signals are output from the processor by configuring the GPIO's.

The processor contains four pulse width modulators: PWM0-3. Each PWM operates independently of the other and is controlled by its own set of registers. They provide a pulse width modulated signal on an external pin. Since each PWM contains identical circuitry, a generic PWM*n*, where *n* is 0 to 3, as described.
PWM0 signal is used onboard the CM-X270 thus is not available for external usage.

Each PWM contains:

- Four Pulse Width Modulator channels
- Enhanced Period control through 6-Bit Clock divider and 10-Bit Period counter
- 10-Bit Pulse control

A block diagram of one PWM is shown below.



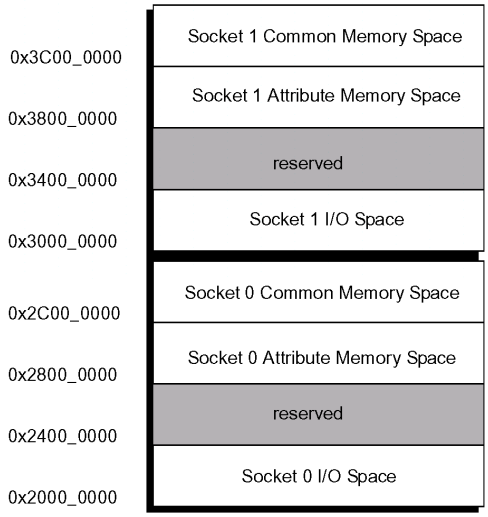
5.3. PC Card / PCMCIA / Compact Flash Interface

The processor card interface is based on *The PC Card Standard - Volume 2 - Electrical Specification, Release 2.1*, and *CF+ and CompactFlash Specification Revision 1.4*. The 16-bit PC Card / Compact Flash interface provides control signals to support any combination of 16-bit PC Card (PCMCIA) / Compact Flash in two card sockets, using address lines (MA[25:0]) and data lines (MD[15:0]).

The processor 16-bit PC Card / Compact Flash Controller provides the following signals:

- nPREG is muxed with MA[26] and selects register space (I/O or attribute) versus memory space
- nPOE and nPWE allow memory and attribute reads and writes
- nPIOR, nPIOW, and nIOIS16 control I/O reads and writes
- nPWAIT allows extended access times
- nPCE2 and nPCE1 are byte select high and low for a 16-bit data bus
- PSKTSEL selects between the two card sockets

The PXA270 processor 16-bit PC Card interface provides control for one 16-bit PC Card slot with a PSKTSEL pin for support of a second slot. The PXA270 processor interface supports 8- and 16-bit peripherals and handles common memory, I/O, and attribute-memory accesses. The duration of each access is based on the values programmed in the fields in the MCMEMx, MCATTx, and MCIOx registers. The figure below shows the memory map for the 16-bit PC Card space.



The 16-bit PC Card Memory Map space is divided into eight partitions, four for each card slot. The four partitions for each card slot are: common memory, I/O, attribute memory, and a reserved space. Each partition starts on a 64-Mbyte boundary.

During an access, pins MA[25:0], nPREG, and PSKTSEL are driven at the same time. nPCE1 and nPCE2 are driven concurrently with the address signals for common memory and attribute- memory accesses. For I/O accesses, their value depends on the value of nIOIS16 and is valid a fixed amount of time once nIOIS16 is valid.

Common memory and attribute memory accesses assert the nPOE or nPWE control signals. I/O accesses assert the nIOR or nIOW control signals and use the nIOIS16 input signal to determine the bus width of the transfer (8 or 16 bits). The PXA270 processor uses nPCE2 to indicate to the expansion device that the upper half of the data bus (MD[15:8]) is used for the transfer and nPCE1 to indicate that the lower half of the data bus (MD[7:0]) is used. nPCE1 and nPCE2 are asserted for 16-bit accesses.

When writes go to a card socket and a byte has been masked via an internal byte enable, the write does not occur on the external bus. For reads, one half-word is always read from the socket, even if only 1 byte is requested. In some cases, based on internal address alignment, one word is read, even if only 1 byte is requested.

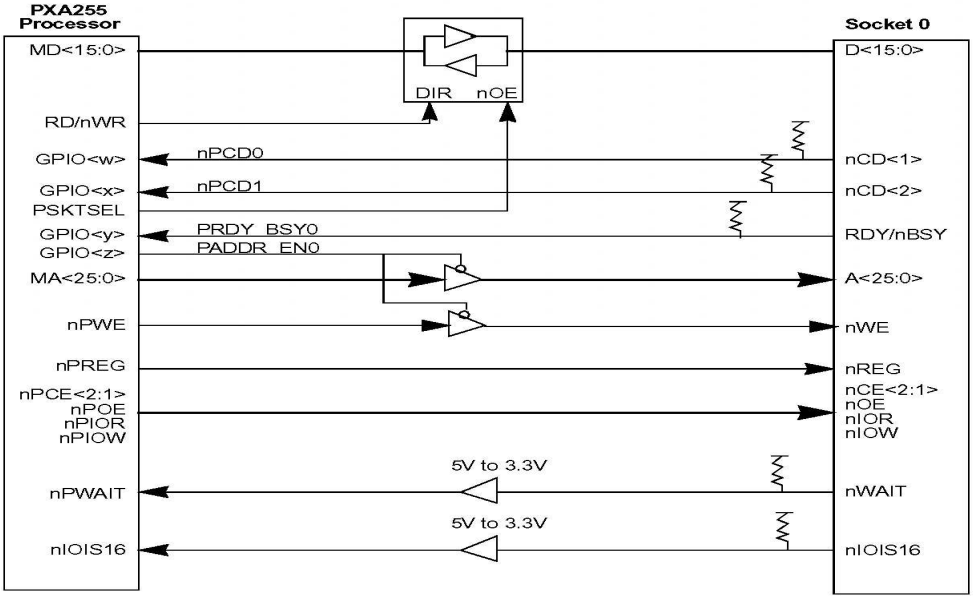
External Logic for PCMCIA Implementation

PCMCIA Interface shares most of the signals with Local Bus, and also adds several dedicated signals.

The CM-X270 requires minor glue logic to complete the PCMCIA socket interface. The figure below shows an example of glue logic required for single socket interface. For detailed reference of implementation one PCMCIA socket (plus one CardBus socket) refer to SB-X270 reference design, available following [Developer] >> [CM-X270] >> [SB-X270 Design Schematics] in CompuLab's web-site. For reference of two PCMCIA sockets implementation refer to SB-X255 design, which is also valid for X270.

Use GPIO to control the PCMCIA interface’s reset, power selection (V_{CC} and V_{PP}), and drive enables, if these functions are indeed required in your application. The diagram below shows the logical connections necessary to support hot insertion capability. For dual-voltage support, level shifting buffers are required for all the processor input signals, CM-X270 doesn't provide these buffers on-board. Hot insertion capability requires each socket be electrically isolated from the other and from the remainder of the memory system. If one or both of these features are not required, you may eliminate some of the logic shown in these diagrams. The processor allows either 1-socket or 2-socket solutions. In the 1-socket solution, only minimal glue logic is required. Note that CAMI local bus signals must be buffered when routed to PCMCIA socket.

Software is responsible for setting the MECR[NOS] and MECR[CIT] bits. NOS indicates the number of sockets that the system supports while CIT is written when a card is in place. Input pins nPWAIT and nIOIS16 are tri-stated until the card detect (CD) signal is asserted. To achieve this, software programs the MECR[CIT] bit when a card is detected. If the MECR[CIT] is 0, the nPWAIT and nIOIS16 inputs are ignored.



PCMCIA Signals

CAMI Name	CAMI Pin	PXA270 Name	Type	Description
PCM-MEMR#	P1-117	nPOE GPIO[48]	Out	**PCMCIA output enable.** Reads from PCMCIA memory and from PCMCIA attribute space.
PCM-MEMW#	P1-120	nPWE	Out	**PCMCIA write enable.** Performs writes to PCMCIA memory and to PCMCIA attribute space. Also used as the write enable signal for Variable Latency I/O.
PCM-IOR#	P1-119	nPIOR GPIO[50]	Out	**PCMCIA I/O read.** Performs read transactions from PCMCIA I/O space.
PCM-IOW#	P1-121	nPIOW GPIO[51]	Out	**PCMCIA I/O write.** Performs write transactions to PCMCIA I/O space.
PCM-WAIT#	P1-123	nPWAIT GPIO[56]	In	**PCMCIA wait.** Driven low by the PCMCIA card to extend the length of the transfers to/from the PXA270 processor.
PCM-RST#	P1-125	GPIO[53]	Out	**PCMCIA reset.** Hardware reset the PCMCIA card.

PCM-REG#	P1-129	nPREG GPIO[55]	Out	**PCMCIA Register select.** Indicates that the target address on a memory transaction is attribute space. Has the same timing as the address bus.
PCM-CE2#	P1-131	nPCE[2] GPIO[54]	Out	**PCMCIA card enable 2.** Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane.
PCM-CE1#	P1-124	nPCE[1] GPIO[85]	Out	**PCMCIA card enable 1.** Selects a PCMCIA card. nPCE[2] enables the high byte lane and nPCE[1] enables the low byte lane.
PCM-CDA#	P1-126	GPIO[84]	In	**Card Detect A.** Pulled down when a card is inserted.
PCM-INTRDYA	P1-128	GPIO[82]	In	**PCMCIA socket A interrupt/ready signal.**
PCM-WE#	P1-130	RDnWR	Out	**Read/Write cycle indicator**. High at read cycle and low at write cycle. Controls the direction of external PCMCIA buffers.
PCM-SKTSEL	P1-132	PSKTSEL GPIO[104]	Out	**PCMCIA socket select.** Used by external steering logic to route control, address, and data signals to one of the two PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, socket one is selected. Has the same timing as the address bus.
PCM-CDB#	P2-125	GPIO[83]	In	**Card Detect B.** Pulled down when a card is inserted.
PCM-INTRDYB	P2-128	GPIO[81]	In	**PCMCIA socket B interrupt/ready signal.**
PCM-IOCS16#	P1-114	nIOIS16 GPIO[57]	In	**IO Select 16**. Acknowledge from the PCMCIA card that the current address is a valid 16 bit wide I/O address.

Signals having simple input or output functionality are implemented by GPIO pins. Other signals are implemented by dedicated PCMCIA logic in the processor. They are sharing interface with GPIO's, marked in gray color above.

5.4. MultiMediaCard Controller

The MMC/SD/SDIO controller acts as a link between the software that accesses the PXA270 processor and the MMC stack (a set of memory cards) and supports Multimedia Card, Secure Digital, and Secure Digital I/O communications protocols. The MMC controller in the PXA270 processor is based on the standards outlined in the *MultiMediaCard System Specification Version 3.2*. The SD controller supports one SD or SDIO card based on the standards outlined in the *SD Memory Card Specification Version 1.01* and *SDIO Card Specification Version 1.0 (Draft 4*).

The MMC/SD/SDIO controller supports the translation protocol from a standard MMC or serial peripheral interface (SPI) bus to the MMC stack. The software that accesses the PXA270 processor must indicate whether to use MMC/SD/SDIO or SPI mode as the protocol to communicate with the MMC/SD/SDIO controller.

The MMC/SD/SDIO controller features:

- Data-transfer rates up to 19.5 Mbps for MMC, 1-bit SD/SDIO, and SPI mode data transfers
- Data-transfer rates up to 78 Mbps for 4-bit SD/SDIO data transfers
- A response FIFO
- Two transmit FIFOs and two receive FIFOs
- Two modes of operation: MMC/SD/SDIO mode and SPI mode. MMC/SD/SDIO mode supports MMC, SD, and SDIO communications protocols. SPI mode supports the SPI communications protocol.
- 1-and 4-bit data transfers are supported for SD and SDIO communications protocols.
- Clock on and off, based on status of FIFOs, to prevent overflows and underruns.
- Support for all valid MMC and SD/SDIO protocol data-transfer modes
- Interrupt-based application interface to control software interaction
- Using the MMC communications protocol, multiple MMC cards are supported.
- Using the SD or SDIO communications protocol, one SD or SDIO card is supported.

* For stream writes, only data sizes of 10 bytes or more are allowed.

MMC Signals

MMC signals share interface pins with other functions. There are several options to program which alternate functions are traded for MMC. Therefore, same MMC signal can be routed to several optional pins, which alternative functions are specified in gray in the below table.

Signal	Pin number	Type	Description
MMC-CMD	P1-13	I/O	MMC Command
MMC-DAT0	P1-15	I/O	MMC Data
MMC-DAT1	P1-16	I/O	MMC Data
MMC-DAT2/ MMCS0	P2-04	I/O	MMC Data
MMC-DAT3/ MMCS1	P1-18	I/O	MMC Data
MMCCLK	P1-12	O	MMC Controller clock

5.5. LCD Controller of PXA270

CM-X270 graphics controller is integrated in the PXA270 chip, providing cost-efficient solution for applications requiring low-to-medium graphics resolution (up to 800 x 600) and performance. The LCD controller provides an interface between the PXA270 processor and a flat-panel display module. The flat-panel display module can be passive (DSTN), active (TFT), or an LCD panel with internal frame buffering.

The LCD/flat-panel controller is backward-compatible with Intel's PXA255 processor LCD controller. Several additional features are also supported. These additional features are:

- Pixel formats of 18, 19, 24, and 25 bits per pixel (bpp)
  - 18 bpp—RGB 6:6:6
  - 19 bpp—RGBT 6:6:6
  - 24 bpp—RGB 8:8:8, RGBT 8:8:7
  - 25 bpp—RGBT 8:8:8

Note: RGBT uses the most significant bit to indicate transparency for overlay support.

- Base plane with software control of two overlay windows and a hardware cursor
- Color management:
  - Up-scaling for YCbCr 4:2:0 and 4:2:2 to YCbCr 4:4:4
  - Color space conversion CCIR 601—YCbCr 4:4:4 to RGB 8:8:8

  - Conversion from true color, (RGB 8:8:8) to high color (RGB 5:5:5) and the various configurations of RGBT
- Support for LCD panels with an internal frame buffer (smart panels)

Features

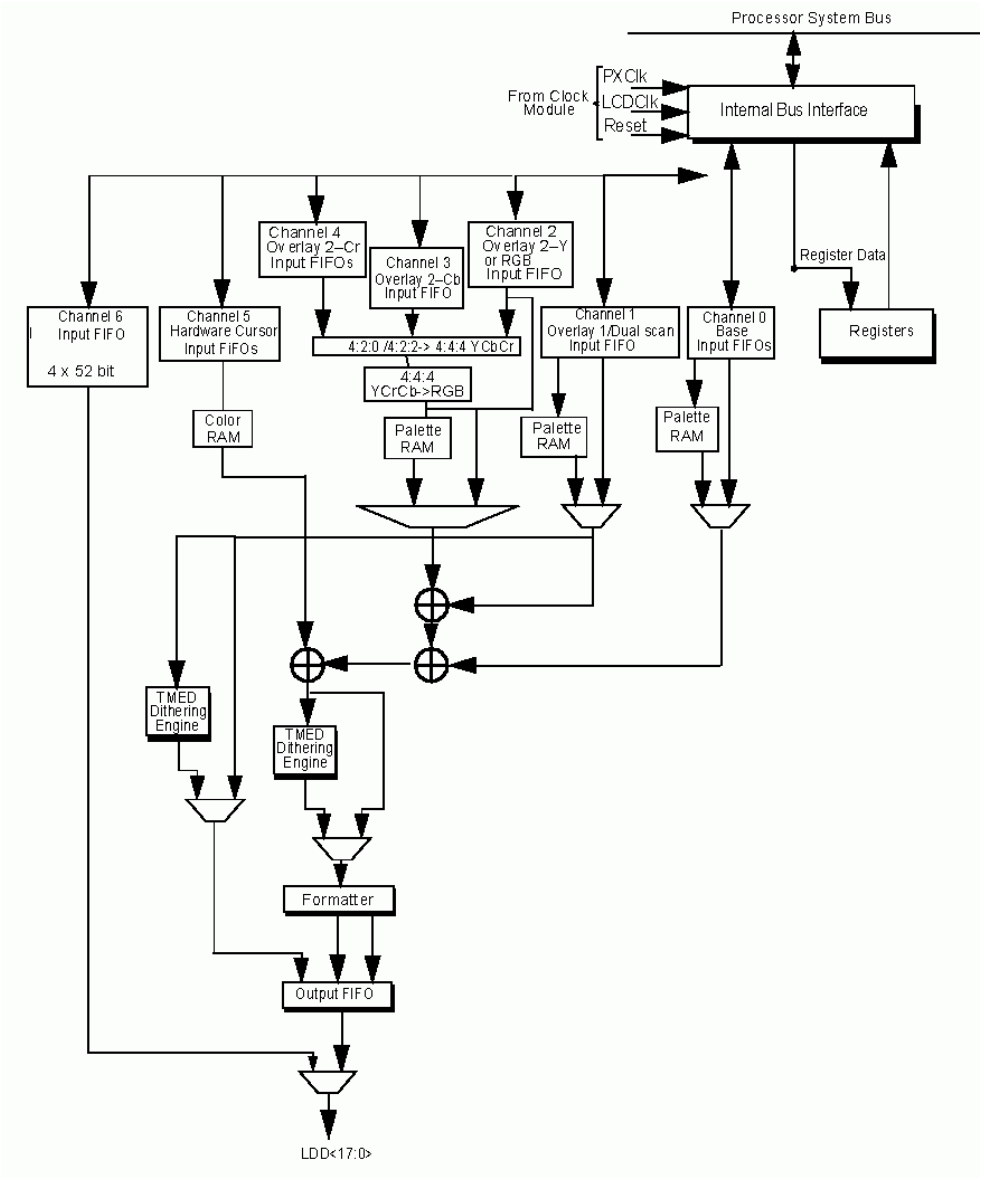
The following list describes features supported by the PXA270 processor LCD controller:

- Display modes
  - Support for single- or dual-scan display modules
  - Passive monochrome mode supports up to 256 gray-scale levels (8 bits)
  - Active color mode supports up to 16777216 colors (24 bits)
  - Passive color mode supports a total of 16777216 colors (24 bits)
  - Support for LCD panels with an internal frame buffer
  - Support for 8-bit (each) passive dual-scan color displays
  - Support for up to 16-bit per pixel single-scan color displays without an internal frame buffer
  - Support for up to 24-bit per pixel single-scan color displays with an internal frame buffer
- Support for display sizes from 1x1 to 800 x 600 pixels.
- 64-entry (by 24 bits) output FIFO
- Three 256-entry by 25-bits internal color-palette RAMs (one for each overlay and Base) programmable to be automatically loaded at the beginning of each frame
- Command data RAM (16 x 9 bits) to hold command data
- Supports pixel depths of 2, 4, 8, 16, and 24 bits per pixel (bpp) in RGB format
- Overlays supported with pixel depths of 16, 19, 24, and 25 bpp in RGBT format
- Provides one base layer plus two overlays for single-scan displays; maximum size of each overlay can equal the display size
- Integrated seven-channel DMA (one channel for base plane, one channel for Overlay 1 and three channels for Overlay 2, one channel for the hardware cursor, and one channel to for the command data)
- Hardware support for color-space conversion from YCbCr to RGB for video streams
- Supports hardware cursor for single-scan display (see Section 7.4.11 in PXA270 manual for cursor modes and sizes)
- Programmable toggle of AC bias pin output (toggled by line count)
- Programmable pixel clock from 52.0 MHz to 25.4 kHz (104.0 MHz/2 to 13 MHz/512)
- Supports little-endian ordering of pixels in frame buffer
- Programmable wait-state insertion at beginning and end of each line
- Programmable polarity for output enable, frame clock, and line clock
- Programmable interrupts for input and output FIFOs (underrun)
- Six 16 x 64-bit input FIFOs: one for the base channel, one for Overlay 1, three for Overlay 2, and one for the hardware cursor; plus a seventh 4 x 52-bit input FIFO for command data for panels with internal frame buffer

- Backward-compatible with the Intel's PXA255 graphics controller. Graphics applications developed for CM-X255 will run on CM-X270 as well.

Block Diagram

The LCD controller supports a hardware cursor and three image planes, Base, Overlay 1, and Overlay 2. The combination of the three image planes allows multiple images to be displayed simultaneously with software control of window size and position. The simplified top-level block diagram for the LCD controller is illustrated below. The palette, frame, cursor, and command data utilize a dedicated DMA controller that provides seven channels for fetching the appropriate data from memory into associated input FIFOs.


Processor System Bus
From Clock Module
PXClk
LCDClk
Reset
Internal Bus Interface
Register Data
Registers
Channel 6 Input FIFO
4 x 52 bit
Channel 5 Hardware Cursor Input FIFOs
Channel 4 Overlay 2–Cr Input FIFOs
Channel 3 Overlay 2–Cb Input FIFO
Channel 2 Overlay 2–Y or RGB Input FIFO
Channel 1 Overlay 1/Dual scan Input FIFO
Channel 0 Base Input FIFOs
4:2:0 /4:2:2-> 4:4:4 YCbCr
4:4:4 YCrCb->RGB
Color RAM
Palette RAM
Palette RAM
Palette RAM
TMED Dithering Engine
TMED Dithering Engine
Formatter
Output FIFO
LDD<17:0>

Pin Descriptions

When the LCD controller is enabled, all of the LCD pins are outputs only. When the LCD controller is disabled, its pins can be used for general-purpose input/output (GPIO). The table below describes the LCD controller's pins.

LCD Panel Interface Signals

CAMI Name	PXA270 Name	CAMI Pin	Type	Description
LCD-B1	LDD0	P2-95	O	**LCD Panel Data Bus**. These data lines transmit either four, eight or sixteen bit data values at a time to the LCD display. For monochrome displays, each pin value represents a single pixel. For passive color, groupings of three pin values represent one pixel (red, green, and blue subpixel data values). In single-panel monochrome mode, four pins are used. For double-pixel data, single-panel monochrome, dual-panel monochrome, single-panel color, and active color modes, eight pins are used. When TFT (active color mode) operation is programmed, all sixteen data outputs are used. The pin naming given represents this situation.
LCD-B2	LDD1	P2-97	O	
LCD-B3	LDD2	P2-100	O	
LCD-B4	LDD3	P2-99	O	
LCD-B5	LDD4	P2-102	O	
LCD-G0	LDD5	P2-101	O	
LCD-G1	LDD6	P2-104	O	
LCD-G2	LDD7	P2-106	O	
LCD-G3	LDD8	P2-105	O	
LCD-G4	LDD9	P2-108	O	
LCD-G5	LDD10	P2-107	O	
LCD-R1	LDD11	P2-109	O	
LCD-R2	LDD12	P2-113	O	
LCD-R3	LDD13	P2-116	O	
LCD-R4	LDD14	P2-118	O	
LCD-R5	LDD15	P2-117	O	
LCD-SCK	PCLK	P2-112	O	**Display Data Clock.** Pixel clock for flat panel data. Used by the LCD display to clock the pixel data into the line shift register. In passive mode, the pixel clock toggles only when valid data is available on the data pins. In active mode, the pixel clock toggles continuously, and DE serves as an output to the signal when data is valid on the LCD's data pins.

LCD-FRM	FCLK	P2-111	O	**Frame Sync.** Flat Panel equivalent of VSYNC. The Frame Sync clock is used by the LCD display to signal the start of a new frame of pixels. The display resets the line pointer to the top of the screen.
LCD-LP	LCLK	P2-96	O	**Line Sync.** Flat Panel equivalent of HSYNC. The Line Sync clock is used by the LCD display to signal the end of a line of pixels. The display transfers the line data from the shift register to the screen and increments the line pointer.
LCD-DE-M	BIAS	P2-114	O	**Display Enable signal** (DE) for TFT Panels. Also used as a Modulation (Bias) signal - to switch the polarity of the power supplies to the row and column drivers of the screen to counteract DC offset.

Limitations of Display Controller Capabilities

PXA270 Display Controller provides a cost-efficient solution for the requirements of a typical embedded application. However, display capabilities are traded with cost-effectiveness to a certain extent, which is translated into limitations requiring a user's awareness.

The display controller shares memory bandwidth with other on-board functions using the local bus. When the bit rate is high and the bus is locked by another device, the display FIFO may reach the underrun state, thereby disturbing the displayed image.

Possible sources of disturbance:

- Host USB ports of Interface Bridge
- Off-board devices on LPC and PCI busses. (There are no on-board devices connected to the PCI bus)

Disturbance level depends on the display's bit rate and panel type. STN panels are not affected at all. TFT panels at resolutions lower than or equal to 640 x 480 x 16-bit practically don't exhibit disturbance either. At higher resolutions, the display quality depends on the activity level of the above-mentioned sources. If the disturbance sources aren't active, resolutions such as 640 x 480 x 16 or even 800 x 600 x 16 are displayed well. Taking into account the requirements of a typical embedded design, the display quality has been found satisfactory in almost all cases.

Limitations with CRT and Flat Panel Monitors

Using off-board DAC, the CM-X270 can be connected to CRT or Flat Panel (FP) monitors with analog RGB interface. On CRT / FP monitors the disturbance more noticeable, because they don't use pixel clock input (in contrast to LCD panels). Monitors regenerate the pixel clock from sync pulses, which makes them more sensitive to short distractions.

Flat Panel monitors with RGB interface are especially sensitive. Monitors with newer DVI interface are less sensitive, similar to regular LCD panels.

5.6. UART's

The CM-X270 has four serial ports, available from PXA270 and Interface Bridge components:

CAMI Name	Type of module	Interface Signals	Origin	Max Baud rate (Kbps)	DMA & 64-byte FIFO	Interf
COM-A	X270W	Full modem	CPU / FFUART	921	+	RS232
	X270L	Rx/Tx	CPU / BTUART			
COM-B	Any	Rx/Tx	Interface Bridge	115	-	TTL
COM-C	X270W	Rx/Tx & CTS/RTS	CPU / BTUART	921	+	TTL
	X270L	Full modem	CPU / FFUART			
COM-D	Any	Rx/Tx	CPU / STUART	921	+	TTL

* TTL - 3.3V levels

BTUART and FFUART assignment to connector pins is different between X270W and X270L, as shown in the above table. However, these differences are hidden by firmware. All software packages check card type and assign port numbers accordingly. ARMmon always routes console to COM-A, Linux always assigns COM-A as ttyS0 and COM-C as ttyS1, invariant to card type.

Feature List

The serial ports are controlled via direct memory access (DMA) or programmed I/O. The PXA270 processor has three UART's: Full Function UART (FFUART), Bluetooth UART (BTUART) and Standard UART (STUART). One additional UART is provided by an optional Bridge component. All UART's are using the same programming model.

All UART's share the following features:

- Functionally compatible with the 16550
- Ability to add or delete standard asynchronous communications bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud rate generator that allows the internal clock to be divided by 1 to (2^{16} –1) to generate an internal 16X clock

- Modem control pins that allow flow control through software. Each UART has its own modem control capability.
- Fully programmable serial-interface:
  - 5-, 6-, 7- or 8-bit characters
  - Even, odd and no parity detection
  - 1, 1.5 or 2 stop bit generation
  - Baud rate generation. The maximum baud rate is different for each UART and ranges from 115.2 to 921 Kbps
- 64-byte transmit FIFO (16-byte in UART of Bridge)
- 64-byte receive FIFO (16-byte in UART of Bridge)
- Complete status reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include:
  - Loopback controls for communications link fault isolation
  - Break, parity and framing error simulation
- Fully prioritized interrupt system controls

UART's of the PXA270 processor have additional capabilities:

- Separate DMA requests for transmit and receive data services
- 16750 compatibility mode
- Extended 64-bytes FIFO
- Slow infrared asynchronous interface that conforms to the Infrared Data Association (IRDA) standard

Overview

Each serial port contains a UART and a slow infrared transmit encoder and receive decoder that conforms to the IRDA Serial Infrared (SIR) Physical Layer Link Specification.

Each UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the processor. The processor can read a UART's complete status during functional operation. Status information includes the type and condition of transfer operations and error conditions (parity, overrun, framing or break interrupt) associated with the UART.

Each serial port operates in FIFO or non-FIFO mode. In FIFO mode, a 64-byte transmit FIFO holds data from the processor until it is transmitted on the serial link and a 64-byte receive FIFO buffers data from the serial link until it is read by the processor. In non-FIFO mode, the transmit and receive FIFO's are bypassed.

Each UART includes a programmable baud rate generator that can divide the input clock by 1 to (2^{16} –1). This produces a 16X clock that can be used to drive the internal transmitter and receiver logic. Software can program interrupts to meet its requirements. This minimizes the number of computations required to handle the communications link. Each UART operates in an environment that is controlled by software and can be polled or is interrupt driven.

Serial Port Signals

Signal	Pin Number	Type	Description
COM-A-TX	P1-24	O	**Serial Data Out** transmits the serial data from the internal serial port controller to the external serial device or DCE.
COM-A-RX	P1-22	I	**Serial Data In** receives the serial data from the external serial device or DCE into the internal serial port controller.
COM-A-CTS#	P3-27	I	**Clear To Send** is driven back to the serial port to indicate that the external data carrier equipment (DCE) is ready to accept data.
COM-A-RTS#	P3-28	O	**Request To Send** indicates to the external DCE that the internal serial port controller is ready to send data.
COM-A-DCD#	P3-21	I	**Data Carrier Detect** is driven back to the serial port from data carrier equipment when it detects a carrier signal from a communications target.
COM-A-DSR#	P3-25	I	**Data Set Ready** indicates that the external DCE is ready to establish a communication link with the serial port controller.
COM-A-DTR#	P3-23	O	**Data Terminal Ready** indicates to the external DCE that the serial port controller is ready to communicate
COM-A-RI#	P3-30	I	**Ring Indicate** is used by an external modem to inform the serial port that a ring signal was detected. A change in state on this signal by the external modem can be configured to cause a modem status interrupt.
COM-B-RX	P1-23	I	
COM-B-TX	P1-25	O	
COM-C-RX	P1-28	I	
COM-C-TX	P1-30	O	
COM-C-DCD#	P1-32	I	
COM-C-DTR#	P1-34	O	
COM-C-DSR#	P1-36	I	
COM-C-CTS#	P1-40	I	
COM-C-RTS#	P1-42	O	
COM-C-RI#	P1-44	I	
COM-D-RX	P1-27	I	
COM-D-TX	P1-29	O	

Mapping of UART Ports under Linux

Port Name	Linux Name
COM-A	ttyS0
COM-B	ttyS3
COM-C	ttyS1
COM-D	ttyS2

5.7. Fast Infrared Communication Port

The Fast Infrared Communications Port (FICP) for the PXA270 processor operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FICP is based on the 4-Mbps IrDA standard and uses four-position pulse modulation (4PPM) and a specialized serial packet protocol developed for IrDA transmission. To support the standard, the FICP has:

- A bit encoder / decoder
- A serial-to-parallel data engine
- A transmit FIFO 128 entries deep and 8 bits wide
- A receive FIFO 128 entries deep and 11 bits wide

Infrared Port Signals

Signal	Pin Number	Type	Description
IRDA-RX	P2-123	I	**Infrared Serial Input** is the digital input for the serial infrared interface.
IRDA-TX	P2-121	O	**Infrared Serial Output** is the digital output for the serial infrared interface.

IrDA interface is shared with STUART, therefore only one can be available at time. Due to this reason, IrDA signals will also appear on STUART pins of CAMI connector.

5.8. USB Host Ports

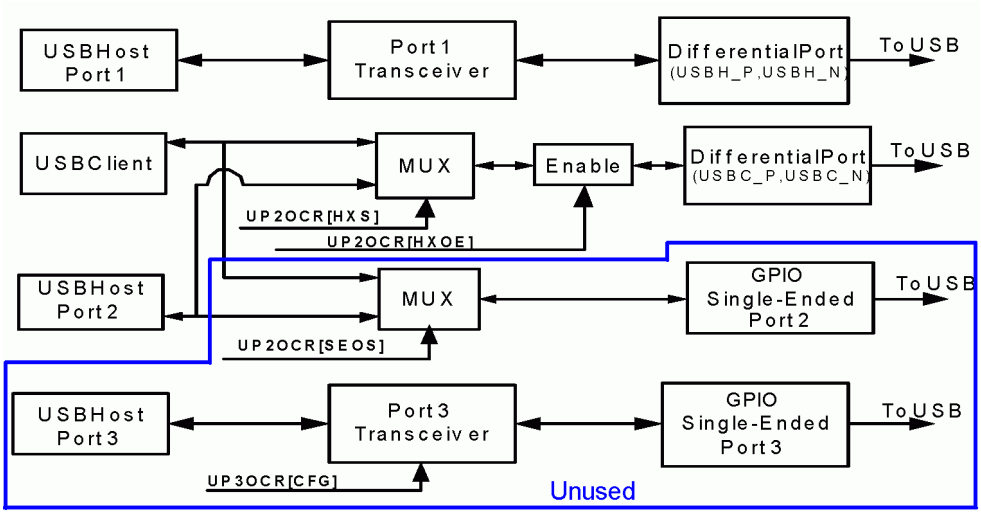
CM-X270 can contain one to four host USB ports - two ports from PXA270 processor and two ports from optional Interface Bridge. The interface of one USB host port of PXA270 is shared with slave port, and is configured by default as slave. These USB ports are Open Host Controller Interface (Open-HCI) compliant. The Open-HCI specification provides a register level description for a host controller, as well as common industry hardware/software interface and drivers, including keyboard and mouse support.

Features

- One to four host USB ports, depending on Host/Slave selection and presence of Interface Bridge.
- 12 Mbps or 1.5 Mbps speed
- Supports power management and overcurrent protection
- Fully compatible with USB specification version 1.1 and OHCI 1.0 register model

Since the USB Host Ports conform to OHCI standard, the description of their operation is not provided in this manual. For more information about USB Host ports, please refer to “USB Specification”, Version 1.1 and “OpenHCI Specification”, Version 1.0

The block diagram below shows routing of USB host and salve ports inside PXA270 chip. The porting marked "unused" is not implemented in CM-X270, because it requires additional hardware.



USB Host Signals

Signal	Pin Number	Type	Source	Description
USB-OVC#	P2-133	I		**Overcurrent. I**ndicates that the USB hub has detected an overcurrent on the USB. Has a 8.2k pull-up
USB1-N	P2-140	I/O	PXA270	USB Port 1 differential data Always available in CM-X270L. Available in CM-X270W only if the Bluetooth option is not assembled.
USB1-P	P2-138			
USB2-N	P2-139	I/O	Interface Bridge	USB Port 2 differential data
USB2-P	P2-137			
USB3-N	P1-138	I/O	PXA270	USB Port 3 differential data Shared with slave port
USB3-P	P1-136			
USB4-N	P3-139	I/O	Interface Bridge	USB Port 4 differential data Available only in X270W
USB4-P	P3-137			

5.9. USB Client (Slave) Controller

USB Client Controller is contained in the PXA270 processor chip. The Universal Serial Bus device controller (UDC) is USB 1.1-compliant and supports all standard device requests issued by any USB host controller. Refer to the *Universal Serial Bus Specification, Revision 1.1,* and the *On-The-Go Supplement to Universal Serial Bus Specification, Revision 2.0* for a full description of the USB protocol and its operation.

The UDC supports 24 endpoints (endpoint 0 plus 23 programmable endpoints). The UDC is a USB Revision 1.1-compliant, full-speed device that operates half-duplex at a baud rate of 12 Mbps.

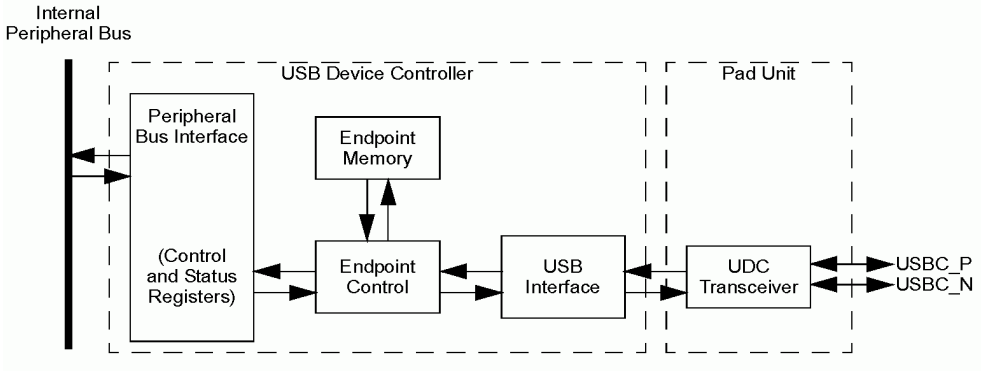
The UDC uses single-ported memory to support FIFO operations. Bulk, isochronous, and interrupt endpoint FIFO structures can be double-buffered to enable the endpoint to process one packet while assembling another. Either DMA or the software loop can be used to fill and empty the FIFOs. An interrupt, DMA service request, or polling can be used to detect packet receipt.

Features

- USB Revision 1.1, full-speed compliant device
- 23 programmable endpoints
  - Type: bulk, isochronous, or interrupt
  - Direction: in or out
  - Maximum packet size
  - Programmable configuration, interface and alternate interface setting numbers
- Endpoint 0 for control IN and OUT
- Four configurations:
  - Three programmable configurations with up to seven interfaces with seven alternate interface settings
  - Default configuration 0 with one interface and control endpoint 0
- Configurable 4-Kbyte memory for endpoint data storage

The UDC consists of four major components: the peripheral bus interface, endpoint memory, endpoint control, and USB interface. The peripheral bus interface contains the UDC control and status registers for the endpoint configuration data and provides the interface between the PXA270 processor and the USB data. The endpoint memory is a 4-Kbyte SRAM used for USB endpoint data storage. It has 32 bytes dedicated to endpoint 0, allowing the remainder of its memory to be allocated to any of the 23 programmable endpoints. The endpoint control and USB interface blocks provide the USB functionality.

USB Client Controller Block Diagram



USB Slave Signals

Signal	Pin Number	Type	Description
USB3-N	P1-138	I/O	Slave USB port interface. Shared with host USB port.
USB3-P	P1-136		

5.10. 10/100 Mbit Ethernet Port

The CM-X270 contains one full-featured 10/100 Mbit Ethernet interface. The Ethernet interface is based on the Davicom DM9000 component. The DM9000 consists of both a Media Access Controller (MAC) and a physical layer (PHY) combined into a single component solution. DM9000 is compliant with PC99 and PC2001 standards. DM9000 communicates with the processor using DMA on 32-bit local bus.

The controller can operate in either full duplex or half duplex mode. In full duplex mode, it adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a collision reduction mechanism.

The DM9000 includes a PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex and flow control. DM9000 initialization parameters, including MAC Address, are stored in NOR flash and uploaded into the component on power-up.

The CSMA/CD unit of the DM9000 allows it to be connected to either a 10 or 100 Mb Ethernet network. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The CSMA/CD unit can also be placed in full-duplex mode allowing simultaneous transmission and reception of frames.

The Physical Layer (PHY) unit of the DM9000 allows connection to either a 10 or 100 Mbp Ethernet network. The PHY unit supports Auto-Negotiation for 100BASE-TX Full Duplex, 100BASE-TX Half Duplex, 10BASE-T Full Duplex and 10BASE-T Half Duplex. It also supports LED pins to indicate link status, network activity and speed. The DM9000 does not support external PHY devices and does not expose its internal MII bus.

Address range and interrupts

DM9000 controller contents are accessed through on-chip address register.
Physical addresses of the ports in PXA270 address space:

DM9000 address port	0x05800000
DM9000 data port	0x05800008

DM9000 interrupt line is connected to GPIO[10] of PXA270.

Magnetic Modules

The CM-X270's Twisted Pair interface requires an external transformer (magnetic module) for interface to an RJ-45 connector. Two options exist:

1. An RJ-45 connector with a built-in transformer. Examples:

Vendor	Model
YCL	PTC1111-01
PCA	EPJ9025
Bothhand	LU1S041C

2. A separate transformer and RJ-45 connector. Examples of available transformers:

Vendor	Model
Delta	LF8200A
Pulse Engineering	PE-68515
Pulse Engineering	H1012

It is recommended to tie the transformer TX central winding to VCC3 and connect 100nF capacitor from VCC3 to GND nearby.
It is recommended to connect RX central winding to GND through 100nF capacitor.
Refer to ATX or SB-X270 baseboards reference design for implementation example.

Routing Ethernet Signals

The following rules should be applied when routing differential transmit and receive signals between the CM-X270 interface connector and an external connector/transformer module:

1. Route the differential signal pairs (TXN, TXP) and (RXN, RXP) in parallel, with minimal and consistent clearance within the pair. The distance between RX and TX pairs should be maximized, otherwise TX will induce crosstalk into RX.

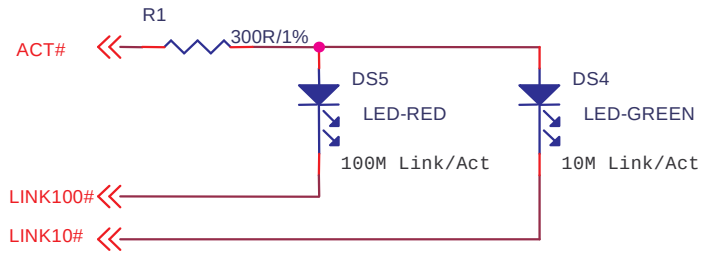
2. It is preferable (but not mandatory) to keep the trace length of Ethernet signals as short as possible. If trace length exceeds 2 inches, additional steps, not specified here, should be taken. Recommended trace width: 5 to 8 mil.
3. Don't route any other traces nearby or across the Ethernet signals' path.
4. It is preferable (but not mandatory) to remove the ground and other planes from beneath the Ethernet trace area.

The listed rules cover the routing requirements if an RJ-45 connector with a built-in transformer is used. If a separate transformer is used, additional rules should be followed for transformer-to-connector routing.

Ethernet Port Signals

Signal	Pin Number	Description
ETH1-TDN	P1-03	**Analog Twisted Pair Ethernet Transmit Differential Pair.** The differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer. TDP and TDN pins are connected by a 100 ohm termination resistor.
ETH1-TDP	P1-01	
ETH1-RDN	P1-02	**Analog Twisted Pair Ethernet Receive Differential Pair.** These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. RDP and RDN pins are connected by a 100 ohm termination resistor.
ETH1-RDP	P1-04	
ETH1-ACT#	P1-10	**Activity LED.** The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH1-LINK100#	P1-05	**100 Link LED.** The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH1-LINK10#	P1-06	**10 Link LED.** The 10 Link LED pin indicates link integrity and 10Mbps connection speed.

Recommended LED connection



This connection supplies full information about speed/link/activity.

LED-RED : 100 Mbps link / activity indicator
LED-GREEN : 10 Mbps link / activity indicator

Activity	LED (Red/Green)
none	off
Link (only)	on
Tx / Rx (and Link)	blink

5.11. Audio Interface

The CM-X270 implements audio interface using AC'97 compatible audio CODECs. If "A" (no touch screen) assembly option is specified, Cirrus Logic's CS4202 (or compatible) chip is used. If "AT" option is specified, then Phillips UCB1400 CODEC is used for CM-X270W rev 1.x and Wolfson WM9715 CODEC is used for CM-X270W rev 2.x. Both "AT" option CODECs also include touch screen controller. The chips are AC'97 2.1 compliant stereo audio CODECs designed for PC multimedia systems. Industry-leading delta-sigma and mixed signal technology is used. This advanced technology and its features are designed to help in enabling the design of PC 99 and PC 2001 compliant high-quality audio systems. The CODECs surpass PC 99, PC 2001 and AC '97 2.1 audio quality standards. The audio system also includes a power amplifier for matching the stereo output for a direct connection of stereo headphones.

Features

- Sample Rate Converters
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Line-level Stereo Input for LINE IN
- Microphone Input
- Integrated High-Performance Microphone Pre-Amplifier
- Meets or Exceeds the Microsoft PC 99 and PC 2001 Audio Performance Requirements

Audio specifications

Speaker Output	Type	Stereo
	Power	Option "A" - 1 mW/ch into 1K load (amplifier input) Option "AT" - 25 mW/ch into 8 ohm or 32 ohm load (speakers)
	Decoupling	Requires external 220uF capacitors, for 8 ohm load. Smaller capacitors (like 1uF) can be used high-impedance loads.
Microphone Input	Type	Mono, electret or dynamic
	Decoupling	On-board
Line Input	Type	Stereo
	Decoupling	On-board

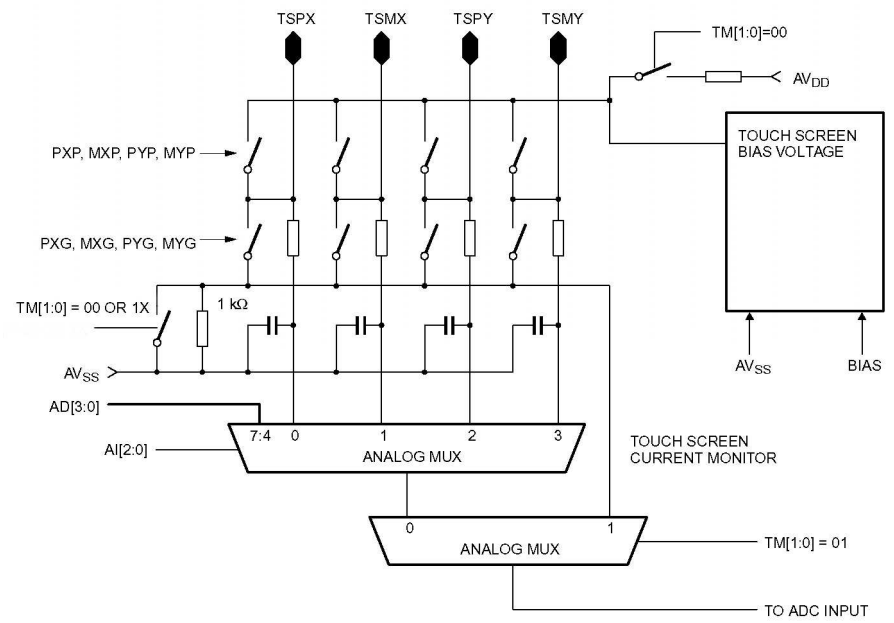
Audio Interface Signals

Signal	Pin Number	Type	Output Drive & Max Load	Description
AUD-INL-MIC [AC97-BITCLK]	P2-132	I	-	Audio stereo line input left and microphone mono input.
AUD-INR [AC97-SDOUT]	P2-130	I	-	Audio stereo line input right.
AUD-OUTL [AC97-SDIN0]	P2-131	O	25 mW	Speaker stereo output left. Can be used as line output.
AUD-OUTR [AC97-SYNC]	P2-136	O	25 mW	Speaker stereo outputs right. Can be used as line output.
AUD-SPDIF [AC97-RST#]	P2-129	O		Digital audio output Not available if UCB1400 codec (with touch screen controller) is used.
AC_AD1	P3-117	I		WM9715 A/D input 1

AC_AD2	P3-113	I		WM9715 A/D input 2
AC_AD3	P3-10	I		WM9715 A/D input 3
AC_AD4	P3-5	I		WM9715 A/D input 4
AUD_OUTC	P2-126	O		Audio center signal. Can be used for direct headphones connection without DC blocking capacitors.

5.12. Touch Screen Controller

CM-X270 optional UCB1400 codec chip includes universal touch screen controller. Touch screen interface is for 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. Touch screen interface is fully supported by drivers in Linux and Win CE packages provided by CompuLab.



The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or grounded in the touch screen switch matrix. The setting of each touch screen pin is programmable by the PXP, MXP, PYP, MYP and PXG, MYG, PYG, MYG bits in the touch screen control register. Possible conflicting settings (grounding and powering of a touch screen pin at the same time) are detected by the UCB1400. In that case, the UCB1400 will ground the touch screen pin.

Each of the four touch screen signals can be selected as input for the built-in 10-bit ADC, which is used to determine the voltage on the selected touch screen pin in position measurement mode. In addition, the UCB1400 can monitor touch screen current via an internal 1 Kohm resistor that can act as the input to the 10-bit ADC in pressure or plate resistance measurement mode. The flexible switch matrix and the multi-functional touch

screen bias circuit enable the user of the UCB1400 to set each desired touch screen configuration.

The UCB1400's internal voltage reference (Vref) acts as the reference voltage for the touch screen bias circuitry. This makes the touch screen biasing independent of supply voltage and temperature variations. Four low pass filters, one on each touch screen terminal, are built in to minimize the noise coupled from the LCD into the touch screen signals. An LCD typically generates large noise glitches on the touch screen, since they are closely coupled.

Touch Screen Interface Signals

Signal	Pin Number	Type	Description
TS-PX	P1-53	Analog	Plate X, plus (Left)
TS-MX	P2-71	Analog	Plate X, minus (Right)
TS-PY	P1-57	Analog	Plate Y, plus (Top)
TS-MY	P2-73	Analog	Plate Y, minus (Bottom)

Left, Right, Top, Bottom are alternative signal names used in some panels.

5.13. IDE (Hard disk) interface Implementation

The IDE interface is implemented by CPU local bus address/data lines and logic necessary to generate the control signals.

IDE Interface Signals

Signal	Pin Number	Type	Description
IDE-CS0#	P1-47	Out	**IDE Device Chip Select** for ATA command register block.
IDE-CS1#	P1-52	Out	**IDE Device Chip Select** for ATA control register block.
IDE-RD#	P1-46	Out	**Disk I/O Read.** This is the command to the IDE device that it may drive data onto the Data lines. Data is latched on the de-assertion edge of IDE-RD#.
IDE-WR#	P1-48	Out	**Disk I/O Write.** This is the command to the IDE device that it may latch data from the Data lines. Data is latched by the IDE device on the de-assertion edge of IDE-WR#.
IDE-IRQ	P1-49	In	**Interrupt Request** from IDE device

All other signals are derived from CM-X270 Local Bus interface.

IDE-CS0# & IDE-CS1# , as other general purpose chip selects available on the CAMI connectors are generated by onboard logic by combining the processor's nCS3 and MA[25:22] lines. IDE-CS signals can have maximum delay of 10 ns referred to nCS3. IDE-CS transactions are accompanied by IDE-RD# and IDE-WR# signals.
The appropriate addresses are listed in the memory-mapping table at the end of the manual.
IDE_IRQ is routed to PXA-270 GPIO[100].

5.14. Video Interface

This section describes the operation and signals of the quick capture interface of PXA270 processor, which provides a connection between the processor and a camera image sensor. The quick capture interface was designed to work primarily with CMOS-type image sensors. However, it may be possible to connect some CCD-type image sensors to the PXA270 processor, depending on a specific CCD sensor’s interface requirements.

The quick capture interface acquires data and control signals from the image sensor and performs the appropriate data formatting prior to routing the data to memory using direct

memory access (DMA). A broad range of interface and signaling options provides direct connection. The image sensor can provide raw data through a variety of parallel and serial formats. For sensors that provide pre-processing capabilities, the quick capture interface supports several formats for RGB and YCbCr color space. The interface supports the *International Telecommunication Union Recommendation ITU-R BT.656-4 (www.itu.int)* Start-of-Active-Video (SAV) and End-of-Active-Video (EAV) embedded synchronization sequences for four- and eight-bit configurations.

Features

- Parallel interface support for 8 bits
- Serial interface support for 4-bit and 5-bit device connections
- Support for ITU-R BT.656-4 SAV and EAV embedded synchronization
- Pre-processed capture modes:
  - RGB 8:8:8, RGBT 8:8:8, RGB 6:6:6, RGB 5:6:5, RGB 5:5:5, RGBT 5:5:5, RGB 4:4:4 data formats
  - YCbCr 4:2:2 data format
  - RGB component precision reductions for RGB 8:8:8
- Raw capture mode
  A common raw format is RGGB. The quick capture interface is capable of capturing most any raw format as long as the software running on the PXA270 processor has been written to correctly interpret that particular raw format.
- Support for packing of 8-, 9-, and 10-bit raw pixel precision
- Support for both packed and planar data formatting for YcbCr 4:2:2 formats
- Programmable vertical and horizontal resolutions up to 2048 x 2048
- Two 8-entry (by 64 bits) and one 16-entry (by 64 bits) FIFOs
- Programmable sensor clock output from 196.777 kHz to 52 MHz
- Programmable interface timing signals for internal and external synchronization
- Programmable interrupts for FIFO overflow, end-of-line, and end-of-frame
- Programmable frame capture rate allows users to capture all frames or 1 out of every 2 to 8 frames

For additional information, see “Quick Capture Interface” chapter 27 in PXA270 Reference Guide.

Interface Signals

CAMI Signal	CAMI pin in X270W (X270L)	PXA270 Name	Type	Description
VIP-CLK	P3-88 (P1-59)	CIF_PCLK	I	Pixel clock used by the quick capture interface to clock pixel data into the input FIFO. Cannot exceed 1/4 of CICLK, where CICLK is the same frequency as the LCD clock. For 104-MHz CICLK, the maximum CIF_PCLK is 26 MHz.
VIP-D0	P3-80 (P2-81)	CIF_DD [7:0]	I	Data lines to transmit 4, 5 or 8 bits of data per pixel clock cycle (9 & 10 bit data formats are not supported)
VIP-D1	P3-82 (P2-77)			
VIP-D2	P3-84 (P2-75)			
VIP-D3	P3-90 (P2-76)			
VIP-D4	P3-92 (P2-78)			
VIP-D5	P3-94 (P2-80)			
VIP-D6	P3-96 (P2-82)			
VIP-D7	P3-89 (P2-84)			
VIP-CS	P3-78 (P2-90)	CIF_LV	I/O	Line start or alternate synchronization signal used by the sensor to signal line readout or for external horizontal synchronization
VIP-ODD-EVEN	P3-93 (P2-87)	CIF_FV	I/O	Frame start or alternate synchronization signal used by the sensor to signal frame readout or for external vertical synchronization

5.15. Universal Subscriber Identity Module (USIM) Interface

The USIM interface of PXA270 processor is a primary device and communications interface for a GSM mobile handset. The USIM interface supports communication with smart cards as specified in the standard *ISO 7816-3* and technical specification 3G *TS 31.101* of the 3rd Generation Partnership Project.

Software controls the session between the USIM interface and the card by updating the USIM interface registers. Choosing protocol type and parameters, receiving or sending a byte to/from the card, activating/deactivating the card, setting transmitter/receiver baud rates, and similar operations are accomplished with read/write operations to the USIM interface registers. Transforming byte convention (inverse to direct and vice-versa, according to the session convention) is performed within the USIM interface. Hence, software does not have to perform format inversion before character receipt. The USIM interface provides functionality to support the above standards, but it is the responsibility of software to ensure the standards are met.

Features

- Compatible with any USIM card that is compliant with standard *ISO 7816-3* and *3G TS 31.101* and operates in voltages of 1.8 V or 3 V
- Supports control lines for two-level voltage supply (1.8V and 3V)
- Supports USIM card reset pin control (using reset pin control and power supply control, warm/cold reset can be software-initiated)
- Supports T = 0 and T = 1 protocols
- Programmable card clock frequency
- Supports any combination of the following clock-rate conversion factor F, and bit-rate adjustment factor D:
  F = {372, 512, 558}
  D = {1,2,4,8,16, 32, 12, 20}
- Auto-error signal in T = 0 receive mode
- Auto-character repeat in T = 0 transmit mode
- Transforms inverted format to regular format and vice-versa
- Programmable block guard time period
- Programmable extra guard time period
- Programmable character waiting time period
- Programmable block waiting time period
- Programmable time-out period
- Programmable CPU interrupt on an error-signal detection
- Programmable CPU interrupt when a smart card is connected

Interface Signals

PXA270 Name	Type	CAMI pin in X270W (X270L)	Description
UIO	I/O	P3-9 (P2-119)	USIM I/O Data. Receive and transmit data connection. The bidirectional pad is connected directly to the off-chip USIM card. When asserted, the I/O line is forced to low. When deasserted, the I/O line is pulled-up by a pull-up resistor.
UVS0/ UEN	O	P3-82 (P2-77)	Select for power transistor controlling voltage level supplied for card. Selects zero voltage on the USIM card power-supply pad (VCC). Alternative: USIM enable for VCC_USIM connection.
nUVS1/ UEN	O	P3-90 (P2-76)	Select for power transistor controlling voltage level supplied for card. Selects 1.8 V on the USIM card power-supply pad (VCC). Alternative: USIM enable for VCC_USIM connection.
nUVS2/ UDET	I/O	P3-84 (P2-75)	Select for power transistor controlling voltage level supplied for card. Selects 3.0 V on the USIM card power-supply pad (VCC). Alternative: USIM detection for card present.
UCLK	O	P3-42 P3-94 (P2-80)	Clock supplied to the card. This pin connects directly to the card clock pin. The card cannot use any other clock
nURST	O	P3-40 P3-92 (P2-78)	Card reset pin. Connects to card reset pin. The card is reset when this output is asserted.

* CAMI standard definition doesn't contain dedicated interface pins for USIM. Most of USIM signals are sharing interface with video input port.

5.16. WLAN interface

The following section refers to CM-X270L - revisions 1.4 and above. For CM-X270W and previous revisions of CM-X270L please refer to the following grayed section below.

The CM-X270 module incorporates full-featured 802.11 b/g capabilities, implemented by Wi2Wi W2SW0001 WLAN controller module. The W2SW0001 is a complete IEEE 802.11 b/g radio solution based on the Marvell's 88W8686 chipset.

W2SW0001 controller supports security features:

- WEP encryption (64 bit/128 bit)
- WPA TKIP security
- WPA2

Antenna connection

The W2SW0001 requires a single 2.45GHz antenna. The antenna is connected to the UFL (sometimes referred to as MHF or IPEX) high frequency on-board connector J3. Any type of 2.45GHz WLAN antenna may be used.

On-board interface

W2SW0001 is connected to the PXA-270 CPU using SPI2 interface:

Signal name (internal)	PXA270 GPIO	Alternate function setting	Description
WLAN-SSPFRM	14	SSPSFRM2 (out)	SPI frame
WLAN-SSPCLK	19	SSPSCLK2 (out)	SPI clock
WLAN-SSPTXD	87	SSPTXD2 (out)	SPI data out (MOSI)
WLAN-SSPRXD	88	SSPRXD2 (in)	SPI data in (MISO)
WLAN-EN	102	GPIO (out)	Power enable, active high
WLAN-INT	95 (270L)	GPIO (in)	Interrupt signal, active high

RF Specifications

802.11b RF system specifications			
Transmit Power Output		15	dBm
Receive Sensitivity	1 Mbps, 8% PER	-87	dBm
	2 Mbps, 8% PER	-87	dBm
	5.5 Mbps, 8% PER	-87	dBm
	11 Mbps, 8% PER	-85	dBm

Maximum Receive Level	PER < 8%	IEEE Compliant	
Transmit Frequency Offset	Low, Middle, High channels	+/-10	PPM
Spectral Mask	Max. TX power	-40@fc+/-11MHz	dBc
		-60@fc+/-22MHz	
Error Vector Magnitude	Max. TX power @ 11Mbps	-36	dB
Carrier Suppression	Max. TX power	-25	dBc
Adjacent channel rejection	Desired channel is 3dB above sensitivity, 11Mbps, PER < 8%	48	dBc
802.11g RF system specifications			
Transmit Power Output		15	dBm
Receive Sensitivity	6 Mbps, 10% PER	-86	dBm
	9 Mbps, 10% PER	-85	dBm
	12 Mbps, 10% PER	-85	dBm
	18 Mbps, 10% PER	-84	dBm
	24 Mbps, 10% PER	-80	dBm
	36 Mbps, 10% PER	-77	dBm
	48 Mbps, 10% PER	-73	dBm
	54 Mbps, 10% PER	-72	dBm
Maximum Receive Level	PER < 8%	IEEE Compliant	
Transmit Frequency Offset	Low, Middle, High channels	+/-10	PPM
Spectral Mask	Max. TX power	-30@fc+/-11MHz	dBc
		-40@fc+/-20MHz	
		-50@fc+/-30MHz	
Error Vector Magnitude	Max. TX power @ 54Mbps	-29	dB
Carrier Suppression	Max. TX power	-25	dBc
Adjacent channel rejection	Desired channel is 3dB above sensitivity, 54Mbps, PER < 8%	15	dBc

Power Consumption

Mode	Conditions	Min	Typ	Max	Units
802.11b Current Consumption at 3.3V					
Initialization			100		mA
Continuous Transmit	@11Mbps	190	210	230	mA
Continuous Receive	@11Mbps	160	180	190	mA
Power Save			10		mA

802.11g Current Consumption at 3.3V					
Initialization			100		mA
Continuous Transmit	@54Mbps	220	230	240	mA
Continuous Receive	@54Mbps	200	210	220	mA
Power Save			10		mA

The following section refers to CM-X270W and CM-X270L - revisions 1.3 and older. Ignore this section if you purchased evaluation kit later than 24-Jun-2008

CM-X270 modules incorporate full-featured 802.11b capability implemented using Phillips BGW200 WLAN controller. The implementation contains baseband MAC subsystem, RF transceiver and high-power RF front-end thus incorporating all components required to provide high-quality WLAN capability.
The BGW200 is based on internal controller subsystem with dedicated CPU, ROM and RAM. The subsystem executes firmware, responsible for all low-level WLAN networking functionality, thus considerably reducing the load on the main CPU.
The RF interface supports antenna diversity for improved stability. It provides +16dBm transmitter output power - the standard level for 802.11 NICs.
BGW200 firmware supports both infrastructure (access point managed) and independent (without access point) network topologies. On the other hand, firmware does not support BGW200 acting as an access point.

Antenna connection

One to two antennas can be connected to the CM-X270L module.
Antennas are attached to the UFL (sometimes referred as MHF or IPEX) high frequency connectors located on the CM-X270L. Any type of 2.45GHz WLAN antenna can be used. The first antenna, connected to J3 is used for both reception and transmission. The second (optional) antenna, connected to J2, is used for reception only when BGW200 is in antenna diversity mode. In latter case, BGW200 subsystem chooses to receive from antenna with the best signal quality. In most cases the second antenna can be omitted. *(Furthermore, in certain cases diversity mode can affect system performance, therefore it is recommended to start evaluation of the system with only one antenna - J3.)*
See section 6.2 for connector location.

On-board interface
BGW200 is connected to the PXA-270 CPU using SPI2 interface:

Signal name (internal)	PXA270 GPIO	Alternate function setting	Description
WLAN-SSPFRM	14	SSPSFRM2 (out)	SPI frame
WLAN-SSPCLK	19	SSPSCLK2 (out)	SPI clock
WLAN-SSPTXD	87	SSPTXD2 (out)	SPI data out (MOSI)
WLAN-SSPRXD	88	SSPRXD2 (in)	SPI data in (MISO)
WLAN-EN	102	GPIO (out)	Power enable, active high
WLAN-INT	95 (270L) 103 (270W)	GPIO (in)	Interrupt signal, active high

CAMI interface

Signal	Pin Number	Type	Description
WLAN-WL (CM-X270L only)	P2-94	Out	Indicates WLAN activity (reception and transmission)

NVM data
During CM-X270L manufacturing process, WLAN subsystem configuration and RF calibration data is stored in the NOR flash. RF calibration data allows BGW200 to provide its best RF performance throughout wide range of temperatures while still staying compliant with FCC regulations . WLAN MAC address is also stored in NOR flash.

RF Specifications

Symbol Parameter	Conditions	Typ. value	Unit
Receiver sensitivity			
1 Mbps sensitivity	PER < 8% PSDU = 1024 bytes	-91	dBm
2 Mbps sensitivity		-87	dBm
5.5 Mbps sensitivity		-83	dBm
11Mbps sensitivity		-83	dBm
Maximum input level			
Max input level for 2 Mbps	PER < 8% PSDU = 1024 bytes	-0.4	dBm
Max input level for 11 Mbps		0.6	dBm
Linear output power			
1 Mbps and 2 Mbps output power	meets FCC restricted band specifications	15.5	dBm
5.5 Mbps and 11 Mbps output power		16	dBm

** All values at nominal supply voltage, 25°C and channel 6*

Maximum power consumption figures:

Receive - 230 mA
Transmit - 320 mA

Security features:

• WEP64
• WEP128

Other firmware features:

• Extended rate protection
• Regulatory domain
• Power save protocol
• Fragmentation & De-fragmentation
• Antenna diversity

Infrastructure/Ad-hoc modes:

• BSS
• IBSS

5.17. GPRS/GSM Module

The cellular GSM/GPRS connectivity feature of the CM-X270W is based on the Telit GE864 module. The GE864 module allows digital communication services wherever a GSM 850, 900, DCS 1800 or PCS 1900 network is present.
The GE864 includes features like GPRS Class 10, Voice, Circuit Switched Data transfer, Fax, Phone book, SMS support and 'EASY GPRS' embedded TCP/IP stack.
The module also provides SIM card interface with auto-detection and hot insertion.
The interface supports phase 2 GSM11.14 - SIM 3V.

The GE864 module is interfaced to the PXA270 processor via the BTUART.
The SIM interface is available on the CAMI connectors. SIM card socket should be provided externally. GSM/GPRS feature is available only in CM-X270W revision 2.

Interface Signals

Signal Name	Type	CAMI pin in X270W	Description
GPRS_SIMRST	O	P3-51	SIM card reset
GPRS_SIMCLK	O	P3-53	SIM card clock
GPRS_SIMIO	I/O	P3-57	SIM card data I/O
GPRS_SIMIN	I	P3-59	SIM card detect. Should be pulled down when a card is inserted.
GPRS_SIMVCC	POWER	P3-61	SIM card power supply
GPRS_STATLED	O	P2-124	GPRS MODEM status LED indicator. Active high, 0-1.8V. Intended to control a LED-driving transistor.
GPRS_TXMON	O	P3-6	GPRS MODEM transmit indicator.

GPRSFUNC register

Physical address in PXA270 address space: 0x5200000
This register is a two bit, write only register.
The data is provided on address lines A17 and A19 during write cycle.

A17 high – enable BTUART to GPRS MODEM.
A17 low – disable BTUART to GPRS MODEM.

When BTUART to GPRS MODEM is disabled, it can be used for communication with other off-board devices or as a GPIO.

A19 high – assert GPRS ON signal
A19 low – deassert GPRS ON signal

In order to turn on the GPRS MODEM, the GPRS ON signal should be asserted for at least one second and then deasserted.

Audio Path Connection

The GE864 audio signals are connected to the CM-X270W audio system, providing the audio functionality of a standard cellular phone. The MONOOUT output channel of the WM9712 CODEC is connected to the MIC_MT input of the GPRS MODEM. The EAR_MT audio output of the GPRS MODEM is connected to the PHONE input channel of the WM9712 CODEC.

Power supply

The GPRS MODEM is powered by the common VCC3_3 rail of the CM-X270W. However, the GPRS modem requires 3.6V supply to operate properly. Thus, on cards with GPRS (K) option, the main VCC3-3 rail has to be raised to 3.6V. All other on-board components connected to 3.3V rail are capable to operate properly from 3.6V supply. Please see section 4.6 in the "SB-X270 Reference Guide" for more details about the power supply modification.

Antenna

The antenna should fulfill the following requirements:

Frequency range	Depending on frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	136 MHz in GSM 850/900, 170 MHz in DCS, 140 MHz PCS
Gain	> 1.5 dBi
Impedance	50 ohm
Input power	> 2 W peak power
VSWR absolute max	10:1
VSWR recommended	< 2:1

The module RF signal is routed to the J6 standard UFL connector for off-board antenna connection. See section 6.2 for connector location.

RF Specifications

Operating Frequency				
Mode	Freq. TX (MHz)	Freq. RX (MHz)	Channels (ARFC)	TX - RX offset
E-GSM-850	824.2÷848.8	869.2÷893.8	0 – 124	45 MHz
E-GSM-900	890.0 - 914.8	935.0 - 959.8	0 – 124	45 MHz
	880.2 - 889.8	925.2 - 934.8	975 - 1023	45 MHz
DCS-1800	1710.2 - 1784.8	1805.2 - 1879.8	512 – 885	95 MHz
PCS-1900	1850.2 - 1909.8	1930.2 - 1989.8	512 – 810	80 MHz

Output Power		
Mode	Device class	Nominal Peak Power
GSM–850/900	class 4	+33dBm
DCS–1800/PCS–1900	class 1	+30dBm

Reference sensitivity		
Mode	Device class	Nominal Peak Power
GSM–850/900	class 4	-107dBm
DCS–1800/PCS–1900	class 1	-106dBm

NOTE: The modem default configuration is set to the European (GSM-900 GSM-1800) band frequencies. Users in the US and Canada need to re-configure the modem to the GSM-850 GSM-1900 bands. Use the "AT#BND=3" command to set the proper band settings. Please see page 300 in the “Telit AT Commands Reference Guide” for detailed info about the band configurations.

LED Indication

The onboard the GPRS_STATLED signal provides information regarding network service availability and call status.

LED status	**GSM module status**
Permanently off	GSM module off
Fast blinking (period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (period 3s, Ton 0,3s)	Registered full service
Permanently on	A call is active

5.18. Bluetooth Module (CM-X270W rev 2.x only)

The CM-X270W Bluetooth system is based on the CSR BlueCore 4-ROM component. The BlueCore 4-ROM is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.
With the on-chip CSR Bluetooth software stack, it provides a fully-compliant Bluetooth system to v2.0 of the specification for data and voice communications.

Features:

- Fully Qualified Bluetooth v2.0+EDR system
- Enhanced Data Rate (EDR) compliant with v2.0 of specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support

The BlueCore 4-ROM is connected PXA270 processor through USB port.

Antenna Connection

The CM-X270W features a small on-board ceramic patch antenna dedicated to Bluetooth connectivity. Alternatively, an external antenna may be connected via the on-board J4 UFL high frequency connector. See section 6.2 for connector location.
Note: The external antenna cannot operate together with the on-board patch antenna. In order to use an external Bluetooth antenna, the on-board antenna must be disabled.

RF Specification

Standards	IEEE 802.15.1
BlueTooth Class	Class II device
Wireless Signal Rates	2.1Mbps (Bluetooth 2.0)
Wireless Transmit Power*	4dBm
Wireless Operating Range*	Up to 10m
Receiver Sensitivity*	-84dBm

* Preliminary data

Interface Signals

Signal Name	Type	CAMI*	Description
BT_PIO0_RXEN	O	P3-64	CSR BC-4 GPIO/RX indicator. Can be used to drive a status LED.
BT_PIO1_TXEN	O	P2-120	CSR BC-4 GPIO/TX indicator. Can be used to drive a status LED.
BT_AUXDAC	O	P3-118	Gain control for external amplifier.

* CAMI pin in CM-X270W only

6. Baseboard Interface

The CM-X270 connects to the external world through P1, P2 and P3 - 0.6 mm pitch 140-pin connectors.

6.1. Connectors Type and Layout

	Mfg.	CM-X270 connector P/N	Baseboard (mating) connector P/N
P1, P2, P3	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab,
see [prices] >> [accessories] links in CompuLab's website.
CompuLab's p/n name for AMP/Tyco 1-5353190-0 connector is "CON140".

Standoffs

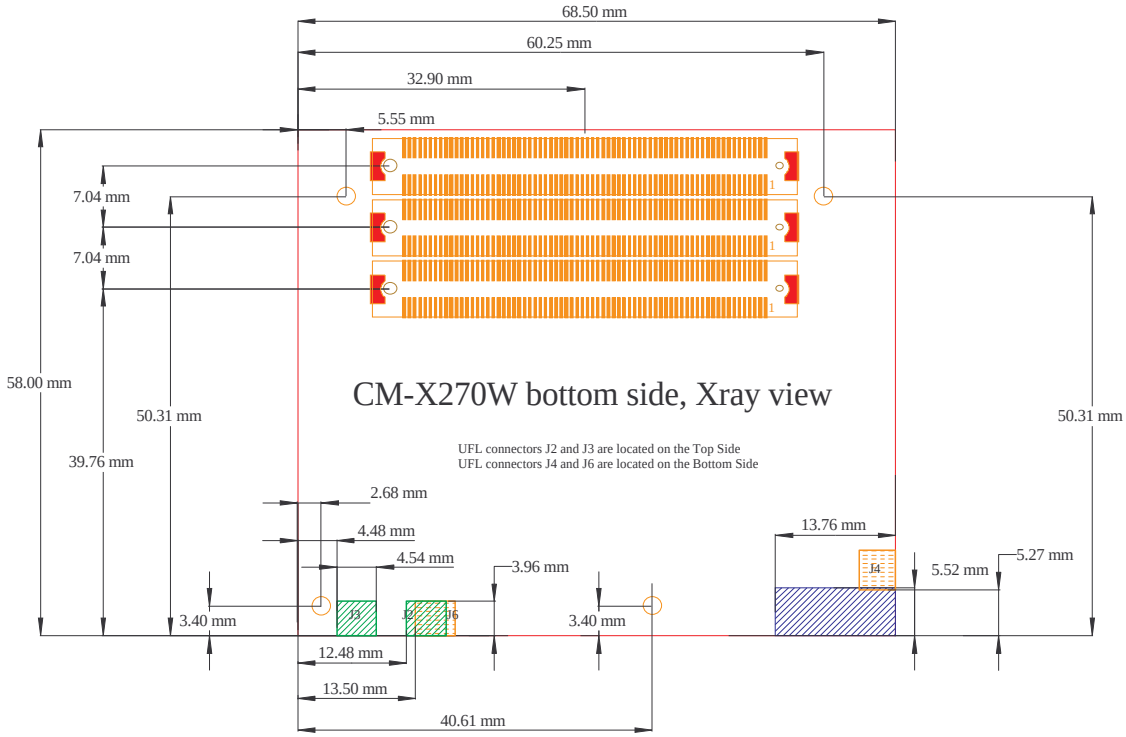
CM-X270 has four mounting holes for standoffs. Standoff implemented by three parts: screw, spacer and nut.

	Description	Manufacturer and P/N
Screw	M2, 10 mm length	▪ FCI 95121-005 ▪ Acton InoxPro BF22102010 ▪ World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	▪ Hirosugi ASU-2004 ▪ MAC8 2SP-4 ▪ World Bridge Machinery M2, L=4.2 mm

Nut	M2, 1.6-2.0mm width	▪ FCI 92869-001 (or 002) ▪ Acton InoxPro BG12102000 ▪ Bossard 1241397 (DIN934-A2 M2) ▪ World Bridge Machinery 381A52000

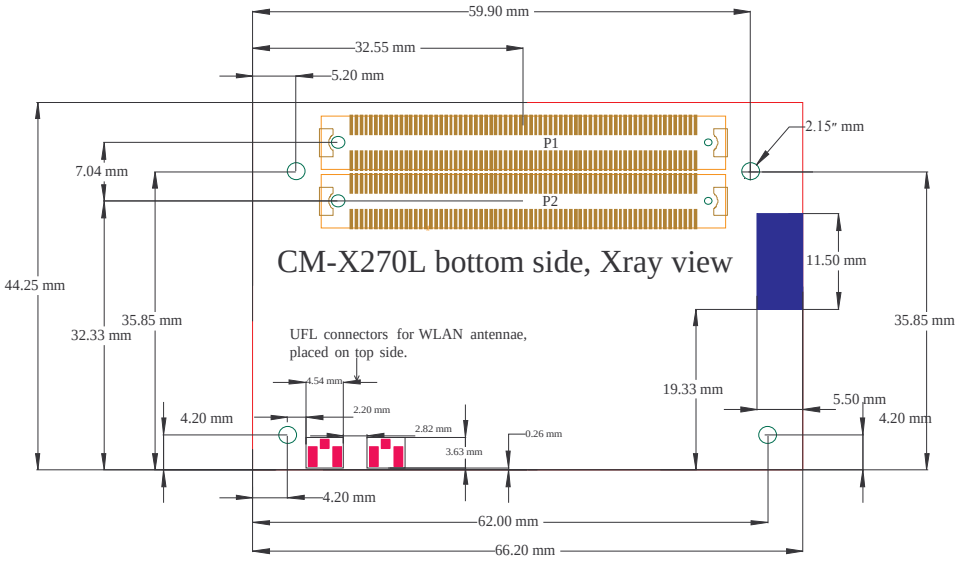
6.2. Mechanical drawings

CM-X270W



* Maximum height of the components which can be placed under the CM-X270W in the area marked with blue is 0.5mm.
* Maximum height of the components which can be placed under the CM-X270W in other areas is 2mm.
* The thickness of the PCB is 1.8mm.
* Maximum height of the components placed on the top side of the CM-X270W is 2.5mm.
* The board-to-board height provided by the CAMI connector is 4mm.

CM-X270L



- Maximum height of the components which can be placed under the CM-X270 (either W or L versions) in the blue colored areas is 0.5mm.
- Maximum height of the components which can be placed under the CM-X270 in other areas is 2mm.
- PCB thickness for CM-X270L is 1.6mm, for CM-X270W is 1.8mm.
- Maximum height of the components assembled on the top side of the CM-X270 is 2.5mm.
- The board-to-board height provided by the CAMI connectors is 4mm.

Mechanical drawings are available in DXF format from CompuLab's website, following [Developer] >> [CM-X270] >> [CM-X270 - Dimensions and Connectors Location] links.

6.3. Connector pin-out sorted by pin numbers

Signals colored in [gray] are not available in CM-X270W. They are specified as placeholder references of generic CAMI pinout.

Connections marked with (*) are valid for CM-X270L only.

P1 connector

P1-02	ETH1-RDN	P1-01	ETH1-TDP
P1-04	ETH1-RDP	P1-03	ETH1-TDN
P1-06	ETH1-LINK10#	P1-05	ETH1-LINK100#
P1-08	**GND**	P1-07	**VCORE**
P1-10	ETH1-ACT#	P1-09	WP1#
P1-12	MM-CLK	P1-11	RST-IN#
P1-14	**GND**	P1-13	GPIO[112] (MM-CMD)
P1-16	GPIO[109] (MM-DAT1)	P1-15	GPIO[92] (MM-DAT0)
P1-18	GPIO[111] (MM-DAT3)	P1-17	PME#
P1-20	VCC-RTC	P1-19	**VCORE**
P1-22	COM-A-RX	P1-21	-
P1-24	COM-A-TX	P1-23	COM-B-RX
P1-26	**GND**	P1-25	COM-B-TX
P1-28	COM-C-RX	P1-27	COM-D-RX
P1-30	COM-C-TX	P1-29	COM-D-TX
P1-32	COM-C-DCD#	P1-31	**VCC3-3-STBY**
P1-34	COM-C-DTR#	P1-33	COM-D-DCD# GPIO[12]*
P1-36	COM-C-DSR#	P1-35	COM-D-DTR# GPIO[52]*
P1-38	**GND**	P1-37	COM-D-DSR# GPIO[97]*
P1-40	COM-C-CTS#	P1-39	COM-D-CTS# GPIO[44]*
P1-42	COM-C-RTS#	P1-41	COM-D-RTS# GPIO[45]*
P1-44	COM-C-RIN#	P1-43	**VCORE**
P1-46	IDE-RD#	P1-45	COM-D-RIN# GPIO[105]*
P1-48	IDE-WR#	P1-47	IDE-CS0#
P1-50	**GND**	P1-49	IDE-IRQ
P1-52	IDE-CS1#	P1-51	LB-IRQ0
P1-54	LB-IRQ1	P1-53	TS-PX
P1-56	DEBUG1	P1-55	**VCORE**
P1-58	DEBUG0	P1-57	TS-PY
P1-60	SDA	P1-59	SSI-DIN*
P1-62	**GND**	P1-61	SCL

P1-64	LB-A0	P1-63	LB-A1
P1-66	LB-A2	P1-65	LB-A3
P1-68	LB-A4	P1-67	**VCC3-3**
P1-70	LB-A6	P1-69	LB-A5
P1-72	LB-A8	P1-71	LB-A7
P1-74	**GND**	P1-73	LB-A9
P1-76	LB-A10	P1-75	LB-A11
P1-78	LB-A12	P1-77	LB-A13
P1-80	LB-A14	P1-79	**VCORE**
P1-82	LB-A16	P1-81	LB-A15
P1-84	LB-A18	P1-83	LB-A17
P1-86	**GND**	P1-85	LB-A19
P1-88	LB-A20	P1-87	LB-A21
P1-90	LB-A22	P1-89	LB-A23
P1-92	LB-A24	P1-91	**VCORE**
P1-94	LB-D0	P1-93	LB-A25
P1-96	LB-D2	P1-95	LB-D1
P1-98	**GND**	P1-97	LB-D3
P1-100	LB-D4	P1-99	LB-D5
P1-102	LB-D6	P1-101	LB-D7
P1-104	LB-D8	P1-103	**VCC3-3**
P1-106	LB-D10	P1-105	LB-D9
P1-108	LB-D12	P1-107	LB-D11
P1-110	**GND**	P1-109	LB-D13
P1-112	LB-D14	P1-111	LB-D15
P1-114	PCM-IOCS16#	P1-113	LB-IORDY
P1-116	LB-RD#	P1-115	**VCORE**
P1-118	LB-WR#	P1-117	PCM-MEMR#
P1-120	PCM-MEMW#	P1-119	PCM-IOR#
P1-122	**GND**	P1-121	PCM-IOW#
P1-124	PCM-CE1#	P1-123	PCM-WAIT#
P1-126	PCM-CDA#	P1-125	PCM-RST#
P1-128	PCM-INTRDYA	P1-127	**VCORE**
P1-130	PCM-WE#	P1-129	PCM-REG#
P1-132	PCM-SKTSEL	P1-131	PCM-CE2#
P1-134	**GND**	P1-133	LB-CS0#
P1-136	USB3-P	P1-135	LB-CS1#
P1-138	USB3-N	P1-137	RST-OUT#
P1-140	**VCC5**	P1-139	**VCC3-3**

Note: DEBUG0,1 pins are reserved for CompuLab's use.

P2 connector

P2-02	**GND**	P2-01	PCI-REQ0#
P2-04	MMC-DAT2	P2-03	PCI-GNT0#
P2-06	PCI-INTA#	P2-05	PCI-GNT1#
P2-08	PCI-INTB#	P2-07	**VCC3-3**
P2-10	LPC-LAD0	P2-09	LPC-LAD1
P2-12	LPC-LAD2	P2-11	LPC-LAD3
P2-14	**GND**	P2-13	LPC-SERIRQ
P2-16	PCI-CLK0	P2-15	LPC-LFRAME#
P2-18	PCI-REQ1#	P2-17	LPC-LDRQ#
P2-20	PCI-AD0	P2-19	**VCORE**
P2-22	PCI-AD1	P2-21	PCI-AD2
P2-24	PCI-AD3	P2-23	PCI-AD4
P2-26	**GND**	P2-25	PCI-AD5
P2-28	PCI-AD6	P2-27	PCI-AD7
P2-30	PCI-CBE0#	P2-29	PCI-AD8
P2-32	PCI-AD9	P2-31	**VCORE**
P2-34	PCI-AD10	P2-33	PCI-AD11
P2-36	PCI-AD12	P2-35	PCI-AD13
P2-38	**GND**	P2-37	PCI-AD14
P2-40	PCI-AD15	P2-39	PCI-CBE1#
P2-42	PCI-PAR	P2-41	PCI-SERR#
P2-44	PCI-PERR#	P2-43	**VCC3-3**
P2-46	PCI-STOP#	P2-45	PCI-DEVSEL#
P2-48	PCI-TRDY#	P2-47	PCI-IRDY#
P2-50	**GND**	P2-49	PCI-FRAME#
P2-52	PCI-CBE2#	P2-51	PCI-AD16
P2-54	PCI-AD17	P2-53	PCI-AD18
P2-56	PCI-AD19	P2-55	**VCORE**
P2-58	PCI-AD20	P2-57	PCI-AD21
P2-60	PCI-AD22	P2-59	PCI-AD23
P2-62	**GND**	P2-61	PCI-CBE3#
P2-64	PCI-AD24	P2-63	PCI-AD25
P2-66	PCI-AD26	P2-65	PCI-AD27
P2-68	PCI-AD28	P2-67	**VCORE**
P2-70	PCI-AD29	P2-69	PCI-AD30
P2-72	PCI-AD31	P2-71	TS-MX

P2-74	**GND**	P2-73	TS-MY
P2-76	GPIO[115]*	P2-75	GPIO[116]*
P2-78	GPIO[90]*	P2-77	GPIO[114]*
P2-80	GPIO[91]*	P2-79	**VCC3-3**
P2-82	GPIO[17]*	P2-81	GPIO[27]*
P2-84	GPIO[108]*	P2-83	GPIO[106]*
P2-86	**GND**	P2-85	GPIO[107]*
P2-88	SSI-CLK*	P2-87	SSI-FRM*
P2-90	SSI-DOUT*	P2-89	SYS_EN*
P2-92	GPIO[86]*	P2-91	**VCORE**
P2-94	WLAN_WL*	P2-93	GPIO[99]*
P2-96	LCD-LP	P2-95	LCD-B1
P2-98	**GND**	P2-97	LCD-B2
P2-100	LCD-B3	P2-99	LCD-B4
P2-102	LCD-B5	P2-101	LCD-G0
P2-104	LCD-G1	P2-103	**VCORE**
P2-106	LCD-G2	P2-105	LCD-G3
P2-108	LCD-G4	P2-107	LCD-G5
P2-110	**GND**	P2-109	LCD-R1
P2-112	LCD-SCK	P2-111	LCD-FRM
P2-114	LCD-DE-M	P2-113	LCD-R2
P2-116	LCD-R3	P2-115	**VCORE**
P2-118	LCD-R4	P2-117	LCD-R5
P2-120	BT_PIO1_TXEN	P2-119	UIO*
P2-122	**GND**	P2-121	IRDA-TX
P2-124	GPRS_STATLED	P2-123	IRDA-RX
P2-126	AUD_OUTC	P2-125	PCM-CDB#
P2-128	PCM-INTRDYB	P2-127	**VCORE**
P2-130	AUD-INR [AC97-SDOUT]	P2-129	AUD-SPDIF [AC97-RST#]
P2-132	AUD-INL-MIC [AC97-BITCLK]	P2-131	AUD-OUTL [AC97-SDIN0]
P2-134	**GND**	P2-133	USB-OVC#
P2-136	AUD-OUTR [AC97-SYNC]	P2-135	**VCC3-3**
P2-138	USB1-P	P2-137	USB2-P
P2-140	USB1-N	P2-139	USB2-N

P3 connector

P3-02	ETH2-RDP	P3-01	ETH2-TDN
P3-04	ETH2-RDN	P3-03	ETH2-TDP
P3-06	ETH2-LINK10# GPRS_TXMON	P3-05	ETH2-LINK100# AC_AD4
P3-08	**GND**	P3-07	**VCORE**
P3-10	ETH2-ACT# AC_AD3	P3-09	UIO
P3-12	SPARE	P3-11	SPARE
P3-14	**GND**	P3-13	PCI-REQ3#
P3-16	PCI-CLK1	P3-15	PCI-GNT3#
P3-18	PCI-GNT2#	P3-17	PCI-INTD#
P3-20	PCI-INTC#	P3-19	**VCC3-3**
P3-22	PCI-REQ2#	P3-21	COM-A-DCD#
P3-24	PCI-CLK2	P3-23	COM-A-DTR#
P3-26	**GND**	P3-25	COM-A-DSR#
P3-28	COM-A-RTS#	P3-27	COM-A-CTS#
P3-30	COM-A-RIN#	P3-29	COM-B-DCD#
P3-32	COM-B-RTS#	P3-31	**VCORE**
P3-34	COM-B-RIN#	P3-33	COM-B-CTS#
P3-36	COM-B-DTR#	P3-35	COM-B-DSR#
P3-38	**GND**	P3-37	GPIO[102]
P3-40	GPIO[19]	P3-39	GPIO[101]
P3-42	GPIO[14]	P3-41	GPIO[100]
P3-44	GPIO[12]	P3-43	**VCORE**
P3-46	GPIO[105]	P3-45	GPIO[86]
P3-48	GPIO[104]	P3-47	GPIO[106]
P3-50	**GND**	P3-49	GPIO[52]
P3-52	GPIO[103]	P3-51	GPRS_SIMRST
P3-54	GPIO[99]	P3-53	GPRS_SIMCLK
P3-56	GPIO[87]	P3-55	**VCC3-3**
P3-58	GPIO[97]	P3-57	GPRS_SIMIO
P3-60	GPIO[107]	P3-59	GPRS_SIMIN
P3-62	**GND**	P3-61	GPRS_SIMVCC
P3-64	BT_PIO0_RXEN	P3-63	IDE-DREQ
P3-66	IDE-RDY#	P3-65	IDE-DACK#
P3-68	LB-CS2#	P3-67	**VCORE**

P3-70	LB-CS3#	P3-69	LB-DREQ0
P3-72	GPIO[88]	P3-71	LB-DACK0#
P3-74	**GND**	P3-73	LB-DREQ1
P3-76	AC97_SYSCLK	P3-75	LB-DACK1#
P3-78	VIP-CS	P3-77	JTAG-TCK
P3-80	VIP-D0	P3-79	**VCORE**
P3-82	VIP-D1	P3-81	JTAG-TMS
P3-84	VIP-D2	P3-83	JTAG-TDI
P3-86	**GND**	P3-85	JTAG-TDO
P3-88	VIP-CLK	P3-87	JTAG-TRST#
P3-90	VIP-D3	P3-89	VIP-D7
P3-92	VIP-D4	P3-91	**VCC3-3**
P3-94	VIP-D5	P3-93	VIP-ODD/EVEN
P3-96	VIP-D6	P3-95	SLEEP-OUT#
P3-98	**GND**	P3-97	SPARE
P3-100	WP2#	P3-99	**VCC5-STBY**
P3-102	**VCC3-STBY**	P3-101	MG-LCD1-PWM
P3-104	**VCC3-STBY**	P3-103	**VCORE**
P3-106	**VCC3-STBY**	P3-105	-
P3-108	SSP_CIF_MCLK	P3-107	**VCC3-STBY**
P3-110	**GND**	P3-109	**VCC3-STBY**
P3-112	MG-B0	P3-111	**VCC3-STBY**
P3-114	PCM-BVD1	P3-113	AC_AD2
P3-116	PCM-VPPEN	P3-115	**VCORE**
P3-118	PCM-CE# BT_AUXDAC	P3-117	AC_AD1
P3-120	AC97-BITCLK	P3-119	AC97-SDIN0
P3-122	**GND**	P3-121	AC97-SDIN1
P3-124	AC97-RST#	P3-123	AC97-SDOUT
P3-126	LCD-B0	P3-125	AC97-SYNC
P3-128	LCD-R0	P3-127	**VCC3-3**
P3-130	LCD-VDDEN	P3-129	MG-R0
P3-132	MG-R1	P3-131	**VCC5**
P3-134	**GND**	P3-133	MG-B1
P3-136	MG-G1	P3-135	**VCC3-3**
P3-138	TV-OUT	P3-137	USB4-P
P3-140	MG-G0	P3-139	USB4-N

6.4. Baseboard Design Guidelines

- All power pins must be connected, including GND, VCC3, VCORE, VCC_USIM, VCC5 and STBY (Standby) power rails. If 5V is not used in the system, VCC5 should be connected to the 3.3V supply.
- Major power rails - GND and VCC3/VCORE must be implemented by planes, rather than traces. Note that in CM-X270, VCC3 and VCORE are the same voltage, therefore the same baseboard plane can be used. Using at least two planes is essential to assure system's signal quality, because planes providing current return path for all interface signals.
- It is recommended to put several 100 nF and 10/100 uF capacitors between VCC3 and GND near the mating connectors.
- It is recommended to connect standoff holes of baseboard to GND, in order to improve EMC. The top right hole of the baseboard should be isolated, for compatibility with future CAMI modules. (referring to module's orientation drawn on pages 111-112)
- Except of power connection, no other connection is mandatory for CM-X270 operation. All powerup electronics and all required pullups/pulldowns are found on the module.
- If for some reason you decide to place external pullup or pulldown resistor on certain signal (for example - on GPIO's), check the documentation of that signal as provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCI bus design must take into account signals skew and reflection.
  - Ethernet and USB signals must be routed in differential pairs and by controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
  - Local bus / PCMCIA signals must be buffered in most cases.

  Certain sections of this manual providing more details regarding routing of specific signals, for example - see Ethernet and local bus sections.

- Be careful when placing component under the CM-X270 module. CAMI connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-X270. In general, maximum allowable height for components placed under the CM-X270 is 2mm. There are special areas where maximum height is 0.5 mm only. For details refer to CM-X270 mechanical documentation.
- Reference designs: two reference designs are available - ATX and SB-X270 baseboard. SB reference is simpler, because it is specific to CM-X270. ATX design is more complicated, because it is generic for all computer-on-modules available from CompuLab.

6.5. Baseboard Troubleshooting

- Using grease solvent and soft brush, clean contacts of mating connectors of both module and baseboard. Remainders of soldering paste can prevent proper contact.
- Using oscilloscope, check voltage levels and quality of VCC3/VCORE power supplies. It should be 3.3V +/- 5%. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of mating connector.
- Using oscilloscope verify that GND pins of mating connector are indeed at zero voltage level, and there is no ground bouncing. Module must be plugged in during the test.
- Create "minimum system" - only power, mating connectors, the module, and serial interface.

  Check if the system starts properly. In system larger than minimum, the possible sources of disturbance could be:

  - Devices improperly driving local bus or PCI bus
  - External pullup / pulldown resistors overriding module’s on-board values, or any other components creating the same "overriding" effect.
  - Bad power supply.

  In order to avoid possible sources of disturbance, it is strongly recommended to start with minimal system and then add/activate off-board devices one by one.
- Check for existence of soldering shorts between pins of mating connectors. Even if signals are not used on the baseboard, shorting them on the connectors can disable module's operation. Initial check can be performed using microscope. However, if microscope inspection finds nothing, it is advised to check using X-ray, because often solder bridges are deeply beneath the connector's body. Note that solder shorts are the most frequent factor disabling module's start.
- Check possible signals shorting due to errors of baseboard PCB design or assembling.

- Improper function of customer baseboard can accidentally delete ARMmon or even damage module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's ATX or SB-X270 baseboard.
- It is recommended to assemble more that one baseboard for prototyping, in order to allow quick sorting out of problems related to specific board assembly.

7. Address Range Mapping

Memory Address	PXA270 Function	Usage in CM-X270
0x60000000 : 0x4C000000	Reserved Address Space	
0x48000000	Memory Mapped Registers	Memory Ctrl
0x44000000	Memory Mapped Registers	LCD
0x40000000	Memory Mapped Registers	PXA270 on-chip peripherals
0x30000000	PCMCIA/CF	Slot 1
0x20000000	PCMCIA/CF	Slot 0
0x1C000000	Reserved Address Space	
0x18000000	Reserved Address Space	
0x14000000	Static Chip Select 5	2700G
0x13E00000	Static Chip Select 4	LPC address window (through Interface Bridge)
0x10000000	Static Chip Select 4	Interface Bridge
0x0C000000	Static Chip Select 3	Local Bus CSx and IDE CS# [0,1]
0x08000000	Static Chip Select 2	2700G
0x04000000	Static Chip Select 1	Onboard peripherals
0x00000000	Static Chip Select 0	NOR Flash

CM-X270 utilizes onboard logic in order to generate chip select signals for onboard peripherals and external local bus. CPU signals nCS1, nCS3 and MA[25:22] are used for this purpose. The table below lists the valid nCSx and MA combinations:

nCS1	nCS3	MA25	MA24	MA23	MA22	Active chip select
L	H	0	0	0	0	NAND flash
L	H	0	1	0	1	RTC
L	H	0	1	1	0	Ethernet (DM9000)
H	L	0	0	0	0	LB-CS0#
H	L	X	X	X	X	LB-CS1#
H	L	0	1	0	0	LB-CS2#
H	L	0	1	1	0	LB-CS3#
H	L	1	1	0	0	IDE-CS0#
H	L	1	0	0	0	IDE-CS1#
H	L	1	0	0	1	IDE-CS1#

X – don’t care

NOR flash block mapping

Refer to description in ARMmon Reference Guide, available following [Developer] >> [CM-X270] >> [ARMmon - image and documentation] links in CompuLab's web-site.

8. Operating Temperature Ranges

The CM-X270 is available with three options of operating temperature range:

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20^{o} to 70^{o} C	Every card undergoes short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every card is extensively tested for both lower and upper limits and at several midpoints.