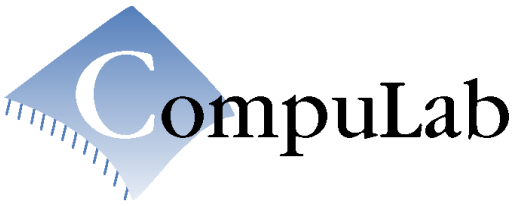
CM-xAM Embedded PC Module

Reference Guide

August 15, 2010



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Revision Information

Date	Description
May 10, 2010	Intermediate Draft Release
Aug 15, 2010	Initial release

Please check for a newer revision of this manual in CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic form version you have.

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1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-xAM Embedded PC Module and found in the Developer section at the CompuLab Web site http://www.compulab.co.il.

1.2 CM-xAM Part Number Legend

CM-xAM part number format is presented below:

CM-xAM–Dx–Cx–Nx–Ex–Px–S–Yx–H–Tx–X

This part number format represents the CM-xAM configuration options available, listed in the table below:

Table 1 CM-xAM configuration options

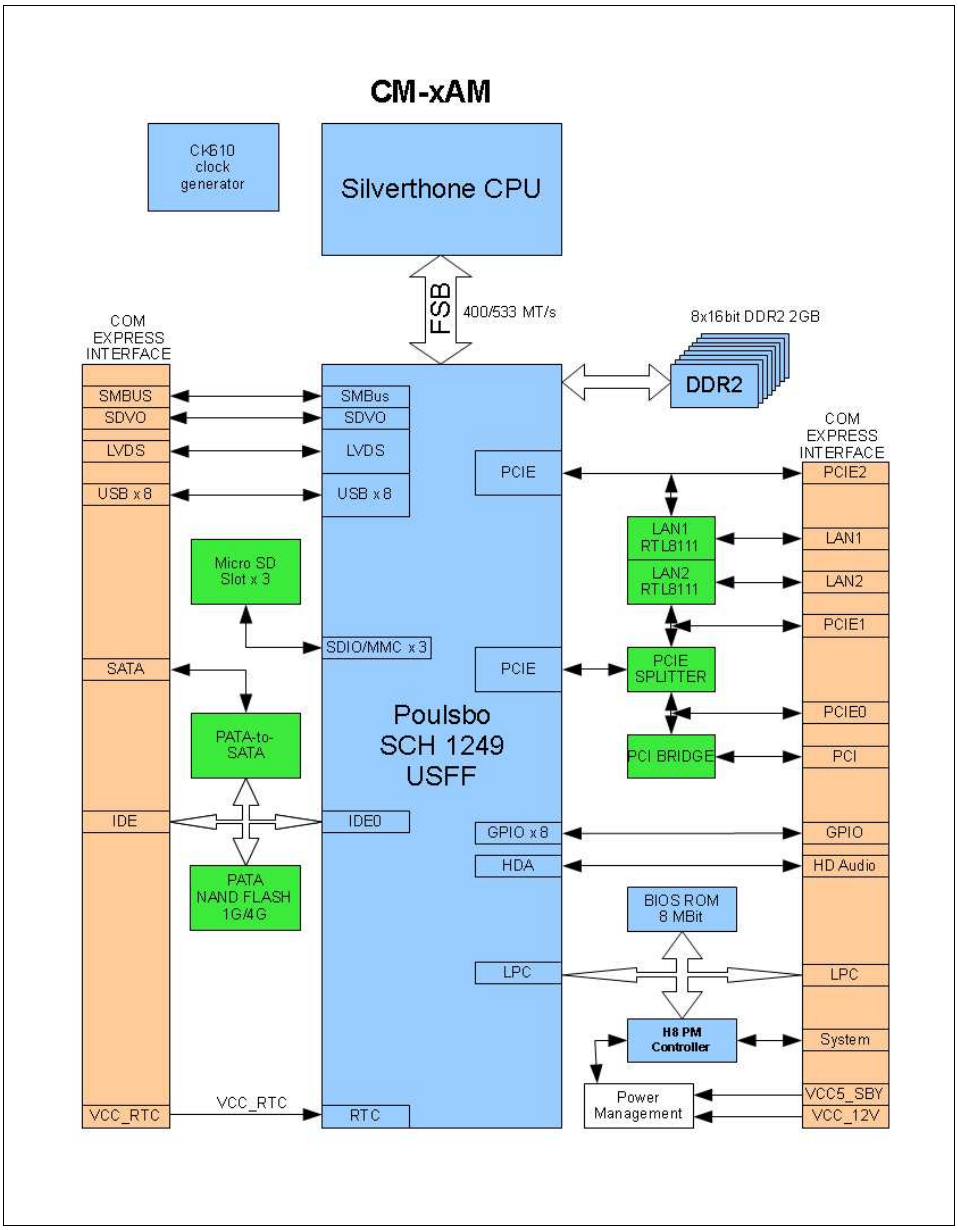
Feature	Options	Part Number Code
DDR SDRAM size	1GB DDR2	D1
	2GB DDR2	D2
CPU type and speed	Z530 1.6Ghz@533MHz FSB	C16
	Z510 1.1GHz@400MHz FSB	C11
Flash Disk size	(none)	–
	1GB	N1
	4GB	N4
Network interfaces	(none)	–
	1 x 1000Base-T	E1
	2 x 1000Base-T	E2*
PCI options	(none)	–
	Additional PCI Express interface	PE
	Parallel PCI interface	PB*
	Both of above	PEB
Heat-spreader	(none)	–
	Heat-spreader	H3
Temperature range	Commercial	–
	Extended	TE
	Industrial	TI
Software preloading	No	–
	Yes	X

Note: options combination PB and E2 is illegal.

2 OVERVIEW

2.1 Block Diagram

Figure 1 CM-xAM Block Diagram



2.2 CM-xAM Features

Table 2 CM-xAM features

Feature	Description
CPU	Intel Atom Processor. Z530 1.6Ghz@533MHz FSB or Z510 1.1GHz@400MHz FSB. 512KB L2 (dynamic sizing), 32KB IC, 24KB DC L1. Intel Deep Power Down (C6) technology support.
Chipset	Intel® SCH US15W Poulsbo Chipset
DRAM	1024/2048 MB onboard 400/533 MHz, 64-bit DDR2 SDRAM
Graphics	Intel® SCH integrated video controller
Display support	LVDS panels; TV-out, VGA, DVI, LVDS by means of external SDVO
Display interfaces	• LVDS with 3-pair (and clock) modes support • SDVO
Network interfaces	1 or 2 x 1000Base-T, activity LED's
USB	• 8 external ports • UHCI controllers • EHCI High-speed USB 2.0 host controller. • USB Client Controller
Bus interfaces	• PCI Express (up to 3 lanes + clocks), up to 5 Gb/s concurrent bandwidth (2.5 Gb/s in each direction) • PCI: 32-bit, 33MHz, Rev 2.3, 3.3V levels, 5V tolerance, arbiter, clock • LPC: including external boot ROM support • Intel High Definition Audio • SMBus
Flash disk	1GB or 4GB, NANDrive based
BIOS Flash	1MB, on-board reprogrammable
External Storage	• Parallel ATA with PIO, ATA-5 and Ultra DMA modes support • Serial ATA port
General purpose I/O	20 lines (some shared with other functions), 3.3V levels, 5V tolerant (some)
Watchdog	Generates SMI and/or reset upon timeout
Heat-spreader	Optional heat-spreader available
Connector interface	COM Express

Table 3 CM-xAM BIOS features

Feature	Description
Bootable devices	Supported boot devices are HDD, USB, CD-ROM, SD-card, PXE boot
Power-on self test	During POST, hardware, including the CPU, RAM, and peripherals, is initialized and tested.
Utilities	Ethrlink System Maintenance Utility for updating BIOS ROM and NAND flash through Ethernet link.
Password protection	When enabled, a password is required for POST to enter BIOS setup.

Table 4 Electrical, Mechanical and Environmental Specifications

Supply Voltage	12.0 VDC main power and 5.0 VDC standby power
Power consumption	5W typical, 7.6W peak (depending on CPU type and speed)
Dimensions	95mm x 95mm x 7.8 mm
Weight	57g max (depending on configuration) without heat spreader
MTBF	> 100,000 hours
Operation temp. (case)	0 to 70 °C (Commercial)
Storage temperature	-40 to 85 °C
Relative humidity	5% to 95% (storage) 10% to 90% (operation)

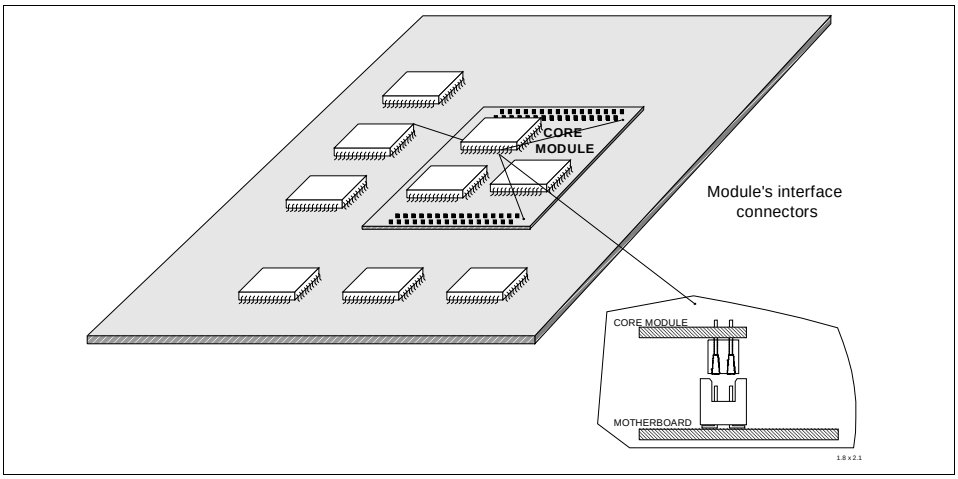
Shock	50G / 20 ms
Vibration	20G / 0–600 Hz
Connector insertion/ removal	20 cycles

2.3 General Description

The CM-xAM module is a small COM Express-compatible single board computer. Its functional content is equivalent to that of a full-featured desktop PC. CM-xAM is intended to serve as a controller and/or user interface in embedded and mobile applications. CM-xAM is designed to plug into target application boards as a mezzanine piggyback module. It thereby replaces the components that would have been put on the application board in order to implement the required functionality. Using CM-xAM 's “off-the-shelf” solution saves months of design and debugging.

CM-xAM comes in a COM Express Compact form factor.

Figure 2 A mezzanine modular system example



2.4 CPU

The CM-xAM utilizes an Intel® Atom Z5xx series CPU.

The Intel® Atom Z5xx series processor is built with 45-nanometer process technology — the first generation of a low-power IA-32 micro-architecture specially designed for the new class of Mobile Internet Devices (MID).

The following list provides some of the key features of this processor:

- New single-core processor for mobile devices with enhanced performance
- On-die, primary 32-kB instructions cache and 24-kB write-back data cache
- 100-MHz and 133-MHz Source-Synchronous front side bus (FSB)
- Supports Hyper-Threading Technology 2-threads
- On-die 512-kB, 8-way L2 cache
- Support for IA 32-bit and Intel® 64 architecture
- Intel® Virtualization Technology (Intel® VT)

- Intel® Streaming SIMD Extensions 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Supports new CMOS FSB signaling for reduced power
- Micro-FCBGA8 packaging technologies
- Thermal management support via TM1 and TM2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- New C6 Deep Power Down Technology
- L2 Dynamic Cache Sizing
- New Split-VTT support for lowest processor power state
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Executes Disable Bit support for enhanced security

2.5 Chipset

The CM-xAM uses an Intel® System Controller Hub (Intel® SCH) US15W Poulsbo chipset. The Intel® SCH chipset of the Atom low-power platform combines the functionality normally found in separate GMCH (integrated graphics, processor interface, memory controller) and ICH (on-board and end-user I/O expansion) components into a single component consuming less than 2.3 W of thermal design power.

2.6 Flash Disk

One of the key advantages of CM-xAM architecture is its high-performance, fully integrated, embedded flash solid state drives (when option Nx is selected) - SST85LD1001K (N1) or SST85LD1004M (N4) NANDrive™ integrated circuits (IC).

It combines an integrated ATA Controller and either 1Gbyte or 4Gbytes of NAND Flash in a multi-chip package. This solution is ideal for solid-state mass storage applications offering new and expanded functionality while enabling cost-effective designs.

The SST NANDrive is a single solid-state drive device, designed for embedded ATA/IDE protocol systems supporting a standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-4 interfaces. The built-in micro-controller and file management firmware communicates with ATA standard interfaces thereby eliminating the need for additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.

The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts and is built into the CM-xAM module.

The NAND Flash provides a storage solution for embedded applications requiring non-volatile on-board storage. The NAND Flash is a block device - optimized for block read and write operations rather than for random access. The NAND Flash is interfaced through a standard ATA-based IDE port and is configured as a primary master device by default.

Key Features:

- Industry Standard ATA/IDE Bus Interface
- Host Interface: 16-bit access
- Supports up to PIO Mode-6

- Supports up to Multi-word DMA Mode-4
- Supports up to Ultra DMA Mode-4
- Advanced power management
- Zero wake-up latency
- Expanded Data Protection
- Data security through user-selectable protection
- User-Programmable 10-byte ID
- Prevents data loss due to unexpected power-down or brownout
- 10 Million write cycles with advanced NAND management technology
- 3 year data retention
- Robust Built-in ECC

Performance

Read	Up to 30Mb/s
Write	Up to 8Mb/s

2.7 SDRAM

CM-xAM can be assembled with up to 2048 Mbytes of DDR2 Synchronous DRAM (DDR2 SDRAM). All SDRAM components are soldered on-board (rather than connected with SODIMM), in order to provide better mechanical reliability, required by most embedded applications. The user selects DDR SDRAM size upon ordering.

2.8 BIOS Flash

BIOS and other initialization code are contained in the LPC ROM component, which is implemented by a 1024 KB flash memory. BIOS ROM is used only for keeping BIOS and BIOS-related settings, all other code and data should be stored in the Nand flash or hard disks. Bios ROM is re-programmable on-board and supports field updates of BIOS code.

3 PERIPHERALS AND FUNCTIONS

3.1 Components Locations

Figure 3 CM-xAM Top Components

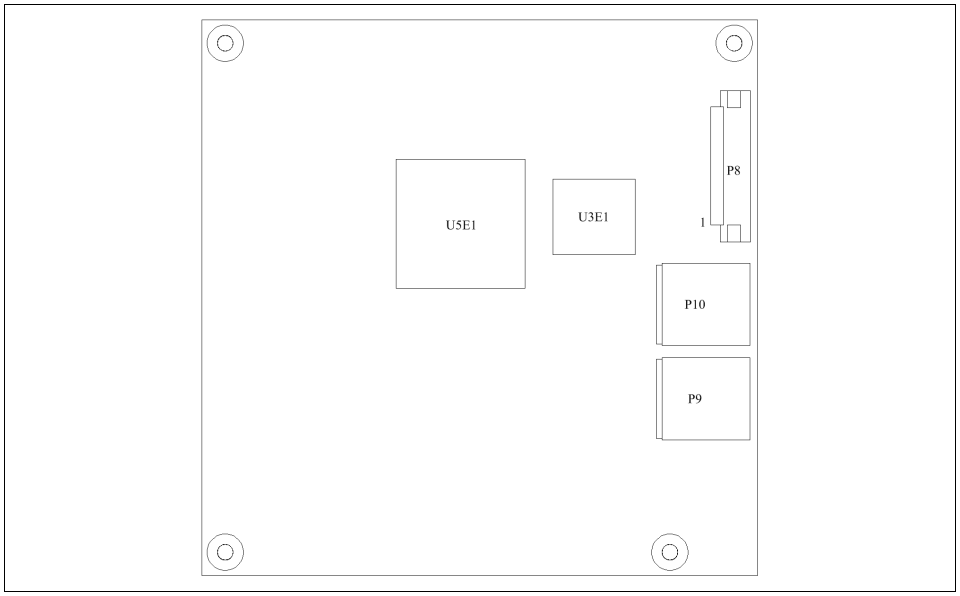
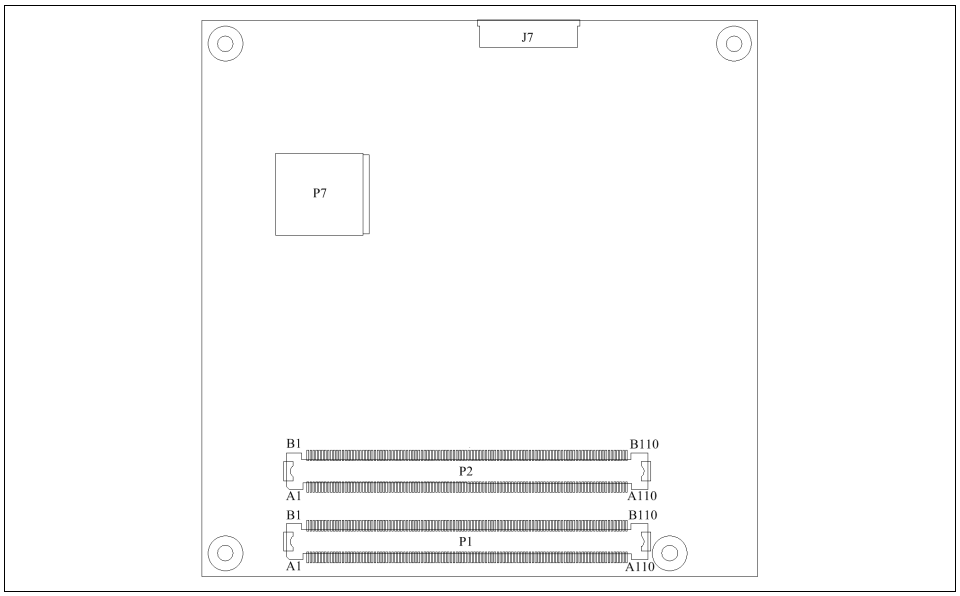


Figure 4 CM-xAM Bottom Components (as seen from top)



3.2 Signal type definition

Table 5 Signal Type Definition

Type	Name	Description
I	Digital Input	CMOS Input pin
O	Digital Output	CMOS Output pin
I/O	Digital Input/Output	CMOS Multiplexed input and output pin to and from CM-xAM
OD	Open Drain	CMOS Open drain output pin, possibly with integrated pull-up
I/OD	Input/Open Drain	CMOS Multiplexed input and open drain output pin to and from CM-xAM , possibly with integrated pull-up
IDIF	Differential (Input)	
ODIF	Differential (Output)	
DIFF	Differential (Bidir)	

3.3 Display Controller

The CM-xAM graphics system is built on the Intel® SCH integrated graphics controller, based on Intel® GMA500 architecture. The highly compact Integrated Graphics Device (IGD) contains advanced shader architecture (model 3.0+) that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance.

Key Features:

- Flexible Programmable Architecture
- Shader-based technology
- 3D Graphics
- 2D and advanced 2D Graphics
- Video - Encode / Decode support
- Image processing
- Deferred Pixel Shading
- Screen Tiling
- On-chip Stencil, Z and Frame buffers
- High Performance
- Low Power
- Industry standard tool support
- Comprehensive OS/API support

3-D Core Key Features:

- Two pipe scaleable unified shader implementation
- 3-D Peak Performance
- Fill Rate: 2 Pixels per clock
- Vertex Rate: One Triangle 15 clocks (Transform Only)
- Vertex / Triangle Ratio average = 1 vtx/tri, peak 0.5 vtx/tri
- Texture max size = 2048 x 2048

- Programmable 4x multi-sampling anti-aliasing (MSAA)
- Rotated grid
- ISP performance related to AA mode, TSP performance unaffected by AA mode
- Optimized memory efficiency using multi-level cache architecture

Video Decode Overview

The video decode accelerator improves video performance-power ratio by providing hardware-based acceleration at the macroblock level (variable length decode stage entry point). The Intel SCH supports full hardware acceleration of the following video decode standards:

CODEC	PROFILE	LEVEL
H.264	Baseline profile	L3
H.264	Main profile	L4.1 (1080i @ 30fps)
H.264	High profile	L4.1 (1080i @ 30fps)
MPEG2	Main profile	High
MPEG4	Simple profile	L3
MPEG4	Advanced simple profile	L5
VC1	Simple profile	Medium
VC1	Main profile	High
VC1	Advanced profile	L3 up to (1080i @ 30fps)
WMV9	Simple profile	Medium
WMV9	Main profile	High

The video decode function is performed in four processing modules:

- Entropy coding processing
- Motion compensation
- Deblocking
- Final pixel formatting

The IGD includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays – LVDS and SDVO. Carrier board may also implement an LVDS to parallel 24-bit RGB converter allowing the connection of different parallel LCD's.

3.3.1 LVDS

The System Controller Hub (Poulsbo SCH) supports a Low-Voltage Differential Signaling interface allowing the IGD to communicate directly with a flat-panel display. The LVDS interface supports pixel color depth of 18 or 24 bits and max pixel clock of 112 MHz

Table 6 LVDS Interface

Signal Name	COM Express Pin	Type	Description
LVDS_A0+	A71	ODIF	LVDS Differential Pair 0
LVDS_A0-	A72	ODIF	
LVDS_A1+	A73	ODIF	LVDS Differential Pair 1
LVDS_A1-	A74	ODIF	
LVDS_A2+	A75	ODIF	LVDS Differential Pair 2
LVDS_A2-	A76	ODIF	

Signal Name	COM Express Pin	Type	Description
LVDS_A3+	A78	ODIF	LVDS Differential Pair 3
LVDS_A3-	A79	ODIF	
LVDS_A_CK+	A81	ODIF	LVDS Differential Clock
LVDS_A_CK-	A82	ODIF	
LVDS_I2C_CK	A83	I/O	LVDS DDC Clock
LVDS_I2C_DAT	A84	I/O	LVDS DDC Data
LVDS_VDD_EN	A77	O	Power sequencing control for panel driver electronics
LVDS_BKLT_EN	B79	O	Panel backlight enable
LVDS_BKLT_CTRL	B83	O	LCD Backlight Control: This signal allows control of LCD brightness

3.3.2 Intel Serial DVO (SDVO) Display

The SCH has a digital display channel capable of driving SDVO adapters providing interfaces to a variety of external display technologies (e.g., DVI, analog CRT). Up to 160 MHz pixel clock supported.

CM-xAM outputs SDVO interface signals on the COM Express PCI Express Graphics pins.

Table 7 SDVO Interface

Signal Name	COM Express Pin	Type	Description
SDVO_BCLK+	D61	ODIF	Serial Digital Video Channel B Clock
SDVO_BCLK-	D62	ODIF	
SDVO_BLUE+	D58	ODIF	Serial Digital Video Channel B Blue
SDVO_BLUE-	D59	ODIF	
SDVO_RED+	D52	ODIF	Serial Digital Video Channel B Red
SDVO_RED-	D53	ODIF	
SDVO_GREEN+	D55	ODIF	Serial Digital Video Channel B Green
SDVO_GREEN-	D56	ODIF	
SDVO_INT+	C55	IDIF	Serial Digital Video Input Interrupt
SDVO_INT-	C56	IDIF	
SDVO_FLDSTALL+	C58	IDIF	Serial Digital Video Field Stall
SDVO_FLDSTALL-	C59	IDIF	
SDVO_TVCLKIN+	C52	IDIF	Serial Digital Video TV-OUT Sync Clock pair
SDVO_TVCLKIN-	C53	IDIF	
SDVO_CTRL_CLK	D73	I/O	SDVO Control Clock (similar to I2C)
SDVO_CTRL_DAT	C73	I/O	SDVO Control Data (similar to I2C)

Notes:

- SDVO signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2V max. Single-ended maximum =1.5V. Single-ended minimum = 0V.
- 100 nF decoupling capacitor must be used on all differential SDVO signals (see SB-xAM reference schematic)

3.4 SATA interface

This interface is available only in modules with the “S” option.

The CM-xAM Serial ATA (SATA) interface is formed from the PATA interface using a PATA to SATA bridge. The CM-xAM ATA (PATA) interface is provided directly by an Intel® SCH PATA controller. PATA interface supports only the primary channel, with one master and one slave device.

Three types of data transfers are supported:

- Programmed I/O (PIO): A protocol used to transfer data between the processor as the ATA device. PIO allows transfer rates of up to 16MB/s.
- Multi-word DMA: DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 16MB/s.
- Ultra-DMA: Source synchronous DMA protocol allowing transfer rates of up to 100MB/s.

Table 8 Supported PATA Standards and Modes

PATA Standard	Transfer Modes Supported	Transfer Rate (MB/s)
ATA-1 (ATA, IDE)	PIO Modes 0, 1, 2	3.3, 5.2, 8.3
	Single-word DMA Modes 0, 1, 2	2.1, 4.2, 8.3
	Multi-word DMA Mode 0	4.2
ATA-2, ATA-3 (EIDE, Fast ATA)	PIO Modes 3, 4	11.1, 16.6
	Multi-word DMA Modes 1, 2	13.3, 16.6
ATA/ATAPI-4 (Ultra DMA, Ultra ATA)	Ultra DMA Modes 0, 1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 (Ultra DMA, Ultra ATA)	Ultra DMA Modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 (Ultra DMA, Ultra ATA)	Ultra-DMA Mode 5 (a.k.a. Ultra DMA/100)	100 (reads) 89 (writes)

PATA to SATA bridge key features are:

- SATA-II with 1.5 Gb/s operation support
- SATA 2.6 Compliant
- ATA/ATAPI 48-bit address feature set
- ATA/ATAPI 7 feature set
- Tagged command queuing (maximum 32 entries)
- SATA power save modes

Table 9 SATA Interface

Signal Name	COM Express Pin	Type	Description
SATA_TX+	A16	ODIF	SATA transmit pair
SATA_TX-	A17	ODIF	
SATA_RX+	A19	IDIF	SATA receive pair
SATA_RX-	A20	IDIF	
ATA_ACT#	A28	O	SATA/PATA activity led

3.5 IDE Interface

IDE interface is unavailable in modules with both “Nx” (Nand) and “S” (Sata) options chosen. When only one of the “Nx” or “S” options chosen, only a slave device may be connected on the external IDE interface. When no “S” or “Nx” options chosen, both slave and master are available.

IDE interface is also unavailable in modules with “E2” option chosen, because IDE bus shares connector pins with LAN2 interface.

Table 10 IDE interface signals

CM-xAM Signal Name	COM Express Pin	Type	Description
IDE_CS1#	D16	O	IDE Device Chip Selects for 100 Range: For ATA command register block. This output signal to be connected to the CS1# signal on the IDE connector.
IDE_CS3#	D17	O	IDE Device Chip Select for 300 Range: For ATA control register block. This output signal is to be connected to the CS3# signal on the IDE connector.
IDE_A0	D13	O	IDE Device Address: These output signals are connected to the corresponding signals on the IDE connector. They indicate which byte in either the ATA command block or control block is being addressed.
IDE_A1	D14		
IDE_A2	D15		
IDE_D0	D7	I/O	IDE Device Data: These signals directly drive the corresponding signals on the IDE connector.
IDE_D1	C10		
IDE_D2	C8		
IDE_D3	C4		
IDE_D4	D6		
IDE_D5	D2		
IDE_D6	C3		
IDE_D7	C2		
IDE_D8	C6		
IDE_D9	C7		
IDE_D10	D3		
IDE_D11	D4		
IDE_D12	D5		
IDE_D13	C9		
IDE_D14	C12		
IDE_D15	C5		
IDE_DREQ	D8	I	IDE Device DMA Request: This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, is used in conjunction with the PCI bus master IDE function and is not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on this signal.
IDE_DACK#	D10	O	IDE Device DMA Acknowledge: This signal directly drives the DAK# signal on the IDE connector. It is asserted by the IDE controller to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of IDE-RD# or IDE-WR#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and is not associated with any AT-compatible DMA channel.

CM-xAM Signal Name	COM Express Pin	Type	Description
IDE_RD#	C14	O	• Disk I/O Read (PIO and Non-Ultra DMA): This is the command to the IDE device that it may drive data onto the LB-D[15:0] lines. Data is latched by the IDE controller on the de-assertion edge of IDE-RD#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0# and IDE-CS1#) and the LB-A[2:0] lines, or the IDE DMA acknowledge (IDE-DACK#). • Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, IDE controller drives valid data on rising and falling edges of IDE-RD#. • Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, IDE controller de-asserts IDE-RD# to pause burst data transfers.
IDE_WR#	D9	O	• Disk I/O Write (PIO and Non-Ultra DMA): This is the command to the IDE device that it may latch data from the LB-D[15:0] lines. Data is latched by the IDE device on the de-assertion edge of IDE-WR#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0# and IDE-CS1#) and the LB-A[2:0] lines, or the IDE DMA acknowledge (IDE-DACK#). • Disk Stop (Ultra DMA): asserted by the host to terminate a burst.
IDE_RDY#	C13	I	• I/O Channel Ready (PIO): This signal will keep the strobe active (IDE-RD# on reads, IDE-WR# on writes) longer than the minimum width. It adds wait states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ide controller latches data on rising and falling edges of this signal from the disk. • Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.
IDE_IRQ	D12	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drives.
IDE_CBLID#	D77	I	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66,100 modes.

3.6 PCI Express Interface

The CM-xAM contains up to three x1 PCI Express expansion interfaces supporting the PCI Express Base Specification Revision 1.0a configured as two x1 lanes. Each root port supports up to 2.5 GB/s bandwidth in each direction.

It is a high-bandwidth, low pin-count serial interface ideal for I/O expansion. An external graphics device can be used via one of the x1 PCI Express lanes/ports.

PCI Express ports availability depends on the CM-xAM module configuration. The options, which affect the PCIE availability, are Ex and Px. The following table defines PCIE ports availability as function of various options chosen.

Table 11 PCIE Ports Availability and Bandwidth

Options	No P	PE	PB	PEB
No E	PCIE1 @ full BW PCIE2 @ full BW	PCIE0 @ ½ BW PCIE1 @ ½ BW PCIE2 @ full BW	PCIE2 @ full BW	PCIE1 @ ½ BW PCIE2 @ full BW
E1	PCIE1 @ full BW LAN1 @ full BW	PCIE0 @ ½ BW PCIE1 @ ½ BW LAN1 @ full BW	No PCIE ports LAN1 @ full BW	PCIE1 @ ½ BW LAN1 @ full BW
E2	No PCIE ports LAN1 and LAN2 @ full BW	PCIE0 @ ½ BW LAN1 @ full BW LAN2 @ ½ BW	Invalid option configuration	No PCIE ports LAN1 @ full BW LAN2 @ ½ BW

Note: options “PE” and “PEB” add another PCIE lane, if possible, as compared to “No P” and “PB” options. This is accomplished by splitting the existing port’s bandwidth, meaning that the total bandwidth of additional port and the splitted port will be 2.5 GB/s in each direction at full load.

Table 12 PCI Express Interface Signals

Signal Name	COM Express Pin	Type	Description
PCIE_TX0+	A68	ODIF	PCIE0 transmit pair
PCIE_TX0-	A69	ODIF	
PCIE_RX0+	B68	IDIF	PCIE0 receive pair
PCIE_RX0-	B69	IDIF	
PCIE_TX1+	A64	ODIF	PCIE1 transmit pair
PCIE_TX1-	A65	ODIF	
PCIE_RX1+	B64	IDIF	PCIE1 receive pair
PCIE_RX1-	B65	IDIF	
PCIE_TX2+	A61	ODIF	PCIE2 transmit pair
PCIE_TX2-	A62	ODIF	
PCIE_RX2+	B61	IDIF	PCIE2 receive pair
PCIE_RX2-	B62	IDIF	
PCIE_CK_REF+	A88	ODIF	PCIE differential clock reference
PCIE_CK_REF-	A89	ODIF	
EXCD0_PERST#	A48	O	Express Card Reset, port PCIE0
EXCD0_CPPE#	A49	I	Express Card capable card request, port PCIE0
EXCD1_PERST#	B47	O	Express Card Reset, port PCIE1
EXCD1_CPPE#	B48	I	Express Card capable card request, port PCIE1
PCIE_WAKE#	B66	I	PCI Express Wake Event: This signal indicates that a PCI Express port wants to wake the system.

Notes:

- PCIE differential signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum =1.5 V. Single-ended minimum = 0 V.
- 100nF decoupling capacitor must be used on the receiver side (_RX* signals on baseboard interface connector. See SB-XAM reference schematic.

3.7 PCI Interface

PCI interface is available only on the modules with “PB” or “PEB” options.

CM-xAM PCI signals are driven by a PCIE-to-PCI bridge. Output drive and maximum load specifications are according to PCI bus Standard Rev-2.3.

Table 13 PCI interface signals

CM-xAM Signal Name	COM Express Pin	Type	Description
PCI_AD0	C24	I/O	Address / Data: Multiplexed address and data bus. Address phase is aligned with first clock of FRAME# assertion. Data phase is aligned with IRDY# or TRDY# assertion. Data is transferred on rising edges of PCI_CLK when both IRDY# and TRDY# are asserted. During bus idle (both FRAME# and IRDY# are deasserted), CM-xAM drives AD to a valid logic level when arbiter is parking to the PCI bridge on PCI bus.
PCI_AD1	D22		
PCI_AD2	C25		
PCI_AD3	D23		
PCI_AD4	C26		
PCI_AD5	D24		
PCI_AD6	C27		
PCI_AD7	D25		
PCI_AD8	C28		
PCI_AD9	D27		
PCI_AD10	C29		
PCI_AD11	D28		
PCI_AD12	C30		
PCI_AD13	D29		
PCI_AD14	C32		
PCI_AD15	D30		
PCI_AD16	D37		
PCI_AD17	C39		
PCI_AD18	D38		
PCI_AD19	C40		
PCI_AD20	D39		
PCI_AD21	C42		
PCI_AD22	D40		
PCI_AD23	C43		
PCI_AD24	D42		
PCI_AD25	C45		
PCI_AD26	D43		
PCI_AD27	C46		
PCI_AD28	D44		
PCI_AD29	C47		
PCI_AD30	D45		
PCI_AD31	C48		
PCI_CBE0	D26	I/O	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE[3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, CM-xAM drives CBE[3:0] signals to a valid logic level when arbiter is parking to the PCI bridge on PCI bus.
PCI_CBE1	C33		
PCI_CBE2	C38		
PCI_CBE3	C44		
PCI_DEVSEL#	C36	I/O	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, CM-xAM waits for the assertion of this signal within 5 cycles of FRAME# assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.

CM-xAM Signal Name	COM Express Pin	Type	Description
PCI_FRAME#	D36	I/O	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME# indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.
PCI_IRDY#	C37	I/O	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a deasserted state for one cycle.
PCI_TRDY#	D35	I/O	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a deasserted state for one cycle.
PCI_STOP#	D34	I/O	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a deasserted state for one cycle.
PCI_PAR	D32	I/O	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD[31:0], CBE[3:0]. If the PCI bridge is an initiator with a write transaction, it will tri-state PAR. If the PCI bridge is a target and a write transaction, the PCI bridge will drive PAR one clock after the address or data phase. If the PCI bridge is a target and a read transaction, the PCI bridge will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, the PCI bridge drives PAR to a valid logic level when arbiter is parking to the PCI bridge on PCI bus.
PCI_PERR#	C34	I/O	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
PCI_REQ0#	C22	I	**Request (Active LOW):** REQ#'s are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ#s for at least 2 PCI clock cycles before asserting them again.
PCI_REQ1#	C19		
PCI_REQ2#	C17		
PCI_REQ3#	D20		
PCI_GNT0#	C20	O	**Grant (Active LOW):** the PCI bridge asserts GNT#s to release PCI bus control to bus master devices. During idle and all GNT#s are de-asserted and arbiter is parking to the PCI bridge, the PCI bridge will drive AD, CBE, and PAR to valid logic levels.
PCI_GNT1#	C18		
PCI_GNT2#	C16		
PCI_GNT3#	D19		
PCI_INTA#	C49	I/OD	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA#, INTB#, INTC#, INTD# signals are inputs and asynchronous to the clock.
PCI_INTB#	C50		
PCI_INTC#	D46		
PCI_INTD#	D47		
PCI_RESET#	C23	O	**PCI Reset:** This is the PCI Bus reset signal.
PCI_SERR#	D33	I/OD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, the PCI bridge will drive this pin on: • Address parity error • Posted write data parity error on target bus • Master abort during posted write transaction • Target abort during posted write transaction • Posted write transaction discarded • Delayed write request discarded • Delayed read request discarded • Delayed transaction master timeout • Errors reported from PCI Express port (advanced error reporting) in transparent mode.

CM-xAM Signal Name	COM Express Pin	Type	Description
PCI_PME#	C15	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5.
PCI_CLK	D50	O	**PCI Clock Output:** PCI clock output provides clocking signals to external PCI Devices.
PCI_LOCK#	C35	I/O	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. The PCI bridge does not support any upstream LOCK transaction.
PCI_M66EN	D49	I	**66MHz Enable:** This input is used to specify if Bridge is capable of running at 66MHz. For 66MHz operation on the PCI bus, this signal should be pulled "HIGH". For 33MHz operation on the PCI bus, this signal should be pulled LOW.

3.8 LPC Interface

The CM-xAM implements an LPC Interface and Controller as described in the LPC 1.1 specification. The LPC bus provides a functional replacement for interfacing legacy ISA functions.

Table 14 LPC interface signals

CM-xAM Signal Name	COM Express Pin	Type	Description
LPC_AD0	B4	I/O	**LPC Address/Data:** Multiplexed Command, Address, Data
LPC_AD1	B5		
LPC_AD2	B6		
LPC_AD3	B7		
LPC_FRAME#	B3	O	**LPC Frame:** This signal indicates the start of an LPC/ FHW cycle.
LPC_CLK	B10	O	**LPC Clock:** driven by the Intel SCH to LPC devices.

LPC_CLK is pre-compensated for an external clock trace length of 5 cm. The maximum allowed length of the external clock trace is 5cm. In addition to the above signals, an LPC device needs the RESET# signal.

3.9 Serial IRQ

The CM-xAM provides another interface for interrupt requests – serial IRQ. This allows a single signal line to be used to report legacy ISA interrupt requests. Interrupt sharing is allowed on Serial IRQ interfaces only for devices external to the chipset. The following interrupts are external to the chipset and are therefore potentially available on the Serial IRQ interface: IRQ1, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ11, IRQ12, IRQ14. The serial IRQ interface is a synchronous interface. Data is clocked by the system's PCI clock.

Table 15 Serial IRQ

CM-xAM Signal Name	COM Express Pin	Type	Description
LPC_SERIRQ	A50	I/O	**Serial Interrupt Request:** This signal conveys the serial interrupt protocol.

3.10 Intel High Definition Audio Link

The audio / modem link in the CM-xAM is High Definition Audio (HD Audio) compliant, supporting high quality audio.

Features Supported by HDA:

- Sample rate ranging from 6 kHz to 192 kHz
- 8-, 16-, 20-, 24-, and 32-bit sample resolution per stream
- Up to 16 channels per stream
- 48-Mbps outbound link transfer rate per SDO
- 24-Mbps inbound transfer rate per SDI
- Support for 2 -SDI codecs to increase available inbound link bandwidth
- Codec architecture is fully discoverable, allowing for codec design flexibility
- Audio codecs, modem codecs, and vendor-defined codecs are all supported
- Command/Response codec communication mechanism for extensibility and flexibility
- Extensive, fine grained power management control in the codec
- Industry standard 48-pin QFP package and pinout for codec
- Audio codecs support advanced jack detection and jack sensing for device discoverability and jack retasking.

Table 16 Intel HD Link Interface

CM-xAM Signal Name	COM Express Pin	Type	Description
HDA_RST#	A30	O	**Intel HD Audio Reset:** This signal is the reset to external Codecs
HDA_SYNC	A29	O	**Intel HD Audio Sync:** This signal is an 48-kHz fixed rate sample sync to the Codec(s). It is also used to encode the stream number.
HDA_BITCLK	A32	I/O	**Intel HD Audio Clock (Output):** This signal is a 24.000-MHz serial data clock generated by the Intel HD Audio controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel HD Audio CODEC (or no CODEC) is connected.
HDA_SDOUT	A33	O	**Intel HD Audio Serial Data Out:** This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio.
HDA_SDIN0	B30	I	**Intel HD Audio Serial Data In:** These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.
HDA_SDIN1	B29		
HDA_SPKR	B32	O	**PC Speaker Output**

3.11 USB Interface

The CM-xAM provides eight ports compliant with USB 1.1(UHCI) and USB 2.0(EHCI) specifications. The HCI specification provides a register-level description for a host controller, as well as a common industry hardware/software interface and drivers. USB ports are supported by all O/S packages provided for the CM-xAM.

Features:

- USB v2.0 / EHCI v1.0 and USB v1.1 / UHCI v1.1 compatible

- Physical layer transceivers with optional three over-current detection status on USB inputs – one for every two ports

Table 17 USB Interface

Signal Name	COM Express Pin	Type	Description
USB0-	A45	DIFF	USB Port 0 Data Pair
USB0+	A46	DIFF	
USB1-	B45	DIFF	USB Port 1 Data Pair
USB1+	B46	DIFF	
USB2-	A42	DIFF	USB Port 2 Data Pair
USB2+	A43	DIFF	
USB3-	B42	DIFF	USB Port 3 Data Pair
USB3+	B43	DIFF	
USB4-	A39	DIFF	USB Port 4 Data Pair
USB4+	A40	DIFF	
USB5-	B39	DIFF	USB Port 5 Data Pair
USB5+	B40	DIFF	
USB6-	A36	DIFF	USB Port 6 Data Pair
USB6+	A37	DIFF	
USB7-	B36	DIFF	USB Port 7 Data Pair
USB7+	B37	DIFF	
USB_OC_0_1#	B44	I	Overcurrent pin for ports 0, 1. May be left not connected (NC) if not used.
USB_OC_2_3#	A44	I	Overcurrent pin for ports 2, 3. May be left not connected (NC) if not used.
USB_OC_4_5#	B38	I	Overcurrent pin for ports 4, 5. May be left not connected (NC) if not used.
USB_OC_6_7#	A38	I	Overcurrent pin for ports 6, 7. May be left not connected (NC) if not used.

3.12 LAN Interface

The CM-xAM provides one (option E1) or two (option E2) Gigabit Ethernet port implemented using a Realtek RTL8111D Gigabit Ethernet controller.

The Realtek RTL8111D Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller and embedded memory. With state-of-art DSP technology and mixed-mode signal technology, the RTL8111D offers high-speed transmission over CAT 5 UTP or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device is compliant with the IEEE 802.3u specification for 10/100M bps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet.

RTL8111D Gigabit Ethernet controller features:

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Crossover Detection & Auto-Correction
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and Largesend Offload support
- Supports Full Duplex flow control (IEEE 802.3x)

- Fully compliant with IEEE 802.3, IEEE 802.3u and IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Transmit/Receive on-chip buffer (48KB) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)

3.12.1 LAN1 Port

This port is available in both “E1” and “E2” configurations.

Table 18 LAN1 Interface

Signal Name	COM Express Pin	Type	Description
LAN1_MDI0-	A12	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T, and transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.
LAN1_MDI0+	A13	DIFF	
LAN1_MDI1-	A9	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T, and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
LAN1_MDI1+	A10	DIFF	
LAN1_MDI2-	A6	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
LAN1_MDI2+	A7	DIFF	
LAN1_MDI3-	A2	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.
LAN1_MDI3+	A3	DIFF	
LAN1_LED0#	B2	O	Active low LED signal, toggling when Tx/Rx in progress
LAN1_LED1#	A4	O	Active low LED signal, asserted when 10/100/1000 mbps link established
LAN1_LED2#	A8	O	Active low LED signal, asserted when 10/100 mbps link established
LAN1_LED3#	A5	O	Active low LED signal, asserted when 1000 mbps link established
LAN1_CTREF	A14	PWR	Reference voltage for carrier board LAN1 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY. In CM-xAM reference voltage is 0V.

3.12.2 LAN2 Port

This port is available only in “E2” configuration. Selecting the “E2” option disables the IDE interface as LAN2 and IDE are sharing common pads on the COM Express connector.

Table 19 LAN2 Interface

Signal Name	COM Express Pin	Type	Description
LAN2_MDI0-	C12	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T, and transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.
LAN2_MDI0+	C13	DIFF	
LAN2_MDI1-	C9	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T, and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
LAN2_MDI1+	C10	DIFF	

Signal Name	COM Express Pin	Type	Description
LAN2_MDI2-	C6	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
LAN2_MDI2+	C7	DIFF	
LAN2_MDI3-	C3	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.
LAN2_MDI3+	C4	DIFF	
LAN2_LED0#	C2	O	Active low LED signal, toggling when Tx/Rx in progress
LAN2_LED1#	C5	O	Active low LED signal, asserted when 10/100/1000 mbps link established
LAN2_LED2#	C14	O	Active low LED signal, asserted when 10/100 mbps link established
LAN2_LED3#	C8	O	Active low LED signal, asserted when 1000 mbps link established
LAN2_CTREF	D18	PWR	Reference voltage for carrier board LAN2 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY. In CM-xAM reference voltage is 0V.

3.13 GPIO Signals

3.13.1 Chipset GPIO Signals

The CM-xAM provides eight general purpose I/O pins (GPIO's) - seven of them are dedicated and one is shared with alternate functionality - with different power domain support.

Table 20 SCH GPIO Signals

CM-xAM Signal Name	COM Express Pin	Type	Description
GPI0	A54	I/O 1.5mA	GPIOSUS0 of the SCH, resume power well. This signal is accessible during the S3 sleep state.
GPI1	A63	I/O 1.5mA	GPIOSUS1 of the SCH, resume power well. This signal is accessible during the S3 sleep state.
GPI2	A67	I/O 1.5mA	GPIOSUS3 of the SCH, resume well. This GPIO can function as an input signifying connection to an external USB host. **NOTE:** If a USB Client is enabled in the system, then GPIOSUS3 cannot be used as a general purpose I/O.
GPI3	A85	I/O 1.5mA	GPIO9 of the SCH. This GPIO can function as a second external thermal sensor input.
GPO0	A93	I/O 1.5mA	GPIO1 of the SCH, core power well.
GPO1	B54	I/O 1.5mA	GPIO2 of the SCH, core power well.
GPO2	B57	I/O 1.5mA	GPIO6 of the SCH, core power well.
GPO3	B63	I/O 1.5mA	GPIO8 of the SCH, optionally – PROCHOT# signal. Defaults to a GPIO. As PROCHOT#, this signal can function as an Open-Drain output to the processor or SMC to signify a processor thermal event. This pin is shared with and defaults to the CM-xAM POWER LED indicator.

3.14 I^2C Interface

This is an alternative system management bus sourcing from the H8S system management IC on the CM-xAM. This bus may be not available for the user and provided for future functionality only.

Table 21 I²C Bus Signals

CM-xAM Signal Name	COM Express Pin	Type	Description
I2C_CLK	B33	I/OD	I²C bus clock. Pulled up internally (2.2K to 3.3V standby rail).
I2C_DAT	B34	I/OD	I²C bus data. Pulled up internally (2.2K to 3.3V standby rail).

3.15 SMBus Interface

The CM-xAM provides a host system management bus interface. This interface is compatible with I²C devices.

Table 22 SMBus signals

CM-xAM Signal Name	COM Express Pin	Type	Description
SMB-CLK	B13	I/OD	SMBus clock. Pulled up internally (2.35K to 3.3V standby rail).
SMB-DATA	B14	I/OD	SMBus data. Pulled up internally (2.35K to 3.3V standby rail).
SMB-ALERT#	B15	I	SMBus Alert: This signal can be used to generate an SMI (10k internal PU)

3.16 System Signals

Table 23 System signals

CM-xAM Signal Name	COM Express Pin	Type	Description
RST_IN#	B49	I	Reset input signal. This signal may be driven to low by external circuitry such as a reset button to hold the system module in hardware reset.
RESET_OUT#	B50	O	Reset output signal from module to carrier board. This signal may be driven low by the module to reset external components located on the carrier board.
PWRBTN#	B12	I	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.
SUS_S3#	A15	O	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).
SUS_S4#	A18	O	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to disk).
SUS_S5#	A24	O	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).
BATLOW#	A27	I	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.
THRM#	B35	I	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.
THRMTRIP#	A35	O	Thermal Trip indicates an overheating condition of the processor. If THRMTRIP# goes active the system immediately transitions to the S5 State (Soft Off).
BIOS_DIS#	A34	I	Input to disable the modules BIOS flash memory chip. This signal provides the ability to implement an external BIOS flash memory chip that can be located on the carrier board.
A20M#	A87	I	Input signal of the module used by an external keyboard controller to control the CPU A20 gate line. The A20 gate restricts the memory access to the bottom megabyte of the system. Pulled high on the module.
KBDRST#	A86	I	Input signal of the module used by an external keyboard controller to force a system reset.

SUS_STAT#	B18	O	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the carrier board as an indication that they should go into power-down mode.

3.17 Power Pins

Table 24 Power signals

CM-xAM Signal Name	COM Express Pin	Description
GND	Multiple	Common ground.
VCC_5V_SBY	B84, B85, B86, B87	
VCC_12V	Multiple	12 VDC power supply. May be switched off in the S4, S5 suspend states.
VCC_RTC	A47	3.3 VDC supply pin. Provides power to the internal real-time clock and on-board static/configuration RAM. This pin can be driven independently of all other power pins. This pin enables direct connection of an external 3.0V lithium battery. The battery is not mandatory for the CM-xAM if the RTC function is not required. In this case, the VCC-RTC pin should be left unconnected.

3.18 Module Type Signals

The Type pins indicate the COM Express pinout type of the module. To indicate the module's pinout type, the pins are either not connected or strapped to ground on the module. The carrier board has to implement additional logic, which prevents the system to switch power on, if a module with an incompatible pinout type is detected.

Table 25 Module Type Signals

CM-xAM Signal Name	COM Express Pin	Type	Description
TYPE0#	C54	OD	TYPE0# is Hi-Z on all modules
TYPE1#	C57	OD	TYPE1# is asserted on modules where neither PB nor PEB option chosen.
TYPE2#	D57	OD	TYPE2# is asserted on modules with E2 option.

4 PINOUT INFORMATION

4.1 CM-xAM Connector Pinout

Table 26 CM-xAM COM Express Connector Rows A and B Pinout

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	LAN1_MDI3-	B2	LAN1_LED0#
A3	LAN1_MDI3+	B3	LPC_FRAME#
A4	LAN1_LED1#	B4	LPC_AD0
A5	LAN1_LED3#	B5	LPC_AD1
A6	LAN1_MDI2-	B6	LPC_AD2
A7	LAN1_MDI2+	B7	LPC_AD3
A8	LAN1_LED2#	B8	N.C.
A9	LAN1_MDI1-	B9	N.C.
A10	LAN1_MDI1+	B10	LPC_CLK
A11	GND	B11	GND
A12	LAN1_MDI0-	B12	PWRBTN#
A13	LAN1_MDI0+	B13	SMB_CLK
A14	LAN1_CTREF	B14	SMB_DATA
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA_TX+	B16	N.C.
A17	SATA_TX-	B17	N.C.
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA_RX+	B19	N.C.
A20	SATA_RX-	B20	N.C.
A21	GND	B21	GND
A22	N.C.	B22	N.C.
A23	N.C.	B23	N.C.
A24	SUS_S5#	B24	N.C.
A25	N.C.	B25	N.C.
A26	N.C.	B26	N.C.
A27	BATLOW#	B27	N.C.
A28	ATA_ACT#	B28	N.C.
A29	HDA_SYNC	B29	HDA_SDIN1
A30	HDA_RST#	B30	HDA_SDIN0
A31	GND	B31	GND
A32	HDA_BITCLK	B32	HDA_SPKR
A33	HDA_SDOUT	B33	I2C_CLK
A34	BIOS_DIS#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_OC_6_7#	B38	USB_OC_4_5#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND	B41	GND
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_OC_2_3#	B44	USB_OC_0_1#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#

Pin	Signal	Pin	Signal
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND	B51	GND
A52	N.C.	B52	N.C.
A53	N.C.	B53	N.C.
A54	GPI0	B54	GPO1
A55	N.C.	B55	N.C.
A56	N.C.	B56	N.C.
A57	GND	B57	GPO2
A58	N.C.	B58	N.C.
A59	N.C.	B59	N.C.
A60	GND	B60	GND
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	PCIE_WAKE#
A67	GPI2	B67	N.C.
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND	B70	GND
A71	LVDS_A0+	B71	N.C.
A72	LVDS_A0-	B72	N.C.
A73	LVDS_A1+	B73	N.C.
A74	LVDS_A1-	B74	N.C.
A75	LVDS_A2+	B75	N.C.
A76	LVDS_A2-	B76	N.C.
A77	LVDS_VDD_EN	B77	N.C.
A78	LVDS_A3+	B78	N.C.
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND	B80	GND
A81	LVDS_A_CK+	B81	N.C.
A82	LVDS_A_CK-	B82	N.C.
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	A20M#	B86	VCC_5V_SBY
A87	KBDRST#	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	RSVD
A89	PCIE0_CK_REF-	B89	N.C.
A90	GND	B90	GND
A91	RSVD	B91	N.C.
A92	RSVD	B92	N.C.
A93	GPO0	B93	N.C.
A94	RSVD	B94	N.C.
A95	RSVD	B95	N.C.
A96	GND	B96	N.C.
A97	VCC_12V	B97	N.C.
A98	VCC_12V	B98	N.C.
A99	VCC_12V	B99	N.C.
A100	GND	B100	GND
A101	VCC_12V	B101	VCC_12V
A102	VCC_12V	B102	VCC_12V
A103	VCC_12V	B103	VCC_12V
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V

Pin	Signal	Pin	Signal
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND	B110	GND

Table 27 CM-xAM COM Express Connector Rows C and D Pinout

Pin	Signal	Pin	Signal
C1	GND	D1	GND
C2	IDE_D7 / LAN2_LED0#	D2	IDE_D5 / N.C.
C3	IDE_D6 / LAN2_MDI3-	D3	IDE_D10 / N.C.
C4	IDE_D3 / LAN2_MDI3+	D4	IDE_D11 / N.C.
C5	IDE_D15 / LAN2_LED1#	D5	IDE_D12 / N.C.
C6	IDE_D8 / LAN2_MDI2-	D6	IDE_D4 / N.C.
C7	IDE_D9 / LAN2_MDI2+	D7	IDE_D0 / N.C.
C8	IDE_D2 / LAN2_LED3#	D8	IDE_DREQ / N.C.
C9	IDE_D13 / LAN2_MDI1-	D9	IDE_WR# / N.C.
C10	IDE_D1 / LAN2_MDI1+	D10	IDE_DACK# / N.C.
C11	GND	D11	GND
C12	IDE_D14 / LAN2_MDI0-	D12	IDE_IRQ / N.C.
C13	IDE_RDY# / LAN2_MDI0+	D13	IDE_A0 / N.C.
C14	IDE_RD# / LAN2_LED2#	D14	IDE_A1 / N.C.
C15	PCI_PME#	D15	IDE_A2 / N.C.
C16	PCI_GNT2#	D16	IDE_CS1# / N.C.
C17	PCI_REQ2#	D17	IDE_CS3# / N.C.
C18	PCI_GNT1#	D18	IDE_RESET# / LAN2_CTREF
C19	PCI_REQ1#	D19	PCI_GNT3#
C20	PCI_GNT0#	D20	PCI_REQ3#
C21	GND	D21	GND
C22	PCI_REQ0#	D22	PCI_AD1
C23	PCI_RESET#	D23	PCI_AD3
C24	PCI_AD0	D24	PCI_AD5
C25	PCI_AD2	D25	PCI_AD7
C26	PCI_AD4	D26	PCI_CBE0#
C27	PCI_AD6	D27	PCI_AD9
C28	PCI_AD8	D28	PCI_AD11
C29	PCI_AD10	D29	PCI_AD13
C30	PCI_AD12	D30	PCI_AD15
C31	GND	D31	GND
C32	PCI_AD14	D32	PCI_PAR
C33	PCI_CBE1#	D33	PCI_SERR#
C34	PCI_PERR#	D34	PCI_STOP#
C35	PCI_LOCK#	D35	PCI_TRDY#
C36	PCI_DEVSEL#	D36	PCI_FRAME#
C37	PCI_IRDY#	D37	PCI_AD16
C38	PCI_CBE2#	D38	PCI_AD18
C39	PCI_AD17	D39	PCI_AD20
C40	PCI_AD19	D40	PCI_AD22
C41	GND	D41	GND
C42	PCI_AD21	D42	PCI_AD24
C43	PCI_AD23	D43	PCI_AD26
C44	PCI_CBE3#	D44	PCI_AD28
C45	PCI_AD25	D45	PCI_AD30
C46	PCI_AD27	D46	PCI_INTC#
C47	PCI_AD29	D47	PCI_INTD#
C48	PCI_AD31	D48	PCI_CLKRUN#

Pin	Signal	Pin	Signal
C49	PCI_INTA#	D49	PCI_M66EN
C50	PCI_INTB#	D50	PCI_CLK
C51	GND	D51	GND
C52	SDVO_TVCLKIN+	D52	SDVO_RED+
C53	SDVO_TVCLKIN-	D53	SDVO_RED-
C54	TYPE0#	D54	N.C
C55	SDVO_INT+	D55	SDVO_GREEN+
C56	SDVO_INT-	D56	SDVO_GREEN-
C57	TYPE1#	D57	TYPE2#
C58	SDVO_FLDSTALL+	D58	SDVO_BLUE+
C59	SDVO_FLDSTALL-	D59	SDVO_BLUE-
C60	GND	D60	GND
C61	N.C.	D61	SDVO_BCLK+
C62	N.C.	D62	SDVO_BCLK-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	N.C.	D65	N.C.
C66	N.C.	D66	N.C.
C67	N.C.	D67	GND
C68	N.C.	D68	N.C.
C69	N.C.	D69	N.C.
C70	GND	D70	GND
C71	N.C.	D71	N.C.
C72	N.C.	D72	N.C.
C73	SDVO_CTRL_DAT	D73	SDVO_CTRL_CLK
C74	N.C.	D74	N.C.
C75	N.C.	D75	N.C.
C76	GND	D76	GND
C77	N.C.	D77	IDE_CBLID#
C78	N.C.	D78	N.C.
C79	N.C.	D79	N.C.
C80	GND	D80	GND
C81	N.C.	D81	N.C.
C82	N.C.	D82	N.C.
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	N.C.	D85	N.C.
C86	N.C.	D86	N.C.
C87	GND	D87	GND
C88	N.C.	D88	N.C.
C89	N.C.	D89	N.C.
C90	GND	D90	GND
C91	N.C.	D91	N.C.
C92	N.C.	D92	N.C.
C93	GND	D93	GND
C94	N.C.	D94	N.C.
C95	N.C.	D95	N.C.
C96	GND	D96	GND
C97	RSVD	D97	N.C.
C98	N.C.	D98	N.C.
C99	N.C.	D99	N.C.
C100	GND	D100	GND
C101	N.C.	D101	N.C.
C102	N.C.	D102	N.C.
C103	GND	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V

Pin	Signal	Pin	Signal
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND	D110	GND

5 ELECTRICAL SPECIFICATION

5.1 Power Consumption

CM-xAM module's power consumption mainly depends on a CPU model used and on the module configuration.

Currents were measured when CM-xAM module inserted into SB-xAM. The current consumed by the SB-xAM alone, has been measured separately and subtracted from the measurement results (150mA avg).

Configuration under test CM-xAM D1024 C1600 N4 E2 S Y3

5.1.1 Windows XP Idle State

Measurement was done with ethernet cables disconnected and with no applications running.

Measurement results:

- Average 450mA @ 12.0VDS
- Peak 500mA @ 12.0VDS

5.1.2 Windows XP Running Quake III Arena

This mode engages most of the system resources simultaneously and gives good estimate of the absolute maximum of the power consumption. The game is played in Skirmish, when Team Spectate mode is entered and following one of the bots.

The game settings are:

- Video mode 1024x768
- Color depth 32 bit
- Geometric detail high
- Texture detail max
- Texture quality 32 bit

Measurement results:

- Average 550mA @ 12.0VDS
- Peak 630mA @ 12.0VDS

6 MECHANICAL SPECIFICATIONS

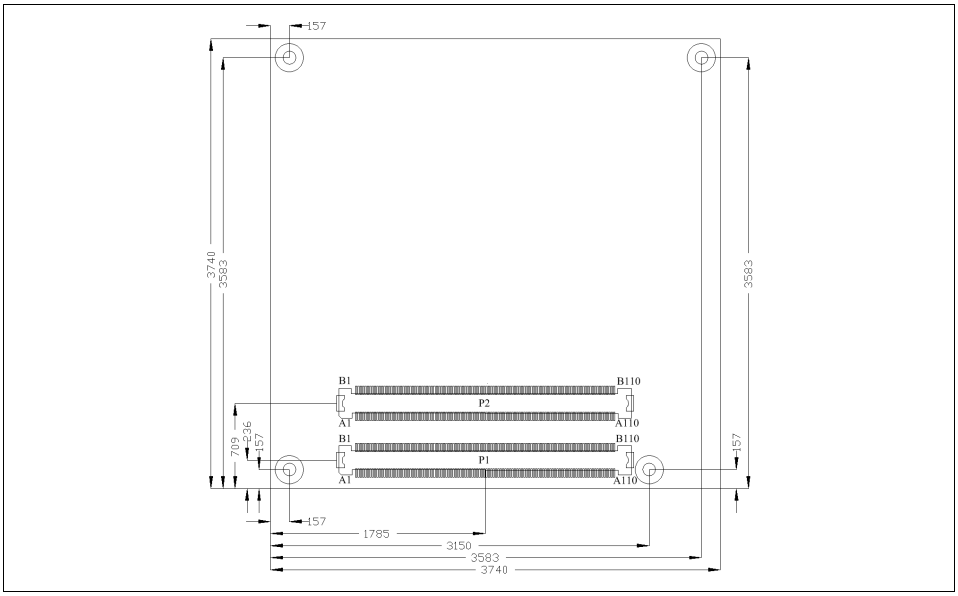
CM-xAM interfaces carrier boards through P1, P2 – 220-pin fine-pitch (0.5mm) connectors.

6.1 Connector Layout

A connector layout drawing is shown in Figure 5. The layout drawing is available also in DXF and PDF format files from the CompuLab web site.

Note: The board is shown as if viewed from the top side. All sizes are in mils.

Figure 5 Connector Layout



6.2 Connector Type

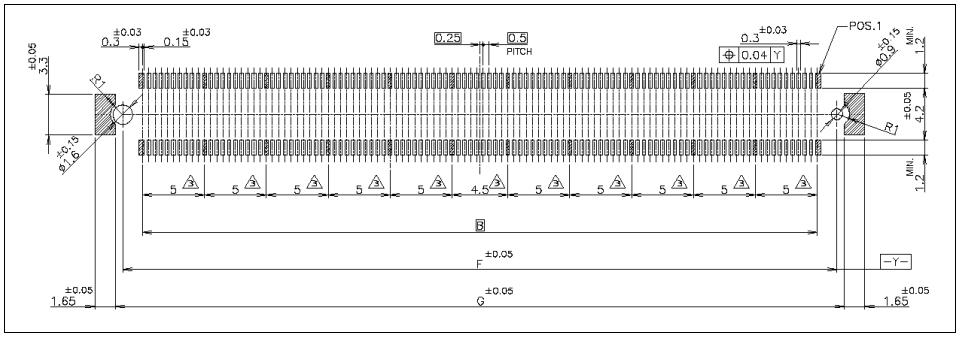
The designer of the baseboard accommodating the CM-xAM should use the mating connector.

Table 28 Interface Connector Type

Connector	Mfg.	CM-xAM Connector P/N	Mating Connector P/N
P1, P2	TYCO-AMP	8-1318490-6	3-1827253-6

Mating connectors are available from manufacturer representatives or from CompuLab.

Figure 6 Connector Footprint Drawing



For better module vs. baseboard alignment CompuLab recommends using the following peg hole tolerances as opposed to those recommended by COM Express specification:

∅1.5 ± 0.05 mm
∅0.8 ± 0.05 mm

Note:
G = 59.5 mm
F = 57.7 mm