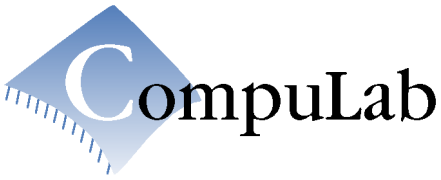


CM-iAM
Computer-On-Module

Reference Guide

Table of Contents

1. Revision Notes

Date	Description
30-September-2009	Preliminary release
04-November-2009	Added heatplate assembly notes
27-December-2009	Added bios flash mapping paragraph
24-January-2010	Connector type update (p 4.1)
26-May-2010	-Updates for Rev. 1.2 (Audio and SIO interfaces) -Added support for bootable/SDHC SD – media -Changed support for NAND flash capacity (only 4Gbyte)
27-December-2010	-Changed Heat-plate assembly instruction chapter

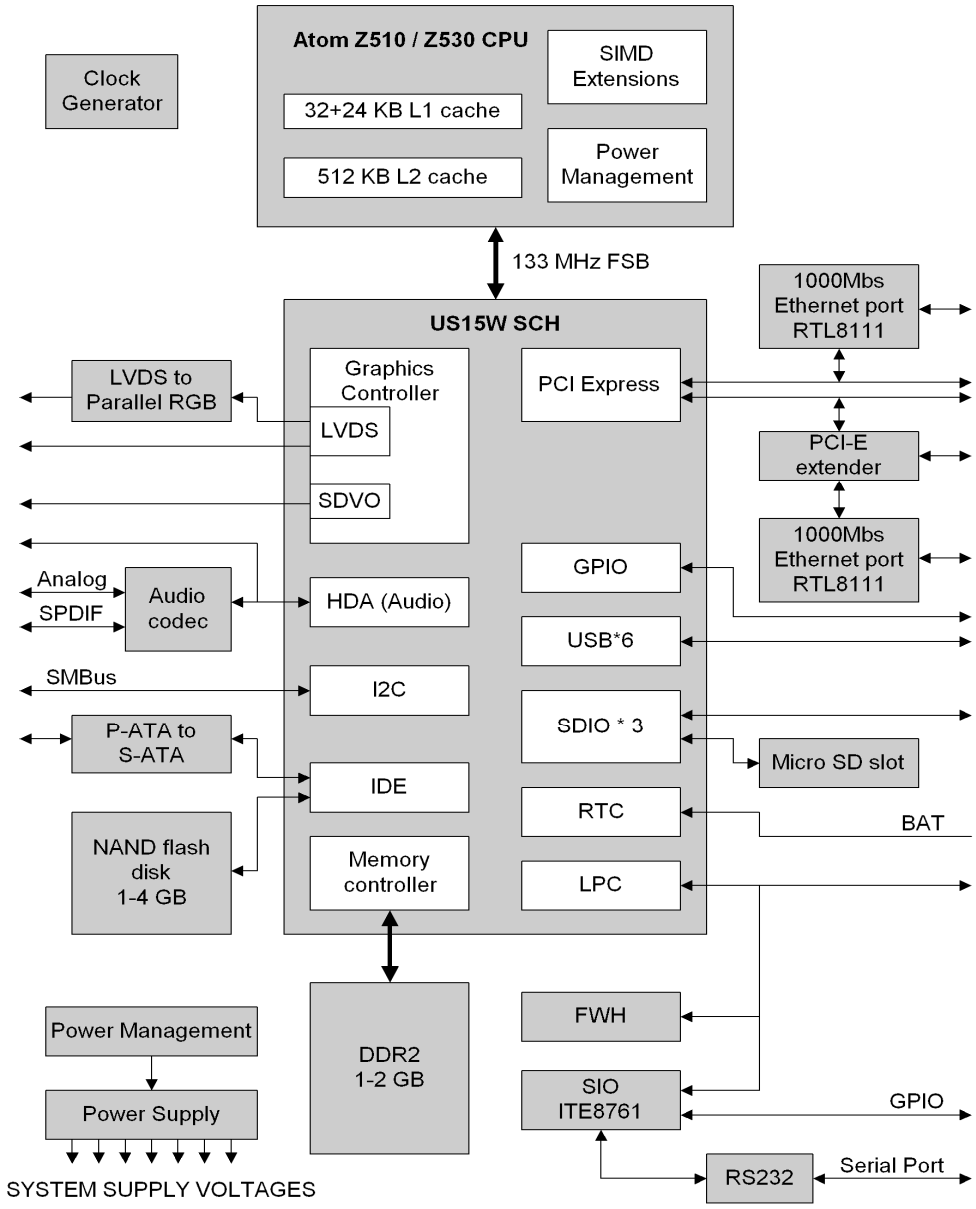
Please check for a newer revision of this manual in CompuLab's website - http://www.compulab.co.il/iam/html/iam-developer.py links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

2. Overview

2.1. Highlights

▪ **Full Featured PC-Compatible Computer-On-Module** ▪ **Intel Atom Z530 CPU @1.6GHz, US15W chipset** ▪ **2 GB DDR2** ▪ **4 GB Flash Disk and on-board microSD socket** ▪ **LVDS, parallel RGB and SDVO display interfaces for LCD panels** ▪ **SATA hard disk interface** ▪ **2 x 1000 BaseT Ethernet ports** ▪ **6 x USB ports** ▪ **2 x SDIO ports** ▪ **Sound codec with support for speaker, microphone and SPDIF. HD audio bus** ▪ **PCIexpress and LPC extension busses** ▪ **Serial port, I2C, GPIO interface** ▪ **Programmable watchdog timer** ▪ **5 watt power consumption** ▪ **Small size - 75 x 65 mm** ▪ **Member of CompuLab's Atom-based products line including SBC-iAM, SBC-FITPC2, fit-PC2 and fit-PC2i**	**The CM-iAM** packs up-to-date year 2009 technologies into the most compact, lightweight PC-on-module available in the market. Its on-board resources suffice to smoothly run operating systems such as Linux, Windows XP and Windows 7, on credit-card sized board capable running on small battery. Board's specifications, in addition to its low cost, make it an ideal building block for any embedded application. The feature set of the CM-iAM comprises a 32-bit X86-compatible CPU, DDR2, Flash Disk and vital computing peripherals. For embedded applications, the CM-iAM provides a variety of display interfaces, PCIexpress bus, two 1000Mbit Ethernet ports, serial port, general purpose I/O lines and many other essential functions. The user interface is supported by an enhanced graphics controller, USB interface for keyboard / mouse and Audio system.

2.2. Block Diagram



2.3. Features

"Option" column specifies the configuration code required to have the particular feature.
"+" means that the feature is available always.

CPU, Memory and Busses

Feature	Specifications	Option
CPU	Intel Atom Processor: Z530 - 1.6Ghz @533MHz FSB, or Z510 - 1.1GHz @400MHz FSB. L2-512KB (dynamic sizing), L1- 32KB IC, 24KB DC. Intel Deep Power Down (C6) technology support	C
DRAM	512/1024/2048 MB DDR2, 400 / 533 MHz, 64-bit	D
BIOS Flash	1 MByte, on-board reprogrammable	+
Flash Disk	4 GBytes, more in future. Up to 10 MB/s transfer rate	N
External Busses	PCI express, LPC, HD audio	+
PCI express bus	PCI Express Base Specification, Revision 1.0a. One or two lanes. Note: Two lanes are available if fewer than two Ethernet controllers are assembled.	+
LPC bus	Host, 33 MHz, Intel LPC v1.0 compatible	+

Peripherals

Feature	Specifications	Option
Graphics Controller	Resolution up to 1920 x 1080 x 32 bpp frame buffer in system memory, 2D, 3D graphics accelerator and multimedia accelerator optimized for HD video	+
Display Interface	LCD – 24 bpp parallel RGB for TFT panels LVDS – 24 bpp, 4 data and 1 clk pairs for TFT panels SDVO – can be directly connected to DVI / HDMI / VGA transmitters	L + +
SDIO	Bootable SD/MMC interface with SDHC support On-board micro-SD slot + 2 external SDIO/MMC interfaces	+
USB	6 Host USB 2.0 ports, 480 Mbps, EHCI / UHCI-compliant	+
Serial Port	UART's, full serial port with modem controls, RS232	S
GPIO	7 dedicated lines + 1 shared line	+
Additional GPIO	7 dedicated lines	S
Hard Disk Interf.	SATA-II, using Marvell 88SA8052	Y
Kbrd & Mouse	USB	+
Ethernet	Two 1000 Mb/s ports, activity LED's. RTL8111	Ex
Audio codec	IDT 92HD83 controller, HD audio interface, stereo microphone and line inputs, 60 mW capless output for 32 Ohm headphones / active speakers, 5.1 channel SPDIF output Rev 1.2 and above uses ALC662 Audio codec , with stereo microphone , line inputs , and line output ,5.1 channel SPDIF output	A
RTC	Real Time Clock, powered by external lithium battery	+
Internal	One internal 4-bit micro SD and two external 4-bit SDIO ports	+

Watchdog	Wide range programmable watchdog timer operational at early power-up stage	+

Electrical, Mechanical and Environmental Specifications

Supply Voltage	5V
Active power consumption	4 - 6 W, depending on configuration and CPU speed
Dimensions	65 x 75 x 8 mm
Weight	37 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0o to 70o C Extended: -20o to 70o C Industrial: -40o to 85o C. Click for availability note
Storage temperature	-40o to 85o C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm. Insertion / removal up to 50 cycles

2.4. General Description

The CM-iAM is a miniature single-board computer packed as a module. It contains a CPU, chipset, memory, flash disk and peripherals. All interface functions of the CM-iAM are routed through miniature high-density connectors, designed for piggyback attachment to a custom baseboard, as shown in the picture below.

2.5. Atom CPU Core Architecture

The CM-iAM utilizes an Intel® Atom Z5xx series CPU.

The Intel® Atom Z5xx series processor is built with 45-nanometer process technology — the first generation of a low-power IA-32 micro-architecture specially designed for the new class of Mobile Internet Devices (MID).

The following list provides some of the key features of this processor:

- New single-core processor for mobile devices with enhanced performance
- On-die, primary 32-kB instructions cache and 24-kB write-back data cache
- 100-MHz and 133-MHz Source-Synchronous front side bus (FSB)
- Supports Hyper-Threading Technology 2-threads
- On-die 512-kB, 8-way L2 cache
- Support for IA 32-bit and Intel® 64 architecture
- Intel® Virtualization Technology (Intel® VT)
- Intel® Streaming SIMD Extensions 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Supports new CMOS FSB signaling for reduced power
- Micro-FCBGA8 packaging technologies
- Thermal management support via TM1 and TM2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- New C6 Deep Power Down Technology
- L2 Dynamic Cache Sizing
- New Split-VTT support for lowest processor power state
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Executes Disable Bit support for enhanced security

2.6. Chipset

The CM-iAM uses an Intel® System Controller Hub (Intel® SCH) US15W Poulsbo chipset. The Intel® SCH chipset of the Atom low-power platform combines the functionality normally found in separate GMCH (integrated graphics, processor interface, memory controller) and ICH (on-board and end-user I/O expansion) components into a single component consuming less than 2.3 W of thermal design power.

2.7. Flash Disk

One of the key advantages of CM-iAM architecture is its high-performance, fully-integrated, embedded flash solid state drives (when option N4G is selected) - SST85LD1004M NANDrive™ integrated circuits (IC).
It combines an integrated ATA Controller and either 1Gbyte or 4Gbytes of NAND Flash in a multi-chip package. This solution is ideal for solid-state mass storage applications offering new and expanded functionality while enabling cost-effective designs.
The SST NANDrive is a single solid-state drive device, designed for embedded ATA/IDE protocol systems supporting a standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-4 interfaces. The built-in micro-controller and file management firmware communicates with ATA standard interfaces thereby eliminating the need for additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.
The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts and is built into the CM-iAM module.
The NAND Flash provides a storage solution for embedded applications requiring non-volatile on-board storage. The NAND Flash is a block device - optimized for block read and write operations rather than for random access. The NAND Flash is interfaced through a standard ATA-based IDE port and is configured as a primary master device by default.

Key Features:

- Industry Standard ATA/IDE Bus Interface
- Host Interface: 16-bit access
- Supports up to PIO Mode-6
- Supports up to Multi-word DMA Mode-4
- Supports up to Ultra DMA Mode-4
- Advanced power management
- Zero wake-up latency
- Expanded Data Protection
- Data security through user-selectable protection
- User-Programmable 10-byte ID
- Prevents data loss due to unexpected power-down or brownout
- 10 Million write cycles with advanced NAND management technology
- 3 year data retention
- Robust Built-in ECC

Performance

Read	Up to 30Mb/s
Write	Up to 8Mb/s

Write Protection
For extended reliability, NAND_WP# input on the module interface completely prevents flash write and erase operations.

3. Peripherals and Functions

3.1. Display Controller

The CM-iAM graphics system is based on the Intel® SCH integrated graphics controller, based on Intel® GMA500 architecture. The highly compact Integrated Graphics Device (IGD) contains advanced shader architecture (model 3.0+) that performs pixel shading and vertex shading within a single hardware accelerator. The processing of pixels is deferred until they are determined to be visible, which minimizes access to memory and improves render performance.

Key Features:

- Flexible Programmable Architecture
- Shader-based technology
- 3D Graphics
- 2D and advanced 2D Graphics
- Video - Encode / Decode support
- Image processing
- Deferred Pixel Shading
- Screen Tiling
- On-chip Stencil, Z and Frame buffers
- High Performance
- Low Power
- Industry standard tool support
- Comprehensive OS/API support

3-D Core Key Features:

- Two pipe scaleable unified shader implementation
- 3-D Peak Performance
- Fill Rate: 2 Pixels per clock
- Vertex Rate: One Triangle 15 clocks (Transform Only)
- Vertex / Triangle Ratio average = 1 vtx/tri, peak 0.5 vtx/tri
- Texture max size = 2048 x 2048
- Programmable 4x multi-sampling anti-aliasing (MSAA)
- Rotated grid
- ISP performance related to AA mode, TSP performance unaffected by AA mode
- Optimized memory efficiency using multi-level cache architecture

Video Decode Overview

The video decode accelerator improves video performance / power by providing

hardware-based acceleration at the macroblock level (variable length decode stage entry point). The Intel SCH supports full hardware acceleration of the following video decode standards:

CODEC	PROFILE	LEVEL
H.264	Baseline profile	L3
H.264	Main profile	L4.1 (1080i @ 30fps)
H.264	High profile	L4.1 (1080i @ 30fps)
MPEG2	Main profile	High
MPEG4	Simple profile	L3
MPEG4	Advanced simple profile	L5
VC1	Simple profile	Medium
VC1	Main profile	High
VC1	Advanced profile	L3 up to (1080i @ 30fps)
WMV9	Simple profile	Medium
WMV9	Main profile	High

The video decode function is performed in four processing modules:
- Entropy coding processing
- Motion compensation
- Deblocking
- Final pixel formatting

The IGD includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays – LVDS and SDVO. The CM-iAM also implements an LVDS to parallel 24-bit RGB converter (option L) allowing the connection of different parallel LCD's in addition to LVDS displays.

LVDS

The System Controller Hub (Poulsbo SCH) supports a Low-Voltage Differential Signaling interface allowing the IGD to communicate directly with a flat-panel display. The LVDS interface supports pixel color depth of 18 or 24 bits and max pixel clock of 112 MHz

LVDS Interface:

Baseboard conn		Type	Description
Signal	Pin		
LVDS_A0-	P1-52	ODIF	LVDS differential pair 0
LVDS_A0+	P1-54	ODIF	
LVDS_A1-	P1-51	ODIF	LVDS differential pair 1
LVDS_A1+	P1-53	ODIF	
LVDS_A2-	P1-58	ODIF	LVDS differential pair 2
LVDS_A2+	P1-60	ODIF	

LVDS_A3-	P1-57	ODIF	LVDS differential pair 3
LVDS_A3+	P1-59	ODIF	
LVDS_CLK-	P1-63	ODIF	LVDS differential clock
LVDS_CLK+	P1-65	ODIF	
LVDS_DID_CLK	P1-47	I/O	Display Data Channel Clock: I2C-based control signal (Clock) for EDID control
LVDS_DID_DAT	P1-49	I/O	Display Data Channel Data: I2C-Data for EDID control
LVDS_BLT_CTR	P1-48	O	LCD Backlight Control: This signal allows control of LCD brightness
LVDS-BLEN	P1-56	O	Panel backlight enable control
LVDS-PPEN	P1-61	O	Power sequencing control for panel driver electronics voltage VDD

Intel Serial DVO (SDVO) Display

The SCH has a digital display channel capable of driving SDVO adapters providing interfaces to a variety of external display technologies (e.g., DVI, analog CRT).
Up to 160 MHz pixel clock supported.

SDVO Interface:

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
SDVO_BCLK+	P1-30	ODIF	Serial Digital Video Channel B Clock
SDVO_BCLK-	P1-28	ODIF	
SDVO_BLUE+	P1-35	ODIF	Serial Digital Video Channel B Blue
SDVO_BLUE-	P1-33	ODIF	
SDVO_RED+	P1-42	ODIF	Serial Digital Video Channel B Red
SDVO_RED-	P1-40	ODIF	
SDVO_GREEN+	P1-29	ODIF	Serial Digital Video Channel B Green
SDVO_GREEN-	P1-27	ODIF	
SDVO_INT+	P1-36	IDIF	Serial Digital Video Input Interrupt
SDVO_INT-	P1-34	IDIF	
SDVO_FLDSTALL+	P1-41	IDIF	Serial Digital Video Field Stall
SDVO_FLDSTALL-	P1-39	IDIF	
SDVO_TVCLKIN+	P1-23	IDIF	Serial Digital Video TV-OUT Synchronization Clock pair
SDVO_TVCLKIN-	P1-21	IDIF	
SDVO_CTRL_CLK	P1-25	I/O	SDVO Control Clock (similar to I2C)
SDVO_CTRL_DAT	P1-32	I/O	SDVO Control Data (similar to I2C)

Notes

- SDVO signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum =1.5 V. Single-ended minimum = 0 V.
- 100 nF decoupling capacitor must be used on all differential SDVO signals (see SB-iAM reference schematic)

LCD Panel Interface

This interface is available only in modules with the "L" option.
LCD Interface:

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
LCD-B0	P1-95	O	LCD Panel Data Bus.
LCD-B1	P1-96	O	
LCD-B2	P1-97	O	
LCD-B3	P1-99	O	
LCD-B4	P1-100	O	
LCD-B5	P1-101	O	
LCD-B6	P1-102	O	
LCD-B7	P1-104	O	
LCD-G0	P1-85	O	
LCD-G1	P1-87	O	
LCD-G2	P1-88	O	
LCD-G3	P1-89	O	
LCD-G4	P1-90	O	
LCD-G5	P1-92	O	
LCD-G6	P1-93	O	
LCD-G7	P1-94	O	
LCD-R0	P1-75	O	
LCD-R1	P1-76	O	
LCD-R2	P1-77	O	
LCD-R3	P1-78	O	
LCD-R4	P1-81	O	
LCD-R5	P1-82	O	
LCD-R6	P1-83	O	
LCD-R7	P1-84	O	
LCD-SCK	P1-108	O	Display Data Clock. Pixel clock for flat panel data
LCD-VSYNC	P2-107	O	VSYNC
LCD-HSYNC	P1-109	O	HSYNC
LCD-DE	P1-105	O	Display Enable signal (DE) for TFT Panels
LCD-PWREN	P1-106	O	Power sequencing control for panel VDD

3.2. SATA interface

This interface is available only in modules with the "Y" option.
The CM-iAM Serial ATA (SATA) interface is formed from the PATA interface using a PATA to SATA bridge. The CM-iAM ATA (PATA) interface is provided directly by an Intel® SCH PATA controller. PATA interface supports only the primary channel, with one master and one slave device.
Three types of data transfers are supported:

- Programmed I/O (PIO): A protocol used to transfer data between the processor as the ATA device. PIO allows transfer rates of up to 16MB/s.
- Multi-word DMA: DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 16MB/s.
- Ultra-DMA: Source synchronous DMA protocol allowing transfer rates of up to 100MB/s.

Supported PATA standards and modes:

PATA Standard	Transfer Modes Supported	Transfer Rate (MB/s)
ATA-1 (ATA, IDE)	PIO Modes 0, 1, 2	3.3, 5.2, 8.3
	Single-word DMA Modes 0, 1, 2	2.1, 4.2, 8.3
	Multi-word DMA Mode 0	4.2
ATA-2, ATA-3 (EIDE, Fast ATA)	PIO Modes 3,4	11.1, 16.6
	Multi-word DMA Modes 1,2	13.3, 16.6
ATA/ATAPI-4 (Ultra DMA, Ultra ATA)	Ultra DMA Modes 0,1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 (Ultra DMA, Ultra ATA)	Ultra DMA Modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 (Ultra DMA, Ultra ATA)	Ultra-DMA Mode 5 (a.k.a. Ultra DMA/100)	100 (reads) 89 (writes)

PATA to SATA bridge key features are:

- SATA-II with 1.5 Gb/s operation support
- SATA 2.6 Compliant
- ATA/ATAPI 48-bit address feature set
- ATA/ATAPI 7 feature set
- Tagged command queuing (maximum 32 entries)
- SATA power save modes

SATA Interface:

Baseboard conn		Type	Description
Signal	Pin		
SATA0_RX+	P2-120	IDIF	SATA receive pair
SATA0_RX-	P2-118	IDIF	
SATA0_TX+	P2-126	ODIF	SATA transmit pair
SATA0_TX-	P2-124	ODIF	
SATA_LED	P2-128	O	SATA/PATA activity led
MASTER/SLAVE*	P1-44	I	Master/Slave toggle (default 1 –SATA slave)

*When the option [Nx] isn't assembled, the default state for P1-44 is "0" – meaning SATA interface becomes primary master.

3.3. PCI Express

The CM-iAM contains two x1 PCI Express expansion interfaces (when no Ethernet is assembled – otherwise only one external PCIE is available), supporting the PCI Express Base Specification, Revision 1.0a configured as two x1 lanes. Each root port supports 2.5 GB/s bandwidth in each direction.
It is a high-bandwidth, low pin-count serial interface ideal for I/O expansion. An external graphics device can be used via one of the x1 PCI Express lanes/ports. When option E2 (two Ethernets) is assembled – external PCIE on the baseboard interface connector is provided through the PCIE-PCIE bridge. Below are PCIE0, PCIE1 and the control signals group. PCIE0 is available only when no Ethernet option is selected. PCIE1 is always available.

PCIE0 signal group:

Baseboard conn		Type	Description
Signal	Pin		
PCIE0_RX+	P2-108	IDIF	PCIE0 receive pair
PCIE0_RX-	P2-106	IDIF	
PCIE0_TX+	P2-114	ODIF	PCIE0 transmit pair
PCIE0_TX-	P2-112	ODIF	
PCIE_CLK0+	P2-101	ODIF	PCIE0 differential clock
PCIE_CLK0-	P2-99	ODIF	
PCIE_CLK0E#	P2-17	I	PCIE0 clock enable (has 8.2k internal PU) – to enable – 1k pull down should be used

PCIE1 signal group:

Baseboard conn		Type	Description
Signal	Pin		
PCIE1_RX+	P2-107	IDIF	PCIE1 receive pair
PCIE1_RX-	P2-105	IDIF	
PCIE1_TX+	P2-113	ODIF	PCIE1 transmit pair

PCIE1_TX-	P2-111	ODIF	
PCIE_CLK1+	P2-83	ODIF	PCIE1 differential clock
PCIE_CLK1-	P2-81	ODIF	
PCIE_CLK1E#	P2-15	I	PCIE1 clock enable (has 8.2k internal PU) –to enable – 1k pull down should be used

PCIE control signals:

Baseboard conn		Type	Description
Signal	Pin		
PCIE_RST#	P2-104	O	PCIE reset signal when option E2 is assembled; otherwise, use general RESET# (P2-20) for this purpose.
PCI_WAKE#	P2-109	I	PCI Express* Wake Event: This signal indicates that a PCI Express port wants to wake the system.

Notes

- PCIE differential signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum =1.5 V. Single-ended minimum = 0 V.
- 100 nF decoupling capacitor must be used on the receiver side (_RX* signals on baseboard interface connector. See SB-iAM reference schematic.

3.4. HDA Interface

The audio / modem link in the CM-iAM is High Definition Audio (HD Audio) compliant, supporting high quality audio.
Features Supported by HDA:

- Sample rate ranging from 6 kHz to 192 kHz
- 8-, 16-, 20-, 24-, and 32-bit sample resolution per stream
- Up to 16 channels per stream
- 48-Mbps outbound link transfer rate per SDO
- 24-Mbps inbound transfer rate per SDI
- Support for 2 -SDI codecs to increase available inbound link bandwidth
- Codec architecture is fully discoverable, allowing for codec design flexibility
- Audio codecs, modem codecs, and vendor-defined codecs are all supported
- Command/Response codec communication mechanism for extensibility and flexibility
- Extensive, fine grained power management control in the codec
- Industry standard 48-pin QFP package and pinout for codec
- Audio codecs support advanced jack detection and jack sensing for device discoverability and jack retasking

HDA Link Interface:

Baseboard conn		Type	Description
Signal	Pin		
HDA_RST#	P2-121	O	Intel® HD Audio Reset: This signal is the reset to external Codec(s)
HDA_SYNC	P2-125	O	Intel HD Audio Sync: This signal is an 48-kHz fixed rate sample sync to the Codec(s). It is also used to encode the stream number.
HDA_BCLK	P2-119	I	Intel HD Audio Clock (Output): This signal is a 24.000-MHz serial data clock generated by the Intel HD Audio controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel HD Audio CODEC (or no CODEC) is connected.
HDA_SDO	P2-123	O	Intel HD Audio Serial Data Out: This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio.
HDA_SDIN0	P2-117	I	Intel HD Audio Serial Data In 0: These serial inputs are single-pumped for a bit rate of 24 MB/s. Has integrated pull-down resistors that are always enabled.
HDA_SDIN1	P1-20	I	Intel HD Audio Serial Data In 1: This serial input is single-pumped for a bit rate of 24 MB/s. Has integrated pull-down resistors that are always enabled.

3.5. LPC - Low Pin Count Interface

The CM-iAM implements an LPC Interface and Controller as described in the LPC 1.1 specification. The LPC bus provides a functional replacement for interfacing legacy ISA functions.

LPC Bus Interface

Baseboard conn		Type	Description
Signal	Pin		
LPC_AD0	P2-90	I/O	LPC Multiplexed Command, Address, Data.
LPC_AD1	P2-92	I/O	
LPC_AD2	P2-94	I/O	
LPC_AD3	P2-96	I/O	

LPC_SERIRQ	P2-89	I/O	Serial Interrupt Request: This signal conveys the serial interrupt protocol.
LPC_FRM#	P2-87	O	LPC Frame: Indicates the start of an LPC cycle, or an abort.
LPC_CLK	P2-88	I/O	LPC clock (33 Mhz)

LPC_CLK is pre-compensated for an external clock trace length of 5 cm. The maximum allowed length of the external clock trace is 5cm. In addition to the above signals, an LPC device needs the RESET# signal.

3.6. Serial IRQ

The CM-iAM provides another interface for interrupt requests – serial IRQ. This allows a single signal line to be used to report legacy ISA interrupt requests. Interrupt sharing is allowed on Serial IRQ interfaces only for devices external to the chipset. The following interrupts are external to the chipset and are therefore potentially available on the Serial IRQ interface: IRQ1, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ11, IRQ12, IRQ14. The serial IRQ interface is a synchronous interface. Data is clocked by the system's PCI clock.

Serial IRQ interface

Baseboard conn		**Interface**	**Description**
Signal	**Pin**		
LPC_SERIRQ	P2-89	I/O	The routing for this signal must be done using PCI layout/routing rules.

The IRQ assignment listed in Interrupt Channel Mapping table is correct for a CM-iAM plugged into CompuLab's baseboard with inserted micro-SD card (such as SB-AM), but may change if additional hardware is attached.

3.7. Serial Ports

This interface is available only in modules with the “S” option.
CM-iAM implements full UART through the Super-I/O (rev 1.1 - IT8761E chip, F71808 for rev 1.2 and above) . The IT8761E is an LPC Interface based Super I/O with concise legacy support. The CM-iAM utilizes a full 16C550 UART with an RS232 level driver.
The serial ports include the following features:

- Fully compatible with 16550 and 16450 devices
- UART mode data rates up to 115 Kbps

Serial Port Signals

Baseboard conn		Interface	Type	Description
Signal	Pin			
COM1_RX	P1-117	RS232	I	Serial Data In
COM1_TX	P1-119	RS232	O	Serial Data Out
COM1_CTS#	P1-123	RS232	I	Clear To Send
COM1_DCD#	P1-113	RS232	I	Data Carrier Detect
COM1_DSR#	P1-111	RS232	I	Data Set Ready
COM1_DTR#	P1-125	RS232	O	Data Terminal Ready
COM1_RI#	P1-124	RS232	I	Ring Indicate
COM1_RTS#	P1-121	RS232	O	Request To Send

3.8. SDIO ports

The CM-iAM contains three SDIO/MMC (one on-board micro-SD and two external SDIO interfaces) expansion ports used to communicate with a variety of internal or external SDIO and MMC devices. Each port supports SDIO Revision 1.1 and MMC Revision 4.1, is 4-bits wide and is backward-compatible with previous interface specifications.

Features:

- MMC 4.1 transfer rates can be up to 48 MHz and bus widths of 1 or 4 bits.
- SDIO 1.1 supports transfer rates up to 24 MHz and bus widths of 1 or 4 bits.

Port 1 is connected to the on-board micro-SD slot, while Ports 0 and 2 are available on the baseboard interface connector. Since the on-board micro-SD card doesn't have WP or an on-board LED – these signals are also provided on the baseboard interface. All SDIO signals have integrated 48R serial termination.

SDIO 0 port signals

Baseboard conn		Type	Description
Signal	Pin		
SDA_D0	P2-54	I/O	SDIO Controller 0 Data: These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SDA_D0 is used for data transfer. Wider data bus widths can be configured for data transfer.
SDA_D1	P2-56	I/O	
SDA_D2	P2-58	I/O	
SDA_D3	P2-60	I/O	
SDA_CMD	P2-78	I/O	SDIO Controller 0 Command: used for card initialization and transferring commands. It has two operating modes: open-drain for initialization mode and push-pull for fast command transfer.

SDA_CLK	P2-76	O	SDIO Controller 0 Clock: this signal is generated by the Intel SCH at a maximum frequency of 24 MHz for SD and SDIO; 48 MHz for MMC.
SDA_CD#	P2-72	I	SDIO Controller 0 Card Detect: indicates a card presence in an external slot.
SDA_PWEN#	P2-84	I/O	SDIO/MMC Power Enable: controls the power supplied to an SDIO/MMC device.
SDA_WP	P2-82	I	SDIO Controller 0 Write Protect: denotes the state of the write-protect tab on SD cards.
SDA_LED	P2-80	O	SDIO Controller 0 LED: used for driving an external LED indicating transfers on the bus.

SDIO 2 port signals

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
SDC_D0	P2-37	I/O	SDIO Controller 2 Data: These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SDC_D0 is used for data transfer. Wider data bus widths can be configured for data transfer.
SDC_D1	P2-39	I/O	
SDC_D2	P2-41	I/O	
SDC_D3	P2-45	I/O	
SDC_CMD	P2-51	I/O	SDIO Controller 2 Command: used for card initialization and transferring commands. It has two operating modes: open-drain for initialization mode and push-pull for fast command transfer.
SDC_CLK	P2-49	O	SDIO Controller 2 Clock: this signal is generated by the Intel SCH at a maximum frequency of 24 MHz for SD and SDIO; 48 MHz for MMC.
SDC_CD#	P2-47	I	SDIO Controller 2 Card Detect: indicates a card presence in an external slot.
SDC_PWEN#	P2-34	I/O	SDIO/MMC Power Enable: controls the power supplied to an SDIO/MMC device.
SDC_WP	P2-32	I	SDIO Controller 2 Write Protect: denotes the state of the write-protect tab on SD cards.
SDC_LED	P2-53	O	SDIO Controller 2 LED: used for driving an external LED indicating transfers on the bus.

SDIO 1 port signals

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
SDB_WP	P2-57	I	SDIO Controller 2 Write Protect: denotes the state of the write-protect tab on SD cards.
SDB_LED	P2-77	O	SDIO Controller 2 LED: used for driving an external LED indicating transfers on the bus.

SDIO 1 micro-SD connector pinout:

Micro-SD conn		Signal Function
Pin #	Pin Name	
1	DAT2	Data Bit 2
2	CD/DAT3	Card Detect / Data Bit 3
3	CMD	Command Line
4	Vdd	Supply Voltage 3.3V (0.5 A max)
5	CLK	Clock
6	Vss	Ground
7	DAT0	Data Bit 0
8	DAT1	Data Bit 1

3.9. USB Interface

The CM-iAM provides six ports compliant with USB 1.1(UHCI) and USB 2.0(EHCI) specifications. The HCI specification provides a register-level description for a host controller, as well as a common industry hardware/software interface and drivers. USB ports are supported by all O/S packages provided for the CM-iAM.

Features:

- USB v2.0 / EHCI v1.0 and USB v1.1 / UHCI v1.1 compatible
- Physical layer transceivers with optional three over-current detection status on USB inputs – one for every two ports

USB Port Signals

Baseboard conn		Type	Description
Signal	Pin		
USB0+	P1-132	DIFF	USB Port 0 Data pair
USB0-	P1-130	DIFF	
USB1+	P1-138	DIFF	USB Port 1 Data pair
USB1-	P1-136	DIFF	
USB2+	P1-131	DIFF	USB Port 2 Data pair
USB2-	P1-129	DIFF	
USB3+	P1-137	DIFF	USB Port 3 Data pair
USB3-	P1-135	DIFF	
USB4+	P2-132	DIFF	USB Port 4 Data pair
USB4-	P2-130	DIFF	
USB5+	P2-140	DIFF	USB Port 5 Data pair
USB5-	P2-138	DIFF	
USB_OC0_1#*	P1-128	I	Overcurrent pin for ports 0,1

Baseboard conn		Type	Description
Signal	Pin		
USB_OC2_3#*	P1-133	I	Overcurrent pin for ports 2,3
USB_OC4_5#*	P2-136	I	Overcurrent pin for ports 4,5

*Can be left not connected (NC) if not used

3.10. Audio Interface

There are 2 revision of CM-iAM , that use different audio codecs.

3.11. Audio Interface (Rev 1.1)

The CM-iAM (Rev. 1.1) implements audio interface using the IDT 92HD83 single-chip audio system, a low-power optimized, high-fidelity, 6-channel audio codec. The 92HD83 is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revisions 4 and 5 as indicated in WLP 3.09. The 92HD83 provides 24-bit, full-duplex stereo resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD83 SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. 92HD83 SPDIF input supports sample rates of 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by driver software.
MIC inputs can be programmed with 0/10/20/30dB boost. The port presence detect capability allows the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and optimizes user experience.

Features:

- Integrated High-Performance Headphone Amplifier
- Multiple Sample Rate Converters
- 24-bit Stereo Digital-to-Analog Converters and Analog-to-Digital Converters
- Two configurable Line In-level/Mic Stereo Inputs
- Integrated High-Performance Microphone Pre-Amplifier with 0/10/20/30dB boost
- SPDI/F output
- Capless Headphone Out
- Audio inactivity transitions codec from D0 to D3 low power mode

Audio specifications

Headphone, speaker Output	Type	Stereo
	Power	60mW peak into 32 ohm speakers
	Decoupling	Capless – requires 5.1R resistor on each channel
Microphone/ Line Input	Type	Stereo, electret or dynamic
	Decoupling	On-board

Audio Interface Signals

Baseboard conn		Type	Description
Signal	Pin		
AIN_L	P2-133	IA	Audio stereo line/mic input left PORT_C
AIN_R	P2-131	IA	Audio stereo line/mic input right. PORT_C
MIC_IN_L	P2-129	IA	Audio Mic/stereo line input left PORT_F
MIC_IN_R	P1-24	IA	Audio Mic/stereo line input right. PORT_F
AOUT_L	P2-139	OA 60mW	Headphone/Line stereo output left. PORT_B
AOUT_R	P2-137	OA 60mW	Headphone/Line stereo output right. PORT_B
SPDIF_OUT	P1-18	O	SPDI/F output
SENSE_A	P1-22	I	Sense detector for ports B and C and SPDIF: PORT_B-20k, PORT_C –10k, SPDIF-5.11k
SENSE_B	P1-46	I	Sense detector for port F – 20k

To enable auto detect functionality, appropriate resistors (see above) must be connected to the jack switch.

3.11.1. Audio Interface (Rev 1.2 and above)

The CM-iAM (Rev. 1.2) implements audio interface using ALC662 single-chip audio system, a low power optimized, high fidelity, 6-channel audio codec. The ALC662 provides 16/20/24-bit, supporting sample rates up to 96kHz by the DAC and ADC. SPDIF output support sample rates of 96kHz, 48kHz, and 44.1kHz.MIC inputs can be programmed with 0/10/20/30dB boost. The port presence detect capability allows the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and optimizes user experience.
Features:

- Multiple Sample Rate Converters
- 16/20/24-bit Stereo Digital-to-Analog Converters and Analog-to-Digital Converters
- Two configurable Line In-level/Mic Stereo Inputs
- Integrated High-Performance Microphone Pre-Amplifier with 0/10/20/30dB boost
- SPDI/F output
- Anti pop mode
- Microphone Acoustic Echo Cancellation (AEC)

Audio specifications

Line output	Type	Stereo
	Decoupling	On-board

Microphone/ Line Input	Type	Stereo, electret or dynamic
	Decoupling	On-board

Audio Interface Signals

Baseboard conn		Type	Description
Signal	Pin		
AIN_L	P2-133	IA	Audio stereo line/mic input left PORT_C
AIN_R	P2-131	IA	Audio stereo line/mic input right. PORT_C
MIC_IN_L	P2-129	IA	Audio Mic/stereo line input left PORT_B
MIC_IN_R	P1-24	IA	Audio Mic/stereo line input right. PORT_B
AOUT_L	P2-139	O	Line stereo output left. PORT_A
AOUT_R	P2-137	O	Line stereo output right. PORT_A
SPDIF_OUT	P1-18	O	SPDI/F output
SENSE_A	P1-22	I	Sense detector for all ports B and C and SPDIF: PORT_B-20k, PORT_C –10k, PORT_A – 39.2k
SENSE_B	P1-46	I	Shorted to SENSE-A(P1-22)

To enable auto detect functionality, appropriate resistors (see above) must be connected to the jack switch.

3.12. Gigabit Ethernet Ports

The CM-iAM provides one (option E1) or two (option E2) Gigabit Ethernet port(s) implemented using a Realtek RTL8111D Gigabit Ethernet controller. The Realtek RTL8111D Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller and embedded memory. With state-of-art DSP technology and mixed-mode signal technology, the RTL8111D offers high-speed transmission over CAT 5 UTP or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery and error correction are implemented to provide robust transmission and reception capability at high speeds.
The device is compliant with the IEEE 802.3u specification for 10/100M bps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet.

RTL8111D Gigabit Ethernet controller features:

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Crossover Detection & Auto-Correction

- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and Largesend Offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u and IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Transmit/Receive on-chip buffer (48KB) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)

Ethernet 1 Port Signals

Baseboard conn		Type	Description
Signal	Pin		
MDI1_0+ MDI1_0-	P1-2 P1-4	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T, and transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.
MDI1_1+ MDI1_1-	P1-1 P1-3	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T, and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
MDI1_2+ MDI1_2-	P1-10 P1-12	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
MDI1_3+ MDI1_3-	P1-9 P1-11	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.
ETH_LED1_0#	P1-6	O	Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH_LED1_1#	P1-5	O	100 Link/ACT LED. The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH_LED1_2#	P1-13	O	10 Link/ACT LED. The 10 Link LED pin indicates link integrity and 10 Mbps FULL connection speed.

Ethernet 2 Port Signals

Baseboard conn		Type	Description
Signal	Pin		
MDI2_0+ MDI2_0-	P2-2 P2-4	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T, and transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.

MDI2_1+ MDI2_1-	P2-1 P2-3	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T, and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
MDI2_2+ MDI2_2-	P2-10 P2-12	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
MDI2_3+ MDI2_3-	P2-9 P2-11	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.
ETH_LED2_0#	P2-6	O	Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH_LED2_1#	P2-5	O	100 Link/ACT LED. The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH_LED2_2#	P2-13	O	10 Link/ACT LED. The 10 Link LED pin indicates link integrity and 10 Mbps FULL connection speed.

Magnetic Modules

The CM-iAM's Twisted Pair interface requires an external transformer (magnetic module) for interface to an RJ-45 connector. The two options use either:

1. An RJ-45 connector with a built-in transformer. Examples:

Vendor	Model
Speed_Tech	P65-101-[1|2]AK9
UDE	RB1-125BAK1A

2. A separate transformer and RJ-45 connector. Examples of available transformers:

Vendor	Model
Pulse Engineering	H5007
Pulse Engineering	H1251

Routing Ethernet Signals

The following rules should be applied when routing differential transmit and receive signals between the CM-iAM interface connector and an external connector/transformer module:

1. Route the differential signal pairs (TXN, TXP) and (RXN, RXP) in parallel, with minimal and consistent clearance within the pair. The distance between the RX and TX pairs should be maximized; otherwise, TX will induce crosstalk into RX.
2. It is preferable (but not mandatory) to keep the trace length of Ethernet signals as short as possible. If trace length exceeds two inches, additional steps, not specified here, should be taken. Recommended trace width: 5 to 8 mil.
3. Don't route any other traces nearby or across the Ethernet signals' path.

The listed rules cover the routing requirements if an RJ-45 connector with a built-in transformer is used. If a separate transformer is used, additional rules should be followed for transformer-to-connector routing.

3.13. General Purpose Input / Output

The CM-iAM provides eight general purpose I/O pins (GPIO's) - seven of them are dedicated and one is shared with alternate functionality - with different power domain support. Seven additional GPIO's are available when option S (SIO) is assembled.

Always available GPIO's:

Baseboard conn		Type	Description	Remarks
Signal	Pin			
GPIO0	P2-16	I/O, 1.5mA	GPIO6 of the Poulsbo chipset	On-board 10k PU
GPIO1	P2-18	I/O, 1.5mA	GPIO1 of the Poulsbo chipset	On-board 10k PU
GPIO2	P2-28	I/O, 1.5mA	GPIO2 of the Poulsbo chipset	On-board 10k PU
GPIO5	P1-71	I/O, 1.5mA	GPIO8 of the Poulsbo chipset	On-board 10k PU Shared with CM-iAM ON Led.
GPIO6	P1-64	I/O, 1.5mA	GPIO9 of the Poulsbo chipset	On-board 10k PU
GPIO3	P2-30	I/O, 1.5mA SUS	GPIOSUS0 of the Poulsbo chipset	On-board 10k PU (SBY)
GPIO4	P1-69	I/O, 1.5mA SUS	GPIOSUS1 of the Poulsbo chipset	On-board 10k PU (SBY)
GPIO14	P1-126	I/O, 1.5mA SUS	GPIOSUS3 of the Poulsbo chipset	On-board 4.7k PU (SBY)

GPIO's available with options S (SIO) with rev 1.1:

Baseboard conn		Type	Description	Remarks
Signal	Pin			

GPIO7	P1-66	I/O, 16mA	GPIO10 on the IT8761 SIO	On-board 8.2k PU
GPIO8	P1-68	I/O, 16mA	GPIO11 on the IT8761 SIO	On-board 8.2k PU
GPIO9	P1-70	I/O, 5mA	GPIO12 on the IT8761 SIO	On-board 8.2k PU
GPIO10	P1-72	I/O, 8mA	GPIO13 on the IT8761 SIO	On-board 8.2k PU
GPIO11	P1-73	I/O, 8mA	GPIO15 on the IT8761 SIO	On-board 8.2k PU
GPIO12	P1-45	I/O, 24mA	GPIO16 on the IT8761 SIO	On-board 8.2k PU
GPIO13	P1-17	I/O, 8mA	GPIO20 on the IT8761 SIO	On-board 8.2k PU

GPIO's available with options S (SIO) with rev 1.1:

Baseboard conn		**Type**		**Description**	**Remarks**
Signal	**Pin**	1.1	1.2+		
GPIO7	P1-66	I/O, 16mA		GPIO10 on the IT8761 SIO	On-board 8.2k PU
GPIO8	P1-68	I/O, 16mA		GPIO11 on the IT8761 SIO	On-board 8.2k PU
GPIO9	P1-70	I/O, 5mA		GPIO12 on the IT8761 SIO	On-board 8.2k PU
GPIO10	P1-72	I/O, 8mA		GPIO13 on the IT8761 SIO	On-board 8.2k PU
GPIO11	P1-73	I/O, 8mA		GPIO15 on the IT8761 SIO	On-board 8.2k PU
GPIO12	P1-45	I/O, 24mA		GPIO16 on the IT8761 SIO	On-board 8.2k PU
GPIO13	P1-17	I/O, 8mA		GPIO20 on the IT8761 SIO	On-board 8.2k PU

GPIO's available with options S (SIO) with rev 1.2 and above :

Baseboard conn		**Type**	**Description**	**Remarks**
Signal	**Pin**			
GPIO7	P1-66	I/OD, 12mA	GPIO20 on the F71808 SIO	On-board 8.2k PU 5V
GPIO8	P1-68	I/OD, 12mA	GPIO21 on the F71808 SIO	On-board 8.2k PU 5V
GPIO9	P1-70	I/OD, 12mA	GPIO22 on the F71808 SIO	On-board 8.2k PU 5V
GPIO10	P1-72	I/OD, 12mA	GPIO23 on the F71808 SIO	On-board 8.2k PU 5V
GPIO11	P1-73	I/OD, 12mA	GPIO24 on the F71808 SIO	On-board 8.2k PU 5V
GPIO12	P1-45	I/OD, 12mA	GPIO25 on the F71808 SIO	On-board 8.2k PU 5V
GPIO13	P1-17	I/OD, 12mA	GPIO10 on the F71808 SIO	On-board 8.2k PU 5V
. All GPIO's are configurable as input/output or open drain output				

3.14. Hardware Monitor (rev. 1.2 and above)

The CM-iAM SIO (rev. 1.2 and above) has incorporated hardware monitor using 8-bit ADC with 8mv LSB, limiting the maximum input voltage of the analog pin to 2.048V .Voltages higher than 2.048V should be reduced by a factor with external resistors.

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
SIO_VIN	P2-42	AIN	VIN4 on the F71808 SIO

Also two analog input pins have internal connections to on-board voltages:

SIO Pin Name[#]	**Type**	**Description**
VIN3[45]	AIN	Connected to VMEM
Vcore[47]	AIN	Connected to VCC CPU

3.15. Watchdog

The CM-iAM implements a watchdog timer using an 8-bit count-down timer clocked by 1Hz. The watchdog generates a system-reset event when the counter reaches zero.
Using the watchdog requires an appropriate driver to be installed before enabling a watchdog in BIOS. To enable or disable the watchdog, enter BIOS Setup (F2), go to the "Advanced" menu and change the "Watchdog Timer" option to On/Off as desired. Once the "Watchdog Timer" option is enabled, the timeout can be set to 31-255 seconds. Entering setup temporarily disables watchdog operation regardless of its current state. A driver and demo for watchdog operation is provided in O/S packages.

3.16. Real-Time Clock

The Real Time Clock (RTC) module provides a date and time keeping device with battery backup. Three interrupt features are available: time of day alarm with a once a second to once a month range, periodic rates of 122 - 500 ms and end of update cycle notification. Seconds, minutes, hours, days, day of week, month and year are counted. The hour is represented in either twelve or twenty-four hour format and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768-kHz oscillating source, which is divided to achieve an update every second.

- Counting of seconds, minutes and hours of the day
- Counting of days of the week, date, month, and year
- 12–24 hour clock with am and pm indication in 12-hour mode
- Two banks of 128 byte each (general and extended)
- Configurable alarms

The RTC uses a dedicated lithium battery backup when the rest of the card is completely powered down (RTC-only mode). The RTC can continue operating even when the rest of the card is not powered. The battery should be connected to the VCC_RTC (V_{BAT}) input of the CM-iAM's interface connector. Typical input current is ~ 6μA

3.17. SMBus (I2C)

The CM-iAM provides a host system management bus interface. This interface is compatible with I2C devices.

Baseboard conn		Type	Comment
Signal	Pin		
SMB_CLK	P2-21	I/O	SMBus clock(2.2k internal PU)
SMB_DAT	P2-23	I/O	SMBus data (2.2k internal PU)
SMB_ALRT	P2-24	I	SMBus Alert: This signal can be used to generate an SMI#.(10k internal PU)

3.18. Clocks, Timers, Reset, Write Protect, Boot, Power Management

Baseboard conn		Type	Comment
Signal	Pin		
RSTIN#	P2-33	I	Reset input, active low. Low level on this pin initiates hardware reset of CM-iAM. This pin is not mandatory for CM-iAM operation as it generates power-on reset using on-board circuitry. It has an internal pull-up and can be left unconnected.
RESET#	P2-20	O 24mA	Reset output, active low. Indicates when CM-iAM undergoes a hardware reset, due to powerup or RESET-IN. Can be used as a reset signal to off-board hardware.
NAND_WP#	P2-29	I	NAND flash write protect, active low. NAND flash writes will be disabled if pulled to logical 0. To enable NAND flash writes pull this input to 1 or leave unconnected. This input has internal pull-up.
TIMER-SPKR	P2-22	O	Speaker: The TIMER-SPKR signal is the output of counter 2 and is internally ANDed with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon SLPMODE, its output state is 0.
PWRBTN#	P2-35	I	Power button/sleep functionality- active low
SUSP_S3	P1-15	O	Suspend mode external device power disable/enable – used in power sequence mechanism
FWH_INIT#	P2-85	O	External FWH init signal. Should be left unconnected if not used
DEBUG0	P1-116	I	Used for first-time factory programming. Should be left unconnected. Irrelevant for any other purpose.
DEBUG1	P1-118	I	
DEBUG2	P1-120	I	

DEBUG3	P2-36	I	
DEBUG4	P2-40	O	

SPARE4*	P2-42	Reserved pins. Must be left unconnected.
SPARE5	P2-44	
SPARE6	P2-48	
SPARE7	P2-50	

* for rev 1.1 only , rev 1.2 and above definition has been changed .

3.19. Power Supply Pins

The CM-iAM requires only 5V for operation. Other supply voltages required for the CPU, DDR and peripherals are generated on-board.

Power Net Description

Signal	Description
GND	Common ground
VCC_SBY	Main 5V stand-by power source. All other stand-by voltages are derived from this source (also used for DDR supply).
VCC	Main 5V power supply. All other voltages are derived from this source,
VCC-RTC	The 3.3V supply pin provides power to the internal real-time clock and on-board static / configuration RAM. This pin can be driven independently of all other power pins. This pin enables the connection of an external lithium battery.

Power Supply Pins

GND	P1-110	P2-98
	P1-134	P2-122
	P1-38	P2-26
	P1-62	P2-134
	P1-122	P2-62
	P1-26	P2-74
	P1-14	P2-7
	P1-8	P2-14
	P1-50	P2-38
	P1-98	P2-8
	P1-86	P2-110
	P1-74	P2-86
	-	P2-52
VCC_SBY	P1-140	P2-97
	P1-80	P2-116
VCC	P1-67	P2-115
	P1-103	P2-103

	P1-79	P2-31
	P1-19	P2-135
	P1-55	P2-55
	P1-43	P2-91
	P1-7	P2-127
	P1-31	P2-19
	P1-127	P2-79
	P1-115	P2-67
	P1-91	P2-43
	P1-139	-
VCC-RTC	P1-37	

3.20. Recommended power sequence

The CM-iAM has an automatic power button function that turns on the device immediately after the insertion of power and readiness of internal circuits.

The power-up sequence should be as follows:

1. Apply VCC5SBY
2. Wait for SUSP_S3 (P1-15, PM_EN_5VS# on the SB-iAM) low to enable VCC5 rail.

The power down/standby sequence:

1. SUSP_S3# high will disable VCC5 rail
2. Shut down VCC5SBY (or leave it connected and use PWRBTN# signal for next power up).

VCCRTC should always be connected for proper RTC operation.

4. Interface Connectors

4.1. Connector Type

The CM-iAM connects to the external world through P1, P2 - 140-pin, 0.6 mm connectors.

Conn	Mfg.	CM-iAM Connector P/N	Mating Connector P/N
P1, P2	AMP	8-5353183-0	8-5353189-0

4.2. Standoffs

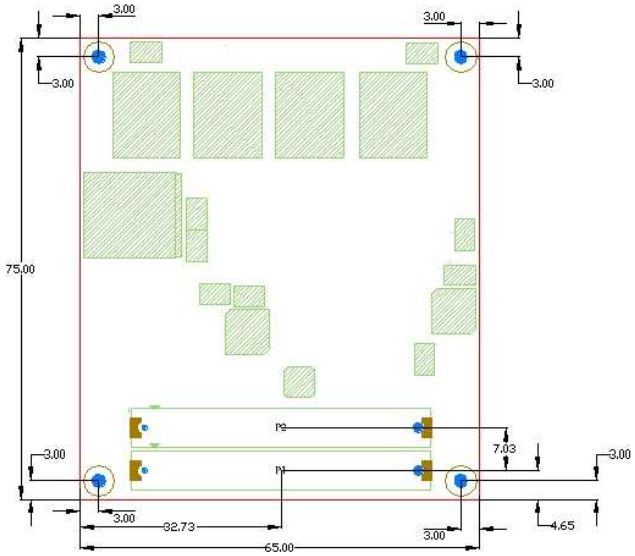
The CM-iAM has four mounting holes for standoffs. All of them are connected to GND. Refer to mechanical drawing of module with baseboard interface connectors. The developer is advised to connect mating holes of the baseboard to GND, in order to improve the EMC.

The standoff is implemented by three parts: a screw, spacer and nut.

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	FCI 95121-005 Acton InoxPro BF22102010 World Bridge Machinery 380J52080
Spacer	M2x.4 thread, 4.2 mm length	Hirosugi ASU-2004 MAC8 2SP-4 World Bridge Machinery M2, L=4.2mm
Nut	M2, 1.6-2.0mm width	FCI 92869-001 (or 002) Acton InoxPro BG12102000 Bossard 1241397 (DIN934-A2 M2) World Bridge Machinery 381A52000

Mating connectors and standoffs are available from manufacturer representatives or from CompuLab, see [prices] >> [accessories] in CompuLab's website.

4.3. Connectors Layout



Bottom side image, viewed from the top side of the module

Board-to-board mating height is 4 mm
Hatched green areas indicate height constraints - don't locate components beneath.

Connectors' and mechanical layout is available in DXF format from CompuLab's website, following [http://www.compulab.co.il/iam/html/iam-developer.py - Dimensions and Connector Location links.

4.4. Connectors Pinout

Note: gray-colored signals are not available. They are either not implemented or routed through other pins of the connector (i.e., mixed with another function). Grayed signals are displayed in order to clarify standard baseboard interface pin assignment.

	P1-A
P1-02	MDI1_0+
P1-04	MDI1_0-
P1-06	ETH_LED1_0#
P1-08	**GND**
P1-10	MDI1_2+
P1-12	MDI1_2-
P1-14	**GND**
P1-16	NC
P1-18	SPDIF_OUT
P1-20	HDA_SDIN1
P1-22	SENSE_A
P1-24	MIC_IN_R
P1-26	**GND**
P1-28	SDVO_BCLK-
P1-30	SDVO_BCLK+
P1-32	SDVO_CTRL_DAT
P1-34	SDVO_INT-
P1-36	SDVO_INT+
P1-38	**GND**
P1-40	SDVO_RED-
P1-42	SDVO_RED+
P1-44	MASTER/SLAVE
P1-46	SENSE_B
P1-48	LVDS_BLT_CTR
P1-50	**GND**
P1-52	LVDS_A0-
P1-54	LVDS_A0+
P1-56	LVDS_BLEN
P1-58	LVDS_A2-
P1-60	LVDS_A2+
P1-62	**GND**
P1-64	GPIO6

	P1-B
P1-01	MDI1_1+
P1-03	MDI1_1-
P1-05	ETH_LED1_1#
P1-07	**VCC5**
P1-09	MDI1_3+
P1-11	MDI1_3-
P1-13	ETH_LED1_2#
P1-15	SUS_S3
P1-17	GPIO13
P1-19	**VCC5**
P1-21	SDVO_TVCLKIN-
P1-23	SDVO_TVCLKIN+
P1-25	SDVO_CTRL_CLK
P1-27	SDVO_GREEN-
P1-29	SDVO_GREEN+
P1-31	**VCC5**
P1-33	SDVO_BLUE-
P1-35	SDVO_BLUE+
P1-37	VCC_RTC
P1-39	SDVO_FLDSTALL-
P1-41	SDVO_FLDSTALL+
P1-43	**VCC5**
P1-45	GPIO12
P1-47	LVDS_DID_CLK
P1-49	LVDS_DID_DAT
P1-51	LVDS_A1-
P1-53	LVDS_A1+
P1-55	**VCC5**
P1-57	LVDS_A3-
P1-59	LVDS_A3+
P1-61	LVDS_PPEN
P1-63	LVDS_CLK-

	P1-A
P1-66	GPIO7
P1-68	GPIO8
P1-70	GPIO9
P1-72	GPIO10
P1-74	**GND**
P1-76	LCD_R1
P1-78	LCD_R3
P1-80	**VCC_SBY**
P1-82	LCD_R5
P1-84	LCD_R7
P1-86	**GND**
P1-88	LCD_G2
P1-90	LCD_G4
P1-92	LCD_G5
P1-94	LCD_G7
P1-96	LCD_B1
P1-98	**GND**
P1-100	LCD_B4
P1-102	LCD_B6
P1-104	LCD_B7
P1-106	LCD_PWREN
P1-108	LCD_CLK
P1-110	**GND**
P1-112	NC
P1-114	NC
P1-116	DEBUG0
P1-118	DEBUG1
P1-120	DEBUG2
P1-122	**GND**
P1-124	COM1_RI#
P1-126	GPIO14
P1-128	USB_OC0_1#
P1-130	USB0-
P1-132	USB0+
P1-134	**GND**
P1-136	USB1-
P1-138	USB1+
P1-140	**VCC_SBY**

	P1-B
P1-65	LVDS_CLK+
P1-67	**VCC5**
P1-69	GPIO4
P1-71	GPIO5
P1-73	GPIO11
P1-75	LCD_R0
P1-77	LCD_R2
P1-79	**VCC5**
P1-81	LCD_R4
P1-83	LCD_R6
P1-85	LCD_G0
P1-87	LCD_G1
P1-89	LCD_G3
P1-91	**VCC5**
P1-93	LCD_G6
P1-95	LCD_B0
P1-97	LCD_B2
P1-99	LCD_B3
P1-101	LCD_B5
P1-103	**VCC5**
P1-105	LCD_DE
P1-107	LCD_VSYNC
P1-109	LCD_HSYNC
P1-111	COM1_DSR#
P1-113	COM1_DCD#
P1-115	**VCC5**
P1-117	COM1_RX
P1-119	COM1_TX
P1-121	COM1_RTS#
P1-123	COM1_CTS#
P1-125	COM1_DTR#
P1-127	**VCC5**
P1-129	USB2-
P1-131	USB2+
P1-133	USB_OC2_3#
P1-135	USB3-
P1-137	USB3+
P1-139	**VCC5**

	P2-A
P2-02	MDI2_0+
P2-04	MDI2_0-
P2-06	ETH_LED2_0#
P2-08	**GND**
P2-10	MDI2_2+
P2-12	MDI2_2-
P2-14	**GND**
P2-16	GPIO0
P2-18	GPIO1
P2-20	RESET#
P2-22	TIMER_SPKR
P2-24	SMB_ALRT
P2-26	**GND**
P2-28	GPIO2
P2-30	GPIO3
P2-32	SDC_WP
P2-34	SDC_PWEN#
P2-36	DEBUG3
P2-38	**GND**
P2-40	DEBUG4
P2-42	SPARE4 **/(SIO_VIN)**
P2-44	SPARE5
P2-46	NC
P2-48	SPARE6
P2-50	SPARE7
P2-52	**GND**
P2-54	SDA_D0
P2-56	SDA_D1
P2-58	SDA_D2
P2-60	SDA_D3
P2-62	**GND**
P2-64	NC
P2-66	NC
P2-68	NC

	P2-B
P2-01	MDI2_1+
P2-03	MDI2_1-
P2-05	ETH_LED2_1#
P2-07	**GND**
P2-09	MDI2_3+
P2-11	MDI2_3-
P2-13	ETH_LED2_2#
P2-15	PCIE_CLK1E#
P2-17	PCIE_CLK0E#
P2-19	**VCC5**
P2-21	SMB_CLK
P2-23	SMB_DAT
P2-25	NC
P2-27	NC
P2-29	NAND_WP#
P2-31	**VCC5**
P2-33	RSTIN#
P2-35	PWRBTN#
P2-37	SDC_D0
P2-39	SDC_D1
P2-41	SDC_D2
P2-43	**VCC5**
P2-45	SDC_D3
P2-47	SDC_CD#
P2-49	SDC_CLK
P2-51	SDC_CMD
P2-53	SDC_LED
P2-55	**VCC5**
P2-57	SDB_WP
P2-59	NC
P2-61	NC
P2-63	NC
P2-65	NC
P2-67	**VCC5**

	P2-A
P2-70	NC
P2-72	SDA_CD#
P2-74	**GND**
P2-76	SDA_CLK
P2-78	SDA_CMD
P2-80	SDA_LED
P2-82	SDA_WP
P2-84	SDA_PWEN#
P2-86	**GND**
P2-88	LPC_CLK
P2-90	LPC_AD0
P2-92	LPC_AD1
P2-94	LPC_AD2
P2-96	LPC_AD3
P2-98	**GND**
P2-100	NC
P2-102	NC
P2-104	PCIE_RST#
P2-106	PCIE0_RX-
P2-108	PCIE0_RX+
P2-110	**GND**
P2-112	PCIE0_TX-
P2-114	PCIE0_TX+
P2-116	**VCC_SBY**
P2-118	SATA0_RX-
P2-120	SATA0_RX+
P2-122	**GND**
P2-124	SATA0_TX-
P2-126	SATA0_TX+
P2-128	SATA_LED
P2-130	USB4-
P2-132	USB4+
P2-134	**GND**
P2-136	USB_OC4_5#
P2-138	USB5-
P2-140	USB5+

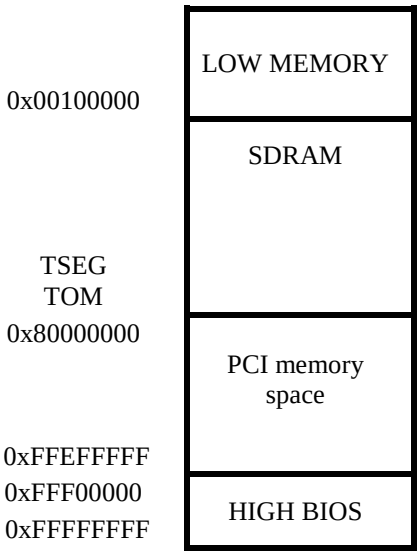
	P2-B
P2-69	NC
P2-71	NC
P2-73	NC
P2-75	NC
P2-77	SDB_LED
P2-79	**VCC5**
P2-81	PCIE_CLK1-
P2-83	PCIE_CLK1+
P2-85	FWH_INIT#
P2-87	LPC_FRM#
P2-89	LPC_SERIRQ
P2-91	**VCC5**
P2-93	NC
P2-95	NC
P2-97	**VCC_SBY**
P2-99	PCIE_CLK0-
P2-101	PCIE_CLK0+
P2-103	**VCC5**
P2-105	PCIE1_RX-
P2-107	PCIE1_RX+
P2-109	PCI_WAKE#
P2-111	PCIE1_TX-
P2-113	PCIE1_TX+
P2-115	**VCC5**
P2-117	HDA_SDIN0
P2-119	HDA_BCLK
P2-121	HDA_RST#
P2-123	HDA_SDO
P2-125	HDA_SYNC
P2-127	**VCC5**
P2-129	MIC_IN_L
P2-131	AIN_R
P2-133	AIN_L
P2-135	**VCC5**
P2-137	AOUT_R
P2-139	AOUT_L

5. MEMORY and I/O mapping

5.1. Memory space usage in the first 1MB

0000:0 - 9FFF:F	Standard Low memory
A000:0 - BFFF:F	Graphic Memory Will be forwarded to PCIE if graphic disabled
C000:0 - DFFF:F	VGA BIOS expansion area
E000:0 - FFFF:F	BIOS

5.2. Memory space usage above first 1MB



TSEG is a 1-MB, 2-MB or 8-MB memory region located below Intel Graphics Media Adapter stolen memory, which is at the top of physical memory (TOM). It is used for System Management Mode accesses by the processor.

5.3. I/O Space Usage

The table below specifies all I/O regions known to be used in standard / legacy PC architecture and regions used by on-board peripheral devices under WinXP.

Address	Function
0x000-0x00F	Slave DMA regs
0x020-0x021	PIC registers
0x024-0x025	PIC registers
0x028-0x029	PIC registers
0x02C-0x02D	PIC registers
0x030-0x031	PIC registers
0x034-0x035	PIC registers
0x038-0x039	PIC registers
0x03C-0x03D	PIC registers
0x040-0x043	System timer
0x062-0x062	Embedded controller
0x066-0x066	Embedded controller
0x070-0x077	System CMOS/real time clock
0x081-0x091	DMA controller registers
0x093-0x09F	DMA controller registers
0x0A0-0x0A1	PIC registers
0x0A4-0x0A5	PIC registers
0x0A8-0x0A9	PIC registers
0x0AC-0x0AD	PIC registers
0x0B0-0x0B1	PIC registers
0x0B4-0x0B5	PIC registers
0x0B8-0x0B9	PIC registers
0x0BC-0x0BD	PIC registers
0x0C0-0x0DF	DMA controller registers
0x0F0-0x0F0	Numeric Data Processor
0x1F0-0x1F7	Primary IDE0 controller
0x3B0-0x3BB	Intel Graphic
0x3C0-0x3DF	Intel Graphic
0x3F6-0x3F6	Primary IDE0 controller alternate
0x3F8-0x3FF	COM1
0x4D0-0x4D1	PIC registers
0xCF8-0xCFF	PCI configuration space
0x1800-0x1807	Intel Graphic
0x1810-0x181F	PCI IDE contrtoller
0x1820-0x183F	USB1 UHCI port 0 [0..1]
0x1840-0x185F	USB1 UHCI port 1 [2..3]
0x1860-0x187F	USB1 UHCI port 2 [4..5]
0x2000-0x2FFF	Realtek Gigabit Ethernet #1
0x3000-0x3FFF	Realtek Gigabit Ethernet #2

5.4. BIOS Flash Mapping

Valid for BIOS versions after 01.12.2009

Starting address in flash window	End address in flash window	Usage
0xFFF00000	0xFFFCFFFF	BIOS area
0xFFF90000	0xFFF97FFF	Setup configuration block & APCC
0xFFF98000	0xFFFFFFFF	BIOS area

Setup and Configuration Block Usage

Addresses	Value / Description
0x0000-0x0001	0xAAAA –signature that a valid CMOS image is in the flash
0x0002-0x01FF	CMOS image, including RTC
0x1000-0x1FFF	Etherlink parameters space
0x2000-0x5FFF	APCC space
0x6000-0x7FFF	Reserved space

5.5. PCI Resource Map

PCI Interrupt Mapping.

The CM-iAM supports an advanced programmable interrupt controller (APIC) for a PCI device in addition to a standard cascaded 8259 controller. All PCI devices are mapped through eight configurable APIC PIRQx (A-H) mapped to IOAPIC IRQ16-23

PCI Device	Vend.	Dev.	BUS	DEV.	FUNC	APIC IRQ
CPU/Bridge	8086	8100	0	0	0	-
Graphic (IGD)	8086	8108	0	2	0	PIRQA
High Definition Audio	8086	811b	0	27(1B)	0	PIRQG
PCIE port 1	8086	8110	0	28(1C)	0	PIRQB
PCIE port 2	8086	8112	0	28(1C)	1	PIRQA
USB[0..1] UHCI port 1	8086	8114	0	29(1D)	0	PIRQH
USB[2..3] UHCI port 2	8086	8115	0	29(1D)	1	PIRQD
USB[4..5] UHCI port 3	8086	8116	0	29(1D)	2	PIRQC
USB 2.0 EHCI [0..5]	8086	8117	0	29(1D)	7	PIRQF
SDIO 0	8086	811c	0	30(1E)	0	PIRQG
SDIO 1	8086	811d	0	30(1E)	1	PIRQE
SDIO 2	8086	811e	0	30(1E)	2	PIRQC
LPC	8086	8119	0	31(1F)	0	-
ATA/IDE controller	8086	811A	0	31(1F)	1	-
Gigabit Ether. Contr #1	10EC	8168	2	0	0	PIRQA
PCIE-PCIE bridge root	12D8	0303	3	0	0	-
PCIE-PCIE bridge port 1	12D8	0303	4	1	0	-
PCIE-PCIE bridge port 2	12D8	0303	4	2	0	-
Gigabit Ether. Contr #2	10EC	8168	5	0	0	PIRQC

PIRQx can also be mapped to the standard 8259 PIC through D31:F0:R60-67[A..H].

The table below shows an map example for the above configuration:

PIRQx	IRQ map
PIRQA	7
PIRQB	11
PIRQC	3
PIRQD	5
PIRQE	10
PIRQF	11
PIRQG	4
PIRQH	10

5.6. Interrupt Channel Mapping

IRQ	I/O Device	Priority	On-board usage
IRQ0	HPET	P1	always
IRQ1	SERIRQ	P2	-
IRQ2	Slave controller cascading	—	always
IRQ3	SERIRQ, PIRQx	P4	-
IRQ4	COM1 , SERIRQ, PIRQx	P12	-
IRQ5	SERIRQ, PIRQx	P5	-
IRQ6	SERIRQ, PIRQx	P8	-
IRQ7	SERIRQ, PIRQx	P9	-
IRQ8	Real-time clock	P3	always
IRQ9	ACPI	P6	always
IRQ10	SERIRQ, PIRQx	P7	-
IRQ11	SERIRQ, PIRQx	P10	-
IRQ12	SERIRQ, PIRQx	P13	-
IRQ13	Math coprocessor	P8	always
IRQ14	IDEIRQ, SERIRQ, PIRQx	P14	-
IRQ15	PIRQx	P11	-

If IRQ is used by an on-board device, disabling the device will free the IRQ. If the on-board device cannot be disabled, than the IRQ is *always* assigned for on-board usage and is therefore marked so in the table above. PCI interrupts (PIRQx) support interrupt sharing, therefore, the same interrupt may be used by several devices (see **PCI resource map**).

6. Power Consumption

The current consumption measurements specified below were performed on a system with the following configuration:

- CM-iAM-D1G-C1600-N4G-L-E2-S-A-Y (CONFIG1)
- CM-iAM-D1G-C1100-N1G-L-E1-S-A-Y (CONFIG2)
- SB-iAM-M-P-A

The configuration also includes a USB mouse and USB keyboard powered from 5VSBY.
Current consumption is specified for both boards; however, 90% of the total current is consumed by the CM-iAM module. Max load was simulated using the SiSoft Sandra Burn-in Test.

CPU Speed	Activity	Current 5V	Current 5VSBY
1600 MHz CONFIG1	Standby	~0(1.8mA)	0.14A
	Average	0.8A	0.33A
	Max load	1.34A	0.59A
1100 CONFIG2	Standby	~0(1.5mA)	0.09A
	Average	0.59A	0.25A
	Max load	1.11A	0.41A

Average power consumption

- Average
- CPU clock - 1600 MHz (CONFIG1)/1100MHz(CONFIG2)

[5V * (0.59A+0.25A)]*0.9(90%) = 3.8 watt (CONFIG2)
[5V * (0.8A+0.33A)] *0.9(90%) = 5 watt(CONFIG1)

Maximum power consumption

- CPU clock - 1600 MHz (CONFIG1)/1100MHz(CONFIG2)
- Max load

[5V * (1.11A+0.41A)]*0.9(90%) = 6.9 watt(CONFIG2)
[5V * (1.34A+0.59A)] *0.9(90%) = 8.7 watt(CONFIG1)

Standby power consumption

[5V * 0.09A] *0.9(90%)= 0.41 watt (CONFIG2)

[5V * 0.14A] *0.9(90%)= 0.63 watt (CONFIG1)

7. Performance Benchmarks

Measured with CPU @ 1600 MHz, using SiSoft Sandra bench test under Windows.

Drystone (integer)	5152 MIPS
Whetstone (floating point)	1770 MFLOPS
Whetstone (iSSE2)	2337 MFLOPS
DDR bandwidth	2904 MB/s

8. Operating Temperature Ranges

The CM-iAM is available with three options of operating temperature range:

Range	Temp.	Description
Commercial	0^o to 70^o C	Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20^o to 70^o C	Every card is individually tested for the lower limit (-20^o C) qualification.
Industrial	-40^o to 85^o C	Every card is individually tested for both lower and upper limits and at several midpoints.

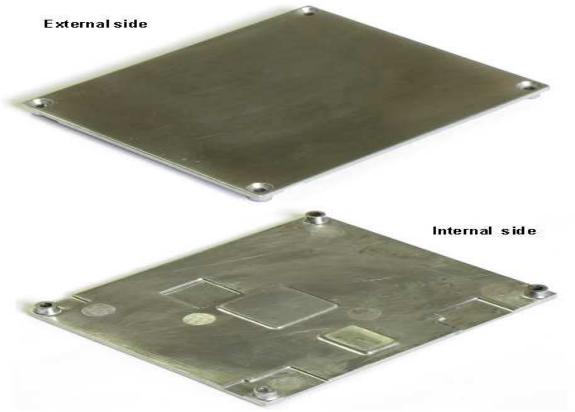
* Temp - maximum temperature measured on hottest spot of heatsink.

For more information regarding the availability of a specific card configuration for Industrial grade, please refer to [Products] >> [Industrial Temperature] links in CompuLab's web-site.

9. Heat Dissipation

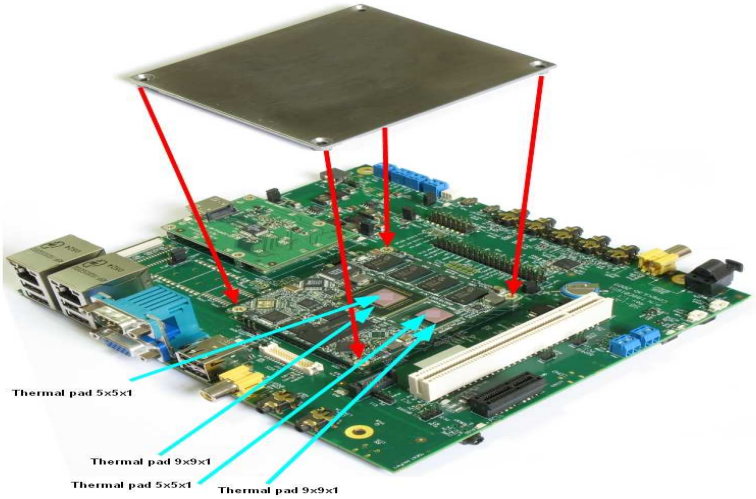
During a regular usage the CM-iAM doesn't require a heatsink for Tamb <25C. In still air, the CPU temperature can rise up to 30-35°C above ambient. For example, at a room temperature of 25°C, a powered card will reach 55-60°C.

The CM-iAM should be cooled by airflow or heat extruders. Any indirect airflow to the board will help to reduce its temperature. For Tamb >25C Compulab provides custom heat-plate (shown below) that can be ordered separately:



9.1. Heat-plate assembly instructions

1. Put 9x9x1 thermal pad & 5x5x1 thermal pad on the Poulsbo chipset
2. Put 9x9x1 thermal pad & 5x5x1 thermal pad on the Atom CPU
3. Ensure heat-plate orientation as shown below:



4.Attach the heat-plate to the CM-iAM and screw up with 4 M2x8mm
5. Final assembly will have look as below: