CompuLab

# CM-iGLX
# Computer-On-Module

# Reference Guide

# Table of Contents

# 1. Revision Notes

| Date | Description |
|---|---|
| 30-Jun-2006 | ▪ Preliminary release |
| 27-Nov-2006 | ▪ Audio sampling rate errata published |
| 06-May-2007 | ▪ UCB1400 (audio codec) reference replaced by WM9715L, as design change. Functionality remains the same.<br>▪ Made clarifications about SMbus signals. |
| 27-Nov-2007 | ▪ Added Power sequence notes |
| 26-Dec-2007 | ▪ Published WiFi specifications in datasheet section |
| 05-Aug-2008 | ▪ Updated DDR maximum size to 512 MB<br>▪ Added WiFi interface section<br>▪ Updated CAMI connector description |
| 11-Oct-2008 | ▪ P3-113 pin was removed from the VCC3_SBY supply pins |
| 11-Feb-2009 | ▪ Baseboard design and troubleshooting sections added |
| 02-Jun-2009 | ▪ Provided guidelines for VCC3STBY peak power design |

Please check for a newer revision of this manual in CompuLab's website - http://www.compulab.co.il, following [Developer] >> [iGLX] links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

# 2. Overview

## 2.1. Highlights

- **Full Featured PC-Compatible Computer-On-Module**
- **AMD Geode LX800 CPU at 500 MHz, 256 KB cache**
- **512 Mbyte DDR**
- **512 Mbyte Flash Disk**
- **Graphics Controller for LCD and FPM, up to 1920 x 1440**
- **General purpose bus and optional PCI, LPC, AC97 busses**
- **WLAN / WiFi 802.11g Interface**
- **Video Input Port**
- **Sound codec with speaker and microphone support**
- **Touchscreen Controller**
- **Up to 3 host USB-2 ports, including keyboard and mouse support**
- **Serial ports, GPIO, hard-disk interface**
- **100 Mbps Ethernet port**
- **Low power consumption**
- **Small size - 68 x 58 mm**
- **Interchangeable with other modules via CAMI connectors**

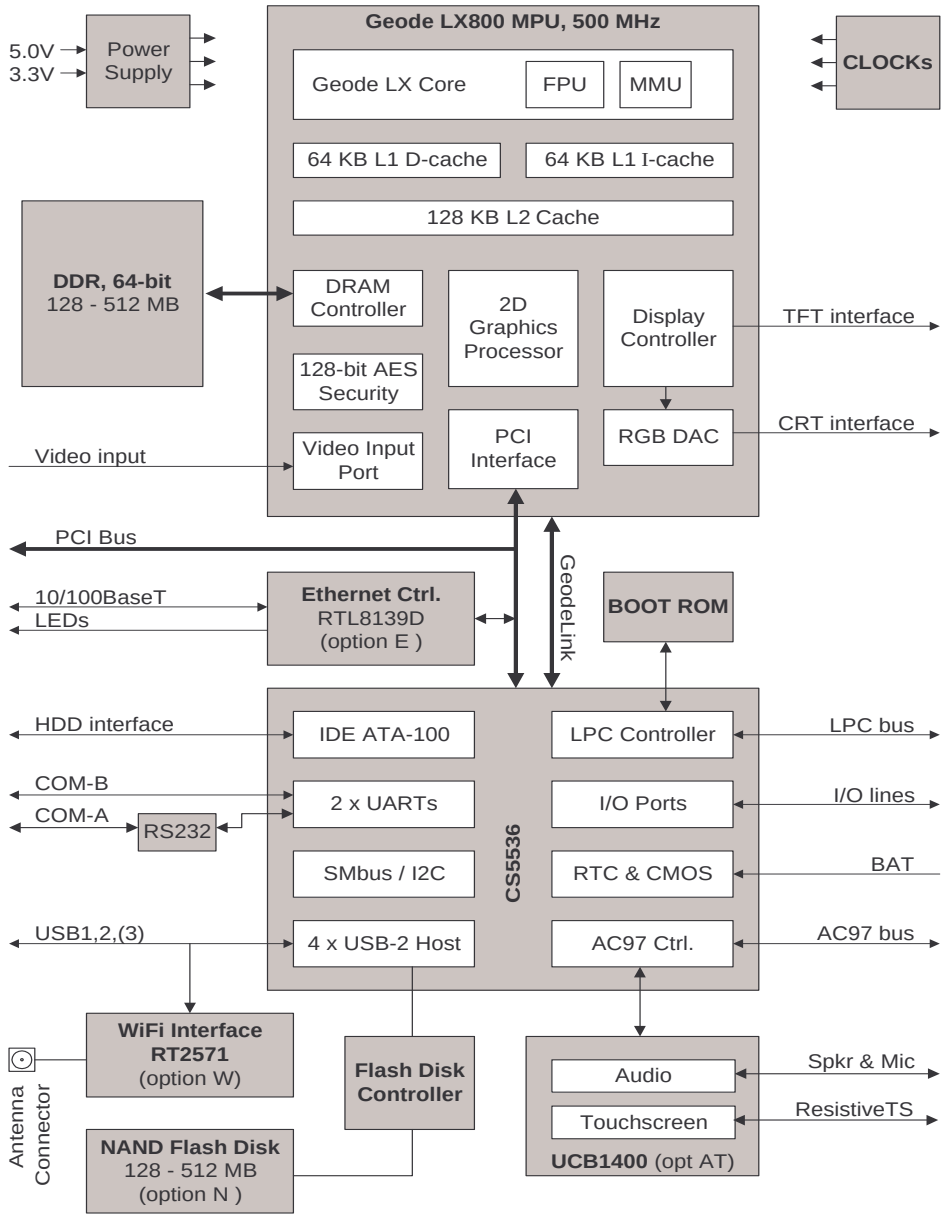
*Note: Some features are optional. Values are specified at their maximum.*

**The CM-iGLX** packs up-to-date technologies into the most compact, lightweight PC-on-module available in the market. Its on-board resources suffice to smoothly run operating systems such as Linux and Windows XP / CE, while it is just as small as a credit card and can run on a battery. These, in addition to the module's low cost, make it an ideal building block for any embedded application.

The feature set of the CM-iGLX combines a 32-bit X86-compatible CPU, DDR, Flash Disk and vital computing peripherals. For embedded applications, the CM-iGLX provides a 32-bit PCI bus, 100Mbit Ethernet, serial ports, general purpose I/O lines and many other essential functions. The user interface is supported by an enhanced graphics controller, touchscreen, USB interface for keyboard / mouse and Audio system. An integrated WLAN (WiFi) interface implements 802.11g industry standard wireless connectivity.

The standardized CAMI ("CompuLab's Aggregated Module Interface") connectors of the CM-iGLX module allow interchangeability with other Computer-On-Module's available from CompuLab, enabling the flexibility required in a dynamic market where application requirements can change rapidly.

## 2.2. Block Diagram



## 2.3. Features

The "Option" column specifies the P/N code required to have the particular feature.
"+" indicates that the feature is always available.

### CPU, Memory and Busses

| Feature | Specifications | Option |
|---|---|---|
| CPU | AMD LX800 / LX700 CPU, Pentium compatible, up to 500 MHz.<br>64 + 64 KB L1 and 128 KB L2 cache.<br>DMA and Interrupt controllers, Timers | C |
| DRAM | 128 / 256 / 512 MB DDR, 333 MHz, 64-bit<br>Note: 512 MB – only if WiFi is not assembled | D |
| BIOS Flash | 1/2 Mbyte, on-board reprogrammable | + |
| NAND Flash Disk | 128 / 512 MB, more in future. 10 MB/s transfer rate. | N |
| External Busses | PCI, LPC, AC97 | + |
| AC97 | AC97 Rev 2.3 compliant | + |
| PCI bus | 32-bit, rev 2.2-compliant, 132 MB/s, 3.3-volt tolerant<br>Arbiter and clock for one or two masters | + |
| LPC bus | Host, 33 MHz, Intel LPC v1.0 compatible | + |

### Peripherals

| Feature | Specifications | Option |
|---|---|---|
| Graphics Controller | Resolution up to 1920 x 1440 x 32 bpp @ 85Hz, frame buffer in system memory, 2D graphic processor | + |
| Display Interface | LCD - 18-bit parallel RGB for TFT panels<br>CRT - 24-bit analog RGB for CRT / FPM | +<br>+ |
| Video Input Port | VESA1.1 & VESA2.0 standard, BT.601, BT.656, 8-bit port, 150 MHz data rate | + |
| USB | Three Host USB 2.0 ports, 480 Mbps, EHCI / OHCI compliant | + |
| Serial Ports | Two UART's, Rx & Tx only | + |
| GPIO | 4 lines dedicated + 4 lines shared | + |
| Hard Disk Interf. | IDE interface, UDMA ATA-100 mode | + |
| Kbrd & Mouse | USB or redirection from serial port | + |
| Ethernet | 100 Mb/s, Activity LED's. RTL8139 | E |
| Audio codec | Wolfson WM9715L controller, AC97 interface, mono microphone input, stereo line input and 25 mW output for active speakers | AT |
| Touchscreen ctrl. | A part of the WM9715L chip. Supports resistive touch panels | AT |
| RTC | Real Time Clock, powered by external lithium battery | + |
| WiFi | Ralink RT2571chipset, 802.11b/g, USB internal interface<br>Mutually exclusive with 512 MB DDR option | W |
| Encryption unit | 128 bit DMA based crypto acceleration block up to 44 Mbps | + |

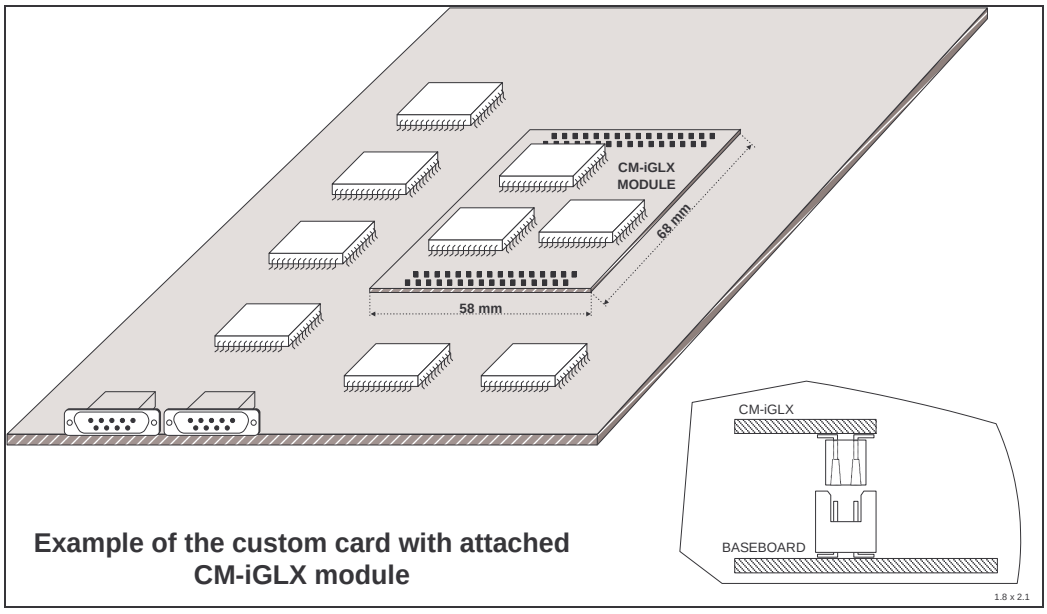
### Electrical, Mechanical and Environmental Specifications

| | |
|---|---|
| Supply Voltage | 3.3V |
| Power consumption | 3 - 5 W, depending on configuration and CPU speed |
| Dimensions | 68 x 58 x 8 mm |
| Weight | 37 gram |

| | |
|---|---|
| MTBF | > 100,000 hours |
| Operation temperature (case) | Commercial : 0° to 70° C<br>Extended : -20° to 70° C<br>Industrial : -40° to 85° C |
| Storage temperature | -40° to 85° C |
| Relative humidity | 10% to 90% (operation)<br>05% to 95% (storage) |
| Shock | 50G / 20 ms |
| Vibration | 20G / 0 - 600 Hz |
| Connectors | 3 x 140 pin, 0.6 mm. Insertion / removal up to 50 cycles |

## 2.4. General Description

The CM-iGLX is a miniature, single-board computer packed as a module. It contains a CPU, chipset, memory, flash disk and peripherals. All interface functions of the CM-iGLX are routed through miniature high-density connectors, designed for piggyback attachment to a custom baseboard, as shown in the picture below.




**Example of the custom card with attached CM-iGLX module**

## 2.5. AMD "LX" CPU Core Architecture

The x86 CPU core consists of an Integer Unit, cache memory subsystem, and Floating Point Unit. The Integer Unit contains the instruction pipeline and associated logic. The memory subsystem contains the instruction and data caches, translation look-aside buffers (TLBs), and an interface to the GeodeLink Interface Units (GLIUs).

The instruction set supported by the core is a combination of Intel's Pentium, the AMD-K6 microprocessor and the Athlon FPU, and the AMD Geode LX processor specific instructions. Specifically, it supports the Pentium, Pentium Pro, 3DNow technology for the AMD-K6 and Athlon processors, and MMX instructions for the Athlon processor. It supports a subset of the specialized Geode LX processor instructions including special SMM instructions. The CPU Core does not support the entire Katmai New Instruction (KNI) set as implemented in the Pentium 3. It does support the MMX instructions for the Athlon processor, which are a subset of the Pentium 3 KNI instructions.

AMD LX processor architecture is relatively simple: instructions are issued, executed and retired in order, one instruction issued per clock. On the other hand, the design is highly optimized to achieve high performance in the targeted environment. Some of the significant features providing this performance are:

**Large on-chip caches and TLB's:**

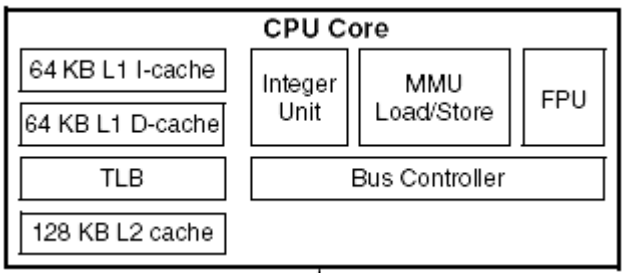
The AMD "LX" CPU implements large caches and TLB's that significantly reduce stalls due to bus traffic:

- Two 64-KB primary (L1) caches with 16-way associativity
- A 4-way 128-KB unified level-2 (L2) victim cache
- A 16-entry TLB (TLB1) with fully associativity
- A 64-entry TLB (TLB2) with 2-way associativity

**Extensive features to minimize bus stalls:**

- Full memory type range registers (MTRR's)
- A non-stalling write-allocate implementation
- Efficient prefetch and branch prediction
- Integrated FPU that supports the MMX® and AMD 3DNow!™ instruction sets
- Fully pipelined single precision FPU hardware with microcode support for higher precision

### AMD "LX" processor Architecture Block Diagram




### Security Block

The Geode LX processor has an on-chip AES 128-bit crypto acceleration block capable of 44 Mbps throughput on either encryption or decryption at a processor speed of 500 MHz. The AES block runs asynchronously to the processor core and is DMA-based. The AES block supports both EBC and CBC modes. The initialization vector for CBC mode can be generated by the True Random Number Generator (TRNG). The TRNG is addressable separately and generates a 32-bit random number.

## 2.6. NAND Flash Disk

CM-iGLX contains on-board NAND flash disk, supported by all operating systems available from CompuLab. The Flash Disk behaves exactly like a regular hard disk drive; however, it doesn't have any moving parts.

The NAND Flash is a block device - optimized for block read and write operations rather than for random access. CM-iGLX also contains on-board Flash Disk Controller, which takes care for translation between operating system commands and NAND flash read/write operations. The controller connected to CPU through USB port. In addition to the flash disk emulation, the controller implements error correction (ECC), write protection and caching for improved performance.
The NAND Flash size is 128 or 512 Mbytes. The CM-iGLX is designed for upward compatibility with future NAND Flash devices of larger capacity.

**Performance**

| | |
|---|---|
| Read | 5000 KB/s |
| Write | 840 KB/s |

# 3. Peripherals and Functions

**Interrupt Channel Mapping**

| IRQ | I/O Device | Priority | On-board usage |
|---|---|---|---|
| IRQ0 | PIT 0 | P1 | always |
| IRQ1 | - | P2 | - |
| IRQ2 | Slave controller cascading | — | always |
| IRQ3 | COM B, off-board PCMCIA | P11 | - |
| IRQ4 | COM A, off-board PCMCIA | P12 | always |
| IRQ5 | PCI | P13 | - |
| IRQ6 | - | P14 | - |
| IRQ7 | Off-board PCMCIA | P15 | - |
| IRQ8 | Real-time clock | P3 | always |
| IRQ9 | PCI | P4 | - |
| IRQ10 | PCI | P5 | - |
| IRQ11 | PCI | P6 | - |
| IRQ12 | - | P7 | - |
| IRQ13 | Floating point error | P8 | always |
| IRQ14 | IDE | P9 | - |
| IRQ15 | Off-board PCMCIA | P10 | - |

If the IRQ is used by the on-board device, disabling the device will free the IRQ. If the on-board device cannot be disabled, then the IRQ is *always* assigned for on-board usage and is therefore marked accordingly in the table above. PCI interrupts support sharing, i.e., the same interrupt may be used by several on-board and off-board devices.

**Serial IRQ**

Serial IRQ allows a single signal line to be used to report the legacy ISA interrupt requests. Interrupt sharing is allowed on Serial IRQ interfaces only for the devices external to the chipset. The following interrupts are external to the chipset and are therefore potentially available on the Serial IRQ interface: IRQ1, IRQ6, IRQ7, IRQ12 and IRQ15. The serial IRQ interface is a synchronous interface. Data is clocked by the system's PCI clock.

**Serial IRQ interface**

| Signal | Pin | Type | Description |
|---|---|---|---|
| SERIRQ | P2-13 | I/O | The routing for this signal must follow PCI layout/routing rules |

## 3.1. Watchdog

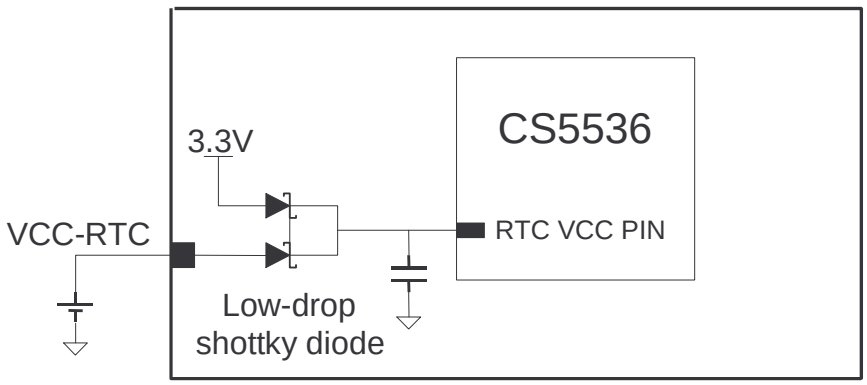
A watchdog is available on the CS5536 companion chip. The timer has a 16-bit counter that counts up until the programmed value using 1 Hz clock. The comparator is loaded with an initial value and start counts from zero. On reaching the programmed value, it generates a system reset. The timer's status can be read and updated at any time. The watchdog can be de-activated and re-activated. A driver and sample application for watchdog operation is provided in the O/S packages.

## 3.2. Real-Time Clock

The RTC is compatible with the standard used in PC/AT systems. The RTC consists of a time-of-day clock with an alarm interrupt and a 100-year calendar. The clock / calendar has a programmable periodic interrupt, 242 bytes of static user RAM and can be represented in either binary or BCD. The RTC includes the following features:

- Counting of seconds, minutes and hours of the day
- Counting of days of the week, date, month and year
- 12–24 hour clock with an am/pm indicator in 12-hour mode
- 242 bytes of general-purpose RAM
- Three separate software-maskable and testable interrupts: (1) time-of-day alarm is programmable to occur from once-per-second to once-per-month, (2) periodic interrupts can be configured to occur at rates from 3.9 ms to 500 ms, and (3) update-ended interrupt provides cycle status.
- The voltage monitor circuit checks the voltage level of the backup lithium battery and sets a bit when the battery voltage level falls below specification.
- The internal RTC reset signal performs a reset when power is applied to the RTC core.

The RTC uses a dedicated lithium backup battery when the rest of the card is completely powered down (RTC-only mode). The RTC can continue operating even when the rest of the card is not powered. The battery should be connected to the VCC-RTC input of the CM-iGLX's interface connector. The equivalent RTC supply circuit is shown in the figure below.




| | Typical | Max |
|---|---|---|
| VCC-RTC Input Current<br>(Rest of the card powered down) | 2 μA | 6 μA |

**Storing of BIOS Settings**

The CM-iGLX's BIOS has two sets of stored settings:

1. Current settings stored in CMOS memory, backed-up by battery as described above. The battery is not located on the CM-iGLX itself, but rather should be provided on the baseboard. When the CMOS is not powered, the settings it saves are lost.
2. Default settings saved in Flash memory. These settings remain valid when the card is not powered, even in the absence of battery backup. The user can update the Flash default settings to any values desired.

On startup, the BIOS checks if valid CMOS settings are available. If they are, BIOS takes the settings from the CMOS. Flash defaults are ignored in that case. If CMOS settings are not valid (i.e., were erased), BIOS uses the default settings from the Flash. In this case, BIOS also copies the default settings from the Flash to the CMOS, to make its contents valid.

## 3.3. Display Controller

The powerful Display Controller of the CM-iGLX contains a comprehensive set of features required for multimedia applications:

### Integrated Graphics / Video Accelerator

- Optimized Unified Memory Architecture (UMA)
- Hardware frame buffer compression
- 2 to 128 MB frame buffer using system memory
- Simultaneous CRT / TFT Support
- Resolutions up to 1920x1440x32 bpp at 85 Hz, or up to 1600x1200x32 bpp at 100 Hz
- Supports down to 7.652 MHz Dot Clock (320x240QVGA)
- Hardware legacy VGA
- Hardware supported 48x64 32-bit cursor with alpha blending

### Extensive Display Support

- Integrated Dot Clock PLL with up to 350 MHz clock
- Integrated 3x8-bit DAC with up to 350 MHz sampling

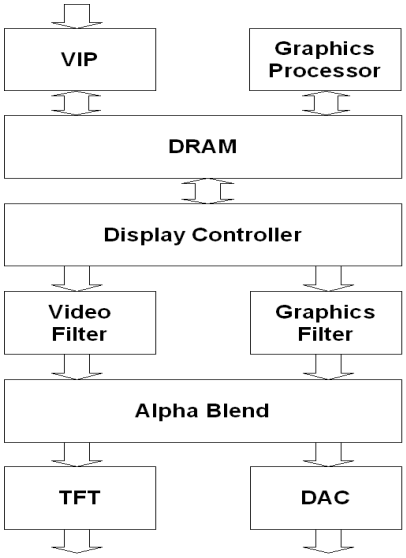
### Video Support

- Supports video scaling and mixing
- Hardware video up/down scalar
- Graphics/video alpha blending and color key mixing
- TFT outputs
- Legacy RGB mode
- VESA 1.1, 2.0

### Video Input Port

- VESA 1.1, 2.0 and BT.601, BT.656 compliant, 150 MHz (excludes host interface).
- Standard 9 pin interface (8 data + clock)
- 8-bit BT.656 video
- VIP 1.1 compatible mode (8 bit)
- 8-bit BT.601 type input video with HSYNC and VSYNC

**Display Controller Block Diagram**




**LCD Panel Interface Signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| LCD-B0 | P3-126 | O | **LCD Panel Data Bus**. |
| LCD-B1 | P2-95 | O | |
| LCD-B2 | P2-97 | O | |
| LCD-B3 | P2-100 | O | |
| LCD-B4 | P2-99 | O | |
| LCD-B5 | P2-102 | O | |
| LCD-G0 | P2-101 | O | |
| LCD-G1 | P2-104 | O | |
| LCD-G2 | P2-106 | O | |
| LCD-G3 | P2-105 | O | |
| LCD-G4 | P2-108 | O | |
| LCD-G5 | P2-107 | O | |
| LCD-R0 | P3-128 | O | |
| LCD-R1 | P2-109 | O | |
| LCD-R2 | P2-113 | O | |
| LCD-R3 | P2-116 | O | |
| LCD-R4 | P2-118 | O | |
| LCD-R5 | P2-117 | O | |
| LCD-SCK | P2-112 | O | **Display Data Clock.** Pixel clock for flat panel data. |
| LCD-FRM | P2-111 | O | **Frame Sync.** Flat Panel equivalent of VSYNC. |
| LCD-LP | P2-96 | O | **Line Sync.** Flat Panel equivalent of HSYNC. |
| LCD-DE | P2-114 | O | **Display Enable signal** (DE) for TFT Panels. |
| LCD-VDDEN | P3-130 | O | Power sequencing control for panel driver electronics voltage VDD. |

**CRT Interface Signals**

| Signal | Pin | Type | Output Drive | Description |
|---|---|---|---|---|
| CRT-HSYNC | P3-129 | O | 1/4 mA | **CRT Horizontal Sync** |
| CRT-VSYNC | P3-140 | O | 1/4 mA | **CRT Vertical Sync** |
| CRT-R | P3-132 | O | 19 mA | **CRT analog video outputs** from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g., 75 ohm resistor on the board, in parallel with the 75 ohm CRT load) |
| CRT-G | P3-136 | O | 19 mA | |
| CRT-B | P3-133 | O | 19 mA | |

**Video Input Port interface signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| VIP-CLK | P3-88 | I | Video Input Port clock input |
| VIP-D0 | P3-80 | I | Video Input Port data input |
| VIP-D1 | P3-82 | I | Video Input Port data input |
| VIP-D2 | P3-84 | I | Video Input Port data input |
| VIP-D3 | P3-90 | I | Video Input Port data input |
| VIP-D4 | P3-92 | I | Video Input Port data input |
| VIP-D5 | P3-94 | I | Video Input Port data input |
| VIP-D6 | P3-96 | I | Video Input Port data input |
| VIP-D7 | P3-89 | I | Video Input Port data input |

## 3.4. General Purpose Input / Output

The CS5536 companion chip integrated in the CM-iGLX provides 8 general purpose I/O pins (GPIO's) – four dedicated and the other four shared with alternative functions. GPIO sample code is available in o/s packages provided by CompuLab.
The dedicated GPIO's are:

| Signal | Pin | Type | Remarks |
|---|---|---|---|
| GPIO6 | P1-13 | I/O | Autosense weak PU/PD |
| GPIO5 | P1-16 | I/O | Autosense weak PU/PD |
| GPIO27 | P1-15 | I/O | Configurable PU/PD, controls Power Led |
| GPIO25 | P1-18 | I/O | Configurable PU/PD |

GPIO's shared with alternative functions:

| Default configuration | Pin | Type | Remarks | On board usage |
|---|---|---|---|---|
| TIMER-OUT [GPIO1] | P3-61 | I/O | Configurable PU | - |
| LPC-LDRQ [GPIO20] | P2-17 | I/O | PU 8.2k | - |
| SERIRQ [GPIO21] | P2-13 | I/O | PU 8.2k | - |
| PME [GPIO26] | P1-17 | I/O | Configurable PU/PD | + |

** GPIO references are specified according to enumeration used in CS5536 manual.*

## 3.5. PCI Bus Host Bridge

The CM-iGLX contains an integrated PCI bus host bridge allowing interface to any PCI bus Revision 2.2-compliant master or target device. The PCI host bridge on the CM-iGLX has the following functionality:

- **Master controller** - Allows the CPU to be a master on the PCI bus. The CPU can generate transactions to configure the PCI host bridge, as well as all external devices on the PCI bus. The CPU can also generate memory and I/O read and write transactions on the PCI bus.
- **Target controller** - Allows external PCI bus masters to access the CM-iGLX's on-board DRAM.

**Features:**

- 33 MHz operation
- Target support for fast back-to-back transactions
- Arbiter support for one or two external PCI bus masters
- Write gathering and write posting for in-bound write requests
- Virtual PCI header support
- Delayed transactions for in-bound read requests
- Zero wait state operation within a PCI burst
- Dynamic clock stop/start support
- Capable of handling out-of-bounds transactions immediately after reset
- PCI-2.2 compliant, 32 bit 3.3V PCI interface

**PCI Clock System**

The clock source is from an on-board oscillator. The CM-iGLX acts as a 'motherboard', providing clocks to all other parts of the application. If a developer needs to synchronize PCI bus operation with another clock source from a custom baseboard, then a PCI-to-PCI bridge should be used. (Suitable bridges are available from PLX and other manufacturers.)
The PCI standard allows up to a 2ns clock skew. In order to minimize the initial skew value, the internal feedback path is designed with a 10 cm trace length - to create the initial delay. Feedback is provided to the clock generation block of the PCI bridge. The timing of all internal clock references is shifted accordingly. In other words, PCI signals are pre-compensated for an external clock trace length of 10 cm. The maximum allowed length of the external clock trace is:
10 cm (pre-compensated) + 30 cm (max propagation delay for a skew less than 2ns)

**PCI Bus Signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| PCI-AD0 | P2-20 | B | **PCI Address Data Bus** |
| PCI-AD1 | P2-22 | B | |
| PCI-AD2 | P2-21 | B | |
| PCI-AD3 | P2-24 | B | |
| PCI-AD4 | P2-23 | B | |
| PCI-AD5 | P2-25 | B | |
| PCI-AD6 | P2-28 | B | |
| PCI-AD7 | P2-27 | B | |
| PCI-AD8 | P2-29 | B | |
| PCI-AD9 | P2-32 | B | |
| PCI-AD10 | P2-34 | B | |
| PCI-AD11 | P2-33 | B | |
| PCI-AD12 | P2-36 | B | |
| PCI-AD13 | P2-35 | B | |
| PCI-AD14 | P2-37 | B | |
| PCI-AD15 | P2-40 | B | |
| PCI-AD16 | P2-51 | B | |
| PCI-AD17 | P2-54 | B | |
| PCI-AD18 | P2-53 | B | |
| PCI-AD19 | P2-56 | B | |
| PCI-AD20 | P2-58 | B | |
| PCI-AD21 | P2-57 | B | |
| PCI-AD22 | P2-60 | B | |
| PCI-AD23 | P2-59 | B | |
| PCI-AD24 | P2-64 | B | |
| PCI-AD25 | P2-63 | B | |
| PCI-AD26 | P2-66 | B | |
| PCI-AD27 | P2-65 | B | |
| PCI-AD28 | P2-68 | B | |
| PCI-AD29 | P2-70 | B | |
| PCI-AD30 | P2-69 | B | |
| PCI-AD31 | P2-72 | B | |

**PCI Bus Signals (continued)**

| Signal | Pin | Type | Description |
|---|---|---|---|
| PCI-CBE0# | P2-30 | B | **Command or Byte-Enable Bus** functions: (1) as a time-multiplexed bus command that defines transaction type on the AD bus, or (2) as byte enables: CBE0 for AD7–AD0 |
| PCI-CBE1# | P2-39 | B | **Command or Byte-Enable Bus** functions: (1) as a time-multiplexed bus command that defines transaction type on the AD bus, or (2) as byte enables: CBE1 for AD15–AD8 |
| PCI-CBE2# | P2-52 | B | **Command or Byte-Enable Bus** functions: (1) as a time-multiplexed bus command that defines transaction type on the AD bus, or (2) as byte enables: CBE2 for AD23–AD16 |
| PCI-CBE3# | P2-61 | B | **Command or Byte-Enable Bus** functions: (1) as a time-multiplexed bus command that defines transaction type on the AD bus, or (2) as byte enables: CBE3 for AD31–AD24 |
| PCI-DEVSEL# | P2-45 | B | **Device Select** is asserted by the target when it has decoded its address as the target of the current transaction. This signal is pulled up on-board with an 8.2K resistor. |
| PCI-FRAME# | P2-49 | B | **Frame** is driven by the transaction initiator to indicate the start and duration of the transaction.<br>This signal is pulled up on-board with an 8.2K resistor. |
| PCI-INTA# | P2-6 | I | **PCI Interrupt Requests** is asserted to request an interrupt. |
| PCI-INTB# | P2-8 | I | |
| PCI-INTC# | P3-20 | I | |
| PCI-INTD# | P3-17 | I | |
| PCI-IRDY# | P2-47 | B | **Initiator Ready** is asserted by the current bus master to indicate that data is ready on the bus (write) or that the master is ready to accept data (read). This signal is pulled up on-board with an 8.2K resistor. |
| PCI-PAR | P2-42 | B | **PCI Parity** is driven by the initiator or target to indicate parity on the AD31–AD0 and CBE3–CBE0 busses. |
| PCI-PERR# | P2-44 | B | **Parity Error** is not supported. This signal is pulled up on-board with an 8.2K resistor. |
| PCI-PCIRST# | P1-137 | O | **Reset** is asserted to reset the PCI devices. |
| PCI-SERR# | P2-41 | I | **System Error** is not supported. This signal is pulled up on-board with an 8.2K resistor. |
| PCI-STOP# | P2-46 | B | **Stop** is asserted by the target to request that the current bus transaction be stopped. This signal is pulled up on-board with an 8.2K resistor. |
| PCI-TRDY# | P2-48 | B | **Target Ready** is asserted by the currently addressed target to indicate its ability to complete the current data phase of a transaction.<br>This signal is pulled up on-board with an 8.2K resistor. |

| Signal | Pin | Type | Description |
|---|---|---|---|
| PCI-REQ0#<br>PCI-REQ1# | P2-1<br>P2-18 | I | **Bus Request** is asserted by the master to request access to the bus. PCI_REQ1# is available only if on-board Ethernet chip is not assembled. |
| PCI-GNT0#<br>PCI-GNT1# | P2-3<br>P2-5 | O | **Bus Grant** is asserted by the CM-iGLX to grant access to the bus. PCI_GNT1# is available only if on-board Ethernet chip is not assembled. |
| PCI-CLK0<br>PCI-CLK1<br>PCI-CLK2 | P2-16<br>P3-16<br>P3-24 | O | **PCI Bus Clock Output** is a 33-MHz clock for PCI bus devices. This signal is derived from an onboard 33MHz source. Clock edge position is internally compensated in order to reduce skew to a minimum. |

**Notes**

1. Output drive and maximum load specifications are according to PCI bus Standard Rev-2.2.
2. PCI Bus inputs / outputs inputs are 3.3V-level

**PCI resource map**

| Device | IDSEL line | PCI dev. / func. | IRQ |
|---|---|---|---|
| CM-iGLX Host bridge | AD11 | 0x01,func.0 | |
| CM-iGLX display controller | AD11 | 0x01, func. 1 | 11 |
| CM-iGLX Encryption Device | AD11 | 0x01, func. 2 | 11 |
| ATX baseboard PCI Slot | AD18 | 0x08, func. 0 | 10,11 |
| ATX baseboard CardBus bridge skt. A | AD19 | 0x09, func. 0 | 10 |
| ATX baseboard CardBus bridge skt. B | AD19 | 0x09, func. 1 | 11 |
| ATX baseboard Ethernet | AD20 | 0x0A, func. 0 | 11 |
| CM-iGLX Ethernet | AD23 | 0x0D,func. 0 | 11 |
| CM-iGLX internal ISA bridge | AD25 | 0x0F, func. 0 | - |
| CM-iGLX IDE controller | AD25 | 0x0F, func. 2 | 14 |
| CM-iGLX audio controller | AD25 | 0x0F, func. 3 | 11 |
| USB 1.1 controller | AD25 | 0x0F, func. 4 | 5 |
| USB 2.0 controller | AD25 | 0x0F, func. 5 | 5 |

PCI devices have no hardcoded IRQ assignment. The IRQ assignment listed in the table is correct for a CM-iGLX plugged into a CompuLab baseboard (such as an ATX), but can change if additional hardware is attached.

## 3.6. AC97 Interface

The audio / modem link in the CM-iGLX is AC97 Revision 2.3 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality two-speaker audio solution. Audio codec is included on-board in the CM-iGLX.

Features Supported by the AC97:

- AC97 version 2.3 compliant interface to codecs: serial in (x2), serial out, sync out and bit clock in.
- Eight-channel buffered bus mastering interface
- Support for industry standard 16-bit pulse code modulated (PCM) audio format
- Support for any AC97 codec with Sample Rate Conversion (SRC)
- Transport for audio data to and from the system memory and AC97 codec
- Capable of outputting multi-channel 5.1 surround sound (Left, Center, Right, Left Rear, Right Rear, and Low Frequency Effects)

Hardware Includes:

- Three 32-bit stereo-buffered bus masters (two for output, one for input)
- Five 16-bit mono-buffered bus masters (three for output, two for input)
- AC Link Control block for interfacing with external AC97 codec(s)

By using an optional audio codec, the CM-iGLX module implements cost-effective, high quality, integrated audio. In addition, an AC97 soft modem can be implemented with the use of a modem codec.

**AC97 link signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| AC97-RST# | P3-124 | O | **AC97 Reset:** Master H/W reset to external Codec(s) |
| AC97-SYNC | P3-125 | O | **AC97 Sync:** 48 KHz fixed rate sample sync to the Codec(s) |
| AC97-BITCLK | P3-120 | I | **AC97 Bit Clock:** 12.288 MHz serial data clock generated by the external Codec(s) |
| AC97-SDOUT | P3-123 | O | **AC97 Serial Data Out:** Serial TDM data output to the Codec(s). AC_SDOUT is sampled at the rising edge of PWROK as a functional strap. |
| AC97-SDIN0 | P3-119 | I | **AC97 Serial Data In 0:** Serial TDM data input from a Codec. The on-board Codec uses this line. |

## 3.7. LPC - Low Pin Count Interface

The CM-iGLX implements an LPC Interface and Controller as described in the LPC 1.0 specification. The LPC bus provides a functional replacement for the interfacing of legacy ISA functions, such as an additional Super-I/O chip.

**LPC bus signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| LPC-LAD0 | P2-10 | I/O | **LPC Multiplexed Command, Address, Data.** |
| LPC-LAD1 | P2-9 | I/O | |
| LPC-LAD2 | P2-12 | I/O | |
| LPC-LAD3 | P2-11 | I/O | |
| LPC-LDRQ# | P2-17 | I | **LPC Serial DMA/Master Request Inputs:** DMA or bus master request |
| LPC-LFRAME# | P2-15 | O | **LPC Frame:** Indicates the start of an LPC cycle, or an abort |

In addition to the above signals, an LPC device should use a PCI clock and the PCIRST#.

## 3.8. Serial Ports

The CM-iGLX includes two serial ports (UART's). The UART's power up as 16450-compatible devices. They are switched to 16550 (FIFO) mode under the control of serial drivers specific to the operating system used. In FIFO mode, the receive and transmit circuitry are each enhanced by separate FIFO's to off-load repetitive service routines from the CPU.

The serial ports include the following features:

- Fully compatible with 16550 and 16450 devices (except modem)
- Extended UART mode
- UART mode data rates up to 115 Kbps
- Transmit deferral
- Automatic fallback to 16550 compatibility mode
- Selectable 16 and 32 level FIFO's
- DMA handshake signal routing for either 1 or 2 channels
- Support for power management

The first UART includes RS232 drivers, the second UART has a TTL signal level interface.

**Serial Port Signals**

| Signal | Pin | Interf | Type | Description |
|---|---|---|---|---|
| COMA-RX | P1-22 | RS232 | I | **Serial Data In** receives the serial data from the external serial device or DCE into the internal serial port controller. |
| COMB-RX | P1-23 | TTL | I | |
| COMA-TX | P1-24 | RS232 | O | **Serial Data Out** transmits the serial data from the internal serial port controller to the external serial device or DCE. |
| COMB-TX | P1-25 | TTL | O | |

## 3.9. USB Ports

The CM-iGLX provides three plus one optional USB-2 ports. The USB ports are Host Controller Interface (HCI) compliant. The HCI specification provides a register level description for a host controller, as well as common industry hardware/software interface and drivers. USB ports are supported by all O/S packages provided for CM-iGLX.

Features:

- USB v2.0 / EHCI v1.0 and USB v1.1 / OHCI v1.1 compatible
- Physical layer transceivers with optional over-current detection status on USB inputs

**USB Port Signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| USB-OVC# | P2-133 | I | **Overcurrent.** This signal indicates that the USB hub has detected an overcurrent on the USB. This pin has a 4.7k pull-up |
| USB1-N | P2-140 | I/O | USB Port 1 Data Negative for Port 1 |
| USB1-P | P2-138 | I/O | USB Port 1 Data Positive for Port 1 |
| USB2-N | P2-139 | I/O | USB Port 2 Data Negative for Port 2 |
| USB2-P | P2-137 | I/O | USB Port 2 Data Positive for Port 2 |
| USB3-N | P1-138 | I/O | USB Port 3 Data Negative for Port 3 |
| USB3-P | P1-136 | I/O | USB Port 3 Data Positive for Port 3 |
| USB4-N* | P1-139 | I/O | USB Port 4 Data Negative for Port 4 |
| USB4-P* | P1-137 | I/O | USB Port 4 Data Positive for Port 4 |

* If the NAND flash is assembled, this port is not available

## 3.10. Audio Interface

The CM-iGLX implements audio interface using a Wolfson WM9715L codec chip, which also includes a touch screen controller. The codec is an AC'97 2.1 compliant stereo audio codec designed for PC multimedia systems. It uses industry-leading delta-sigma and mixed signal technology. This advanced technology and its features are designed to help in enabling the design of PC 99 and PC 2001 compliant high-quality audio systems. The codec surpasses PC 99, PC 2001 and AC '97 2.1 audio quality standards. The audio system also includes a power amplifier for matching the stereo output for a direct connection of stereo headphones.

Features:

- Integrated High-Performance Headphone Amplifier
- Sample Rate Converters
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Line-level Stereo Input for LINE IN
- Microphone Input
- Integrated High-Performance Microphone Pre-Amplifier
- Meets or exceeds Microsoft PC 99 and PC 2001 Audio Performance Requirements

**Audio specifications**

| | | |
|---|---|---|
| Speaker Output | Type | Stereo |
| | Power | 25 mW/ch into 32 ohm speakers |
| | Decoupling | Requires external 220uF capacitors, for 8 ohm load. Smaller capacitors (like 1uF) can be used for high-impedance loads. |
| Microphone Input | Type | Mono, electret or dynamic |
| | Decoupling | On-board |
| Line Input | Type | Stereo |
| | Decoupling | On-board |

**Audio Interface Signals**

| Signal | Pin Number | Type | Output Drive | Description |
|---|---|---|---|---|
| AUD-INL-MIC | P2-132 | I | - | Audio stereo line input left and microphone mono input |
| AUD-INR | P2-130 | I | - | Audio stereo line input right |
| AUD-OUTL | P2-131 | O | 25 mW | Speaker stereo output left. Can be used as line output |
| AUD-OUTR | P2-136 | O | 25 mW | Speaker stereo outputs right. Can be used as line output |

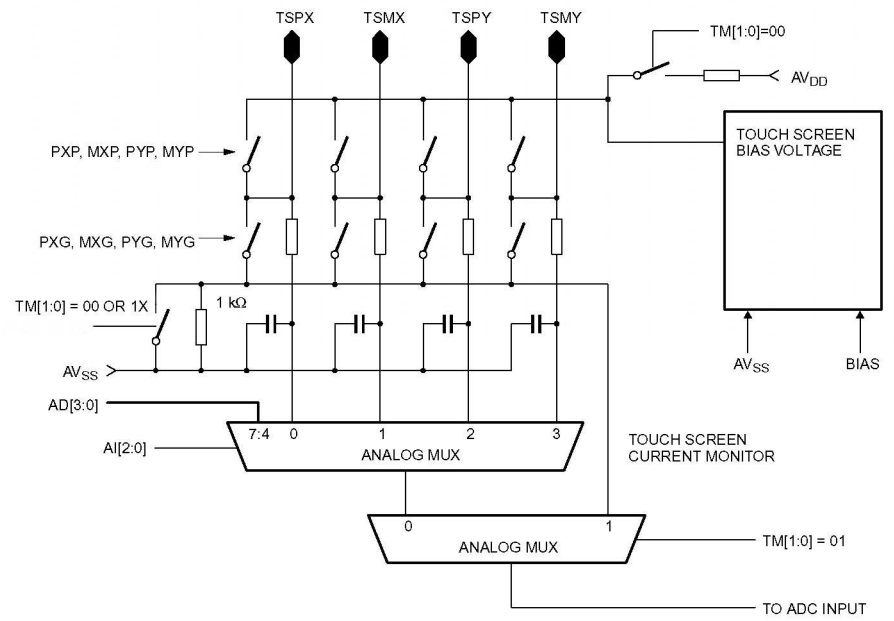
**Audio System Errata**

USB1400 audio codec has a problem to operate at certain sampling rates: 11,025Hz, 22,050Hz, 44,100Hz. It has no problem to operate at other sampling rates: 8,000Hz, 12,000Hz, 16,000Hz, 24,000Hz, 32,000Hz & 48,000Hz, so these should be selected. Sound files included with operating system packages should be resampled to valid rates. Resampling can be performed by tools such as Audacity (http://audacity.sourceforge.net/)

Errata will be fixed until Jun-2007.

## 3.11. Touch Screen Controller

The optional Wolfson WM9715L codec chip includes a universal touch screen controller. Touch screen interface is for a 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements.
Touchscreen is supported by certain operating system available for CM-iGLX. For details refer to [Products] >> [CM-iGLX] >> [O/S Support Coverage Map] page in CompuLab's web-site.




The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or grounded in the touch screen switch matrix. Each of the four touch screen signals can be selected as input for the built-in 10-bit ADC, which is used to determine the voltage on the selected touch screen pin in position measurement mode. In addition, the WM9715L can monitor touch screen current via an internal 1 Kohm resistor that can act as the input to the 10-bit ADC in pressure or plate resistance measurement mode. The flexible switch matrix and the multi-functional touch screen bias circuit enable the user of the WM9715L to set each desired touch screen configuration.

The WM9715L's internal voltage reference (Vref ) acts as the reference voltage for the touch screen bias circuitry. This makes touch screen biasing independent of supply voltage and temperature variations. Four low-pass filters, one on each touch screen terminal, are built-in to minimize the noise coupled from the LCD into the touch screen signals. An LCD typically generates large noise glitches on the touch screen, since they are closely coupled.

**Touch Screen Interface Signals**

| Signal | Pin Number | Type | Description |
|---|---|---|---|
| TS-PX | P1-53 | Analog | Plate X, plus (Left) |
| TS-MX | P2-71 | Analog | Plate X, minus (Right) |
| TS-PY | P1-57 | Analog | Plate Y, plus (Top) |
| TS-MY | P2-73 | Analog | Plate Y, minus (Bottom) |

## 3.12. Hard disk Controller - Parallel ATA

**Features**

- Single channel hard disk controller supporting two Enhanced IDE devices
- Transfer rate up to 100MB/sec
- UltraDMA-100/66/33 transfer protocol
- Support for legacy PIO mode 4 and multi-word DMA mode 2 drives
- DMA engine for concurrent operation, scatter-gather capability
- Bus master programming interface for SFF-8038i rev.1.0 and Windows compliant
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support under Linux and Windows

**Hard disk Interface Signals**

Note: connector signal names reflect the naming of PIO mode. In DMA mode, signal functionality is redefined.

| Signal | Pin | Type | Description |
|---|---|---|---|
| IDE-CS0# | P1-47 | O | **IDE Device Chip Select for 1F0h Range:** for ATA command register block |
| IDE-CS1# | P1-52 | O | **IDE Device Chip Select for 3F6h Range:** for ATA control register block |
| LB-A0 | P1-64 | O | **IDE Device Address:** Used to indicate which byte in either the ATA command block or control block is being addressed |
| LB-A1 | P1-63 | O | |
| LB-A2 | P1-66 | O | |
| LB-D0 | P1-94 | I/O | **IDE Device Data**<br><br>IDE Address and Data lines are shared with "Local Bus" pins on CAMI connectors |
| LB-D1 | P1-95 | I/O | |
| LB-D2 | P1-96 | I/O | |
| LB-D3 | P1-97 | I/O | |
| LB-D4 | P1-100 | I/O | |
| LB-D5 | P1-99 | I/O | |
| LB-D6 | P1-102 | I/O | |
| LB-D7 | P1-101 | I/O | |
| LB-D8 | P1-104 | I/O | |
| LB-D9 | P1-105 | I/O | |
| LB-D10 | P1-106 | I/O | |
| LB-D11 | P1-107 | I/O | |
| LB-D12 | P1-108 | I/O | |
| LB-D13 | P1-109 | I/O | |
| LB-D14 | P1-112 | I/O | |
| LB-D15 | P1-111 | I/O | |
| IDE-DREQ | P3-63 | I | **IDE Device DMA Request:** asserted by the IDE device to request a data transfer |
| IDE-DACK# | P3-65 | O | **IDE Device DMA Acknowledge:** asserted to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of RD# or WR#) is a DMA data transfer cycle |
| IDE-RD# | P1-46 | O | **Disk I/O Read (PIO mode):** the command to the IDE device that it may drive data onto the IDE-D lines. Data is latched on the de-assertion edge of IDE-RD#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0#, IDE-CS1#) and the IDE-A lines, or the IDE DMA acknowledge (IDE-DACK#).<br>**Disk Write Strobe (UDMA Writes to Disk):** This is the data write strobe for writes to disk.<br>**Disk DMA Ready (UDMA Reads from Disk):** This is the DMA ready for reads from disk. |

| Signal | Pin | Type | Description |
|---|---|---|---|
| IDE-WR# | P1-48 | O | **Disk I/O Write (PIO and Non-UDMA):** the command to the IDE device that it may latch data from the IDE-D lines. Data is latched by the IDE device on the de-assertion edge of IDE-WR#. The IDE device is selected either by the ATA register file chip selects (IDE-CS0, IDE-CS1) and the IDE-A line, or the IDE DMA acknowledge (IDE-DACK#).<br>**Disk Stop (UDMA):** the controller asserts this signal to terminate a burst. |
| LB-IORDY | P1-113<br>P3-66 | I | **I/O Channel Ready (PIO):** keeps the strobe active (IDE-RD# or IDE-WR#) longer than the minimum width. It adds wait states to PIO transfers.<br>**Disk Read Strobe (UDMA Reads from Disk):** When reading from the disk, the controller latches data on rising and falling edges of this signal from the disk.<br>**Disk DMA Ready (UDMA Writes to Disk):** When writing to the disk, this is de-asserted by the disk to pause burst data transfers. This signal has an internal 1.5k pull-up. |

## 3.13. 10/100 Mbit Ethernet Port

The CM-iGLX contains one full-featured 10/100 Mbit Ethernet interface. The Ethernet interface is based on the on-board RTL8139 chip, supporting the following features:

- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation
- 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
- PCI multi-function capabilities
- Two large (2Kbyte) independent receive and transmit FIFO's
- Programmable PCI burst size and early Tx/Rx threshold
- LED outputs for various network activity indications
- Loopback capability
- Half/Full duplex capability
- Full Duplex Flow Control (IEEE 802.3x)

**Magnetic Modules**

The CM-iGLX's Twisted Pair interface requires an external transformer (magnetic module) for interface to an RJ-45 connector. Two options exist:

1. An RJ-45 connector with a built-in transformer. Examples:

| Vendor | Model |
|---|---|
| YCL | PTC1111-01 |
| PCA | EPJ9025 |
| Bothhand | LU1S041C |

2. A separate transformer and RJ-45 connector. Examples of available transformers:

| Vendor | Model |
|---|---|
| Delta | LF8200A |
| Pulse Engineering | PE-68515 |
| Pulse Engineering | H1012 |

**Routing Ethernet Signals**

The following rules should be applied when routing differential transmit and receive signals between the CM-iGLX interface connector and an external connector/transformer module:

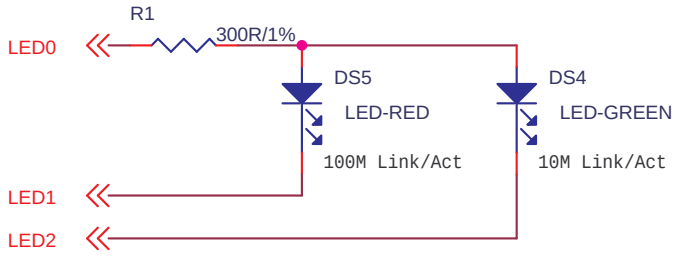
1. Route the differential signal pairs (TXN, TXP) and (RXN, RXP) in parallel, with minimal and consistent clearance within the pair. The distance between RX and TX pairs should be maximized; otherwise, TX will induce crosstalk into RX.
2. It is preferable (but not mandatory) to keep the trace length of Ethernet signals as short as possible. If trace length exceeds 2 inches, additional steps, not specified here, should be taken. Recommended trace width: 5 to 8 mil.
3. Don't route any other traces near or across the Ethernet signals' path.
4. It is preferable (but not mandatory) to remove the ground and other planes from beneath the Ethernet trace area.

The listed rules cover the routing requirements if an RJ-45 connector with a built-in transformer is used. If a separate transformer is used, additional rules should be followed for transformer-to-connector routing.

**Ethernet Port Signals**

| Signal | Pin | Type | Output Drive | Description |
|---|---|---|---|---|
| ETH1-TDN<br>ETH1-TDP | P1-3<br>P1-1 | A/O | | **Analog Twisted Pair Ethernet Transmit Differential Pair.** These signals interface directly with an isolation transformer. TDP and TDN pins are connected by a 100 ohm termination resistor. |
| ETH1-RDN<br>ETH1-RDP | P1-2<br>P1-4 | A/I | | **Analog Twisted Pair Ethernet Receive Differential Pair.** These pins receive the serial bit stream from the isolation transformer. RDP and RDN pins are connected by a 100 ohm termination resistor. |
| ETH1-ACT#<br>(LED0) | P1-10 | O | 10 mA | **Activity LED.** The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high. |
| ETH1-LINK100#<br>(LED1) | P1-5 | O | 10 mA | **100 Link LED.** The 100 Link LED pin indicates link integrity and 100Mbps connection speed. |
| ETH1-LINK10#<br>(LED2) | P1-6 | O | 10 mA | **10 Link LED.** The 10 Link LED pin indicates link integrity and 10 or 100 Mbps connection speed. |

**Recommended LED connection**




This connection supplies full information about speed/link/activity.

LED-RED with LED-GREEN: 100 Mbps link / activity indicator
LED-GREEN: 10 Mbps link / activity indicator

| Activity | LED (Red/Green) |
|---|---|
| none | off |
| Link (only) | on |
| Tx / Rx (and Link) | blink |

## 3.14. WiFi interface

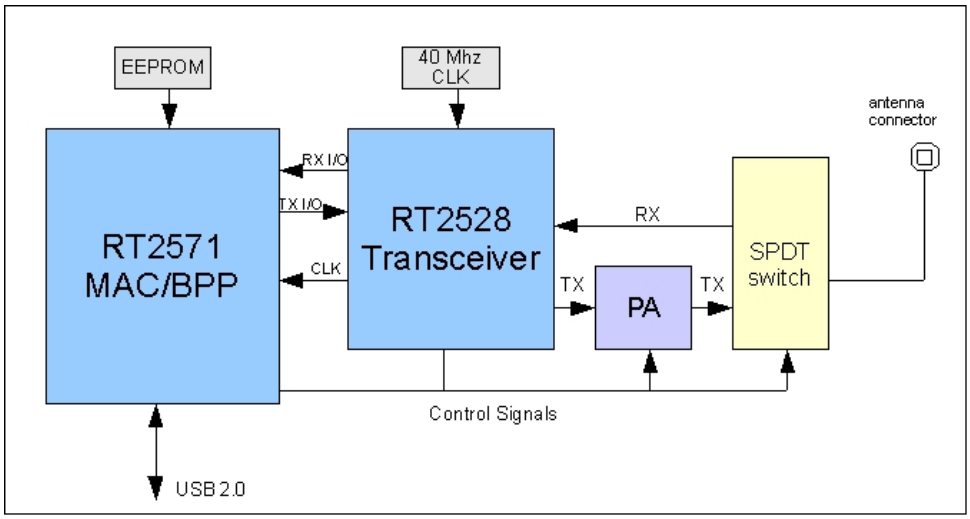
WiFi interface is available in cards revision 2 only.

The wireless LAN is based on Ralink chipset - RT2571W MAC/BBP and RT2528 transceiver, and external power amplifier.

Features:

- USB 2.0 interface to processor sub-system
- IEEE802.11/802.11g compliant
- Supports DSSS, CCK, OFDM modulation
- Support TKIP and AES
- Support 64/128 WEP, WPA, AES
- Wide software support for Windows XP and Linux
- Access Point mode capability

**802.11 Wireless LAN block diagram:**



**Channel assignment**

| Channel | Frequency (MHz) | | Channel | Frequency (MHz) |
|---|---|---|---|---|
| **1** | 2412 | | **8** | 2447 |
| **2** | 2417 | | **9** | 2452 |
| **3** | 2422 | | **10** | 2457 |
| **4** | 2427 | | **11** | 2462 |
| **5** | 2432 | | **12** | 2467 |
| **6** | 2437 | | **13** | 2472 |
| **7** | 2442 | | **14** | 2484 |

**Modulation methods**

| Bit rate(802.11b CCK) | Modulation | | Bit rate(802.11g OFDM) | Modulation |
|---|---|---|---|---|
| 1 Mbps | BPSK | | 6,9 Mbps | BPSK |
| 2, 5.5, 11 Mbps | QPSK | | 12,18 Mbps | QPSK |
| | | | 24,36 Mbps | 16QAM |
| | | | 48,54 Mbps | 64QAM |

**Electrical specification**

| Characteristic | CCK | OFDM | Units |
|---|---|---|---|
| **RX supply current** | 220 | 225 | mA |
| **TX supply current** | 232 | 240 | mA |
| **Power save mode current** | 124 | | mA |
| **RX sensitivity** | -87 | -73 | dBm |
| **TX output power** | 17 | 16 | dBm |
| **TX spectral mask** | PASS | PASS | - |

**Antenna connector**

- SMD U.FL, I-PEX ,3x3 mm
- Must use 50 Ohm impedance antenna with gain > 2 dBi and VSWR < 2.0

**WiFi vs. 512 MB DDR tradeoff**

WiFi interface is available only in cards revision 2.x, while 512 MB DDR is available only in cards revision 1.4 or later 1.x revisions. This limitation is a result of board space constrains. Therefore, WiFi and 512 MB DDR options are mutually exclusive.

## 3.15. JTAG interface

- JTAG interface: ATPG, Full Scan, BIST on 1149.1 Boundary Scan compliant
- ICE (in-circuit emulator) interface
- Reset and clock control
- Designed for improved software performance analysis

**JTAG interface Signals**

| Signal | Pin | Type | Description |
|---|---|---|---|
| JTAG-TCK | P3-77 | I | **Test Clock** is the input clock for the test access port. This pin is tied to a 4.7k pull-up resistor. |
| JTAG-TDI | P3-83 | I | **Test Data Input** is the serial input stream for input data. This pin is tied to a 4.7k pull-up resistor. |

| | | | |
|---|---|---|---|
| JTAG-TDO | P3-85 | O/TS | **Test Data Output** is the serial output stream for result data. It is in high-impedance state except when scanning is in progress. |
| JTAG-TMS | P3-81 | I | **Test Mode Select** is an input for controlling the test access port. This pin is tied to a 4.7k pull-up resistor. |
| JTAG-TRST# | P3-87 | I | **JTAG Reset** is the test access port (TAP) reset. |

## 3.16. Clocks, Timers, Reset, Write Protect, Boot, Power Management

| Signal | Pin | Type | Description |
|---|---|---|---|
| RST-IN# | P1-11 | I | Reset input, active low. Low level on this pin initiates a hardware reset of the CM-iGLX. The CM-iGLX will exist in reset state one second after deactivation of RST-IN. This pin is not mandatory for CM-iGLX operation, as it generates power-on reset using on-board circuitry. It has an internal pull-up and can be left unconnected. |
| RST-OUT# | P1-137 | ODP | Reset output, active low. Indicates that CM-iGLX is undergoing a hardware reset, due to a power-up or RST-IN. Can be used as a reset signal to off-board hardware. RST-OUT minimum duration is approximately 0.5 seconds. The output type is open drain with a 10K pull-up resistor. |
| WP1# | P1-9 | I | BIOS flash write protect. Writes to flash will be disabled if pulled to "0". To enable writes, pull this input to "1" or leave unconnected. This input has an internal pull-up. |
| WP2# | P3-100 | I | NAND flash write protect, active low. NAND flash writes will be disabled if pulled to "0". To enable NAND flash writes, pull this input to "1" or leave unconnected. This input has an internal pull-up. |
| CLKOUT | P3-76 | O | 14.318 MHz clock output |
| TIMER-OUT | P3-61 | O | General purpose timer of CS5536. Normally used as PC speaker in PC-compatible systems |
| PME | P1-17 | I | Power management event / generic SMI source (for future use) |
| SUSP-IN | P1-21 | I | Power button/sleep functionality |
| SLEEP_OUT# | P3-95 | O | Sleep mode external device power disable/enable (for future use) |

| | | | |
|---|---|---|---|
| DEBUG1 | P1-56 | O | For factory use only. Should be left unconnected. |
| DEBUG0 | P1-58 | I | Irrelevant for any other purpose |

## 3.17. SMBus (I2C)

The CM-iGLX provides a host system management bus interface. This interface is compatible with I2C devices.

| Signal | Pin | Type | Description |
|---|---|---|---|
| SSI-DOUT<br>SSI-DIN | P1-60<br>P1-59 | I/O | SMBus data. Two pins are connected together on module. Note: CAMI connector defines separate In & Out pins, for compatibility with other serial interface standards. But CM-iGLX supports only standards having single bi-directional data signal. |
| SSI- CLK | P1-61 | I/O | SMBus clock |

Note: SPI mode is not supported.

## 3.18. Power Supply Pins

The CM-iGLX requires 3.3V supply for operation. All other required supply voltages are generated on-board using DC-DC converters. Supply voltage allowed variation is +/- 5%

**Power Net Description**

| Signal | Description |
|---|---|
| GND | Common ground |
| VCC3_3 | Main power supply, 3.3V.<br>Used together with VCORE, tied to VCORE on-board. |
| VCC3_3SBY | Additional power supply for DDR and stand-by support circuitry.<br>Should be connected to 3.3V stand-by power supply.<br>Design considerations:<br>1. Connecting these pins to the regular VCC3_3 may lead to improper power sequencing and RTC problems (reset to default values). For reference design of proper power up sequencing see SB-iGLX schematics.<br>2. VCC3SBY power supply should be capable to carry up to 1.5A peak power and should be connected using trace width 20 mil or more. Although standby current is low during system sleep, this supply must be capable to bear full operation load. |
| VCORE | Supply source for CPU core logic, should be 3.3V.<br>Reduced to lower voltages by on-board converters.<br>Compatibility note: when designing baseboard compatible with several CompuLab's CoM's, check VCORE voltage level requirements of all potential candidates. In some CoM's VCORE voltage is different than 3.3V. In such case you should design supply capable of providing the required range of voltages. On the other hand, if you intend to use only the CM-iGLX module, VCORE could be tied directly to the main 3.3V supply of the baseboard. |
| VCC5 | This voltage is specified only for compatibility purpose.<br>In CM-iGLX it can be connected either to 3.3V or to 5V.<br>When designing baseboard compatible with several CompuLab's CoM's, check if other modules require that VCC5 will be 5V. |
| VCC-RTC | The 3.3 Volt supply pin provides power to the internal real-time clock and on-board static / configuration RAM. This pin can be driven independently of all other power pins. This pin enables the connection of an external lithium battery. The battery is not mandatory for the CM-iGLX, if the RTC function is not required. In such cases, the VCC-RTC pin should be left unconnected. |

Note: all power pins must be connected.

Power sequence should be as below:

1. Apply VCC3SBY
2. Wait for SLEEP_OUT# (P3-95, WORK_AUX on the SB-iGLX) high and then enable VCC3_3 rail.

Power down sequence :

1. SLEEP_OUT# low will disable VCC3_3 rail
2. Shut down VCC3SBY (or leave it connected and use PWRBTN signal for next power up).

**Power Supply Pins**

| | |
|---|---|
| GND | P1-8, P1-14, P1-26, P1-38, P1-50, P1-62, P1-74, P1-86, P1-98, P1-110, P1-122, P1-134,<br>P2-2, P2-14, P2-26, P2-38, P2-50, P2-62, P2-74, P2-86, P2-98, P2-110, P2-122, P2-134<br>P3-8, P3-14, P3-26, P3- 38, P3-50, P3-62, P3-74, P3-86, P3-98, P3-110, P3-122, P3-134 |
| VCC3_3 | P1-31, P1-67, P1-103, P1-139<br>P2-7, P2-43, P2-79, P2-135<br>P3-19, P3-55, P3-91, P3-127, P3-135 |
| VCC3_3SBY | P3-102,P3-104,P3-106, P3-107, P3-109, P3-111 |
| VCORE | P1-7, P1-19, P1-43, P1-55, P1-79, P1-91, P1-115, P1-127<br>P2-19, P2-31, P2-55, P2-67, P2-91, P2-103, P2-115, P2-127<br>P3-7, P3-31, P3- 43, P3-67, P3-79, P3-103, P3-115 |
| VCC5 | P1-140, P3-131 |
| VCC-RTC | P1-20 |

## 3.19. Restrictions On Using Pull-ups / Pull-downs

Some of the interface pins are also used as CPU pinstrap options. These pinstrap options are not relevant to the user; however, overriding them will lead to module malfunction. In any design, these pins must not have pull-up or pull-down resistors connected and must not be driven by any external source during boot.

| Name | Pin | Pinstrap function |
|---|---|---|
| AC97-SYNC | P3-125 | LPC/FWH BootROM |
| AC97-SDOUT | P3-123 | LPC/FWH BootROM |
| PCI_GNT#0 | P2-3 | CPU frequency strap option |
| PCI_GNT#1 | P2-5 | CPU frequency strap option |

## 3.20. Unconnected Pins

The following pins must be left unconnected for normal operation:

| Name | Pin |
|---|---|
| SPARE5 | P3-101 |
| SPARE7 | P3-105 |
| PCM_BVD2 | P3-113 |

# 4. Baseboard Interface

## 4.1. Baseboard Design Guidelines

- All power pins must be connected, including GND, VCC3, VCORE, VCC5 and STBY (Standby) power rails. If 5V is not used in the system, VCC5 should be connected to the 3.3V supply.
- Major power rails - GND and VCC3/VCORE must be implemented by planes, rather than traces. Note that in CM-iGLX, VCC3 and VCORE are the same voltage, therefore the same baseboard plane can be used. Using at least two planes is essential to assure system's signal quality, because planes providing current return path for all interface signals.
- Review and implement VCC3STBY design considerations
- It is recommended to put several 100 nF and 10/100 uF capacitors between VCC3 and GND near the mating connectors.
- It is recommended to connect standoff holes of baseboard to GND, in order to improve EMC. The hole near the pin #1 of CAMI connectors should be isolated, for compatibility with future CAMI modules.
- Except of power, no other connection is mandatory for CM-iGLX operation. All powerup electronics and all required pullups/pulldowns are found on the module.
- If for some reason you decide to place external pullup or pulldown resistor on certain signal (for example - on GPIO's), check the documentation of that signal as provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCI bus design must take into account signals skew and reflection.
  - Ethernet and USB signals must be routed in differential pairs and by controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
  - Local bus signals must be buffered in most cases.
- Be careful when placing component under the CM-iGLX module. CAMI connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-IGLX. In general, maximum allowable height for components placed under the CM-iGLX is 2mm. There are special areas where maximum height is 0.5 mm only. For details refer to CM-iGLX mechanical documentation.
- Reference designs: two reference designs are available - ATX and SB-iGLX baseboard. SB reference is simpler, because it is specific to CM-iGLX. ATX design is more complicated, because it is generic for all computer-on-modules available from CompuLab.

## 4.2. Baseboard Troubleshooting

- Using grease solvent and soft brush, clean contacts of mating connectors of both module and baseboard. Remainders of soldering paste can prevent proper contact.
- Using oscilloscope, check voltage levels and quality of VCC3/VCORE power supplies. It should be 3.3V +/- 5%. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of mating connector.
- Using oscilloscope verify that GND pins of mating connector are indeed at zero voltage level, and there is no ground bouncing. Module must be plugged in during the test.
- Create "minimum system" - only power, mating connectors, the module, and serial interface.

  Check if the system starts properly. In system larger than minimum, the possible sources of disturbance could be:

- Devices improperly driving local bus or PCI bus

- External pullup / pulldown resistors overriding module's on-board values, or any other components creating the same "overriding" effect.
- Bad power supply.

In order to avoid possible sources of disturbance, it is strongly recommended to start with minimal system and then add/activate off-board devices one by one.

- Check for existence of soldering shorts between pins of mating connectors. Even if signals are not used on the baseboard, shorting them on the connectors can disable module's operation. Initial check can be performed using microscope. However, if microscope inspection finds nothing, it is advised to check using X-ray, because often solder bridges are deeply beneath the connector's body. Note that solder shorts are the most frequent factor disabling module's start.
- Check possible signals shorting due to errors of baseboard PCB design or assembling.
- Improper function of customer baseboard can accidentally delete BIOS or even damage module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's ATX or SB-iGLX baseboard.
- It is recommended to assemble more that one baseboard for prototyping, in order to allow quick sorting out of problems related to specific board assembly.

## 4.3. Connector Type

The CM-iGLX connects to the external world through P1, P2 and P3 - 140-pin, 0.6 mm connectors.

| | Mfg. | CM-iGLX Connector P/N | Mating Connector P/N |
|---|---|---|---|
| **P1, P2, P3** | AMP | 1-5353183-0 | 1-5353190-0 |

**Standoffs**

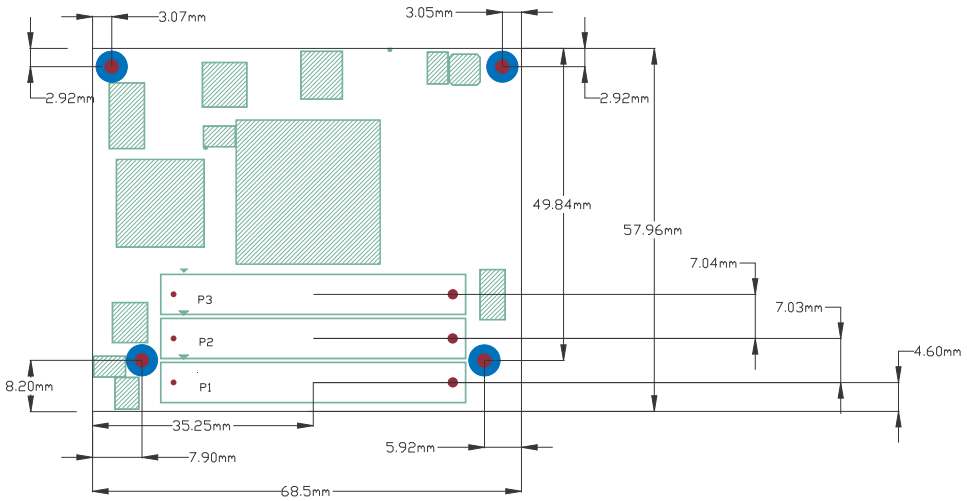
CM-iGLX has four mounting holes for standoffs. Three of the mounting holes - two top and bottom right are connected to GND. The bottom left hole is isolated. (see drawings on the next page.) The developer is advised to connect the mating holes of the baseboard to GND, in order to improve EMC. The bottom left hole on the baseboard should be isolated, for compatibility with future CAMI modules.

The standoff is implemented by three parts: screw, spacer and nut:

| | Description | Manufacturer and P/N |
|---|---|---|
| Screw | M2, 10 mm length | FCI 95121-005<br>Acton InoxPro BF22102010<br>World Bridge Machinery 380J52080 |
| Spacer | M2x.4 thread, 4.2 mm length | Hirosugi ASU-2004<br>MAC8 2SP-4<br>World Bridge Machinery M2, L=4.2mm |
| Nut | M2, 1.6-2.0mm width | FCI 92869-001 (or 002)<br>Acton InoxPro BG12102000<br>Bossard 1241397 (DIN934-A2 M2)<br>World Bridge Machinery 381A52000 |

Mating connectors and standoffs are available from manufacturer representatives or from CompuLab. For details see [prices] >> [accessories] in CompuLab's website.

## 4.4. Connector Layout




**Bottom side image, viewed from the top side of the module**

- The tolerance for all dimension is +/-0.05mm.
- Board-to-board mating height is 4.2 mm.
- Green hatched colored areas indicate height constraints - don't locate components beneath.
- Connectors' and mechanical layout is available in DXF format from CompuLab's website, following [Developer] >> [CM-iGLX] >> [CM-iGLX - Dimensions and Connectors Location] links.

## 4.5. Connectors Pinout

Note: gray-colored signals are not available. They are either not implemented or are routed through other pins of the connector (i.e., mixed with another function). Grayed signals are displayed in order to clarify standard CAMI pin assignment.

| | **P1-A** |
|---|---|
| P1-02 | ETH1-RDN |
| P1-04 | ETH1-RDP |
| P1-06 | ETH1-LINK10# |
| P1-08 | **GND** |
| P1-10 | ETH1-ACT# |
| P1-12 | SPARE |
| P1-14 | **GND** |
| P1-16 | GPIO5 |
| P1-18 | GPIO25 |
| P1-20 | VCC-RTC |
| P1-22 | COMA-RX |
| P1-24 | COMA-TX |
| P1-26 | **GND** |
| P1-28 | COMC-RX |
| P1-30 | COMC-TX |
| P1-32 | COMC-DCD# |
| P1-34 | COMC-DTR# |
| P1-36 | COMC-DSR# |
| P1-38 | **GND** |
| P1-40 | COMC-CTS# |
| P1-42 | COMC-RTS# |
| P1-44 | COMC-RIN# |
| P1-46 | IDE-RD# |
| P1-48 | IDE-WR# |
| P1-50 | **GND** |
| P1-52 | LB/IDE-CS1# |
| P1-54 | LB-IRQ1 |
| P1-56 | DEBUG1 |
| P1-58 | DEBUG0 |
| P1-60 | SSI-DOUT |
| P1-62 | **GND** |
| P1-64 | LB-A0 |

| | **P1-B** |
|---|---|
| P1-01 | ETH1-TDP |
| P1-03 | ETH1-TDN |
| P1-05 | ETH1-LINK100# |
| P1-07 | **VCORE** |
| P1-09 | WP1# |
| P1-11 | RST-IN# |
| P1-13 | GPIO6 |
| P1-15 | GPIO27 |
| P1-17 | PME# |
| P1-19 | **VCORE** |
| P1-21 | SUSP-IN |
| P1-23 | COMB-RX |
| P1-25 | COMB-TX |
| P1-27 | COMD-RX |
| P1-29 | COMD-TX |
| P1-31 | **VCC3-3** |
| P1-33 | COMD-DCD# |
| P1-35 | COMD-DTR# |
| P1-37 | COMD-DSR# |
| P1-39 | COMD-CTS# |
| P1-41 | COMD-RTS# |
| P1-43 | **VCORE** |
| P1-45 | COMD-RIN# |
| P1-47 | LB/IDE-CS0# |
| P1-49 | IDE-IRQ |
| P1-51 | LB-IRQ0 |
| P1-53 | TS-PX |
| P1-55 | **VCORE** |
| P1-57 | TS-PY |
| P1-59 | SSI-DIN |
| P1-61 | SSI-CLK |
| P1-63 | LB-A1 |

| | | | |
|---|---|---|---|
| P1-66 | LB-A2 | P1-65 | LB-A3 |
| P1-68 | LB-A4 | P1-67 | **VCC3-3** |
| P1-70 | LB-A6 | P1-69 | LB-A5 |
| P1-72 | LB-A8 | P1-71 | LB-A7 |
| P1-74 | **GND** | P1-73 | LB-A9 |
| P1-76 | LB-A10 | P1-75 | LB-A11 |
| P1-78 | LB-A12 | P1-77 | LB-A13 |
| P1-80 | LB-A14 | P1-79 | **VCORE** |
| P1-82 | LB-A16 | P1-81 | LB-A15 |
| P1-84 | LB-A18 | P1-83 | LB-A17 |
| P1-86 | **GND** | P1-85 | LB-A19 |
| P1-88 | LB-A20 | P1-87 | LB-A21 |
| P1-90 | LB-A22 | P1-89 | LB-A23 |
| P1-92 | LB-A24 | P1-91 | **VCORE** |
| P1-94 | LB-D0 | P1-93 | LB-A25 |
| P1-96 | LB-D2 | P1-95 | LB-D1 |
| P1-98 | **GND** | P1-97 | LB-D3 |
| P1-100 | LB-D4 | P1-99 | LB-D5 |
| P1-102 | LB-D6 | P1-101 | LB-D7 |
| P1-104 | LB-D8 | P1-103 | **VCC3-3** |
| P1-106 | LB-D10 | P1-105 | LB-D9 |
| P1-108 | LB-D12 | P1-107 | LB-D11 |
| P1-110 | **GND** | P1-109 | LB-D13 |
| P1-112 | LB-D14 | P1-111 | LB-D15 |
| P1-114 | LB-IOCS16# | P1-113 | LB-IORDY |
| P1-116 | LB-RD# (a) | P1-115 | **VCORE** |
| P1-118 | LB-WR# (b) | P1-117 | PCM-MEMR# (c ) |
| P1-120 | PCM-MEMW# (d) | P1-119 | PCM-IOR# (e) |
| P1-122 | **GND** | P1-121 | PCM-IOW# (f) |
| P1-124 | PCM-CE1# | P1-123 | PCM-WAIT# |
| P1-126 | PCM-CDA# | P1-125 | PCM-RST# |
| P1-128 | PCM-INT0 | P1-127 | **VCORE** |
| P1-130 | PCM-WE# | P1-129 | PCM-REG# |
| P1-132 | PCM-SKTSEL | P1-131 | PCM-CE2# |
| P1-134 | **GND** | P1-133 | LB-CS0# |
| P1-136 | USB3-P[1] | P1-135 | LB-CS1# |
| P1-138 | USB3-N[2] | P1-137 | RST-OUT# |
| P1-140 | **VCC5** | P1-139 | **VCC3-3** |

[1] For version 2.x  available only if WIFI (W option) isn't assembled
[2] For version 2.x  available only if WIFI (W option) isn't assembled

| | P2-A |
|---|---|
| P2-02 | **GND** |
| P2-04 | SPARE |
| P2-06 | PCI-INTA# |
| P2-08 | PCI-INTB# |
| P2-10 | LPC-LAD0 |
| P2-12 | LPC-LAD2 |
| P2-14 | **GND** |
| P2-16 | PCI-CLK0 |
| P2-18 | PCI-REQ1# |
| P2-20 | PCI-AD0 |
| P2-22 | PCI-AD1 |
| P2-24 | PCI-AD3 |
| P2-26 | **GND** |
| P2-28 | PCI-AD6 |
| P2-30 | PCI-CBE0# |
| P2-32 | PCI-AD9 |
| P2-34 | PCI-AD10 |
| P2-36 | PCI-AD12 |
| P2-38 | **GND** |
| P2-40 | PCI-AD15 |
| P2-42 | PCI-PAR |
| P2-44 | PCI-PERR# |
| P2-46 | PCI-STOP# |
| P2-48 | PCI-TRDY# |
| P2-50 | **GND** |
| P2-52 | PCI-CBE2# |
| P2-54 | PCI-AD17 |
| P2-56 | PCI-AD19 |
| P2-58 | PCI-AD20 |
| P2-60 | PCI-AD22 |
| P2-62 | **GND** |
| P2-64 | PCI-AD24 |
| P2-66 | PCI-AD26 |
| P2-68 | PCI-AD28 |

| | P2-B |
|---|---|
| P2-01 | PCI-REQ0# |
| P2-03 | PCI-GNT0# |
| P2-05 | PCI-GNT1# |
| P2-07 | **VCC3-3** |
| P2-09 | LPC-LAD1 |
| P2-11 | LPC-LAD3 |
| P2-13 | LPC-SERIRQ |
| P2-15 | LPC-LFRAME# |
| P2-17 | LPC-LDRQ# |
| P2-19 | **VCORE** |
| P2-21 | PCI-AD2 |
| P2-23 | PCI-AD4 |
| P2-25 | PCI-AD5 |
| P2-27 | PCI-AD7 |
| P2-29 | PCI-AD8 |
| P2-31 | **VCORE** |
| P2-33 | PCI-AD11 |
| P2-35 | PCI-AD13 |
| P2-37 | PCI-AD14 |
| P2-39 | PCI-CBE1# |
| P2-41 | PCI-SERR# |
| P2-43 | **VCC3-3** |
| P2-45 | PCI-DEVSEL# |
| P2-47 | PCI-IRDY# |
| P2-49 | PCI-FRAME# |
| P2-51 | PCI-AD16 |
| P2-53 | PCI-AD18 |
| P2-55 | **VCORE** |
| P2-57 | PCI-AD21 |
| P2-59 | PCI-AD23 |
| P2-61 | PCI-CBE3# |
| P2-63 | PCI-AD25 |
| P2-65 | PCI-AD27 |
| P2-67 | **VCORE** |

| | | | |
|---|---|---|---|
| P2-70 | PCI-AD29 | P2-69 | PCI-AD30 |
| P2-72 | PCI-AD31 | P2-71 | TS-MX |
| P2-74 | **GND** | P2-73 | TS-MY |
| P2-76 | PP-PD3 | P2-75 | PP-PD2 |
| P2-78 | PP-PD4 | P2-77 | PP-PD1 |
| P2-80 | PP-PD5 | P2-79 | **VCC3-3** |
| P2-82 | PP-PD6 | P2-81 | PP-PD0 |
| P2-84 | PP-PD7 | P2-83 | PP-STROBE# |
| P2-86 | **GND** | P2-85 | PP-ALF# |
| P2-88 | PP-ACK# | P2-87 | PP-ERROR# |
| P2-90 | PP-BUSY | P2-89 | PP-INIT# |
| P2-92 | PP-PE | P2-91 | **VCORE** |
| P2-94 | PP-SLCT | P2-93 | PP-SLCTIN# |
| P2-96 | LCD-LP | P2-95 | LCD-B1 |
| P2-98 | **GND** | P2-97 | LCD-B2 |
| P2-100 | LCD-B3 | P2-99 | LCD-B4 |
| P2-102 | LCD-B5 | P2-101 | LCD-G0 |
| P2-104 | LCD-G1 | P2-103 | **VCORE** |
| P2-106 | LCD-G2 | P2-105 | LCD-G3 |
| P2-108 | LCD-G4 | P2-107 | LCD-G5 |
| P2-110 | **GND** | P2-109 | LCD-R1 |
| P2-112 | LCD-SCK | P2-111 | LCD-FRM |
| P2-114 | LCD-DE-M | P2-113 | LCD-R2 |
| P2-116 | LCD-R3 | P2-115 | **VCORE** |
| P2-118 | LCD-R4 | P2-117 | LCD-R5 |
| P2-120 | PS2-KCLK | P2-119 | PS2-KDAT |
| P2-122 | **GND** | P2-121 | IRDA-TX |
| P2-124 | PS2-MDAT | P2-123 | IRDA-RX |
| P2-126 | PS2-MCLK | P2-125 | PCM-CDB# |
| P2-128 | PCM-INT-RDYB | P2-127 | **VCORE** |
| P2-130 | AUD-INR | P2-129 | AUD-SPDIF |
| P2-132 | AUD-INL-MIC | P2-131 | AUD-OUTL |
| P2-134 | **GND** | P2-133 | USB-OVC# |
| P2-136 | AUD-OUTR | P2-135 | **VCC3-3** |
| P2-138 | USB1-P | P2-137 | USB2-P |
| P2-140 | USB1-N | P2-139 | USB2-N |

| | P3-A |
|---|---|
| P3-02 | ETH2-RDP |
| P3-04 | ETH2-RDN |
| P3-06 | ETH2-LINK10# |
| P3-08 | **GND** |
| P3-10 | ETH2-ACT# |
| P3-12 | SPARE |
| P3-14 | **GND** |
| P3-16 | PCI-CLK1 |
| P3-18 | PCI-GNT2# |
| P3-20 | PCI-INTC# |
| P3-22 | PCI-REQ2# |
| P3-24 | PCI-CLK2 |
| P3-26 | **GND** |
| P3-28 | COMA-RTS# |
| P3-30 | COMA-RIN# |
| P3-32 | COMB-RTS# |
| P3-34 | COMB-RIN# |
| P3-36 | COMB-DTR# |
| P3-38 | **GND** |
| P3-40 | GPIO5 |
| P3-42 | GPIO7 |
| P3-44 | GPIO9 |
| P3-46 | GPIO10 |
| P3-48 | GPIO12 |
| P3-50 | **GND** |
| P3-52 | GPIO15 |
| P3-54 | GPIO16 |
| P3-56 | GPIO17 |
| P3-58 | GPIO18 |
| P3-60 | GPIO19 |
| P3-62 | **GND** |
| P3-64 | TIMER-START |
| P3-66 | IDE-RDY# |
| P3-68 | LB-CS2# |

| | P3-B |
|---|---|
| P3-01 | ETH2-TDN |
| P3-03 | ETH2-TDP |
| P3-05 | ETH2-LINK100# |
| P3-07 | **VCORE** |
| P3-09 | DISP-EN (rev 2 only) |
| P3-11 | SPARE |
| P3-13 | PCI-REQ3# |
| P3-15 | PCI-GNT3# |
| P3-17 | PCI-INTD# |
| P3-19 | **VCC3-3** |
| P3-21 | COMA-DCD# |
| P3-23 | COMA-DTR# |
| P3-25 | COMA-DSR# |
| P3-27 | COMA-CTS# |
| P3-29 | COMB-DCD# |
| P3-31 | **VCORE** |
| P3-33 | COMB-CTS# |
| P3-35 | COMB-DSR# |
| P3-37 | GPIO4 |
| P3-39 | GPIO6 |
| P3-41 | GPIO8 |
| P3-43 | **VCORE** |
| P3-45 | GPIO11 |
| P3-47 | GPIO13 |
| P3-49 | GPIO14 |
| P3-51 | FW-TPBM |
| P3-53 | FW-TPBP |
| P3-55 | **VCC3-3** |
| P3-57 | FW-TPAP |
| P3-59 | FW-TPAM |
| P3-61 | TIMER-OUT |
| P3-63 | IDE-DREQ |
| P3-65 | IDE-DACK# |
| P3-67 | **VCORE** |

| | |
|---|---|
| P3-70 | LB-CS3# |
| P3-72 | CLKIN |
| P3-74 | **GND** |
| P3-76 | CLKOUT |
| P3-78 | VIP-CS |
| P3-80 | VIP-D0 |
| P3-82 | VIP-D1 |
| P3-84 | VIP-D2 |
| P3-86 | **GND** |
| P3-88 | VIP-CLK |
| P3-90 | VIP-D3 |
| P3-92 | VIP-D4 |
| P3-94 | VIP-D5 |
| P3-96 | VIP-D6 |
| P3-98 | **GND** |
| P3-100 | WP2# |
| P3-102 | VCC3-STBY |
| P3-104 | VCC3-STBY |
| P3-106 | VCC3-STBY |
| P3-108 | SPARE |
| P3-110 | **GND** |
| P3-112 | SPARE |
| P3-114 | PCM-BVD1 |
| P3-116 | PCM-VPPEN |
| P3-118 | PCM-CE# |
| P3-120 | AC97-BITCLK |
| P3-122 | **GND** |
| P3-124 | AC97-RST# |
| P3-126 | LCD-B0 |
| P3-128 | LCD-R0 |
| P3-130 | LCD-VDDEN |
| P3-132 | CRT-R |
| P3-134 | **GND** |
| P3-136 | CRT-G |
| P3-138 | TV-OUT |
| P3-140 | CRT-VSYNC |

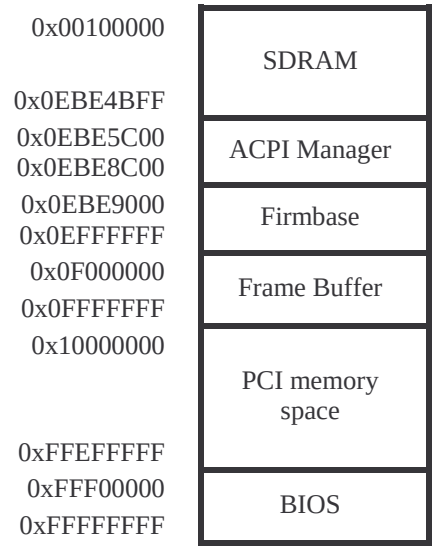
| | |
|---|---|
| P3-69 | LB-DREQ0 |
| P3-71 | LB-DACK0# |
| P3-73 | LB-DREQ1 |
| P3-75 | LB-DACK1# |
| P3-77 | JTAG-TCK |
| P3-79 | **VCORE** |
| P3-81 | JTAG-TMS |
| P3-83 | JTAG-TDI |
| P3-85 | JTAG-TDO |
| P3-87 | JTAG-TRST# |
| P3-89 | VIP-D7 |
| P3-91 | **VCC3-3** |
| P3-93 | VIP-ODD/EVEN |
| P3-95 | SLEEP-OUT# |
| P3-97 | SPARE |
| P3-99 | **VCC5-STBY** |
| P3-101 | SPARE |
| P3-103 | **VCORE** |
| P3-105 | SPARE |
| P3-107 | VCC3-STBY |
| P3-109 | VCC3-STBY |
| P3-111 | VCC3-STBY |
| P3-113 | PCM-BVD2 |
| P3-115 | **VCORE** |
| P3-117 | PCM-VCCEN |
| P3-119 | AC97-SDIN0 |
| P3-121 | AC97-SDIN1 |
| P3-123 | AC97-SDOUT |
| P3-125 | AC97-SYNC |
| P3-127 | **VCC3-3** |
| P3-129 | CRT-HSYNC |
| P3-131 | **VCC5** |
| P3-133 | CRT-B |
| P3-135 | **VCC3-3** |
| P3-137 | USB4-P |
| P3-139 | USB4-N |

# 5. MEMORY and I/O mapping

## 5.1. Memory space usage in the first 1MB

| | |
|---|---|
| 0000:0 - 9FFF:F | Standard Low memory |
| A000:0 - BFFF:F | Graphic Memory<br>Available if graphics controller is not enabled |
| C000:0 - C7FF:F | VGA BIOS |
| DC00:0 - DFFF:F | SMM reserved area |
| E000:0 - FFFF:F | BIOS |

## 5.2. Memory space usage above first 1MB




The “Frame Buffer” cannot be accessed directly, this address space is left unused in the system; above table includes a 16Mb “Frame buffer”(can vary from 2- 128Mb)

## 5.3. I/O space Usage

The table below specifies all I/O regions known to be used in standard / legacy PC architecture and regions used by on-board peripheral devices.

| Address | Function | Comments |
|---|---|---|
| 0x000-0x00F | Slave DMA regs | |
| 0x020-0x021 | Master Interrupt controller | |
| 0x040-0x043 | PIT registers | |
| 0x060-0x060 | Keyboard / PS2 mouse registers | |
| 0x061-0x061 | System speaker | |
| 0x064-0x064 | Keyboard / PS2 mouse registers | |
| 0x070-0x071 | System CMOS/real time clock | |
| 0x081-0x083 | DMA controller registers | |
| 0x084-0x086 | General purpose IO register | |
| 0x087 | DMA controller registers | |
| 0x088 | General purpose IO register | |
| 0x089-0x08B | DMA controller registers | |
| 0x08F-0x091 | DMA controller registers | |
| 0x0A0-0x0A1 | Slave interrupt controller registers | |

| | | |
|---|---|---|
| 0x0F0-0x0FF | Numeric Data Processor | |
| 0x1F0-0x1F7 | IDE0 controller | |
| 0x2F8-0x2FF | COM-B | |
| 0x3B0-0x3DF | Legacy VGA base | |
| 0x3E0-0x3E1 | PCMCIA / CardBus | |
| 0x3F8-0x3FF | COM-A | |
| 0x3F0-0x3F7 | alternate IDE0 address | |
| 0xCF8-0xCFF | PCI configuration space access window | |
| 0xD400-0xD47F | Geode LX Audio driver | |
| 0xD800-0xD80F | PCI IDE controller | |
| 0xF400-0xF4FF | Core Ethernet controller | |
| 0xF800-0xF8FF | Base Ethernet controller | |

## 5.4. BIOS Flash Mapping

| Starting address in flash window | End address in flash window | Usage |
|---|---|---|
| 0xFFF80000 | 0xFFFCFFFF | BIOS area |
| 0xFFFD0000 | 0xFFFDFFFF | Setup and configuration block |
| 0xFFFC0000 | 0xFFFFFFFF | BIOS area |

**Setup and Configuration Block Usage**

| Addresses | Value / Description |
|---|---|
| 0x0000-0x0001 | 0xAAAA –signature that a valid CMOS image is in the flash |
| 0x0002-0x01FF | CMOS image, including RTC |

# 6. Power Consumption

The current consumption measurements specified below were performed on a system with the following configuration:

- CM-iGLX-D256-C500-N512-E-AT
- ATX-E-L-V-A-C3-X6-Y2-Z6

Current consumption is specified for both boards. However, 95% of the total current is consumed by the CM-iGLX module.

| CPU Clock | Activity | Current from 3.3V |
|---|---|---|
| 200 MHz | Idle | 0.98A |
| | Max load | 1.04A |
| 500 MHz | Idle | 1.26A |
| | Max load | 1.51A |

Minimum power consumption : [3.3V * 0.98A] = 3.25 watt

Maximum power consumption : [3.3V * 1.51A] = 5.0 watt

# 7. Performance Benchmarks

Measured with CPU @ 500 MHz, using SiSoft Sandra bench test under Windows.

| | |
|---|---|
| Drystone (integer) | 990 MIPS |
| Wetstone (floating point) | 270 MFLOPS |
| DDR bandwidth | 557MB/s |

# 8. Operating Temperature Ranges

The CM-iGLX is available with three options for operating temperature range:

| Range | Temp. | Description |
|---|---|---|
| Commercial | $0^o$ to $70^o$ C | Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested. |
| Extended | $-20^o$ to $70^o$ C | Every card is individually tested for the lower limit ($-20^o$ C) qualification. |
| Industrial | $-40^o$ to $85^o$ C | Every card is individually tested for both lower and upper limits and at several midpoints. |

* Temp - maximum temperature measured on hottest spot of the card - CPU case.

For more information regarding the availability of cards for industrial grade, please refer to [Products] >> [Industrial Temperature] links in CompuLab's website.

**Heat Dissipation**

Heatsink is not mandatory for CM-iGLX operation, however it does affect the CM-iGLX's working condition. In still air CPU temperature can rise up to 35°C above ambient. For example, at a room temperature of 25°C, a

powered card without heatsink will reach 60°C, which is just 10°C below the upper limit. Still air and absence of heatsink are therefore limiting maximum allowed ambient temperature. If you need wider operation range, you should consider using forced airflow and/or heatsink.