CompuLab

CM-iTC
Computer-On-Module

Reference Guide

Table of Contents

1. Revision Notes

Date	Description
30-October-2010	Preliminary release
09-February-2011	Added “Power Consumption” and “Performance Benchmarks”

Please check for a newer revision of this manual in CompuLab's website - http://www.compulab.co.il/iTC/html/iTC-developer.py links. Compare the revision notes of the updated manual from the website with those of the printed version you have.

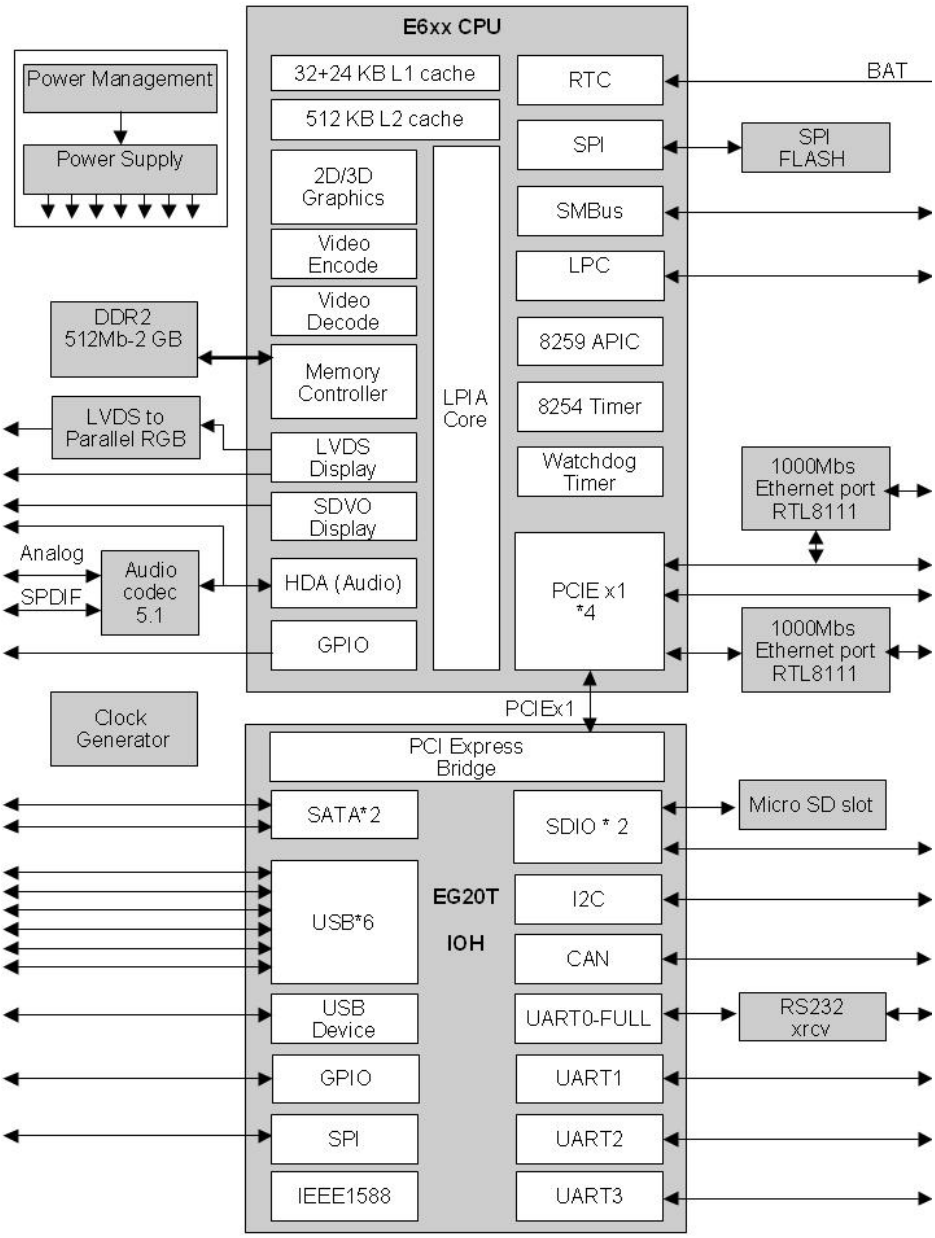
2. Overview

2.1. Highlights

▪ **Full Featured PC-Compatible Computer-On-Module** ▪ **Intel Atom E6xx CPU @1.6GHz, EG20T chipset** ▪ **2 GB DDR2** ▪ **On-board microSD socket** ▪ **LVDS, parallel RGB and SDVO display interfaces for LCD panels up to 1980x1020** ▪ **H.264, MPEG-4, MPEG-2, VC-1 , WMV9 codecs hardware acceleration** ▪ **Video encoding** ▪ **2XSATA hard disk interface** ▪ **2 x 1000 BaseT Ethernet ports** ▪ **6 x USB ports** ▪ **USB device port** ▪ **SDIO port** ▪ **Sound codec with support for speaker, microphone and SPDIF.** **HD audio bus** ▪ **PCIexpress and LPC extension busses** ▪ **4xSerial port** ▪ **2xI2C** ▪ **CAN, SPI, GPIO interfaces** ▪ **IEEE1588 interface over CAN** ▪ **Programmable watchdog timer** ▪ **6 watt power consumption** ▪ **Small size - 75 x 65 mm**	**The CM-iTC** packs up-to-date year 2010 technologies into the most compact, lightweight PC-on-module available. Its on-board resources suffice to smoothly run operating systems such as Linux, Windows XP and Windows 7, on a credit-card sized board capable of running on a small battery. The board's specifications, in addition to its low cost, make it an ideal building block for any embedded application. The feature set of the CM-iTC comprises a 32-bit X86-compatible CPU, DDR2, micro SD-based internal storage and vital computing peripherals. For embedded applications, the CM-iTC provides a variety of display interfaces, two SATA interfaces, PCIexpress buses, two 1000Mbit Ethernet ports, four serial ports, 6 USB ports and one USB slave port, CAN, SPI, two I2C, general purpose I/O lines and many other essential functions. The user interface is supported by an enhanced graphics controller, USB interface for keyboard / mouse and audio system.

2.2. Block Diagram

2.3.



Features

"Option" column specifies the configuration code required to have the particular feature.
"+" means that the feature is available always.

CPU, Memory and Busses

Feature	Specifications	Option
CPU	Intel Atom E6xx Processor: E620@600MHz, E640@ 1GHz, E660@1.3GHz, E680@1.6GHz, L2-512KB (dynamic sizing), L1- 32KB IC, 24KB DC. Intel Deep Power Down (C6) technology support	C
DRAM	512MB/1024 MB/2048 DDR2, 800 MHz, 32-bit	D
BIOS Flash	SPI based, 2 MByte, on-board reprogrammable	+
Solid State Disk	8-32 GB on-board storage based on bootable micro-SD with SDHC support	Nx
External Busses	PCI express, LPC, HD audio	+
PCI express bus	PCI Express Base Specification, Revision 1.0a. One or two lanes. Note: Two lanes are available if fewer than two Ethernet controllers are assembled.	+
LPC bus	Host, 33 MHz, Intel LPC v1.0 compatible	+

Peripherals

Feature	Specifications	Option
Graphics	Resolution up to 1920 x 1080 x 32 bpp frame buffer in	+

Controller	system memory, 2D, 3D graphics accelerator and multimedia accelerator optimized for HD video	
Display Interface	LCD – 24 bpp parallel RGB for TFT panels LVDS – 24 bpp, 4 data and 1 clk pairs for TFT panels SDVO – can be directly connected to DVI / HDMI / VGA transmitters	L + +
USB	6 Host USB 2.0 ports, 480 Mbps, EHCI / UHCI-compliant	+
USB slave	USB device interface	+
Serial Port	4 UART's, one full with RS232 and 3 RX/TX	+
GPIO	18 (14 dedicated lines + 4 shared line)	+
Hard Disk Interf.	2xSATA-II	+
Kbrd & Mouse	USB	+
Ethernet	Two 1000 Mb/s ports, activity LED's. RTL8111	Ex
Audio codec	ALC662 controller, HD audio interface, stereo microphone and line inputs, 5.1 channel SPDIF output	A
SDIO	One 4-bit SDIO port	
SPI	Serial Parallel Interface	+
CAN	CAN bus interface	+
RTC	Real Time Clock, powered by an external lithium battery	+
Watchdog	Wide range programmable watchdog timer operational at early power-up stage	+

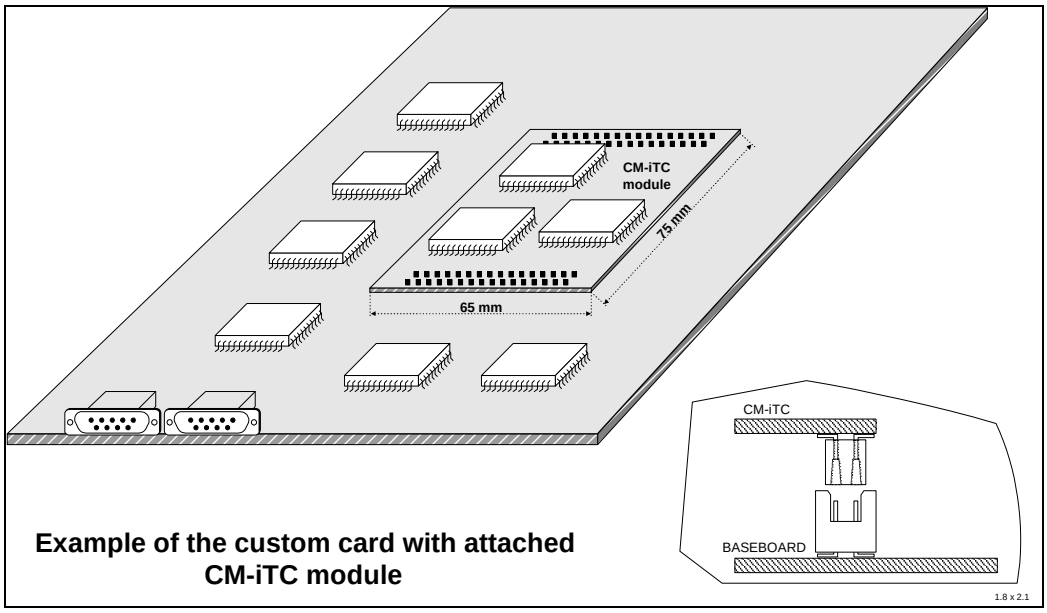
Electrical, Mechanical and Environmental Specifications

Supply Voltage	5V
Active power consumption	5 - 7 W, depending on configuration and CPU speed
Dimensions	65 x 75 x 8 mm
Weight	37 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0^{o} to 70^{o} C

	Extended: -20° to 70° C Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm. Insertion / removal up to 50 cycles

2.4. General Description

The CM-iTC is a miniature single-board computer packed as a module. It contains a CPU, chipset, memory, flash disk and peripherals. All interface functions of the CM-iTC are routed through miniature high-density connectors, designed for piggyback attachment to a custom baseboard, as shown in the picture below.



Example of the custom card with attached CM-iTC module

Atom E6xx CPU Core Architecture

The CM-iTC utilizes Intel® Atom™ Processor E6xx Series in the next-generation Intel® architecture (IA) CPU for small form factor, ultra-low power embedded segments based on a new architecture partitioning. The new architecture partitioning integrates a 3D graphics engine, memory controller and other blocks with an IA CPU core.
The processor departs from the proprietary chipset interfaces used by other IA CPU's to embrace an open-standard, industry-proven PCI Express* v1.0 interface. This allows it to be paired with customer-defined IOH, ASIC, FPGA and off-the-shelf discrete components. This provides ultimate flexibility in IO solutions. This is important for deeply embedded applications in which, unlike for traditional PC-like applications, IO's differ from one application to the other.

The following list provides some of the key features of this processor:

- New single-core processor for embedded devices with enhanced performance
- On-die, primary 32-kB 4-way L1 instructions cache and 24-kB 6-way L1 data cache
- Supports Hyper-Threading Technology 2-threads
- On-die 512-kB, 8-way L2 cache
- Macro-operation execution support
- 2-wide instruction decode and in-order execution
- Intel® Virtualization Technology (Intel® VT)
- Intel® Streaming SIMD Extension 2 and 3 (Intel® SSE2 and Intel® SSE3) and supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Deep Power Down C6-based Technology
- L2 Dynamic Cache Sizing
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Executes Disable Bit support for enhanced security

2.5. Intel® Platform Controller Hub EG20T

The CM-iTC uses an Intel® Platform Controller Hub (Intel® IOH) EG20T Topcliff chipset. The Topcliff IOH provides extensive I/O support including:

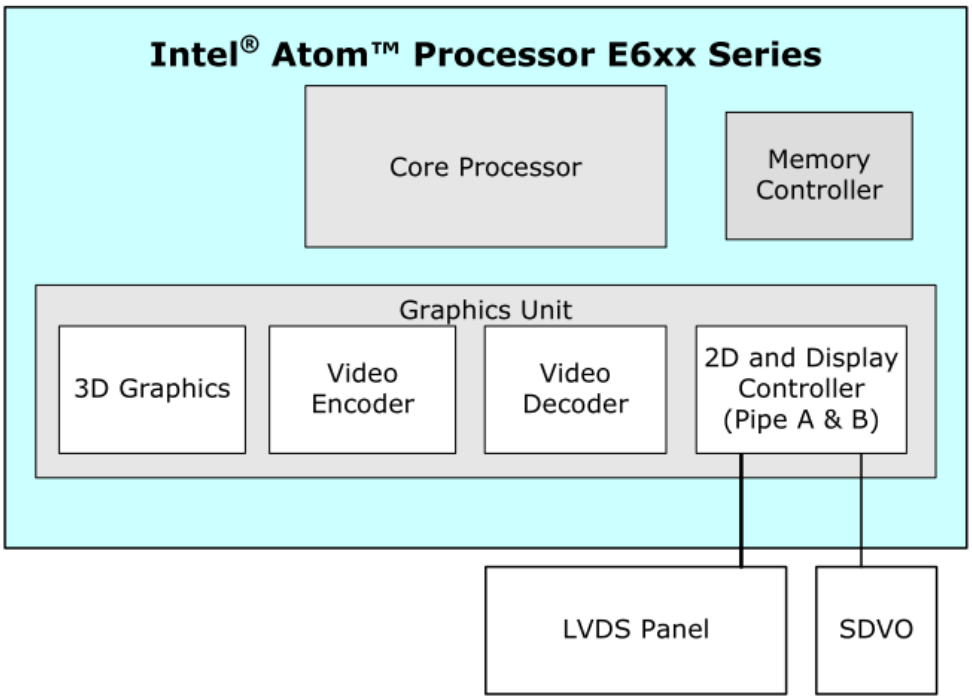
- Fully compliant with all the required features of the PCI Express* 1.1 (2.5Gbps) specification. It is used to connect to the Tunnel Creek Processor.
- 6 USB 2.0 ports (2 USB 2.0 Hosts; 3 ports for each host)
- USB Device
- 2 SATA I, II (3GBps) - including AHCI
- 2 SD Host Controllers (SDHC 2.0 class VI)
- IEEE-1588 (Clock Synchronization) over CAN
- SPI full duplex up to 5Mbps
- CAN (Protocol version 2.0B) up to 1 Mbps
- I2C bus (ver 2.1) conformed controller up to 400kHz

- 1 full UART (8 lines) up to 4Mbps
- 3 RX/TX UART's up to 962 Kbps
- GPIO's

3. Peripherals and Functions

3.1. Display Controller

The Intel® Atom™ Processor E6xx Series contains an integrated graphics engine, video decode and encode capabilities, and a display controller that can support one LVDS display and one SDVO display :



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3-D Core Key Features:

- Two pipe scalable unified shader implementation
- Texture maximum size = 2048 x 2048
- Programmable 4x multi-sampling anti-aliasing (MSAA)
- Optimized memory efficiency using multi-level cache architecture
- Unified programming model
- SIMD pipeline supporting operations

- Static and dynamic flow control
- Procedural geometry
- External data access

Video Decode Overview

The video decode accelerator improves video performance / power by providing hardware-based acceleration at the macroblock level (variable length decode stage entry point). The Intel SCH supports full hardware acceleration of the following video decode standards:

CODEC	PROFILE	LEVEL
H.264	Baseline profile	L3
H.264	Main profile	L4.1 (1080p @ 30fps)
H.264	High profile	L4.1 (1080p @ 30fps)
MPEG2	Main profile	High
MPEG4	Simple profile	L3
MPEG4	Advanced simple profile	L5
VC1	Simple profile	Medium
VC1	Main profile	High
VC1	Advanced profile	L3 up to (1080p @ 30fps)
WMV9	Simple profile	Medium
WMV9	Main profile	High

The video decode function is performed in four processing modules:
- Entropy coding processing
- Motion compensation
- De-blocking
- Final pixel formatting

Video Encode

The Intel® Atom™ Processor E6xx Series supports full hardware video encode. The video encode hardware accelerator improves video capture performance by providing dedicated hardware-based acceleration. Other benefits are low power consumption, low host processor load and high picture quality. The processor supports full hardware acceleration of the following video encode:
- Permits 720P30 H.264 BP encode
- MPEG4 encode and H.263 video conferencing

With integrated hardware encoding the host processor only needs to deal with higher-level control code functions, such as providing the image to encode and processing the video elementary stream.
The processor supports a standard definition video encoder that has as an input, a

series of frames which are encoded to produce an elementary bit stream. This section describes the top level interactions between all modules contained in encode hardware. In general, the encoding process is pipelined into a number of stages. For MPEG-4/H.263/H.264 encoding, the data is processed in macroblocks, with minimum interaction of the embedded controller within each processing stage.
The Intel® Atom™ Processor E6xx Series supports the following profiles and levels as shown below:

Standard	Profile	Maximum Bit Rate (bps)	Typical Picture and Frame Rate
H.264	BP	128K	QCIF @15 fps
H.264	BP	192K	QCIF @30 fps
H.264	BP	384K	CIF @15 fps or QVGA @ 20 fps
H.264	BP	2M	CIF @ 30 fps or QVGA @ 30 fps
H.264	BP	10M	720x480 @ 30 fps, 720x576 @ 25 fps, VGA @ 30 fps
MPEG4	SP	64K	QCIF @ 15 fps
MPEG4	SP	128K	QCIF @ 30 fps, CIF @ 15 fps, QVGA @ 15 fps
MPEG4	SP	384K	CIF @ 30 fps or QVGA @ 30 fps
MPEG4	SP	128K	QCIF @ 15 fps
MPEG4	SP	384K	QCIF @ 30 fps, CIF @ 15 fps, QVGA @ 15 fps
MPEG4	SP	768K	CIF @ 30 fps or QVGA @ 30 fps
MPEG4	SP	8M	720x480 @ 30 fps, 720x576 @ 25 fps, VGA @ 30 fps
H.263	BP	64K	QCIF @ 15 fps
H.263	BP	128K	QCIF @ 30 fps, CIF @ 15 fps, QVGA @ 15 fps
H.263	BP	384K	CIF @ 30 fps, QVGA @ 30 fps
H.263	BP	2M	CIF @ 30 fps, QVGA @ 30 fps
H.263	BP	128K	QCIF @ 15 fps
H.263	BP	4M	CIF @ 60 fps
H.263	BP	8M	720x240 @ 60 fps, 720x288 @ 50 fps
H.264	MP	14M	1280x720 @ 30 fps
MPEG4	SP		1280x720 @ 30 fps
H.263	BP	16M	720x480 @ 60 fps, 720x576 @ 50 fps

Encode Specifications Supported

ITU-T H.264 (03/2005)
• Series H—Audio-visual and multimedia systems. Infrastructure of audio-visual services—Coding of moving video—Advanced video coding for generic audio-visual services

H.263 (01/2005)

• Series H—Audio-visual and multimedia systems. Infrastructure of audio-visual services—Coding of moving video – Video coding for low bit rate communication MPEG4 (06/2004)
• ISO/IEC 14496-2 Second edition, Information Technology—Coding of audio-visual objects - Part 2: Visual

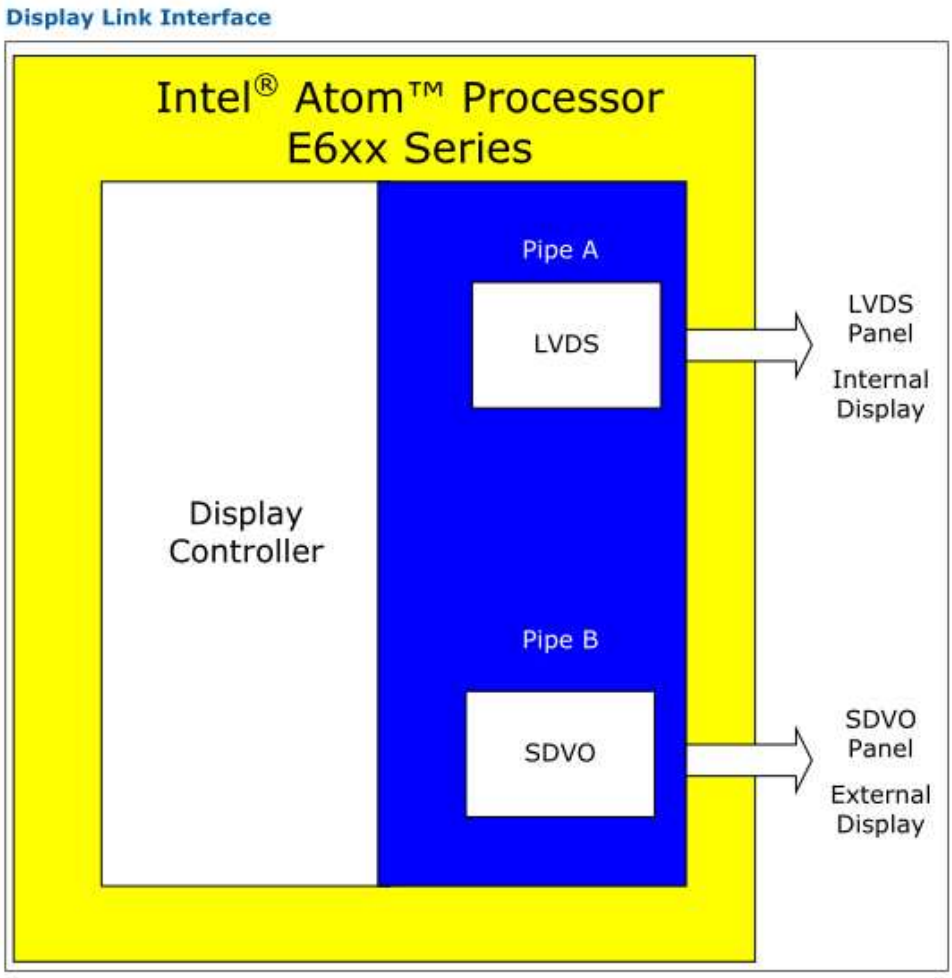
Display

The Display Controller provides the 2D graphics functionalities for the display pipeline. The Display Controller converts a set of source images or surfaces, merges them and then delivers them according to the proper timing to output interfaces connected to the LVDS display devices. Along the display pipe, the display data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.
The Display Controller supports five display planes and two cursor planes and runs in the core display clock domain. The Display Controller supports the following features:
• Seven planes: Display Plane A, B, Display C/sprite, Overlay, Cursor A, Cursor B and VGA
• Dual Independent display pipes -- Pipe A and Pipe B
— Display Pipe A: Outputs directly as LVDS
— Display Pipe B: Outputs directly as SDVO
• Supports 64-bit FP color format, NPO2 Tiling and 180 degree rotation
• Output pixel width: 24-bit RGB (LVDS 24.1, 24.0 and 18.0 as well).
• Supports NV12 data format
• 3x3 Panel Fitter shared by two pipes
• Support Constant Alpha mode on Display C/Video sprite plane
• DPST 3.0
The display contains the following functions:
• Display data fetching
• Out of order display data handling
• Display blending
• Gamma correction
• Panel fitter function

Display Output Stages

The display output can be divided into three stages:
• Planes
— Request/Receive data from memory
— Format memory data into pixels
— Handle fragmentation, tiling, physical address mapping
• Pipes
— Generate display timing
— Scaling, LUT

• Ports
— Format pixels for output (LVDS or SDVO)
— Interface to physical layer



Display Ports

Display ports are the destination of the display pipes. These are the places where the display data ultimately appears to devices outside the graphics device. The Intel® Atom™ Processor E6xx Series has one dedicated LVDS and one SDVO port.
Since two display ports are available for its two pipes, the processor can support up to two different images on two different display devices. The timing and resolution for

these two images may differ. The CM-iTC also implements an LVDS to parallel 24-bit RGB converter (option L) allowing the connection of different parallel LCD's in addition to LVDS displays.

LVDS port

The System Controller Hub (Poulsbo SCH) supports a Low-Voltage Differential Signaling interface allowing the IGD to communicate directly with a flat-panel display. The LVDS interface supports pixel color depth of 18 or 24 bits and a max pixel clock of 112 MHz. To support LVDS Backlight Control, the Intel® Atom™ Processor E6xx Series will generate five types of messages to the display cluster. The display cluster will in turn drive VDDEN and BKLTEN and modulate the duty cycle before driving it out through BKLTCTL. These three signals are multiplexed with the normal GPIO pins under the LVDS_CTL_MODE (address to be defined). The DDC_CLK and DDC_DATA is emulated through software.

LVDS Interface:

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
LVDS_A0-	P1-52	ODIF	LVDS differential pair 0
LVDS_A0+	P1-54	ODIF	
LVDS_A1-	P1-51	ODIF	LVDS differential pair 1
LVDS_A1+	P1-53	ODIF	
LVDS_A2-	P1-58	ODIF	LVDS differential pair 2
LVDS_A2+	P1-60	ODIF	
LVDS_A3-	P1-57	ODIF	LVDS differential pair 3
LVDS_A3+	P1-59	ODIF	
LVDS_CLK-	P1-63	ODIF	LVDS differential clock
LVDS_CLK+	P1-65	ODIF	
LVDS_DID_CLK	P1-47	I/O	Display Data Channel Clock: I2C-based control signal (Clock) for EDID control
LVDS_DID_DAT	P1-49	I/O	Display Data Channel Data: I2C-Data for EDID control
LVDS_BLT_CTR	P1-48	O	LCD Backlight Control: This signal allows control of LCD brightness
LVDS-BLEN	P1-56	O	Panel backlight enable control
LVDS-PPEN	P1-61	O	Power sequencing control for panel driver electronics voltage VDD

Intel Serial DVO (SDVO) Display port

Display Pipe B is configured to use the SDVO port. The SDVO port can support a variety of display types (VGA, LVDS, DVI, TV-Out, etc.) for an external SDVO device. SDVO devices translate SDVO protocol and timings to the desired display format and timings. Up to 160 MHz pixel clocks supported.

SDVO Interface:

Baseboard conn		Type	Description
Signal	Pin		
SDVO_BCLK+	P1-30	ODIF	Serial Digital Video Channel B Clock
SDVO_BCLK-	P1-28	ODIF	
SDVO_BLUE+	P1-35	ODIF	Serial Digital Video Channel B Blue
SDVO_BLUE-	P1-33	ODIF	
SDVO_RED+	P1-42	ODIF	Serial Digital Video Channel B Red
SDVO_RED-	P1-40	ODIF	
SDVO_GREEN+	P1-29	ODIF	Serial Digital Video Channel B Green
SDVO_GREEN-	P1-27	ODIF	
SDVO_INT+	P1-36	IDIF	Serial Digital Video Input Interrupt
SDVO_INT-	P1-34	IDIF	
SDVO_FLDSTALL+	P1-41	IDIF	Serial Digital Video Field Stall
SDVO_FLDSTALL-	P1-39	IDIF	
SDVO_TVCLKIN+	P1-23	IDIF	Serial Digital Video TV-OUT Synchronization Clock pair
SDVO_TVCLKIN-	P1-21	IDIF	
SDVO_CTRL_CLK	P1-25	I/O	SDVO Control Clock (similar to I2C)
SDVO_CTRL_DAT	P1-32	I/O	SDVO Control Data (similar to I2C)

Notes

- SDVO signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum =1.5 V. Single-ended minimum = 0 V.
- A 100 nF decoupling capacitor must be used on all differential SDVO signals (see the SB-iTC reference schematic).

LCD Panel Interface

This interface is available only in modules with the "L" option.
LCD Interface:

Baseboard conn		Type	Description
Signal	Pin		
LCD-B0	P1-95	O	LCD Panel Data Bus.
LCD-B1	P1-96	O	
LCD-B2	P1-97	O	
LCD-B3	P1-99	O	
LCD-B4	P1-100	O	
LCD-B5	P1-101	O	
LCD-B6	P1-102	O	
LCD-B7	P1-104	O	
LCD-G0	P1-85	O	
LCD-G1	P1-87	O	
LCD-G2	P1-88	O	
LCD-G3	P1-89	O	
LCD-G4	P1-90	O	
LCD-G5	P1-92	O	
LCD-G6	P1-93	O	
LCD-G7	P1-94	O	
LCD-R0	P1-75	O	
LCD-R1	P1-76	O	
LCD-R2	P1-77	O	
LCD-R3	P1-78	O	
LCD-R4	P1-81	O	
LCD-R5	P1-82	O	
LCD-R6	P1-83	O	
LCD-R7	P1-84	O	
LCD-SCK	P1-108	O	Display Data Clock. Pixel clock for flat panel data
LCD-VSYNC	P2-107	O	VSYNC
LCD-HSYNC	P1-109	O	HSYNC
LCD-DE	P1-105	O	Display Enable signal (DE) for TFT Panels
LCD-PWREN	P1-106	O	Power sequencing control for panel VDD

3.2. SATA interface

The CM-iTC implements SATA storage interface (on the IOH) for physical storage devices.

The features of the SATA Controller are as follows:
- Supports SATA 1.5-Gbps Generation 1 and 3-Gbps Generation 2 speeds
- Supports two ports
- Compliant with Serial ATA Specification 2.6 and Advanced Host Controller Interface (AHCI) Revision 1.1 specifications
- Supports power management features including automatic Partial to Slumber transition
- An internal DMA engine per port
- Supports hardware-assisted Native Command Queuing for up to 32 entries
- Supports port Multiplier with command-based switching
- Supports Option ROM

SATA0 Interface:

Baseboard conn		Type	Description
Signal	Pin		
SATA0_RX+	P2-120	IDIF	SATA0 receive pair
SATA0_RX-	P2-118	IDIF	
SATA0_TX+	P2-126	ODIF	SATA0 transmit pair
SATA0_TX-	P2-124	ODIF	
SATA0_LED	P2-128	O	SATA0 activity led

SATA1 Interface:

Baseboard conn		Type	Description
Signal	Pin		
SATA1_RX+	P2-102	IDIF	SATA1 receive pair
SATA1_RX-	P2-100	IDIF	
SATA1_TX+	P2-95	ODIF	SATA1 transmit pair
SATA1_TX-	P2-93	ODIF	
SATA1_LED	P2-77	O	SATA1 activity led

3.3. PCI Express

The CM-iTC contains two x1 PCI Express expansion interfaces (when no Ethernet is assembled; otherwise, only one external PCIE is available) supporting the PCI Express Base Specification, Revision 1.0a. Each root port supports 2.5 GB/s bandwidth in each direction.
It is a high-bandwidth, low pin-count serial interface ideal for I/O expansion. An external graphics device can be used via one of the x1 PCI Express lanes/ports. Below are PCIE0, PCIE1 and the control signals group. PCIE0 is available only when no Ethernet or E1 option is selected. PCIE1 is always available.

PCIE0 signal group:

Baseboard conn	Type	Description

Signal	Pin		
PCIE0_RX+	P2-108	IDIF	PCIE0 receive pair
PCIE0_RX-	P2-106	IDIF	
PCIE0_TX+	P2-114	ODIF	PCIE0 transmit pair
PCIE0_TX-	P2-112	ODIF	

PCIE1 signal group:

Baseboard conn		Type	Description
Signal	Pin		
PCIE1_RX+	P2-107	IDIF	PCIE1 receive pair
PCIE1_RX-	P2-105	IDIF	
PCIE1_TX+	P2-113	ODIF	PCIE1 transmit pair
PCIE1_TX-	P2-111	ODIF	
PCIE_CLK1+	P2-83	ODIF	PCIE1 differential clock
PCIE_CLK1-	P2-81	ODIF	
PCIE_CLK1E#	P2-15	I	PCIE1 clock enable (has 8.2k internal PU) –to enable – 1k pull down should be used

PCIE control signals:

Baseboard conn		Type	Description
Signal	Pin		
PCIE_RST#	P2-104	O	PCIE reset signal when option E2 is assembled; otherwise, use general RESET# (P2-20) for this purpose.
PCI_WAKE#	P2-109	I	PCI Express* Wake Event: This signal indicates that a PCI Express port wants to wake the system.

Notes

- PCIE differential signals are compatible with PCI Express 1.0a Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum =1.5 V. Single-ended minimum = 0 V.
- A 100 nF decoupling capacitor must be used on the receiver side (_RX* signals on the baseboard interface connector). See the SB-iTC reference schematic.

3.4. HDA Interface

The audio / modem link in the CM-iTC is High Definition Audio (HD Audio) compliant, supporting high quality audio.

Features supported by HDA:

- Sample rate up to 192 kHz
- Up to 4 audio streams

HDA Link Interface:

Baseboard conn		Type	Description
Signal	Pin		
HDA_RST#	P2-121	O	Intel® HD Audio Reset: This signal is the reset to external Codec(s)
HDA_SYNC	P2-125	O	Intel HD Audio Sync: This signal is a 48-kHz fixed rate sample sync to the Codec(s). It is also used to encode the stream number.
HDA_BCLK	P2-119	I	Intel HD Audio Clock (Output): This signal is a 24.000-MHz serial data clock generated by the Intel HD Audio controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel HD Audio CODEC (or no CODEC) is connected.
HDA_SDO	P2-123	O	Intel HD Audio Serial Data Out: This signal is a serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for HD Audio.
HDA_SDIN0	P2-117	I	Intel HD Audio Serial Data In 0: These serial inputs are single-pumped for a bit rate of 24 MB/s. Have integrated pull-down resistors that are always enabled.
HDA_SDIN1	P1-20	I	Intel HD Audio Serial Data In 1: This serial input is single-pumped for a bit rate of 24 MB/s. Has integrated pull-down resistors that are always enabled.

3.5. LPC – Low Pin Count Interface

The CM-iTC implements an LPC Interface and Controller as described in the LPC 1.1 specification. The LPC bus provides a functional replacement for interfacing legacy ISA functions.

LPC Bus Interface

Baseboard conn		Type	Description
Signal	Pin		
LPC_AD0	P2-90	I/O	LPC Multiplexed Command, Address, Data.
LPC_AD1	P2-92	I/O	

LPC_AD2	P2-94	I/O	
LPC_AD3	P2-96	I/O	
LPC_SERIRQ	P2-89	I/O	Serial Interrupt Request: This signal conveys the serial interrupt protocol.
LPC_FRM#	P2-87	O	LPC Frame: Indicates the start of an LPC cycle or an abort.
LPC_CLK	P2-88	I/O	LPC clock (33 Mhz)

In addition to the above signals, an LPC device requires the RESET# signal.

3.6. Serial IRQ

The CM-iTC provides another interface for interrupt requests – serial IRQ. This allows a single signal line to be used to report legacy ISA interrupt requests. Interrupt sharing is allowed on Serial IRQ interfaces only for devices external to the chipset. The following interrupts are external to the chipset and are therefore potentially available on the Serial IRQ interface: IRQ1, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14. The serial IRQ interface is a synchronous interface. Data is clocked by the system's PCI clock.

Serial IRQ interface

Baseboard conn		**Interface**	**Description**
Signal	**Pin**		
LPC_SERIRQ	P2-89	I/O	The routing for this signal must be done using PCI layout/routing rules.

The IRQ assignment listed in the Interrupt Channel Mapping table is correct for a CM-iTC plugged into CompuLab's baseboard with a micro-SD card (such as SB-AM) inserted, but may change if additional hardware is attached.

3.7. Serial Ports

The CM-iTC provides four UART interfaces implemented on the Intel® PCH EG20T. It is functionally equivalent to the industry standard 16550, and is equipped with a 256-byte (UART0) or 64-byte (UART1-3) FIFO mode for both transmission and reception. Also, the receive FIFO generates 3-bit error data per byte. The CPU can read the status of the UART at any time. The information that can be read includes the type and status of a transfer operation in execution and error statuses such as a parity error, overrun error, framing error and break interrupt. The UART has a built-in programmable baud rate (from 300 bps to 1 Mbps) generator. Additionally, UART0 enables auto hardware flow control by hardware. The first UART includes RS232 drivers, the remaining three UART’s have a TTL signal level interface.

The serial ports include the following features:

- Fully compatible with 16550 devices
- UART mode data rates up to 1Mbps
- 256 bytes FIFO for UART0 and 64 bytes for UART[1,2,3]
- Support for power management

UART0 signals:

Baseboard conn		Interface	Type	Description
Signal	Pin			
COM1_RX	P1-117	RS232	I	Serial Data In
COM1_TX	P1-119	RS232	O	Serial Data Out
COM1_CTS#	P1-123	RS232	I	Clear To Send
COM1_DCD#	P1-113	RS232	I	Data Carrier Detect
COM1_DSR#	P1-111	RS232	I	Data Set Ready
COM1_DTR#	P1-125	RS232	O	Data Terminal Ready
COM1_RI#	P1-124	RS232	I	Ring Indicate
COM1_RTS#	P1-121	RS232	O	Request To Send

UART1 signals:

Baseboard conn		Interface	Type	Description
Signal	Pin			
COM2_RX	P1-112	TTL	I	Serial Data In (8.2k PU to 3.3V)
COM2_TX	P1-114	TTL	O	Serial Data Out

UART2 signals:

Baseboard conn		Interface	Type	Description
Signal	Pin			
COM3_RX	P2-73	TTL	I	Serial Data In (8.2k PU to 3.3V)
COM3_TX	P2-75	TTL	O	Serial Data Out

UART3 signals:

Baseboard conn		Interface	Type	Description
Signal	Pin			
COM4_RX	P2-59	TTL	I	Serial Data In (8.2k PU to 3.3V)
COM4_TX	P2-61	TTL	O	Serial Data Out

3.8. SDIO ports

The CM-iTC contains 2 SDIO/MMC (one on-board micro-SD and one external SDIO interfaces) expansion ports used to communicate with a variety of internal or external SDIO and MMC devices. The controller includes 32-bit X 1024-word Dual Port RAM, supports read/write operations by PIO and SDMA transfer to the SD memory card, SD I/O card and MMC.

Features:

- Conforms to SDHC, speed class 6
- MMC 4.1 transfer rates can be up to 48 MHz and bus widths of 1, 4 bits.
- SDIO 1.10 supports transfer rates up to 24 MHz and bus widths of 1 or 4 bits

Port 1 is connected to the on-board micro-SD slot, while Port 0 is available on the baseboard interface connector. Since the on-board micro-SD card doesn't have WP or an on-board LED – these signals are also provided on the baseboard interface.

SDIO 0 port signals:

Baseboard conn		Type	Description
Signal	Pin		
SDA_D0	P2-54	I/O	SDIO Controller 0 Data: These signals operate in push-pull mode. The SD card includes internal pull-up resistors for all data lines. By default, after power-up, only SDA_D0 is used for data transfer. Wider data bus widths can be configured for data transfer.
SDA_D1	P2-56	I/O	
SDA_D2	P2-58	I/O	
SDA_D3	P2-60	I/O	
SDA_CMD	P2-78	I/O	SDIO Controller 0 Command: used for card initialization and transferring commands. It has two operating modes: open-drain for initialization mode and push-pull for fast command transfer.
SDA_CLK	P2-76	O	SDIO Controller 0 Clock: up to 50 MHz
SDA_CD#	P2-72	I	SDIO Controller 0 Card Detect: indicates a card's presence in an external slot.
SDA_PWEN#	P2-84	I/O	SDIO/MMC Power Enable: controls the power supplied to an SDIO/MMC device.
SDA_WP	P2-82	I	SDIO Controller 0 Write Protect: denotes the state of the write-protect tab on SD cards.
SDA_LED	P2-80	O	SDIO Controller 0 LED: used for driving an external LED indicating transfers on the bus.

SDIO 1 port signals

Baseboard conn		Type	Description
Signal	Pin		
SDB_WP	P2-57	I	SDIO Controller 1 Write Protect: denotes the state of the write-protect tab on SD cards.

SDIO 1 micro-SD connector pinout:

Micro-SD conn		Signal Function
Pin #	Pin Name	
1	DAT2	Data Bit 2
2	CD/DAT3	Card Detect / Data Bit 3
3	CMD	Command Line
4	Vdd	Supply Voltage 3.3V (0.5 A max)
5	CLK	Clock
6	Vss	Ground
7	DAT0	Data Bit 0
8	DAT1	Data Bit 1

3.9. USB host Interface

The CM-iTC provides six ports compliant with USB 1.1 (OHCI) and USB 2.0 (EHCI) specifications. The HCI specification provides a register-level description for a host controller, as well as a common industry hardware/software interface and drivers. USB ports are supported by all O/S packages provided for the CM-iTC.
Features:

- USB v2.0 / EHCI v2.0 and USB v1.1 / OHCI v1.0a compatible
- Physical layer transceivers with optional three over-current detection status on USB inputs – one for every two ports

USB Port Signals

Baseboard conn		Type	Description
Signal	Pin		
USB0+	P1-132	DIFF	USB Port 0 Data pair
USB0-	P1-130	DIFF	
USB1+	P1-138	DIFF	USB Port 1 Data pair
USB1-	P1-136	DIFF	
USB2+	P1-131	DIFF	USB Port 2 Data pair
USB2-	P1-129	DIFF	
USB3+	P1-137	DIFF	USB Port 3 Data pair
USB3-	P1-135	DIFF	

Baseboard conn		Type	Description
Signal	Pin		
USB4+	P2-132	DIFF	USB Port 4 Data pair
USB4-	P2-130	DIFF	
USB5+	P2-140	DIFF	USB Port 5 Data pair
USB5-	P2-138	DIFF	
USB_OC0_1#*	P1-128	I	Overcurrent pin for ports 0,1
USB_OC2_3#*	P1-133	I	Overcurrent pin for ports 2,3
USB_OC4_5#*	P2-136	I	Overcurrent pin for ports 4,5

*Can be left not connected (NC) if not used

There are two separate EHCI controllers: the first is connected to ports 0,2,4 and the second to 1,3,5 respectively.

3.10. USB device

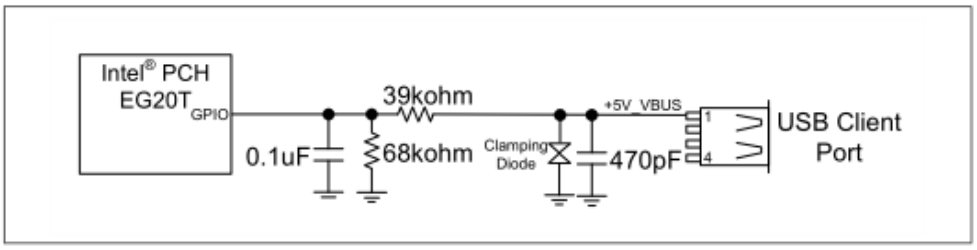
CM-iTC provides one USB device interface using one USB device controller with the following features:

- Complies with USB2.0 and USB1.1 protocol
- Supports High Speed (480 MHz) and Full Speed (12 MHz) operation
- Supports up to 4 IN and 4 OUT physical endpoints (EP0-3)

USB Device Signals

Baseboard conn		Type	Description
Signal	Pin		
USB_DEVN	P2-99	DIFF	USB Device Port Data pair
USB_DEVP	P2-101	DIFF	

When a host device is inserted, IOH (EG20T) must be notified through one of the GPIO's:



The +5V_VBUS detection of the IOH is not a specific GPIO pin. Any GPIO pin can be assigned, in accordance with the user's platform and as long as the GPIO pin is 5V tolerant, but it's necessary to use a level shifter when sharing a GPIO pin with another function. When a GPIO pin is used for VBUS detection only, a level shifter is unnecessary.

3.11. Audio Interface

The CM-iTC implements an audio interface using the ALC662 single-chip audio system, a low power optimized, high fidelity, 6-channel audio codec. The ALC662 provides

16/20/24-bit, supporting sample rates up to 96kHz by the DAC and ADC. The SPDIF output supports sample rates of 96kHz, 48kHz and 44.1kHz. MIC inputs can be programmed with 0/10/20/30dB boost. The port presence detect capability allows the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and optimizes the user's experience.
Features:

- Multiple Sample Rate Converters
- 16/20/24-bit Stereo Digital-to-Analog Converters and Analog-to-Digital Converters
- Two configurable Line In-level/Mic Stereo Inputs
- Integrated High-Performance Microphone Pre-Amplifier with 0/10/20/30dB boost
- SPDI/F output
- Anti pop mode
- Microphone Acoustic Echo Cancellation (AEC)

Audio specifications

Line output	Type	Stereo
	Decoupling	On-board
Microphone/ Line Input	Type	Stereo, electret or dynamic
	Decoupling	On-board

Audio Interface Signals

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
AIN_L	P2-133	IA	Audio stereo line/mic input left PORT_C
AIN_R	P2-131	IA	Audio stereo line/mic input right. PORT_C
MIC_IN_L	P2-129	IA	Audio Mic/stereo line input left PORT_B
MIC_IN_R	P1-24	IA	Audio Mic/stereo line input right. PORT_B
AOUT_L	P2-139	O	Line stereo output left. PORT_A
AOUT_R	P2-137	O	Line stereo output right. PORT_A
SPDIF_OUT	P1-18	O	SPDI/F output
SENSE_A	P1-22	I	Sense detector for all ports -- B and C and SPDIF: PORT_B-20k, PORT_C –10k, PORT_A – 39.2k

To enable auto detect functionality, the appropriate resistors (see above) must be connected to the jack switch.

3.12. Gigabit Ethernet Ports

The CM-iTC provides one (option E1) or two (option E2) Gigabit Ethernet port(s) implemented using a Realtek RTL8111D Gigabit Ethernet controller.

The Realtek RTL8111D Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller and embedded memory. With state-of-art DSP technology and mixed-mode signal technology, the RTL8111D offers high-speed transmission over a CAT 5 UTP or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery and error correction are implemented to provide robust transmission and reception capability at high speeds.
The device is compliant with the IEEE 802.3u specification for 10/100M bps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet.

RTL8111D Gigabit Ethernet controller features:

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Crossover Detection & Auto-Correction
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and Largesend Offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u and IEEE 802.3ab
- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Transmit/Receive on-chip buffer (48KB) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)

Ethernet 1 Port Signals

Baseboard conn		Type	Description
Signal	Pin		
MDI1_0+ MDI1_0-	P1-2 P1-4	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T, nd transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.
MDI1_1+ MDI1_1-	P1-1 P1-3	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
MDI1_2+ MDI1_2-	P1-10 P1-12	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
MDI1_3+ MDI1_3-	P1-9 P1-11	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.

ETH_LED1_0#	P1-6	O	Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH_LED1_1#	P1-5	O	100 Link/ACT LED. The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH_LED1_2#	P1-13	O	10 Link/ACT LED. The 10 Link LED pin indicates link integrity and 10 Mbps FULL connection speed.

Ethernet 2 Port Signals

Baseboard conn		**Type**	**Description**
Signal	**Pin**		
MDI2_0+ MDI2_0-	P2-2 P2-4	DIFF	In MDI mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T.
MDI2_1+ MDI2_1-	P2-1 P2-3	DIFF	In MDI mode, acts as BI_DB pair for 1000Base-T and receive pair for 100Base-T/10Base-T. In MDI crossover mode, acts as BI_DA pair for 1000Base-T and transmit pair for 100Base-T/10Base-T.
MDI2_2+ MDI2_2-	P2-10 P2-12	DIFF	In MDI mode, acts as BI_DC pair for 1000Base-T. In MDI crossover mode, acts as BI_DD pair for 1000Base-T.
MDI2_3+ MDI2_3-	P2-9 P2-11	DIFF	In MDI mode, acts as BI_DD pair for 1000Base-T. In MDI crossover mode, acts as BI_DC pair for 1000Base-T.
ETH_LED2_0#	P2-6	O	Activity LED. The Activity LED pin indicates either transmit or receive activity. When activity is present, the output becomes low for a short time. When no activity is present, the line remains high.
ETH_LED2_1#	P2-5	O	100 Link/ACT LED. The 100 Link LED pin indicates link integrity and 100Mbps connection speed.
ETH_LED2_2#	P2-13	O	10 Link/ACT LED. The 10 Link LED pin indicates link integrity and 10 Mbps FULL connection speed.

Magnetic Modules

The CM-iTC's Twisted Pair interface requires an external transformer (magnetic module) for interface to an RJ-45 connector. The two options use either:

1. An RJ-45 connector with a built-in transformer. Examples:

Vendor	**Model**
Speed_Tech	P65-101-[1|2]AK9

UDE	RB1-125BAK1A

2. A separate transformer and RJ-45 connector. Examples of available transformers:

Vendor	Model
Pulse Engineering	H5007
Pulse Engineering	H1251

Routing Ethernet Signals

The following rules should be applied when routing differential transmit and receive signals between the CM-iTC interface connector and an external connector/transformer module:

1. Route the differential signal pairs (TXN, TXP) and (RXN, RXP) in parallel, with minimal and consistent clearance within the pair. The distance between the RX and TX pairs should be maximized; otherwise, TX will induce crosstalk into RX.
2. It is preferable (but not mandatory) to keep the trace length of Ethernet signals as short as possible. If trace length exceeds two inches, additional steps, not specified here, should be taken. Recommended trace width: 5 to 8 mil.
3. Don't route any other traces nearby or across the Ethernet signals' path.

The listed rules cover the routing requirements if an RJ-45 connector with a built-in transformer is used. If a separate transformer is used, additional rules should be followed for transformer-to-connector routing.

3.13. SPI interface

The CM-iTC provides one SPI interface with the following features:

- Supports bit rates up to 5 Mbps
- Performs full-duplex data transfer
- Operates in master mode or slave mode
- Supports the Bus-master function (includes a shared DMA)
- Provided 16-stage FIFO's on the transmit side and receive side
- Allows selection of 8-bit or 16-bit transfer size
- Allows interrupts to be set within a range of 1 to 16 according to the number of received bytes (words) and the number of not transmitted bytes (words)
- Allows selection of either LSB first or MSB first
- Allows selection of the polarity and phase of the serial clock
- Allows selection of synchronous clocks obtained by dividing the internal-clock (50 MHz=PCLK) by 2 to 2046 (1023 types)
- Allows control of the interval before and after transfer

SPI interface signals:

Baseboard conn		Type	Description
Signal	Pin		
SPI_MISO	P2-64	O-LVTTL3.3	Serial data output from the IOH
SPI_MOSI	P2-66	I- LVTTL3.3	Serial data input to the IOH
SPI_CLK	P2-68	O-LVTTL3.3	SPI clock output from the IOH
SPI_SSN	P2-70	O-LVTTL3.3	SPI chip select output from the IOH

All SPI signals have 10k on-board PU to 3.3V

3.14. CAN bus

The CM-iTC provides a CAN interface for use in commercial systems. This CAN controller performs communication in accordance with BOSCH CAN Protocol Version 2.0B Active (standard format and extended format; defined by ISO 11519, ISO 11898 and SAEJ2411). The bit rate can be programmed to a maximum of 1Mbit/s.
To connect this CAN controller module to the CAN bus, it is necessary to add transceiver hardware (see the SB-iTC reference schematic).
CAN bus signals:

Baseboard conn		Type	Description
Signal	Pin		
CAN_RX	P2-69	I	CAN serial input
CAN_TX	P2-65	O	CAN serial output

CAN_RX/CAN_TX signals have on-board 10k PU to 5V

3.15. General Purpose Input / Output

The CM-iTC provides 18 general purpose I/O pins (GPIO's) – 14 of which are dedicated and 4 are shared with alternate functionality - with different power domain support.
Dedicated GPIO's:

Baseboard conn		Type	Description	Remarks
Signal	Pin			
GPIO0	P2-16	TBD	GPIO1 of the CPU	
GPIO1	P2-18	TBD	GPIO_SUS7 of the CPU	
GPIO2	P2-28	I/O, 8 mA	SB_GPIO0 of the IOH	5V- tolerant
GPIO3	P2-30	I/O, 8 mA	SB_GPIO1 of the IOH	5V- tolerant
GPIO4	P1-69	I/O, 8 mA	SB_GPIO2 of the IOH	5V- tolerant
GPIO5	P1-71	I/O, 8 mA	SB_GPIO3 of the IOH	5V- tolerant
GPIO6	P1-64	I/O, 8 mA	SB_GPIO4 of the IOH	5V- tolerant
GPIO7	P1-66	I/O, 8 mA	SB_GPIO5 of the IOH	5V- tolerant
GPIO8	P1-68	I/O, 8 mA	SB_GPIO6 of the IOH	5V- tolerant
GPIO9	P1-70	I/O, 8 mA	SB_GPIO7 of the IOH	5V- tolerant
GPIO10	P1-72	I/O, 8 mA	SB_GPIO8 of the IOH	10k PU to 3.3V
GPIO11	P1-73	I/O, 8 mA	SB_GPIO9 of the IOH	10k PU to 3.3V

GPIO12	P1-45	I/O, 8 mA	SB_GPIO10 of the IOH	10k PD to GND
GPIO13	P1-17	I/O, 8 mA	SB_GPIO11 of the IOH	10k PD to GND

Shared GPIO's :

Baseboard conn		Description	Share	Remarks
Signal	Pin			
GPIO14	P1-44	GPIO4 of the CPU	Int. LED, WD	Strap, 10k PU to 3.3V
GPIO15	P1-47	GPIO_SUS3 of the CPU	LVDS_DDC_CLK	2.21k PU to 3.3V
GPIO16	P1-48	GPIO_SUS2 of the CPU	LVDS_BCTL	100k PD to GND
GPIO17	P1-49	GPIO_SUS4 of the CPU	LVDS_DDC_DAT	2.21k PU to 3.3V

3.16. Watchdog

The CM-iTC supports a user configurable watchdog timer, providing a resolution ranging from 1 µs to 10 minutes using two selectable prescalers –1MHz (1 µs to 1 s) and 1 KHz (1 ms to 10 min). The timer uses a 35-bit down-counter with 33 MHz Clock (30 ns Clock Ticks). WD drives GPIO[14] /CPU GPIO4/P1-44 (if enabled) high or inverts the previous value. The status bit is preserved in RTC well for possible error detection and correction. The timer can be disabled (default state) or Locked (Hard Reset required to disable WDT).

3.17. Real-Time Clock

The Real Time Clock (RTC) module provides a date and time keeping device with battery backup. Three interrupt features are available: time of day alarm with a once a second to once a month range, periodic rates of 122 - 500 ms and end of update cycle notification. Seconds, minutes, hours, days, day of week, month and year are counted. The hour is represented in either twelve or twenty-four hour format and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768-kHz oscillating source, which is divided to achieve an update every second.

- Counting of seconds, minutes and hours of the day
- Counting of days of the week, date, month and year
- 12–24 hour clock with am and pm indication in 12-hour mode
- Two banks of 128 byte each (general and extended)
- Configurable alarms

The RTC uses a dedicated lithium battery backup when the rest of the card is completely powered down (RTC-only mode). The RTC can continue operating even when the rest of the card is not powered. The battery should be connected to the VCC_RTC (V_{BAT}) input of the CM-iTC's interface connector. Typical input current is ~ 6µA

3.18. SMBus (I2C)

The CM-iTC provides a host system management bus interface inplemented in the E6xx CPU. This interface is compatible with I2C devices. The SMBus runs at between 10-100 kHz.

Baseboard conn		Type	Comment
Signal	Pin		
SMB_CLK	P2-21	I/O	SMBus clock (2.2k internal PU)
SMB_DAT	P2-23	I/O	SMBus data (2.2k internal PU)
SMB_ALRT	P2-24	I	SMBus Alert: This signal can be used to generate an SMI#. (10k internal PU)

3.19. I2C

The CM-iTC provides a 1-channel I2C bus interface conforming to the typical I2C bus specification. It operates as a master or slave device and supports a multi-master bus. The I2C has a speed of up to-400 kHz.

Baseboard conn		Type	Comment
Signal	Pin		
I2C_CLK	P2-27	I/O	Serial data transfer clock
I2C_DAT	P2-25	I/O	Serial data input/output pin

I2C_CLK/I2C_DAT signals have on-board 10k PU to 3.3V

3.20. Clocks, Timers, Reset, Write Protect, Boot, Power Management

Baseboard conn		Type	Comment
Signal	Pin		
RSTIN#	P2-33	I	Reset input, active low. Low level on this pin initiates a hardware reset of the CM-iTC. This pin is not mandatory for CM-iTC operation as it generates power-on reset using on-board circuitry. It has an internal pull-up and can be left unconnected.
RESET#	P2-20	O 24mA	Reset output, active low. Indicates when the CM-iTC undergoes a hardware reset, due to powerup or RESET-IN. Can be used as a reset signal to off-board hardware.
PWRBTN#	P2-35	I	Power button/sleep functionality- active low
SUSP_S3	P1-15	O	Suspend mode external device power disable/enable – used in power sequence mechanism
PWRGOOD	P2-16	I	Power good input from the BASE to the module. Has internal PU to 3.3VSBY. Should be left unconnected if not used (from rev 1.1).

TIMER-SPKR	P2-22	O	Speaker: The TIMER-SPKR signal is the output of counter 2 and is internally ANDed with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon SLPMODE, its output state is 0.
BIOS_WP#	P2-46	I	BIOS SPI flash write protect, active low. This input has internal PU to te 3.3V. Left unconnected if not used.
FWH_INIT#	P2-85	O	External FWH init signal. Should be left unconnected if not used
STRAP_EN	P1-46	O	Strap timeout enable for LVDS controls
DEBUG0	P1-116	O	Used for first-time factory programming. Should be left unconnected. Irrelevant for any other purpose.
DEBUG1	P1-118	O	
DEBUG2	P1-120	I	
DEBUG3	P2-36	I	
DEBUG4	P2-40	O	
SPARE4	P2-42	O	
SPARE6	P2-48	I	
SPARE7	P2-50	O	

3.21. Not connected pins

The pins below are reserved for the future use and must remain unconnected

Baseboard conn		Comment
Signal	**Pin**	
NC	P1-126	
NC	P2-17	
NC	P2-29	
NC	P2-32	
NC	P2-34	
NC	P2-37	
NC	P2-39	
NC	P2-41	
NC	P2-45	
NC	P2-47	
NC	P2-49	
NC	P2-51	
NC	P2-53	
NC	P2-63	
NC	P2-85	

3.22. Power Supply Pins

The CM-iTC requires only 5V for operation. Other supply voltages required for the CPU, DDR and peripherals are generated on-board.

Power Net Description

Signal	Description
GND	Common ground
VCC_SBY	Main 5V stand-by power source. All other stand-by voltages are derived from this source (also used for DDR supply).
VCC	Main 5V power supply. All other voltages are derived from this source,
VCC-RTC	The 3.3V supply pin provides power to the internal real-time clock and on-board static / configuration RAM. This pin can be driven independently of all other power pins. This pin enables the connection of an external lithium battery.

Power Supply Pins

GND (25 pins)	P1-8	P2-7
	P1-14	P2-8
	P1-26	P2-14
	P1-38	P2-26
	P1-50	P2-38
	P1-62	P2-52
	P1-74	P2-62
	P1-86	P2-74
	P1-98	P2-86
	P1-110	P2-98
	P1-122	P2-110
	P1-134	P2-122
	-	P2-134
VCC_SBY (5 pins)	P1-80	P2-71
	P1-140	P2-97
	-	P2-116
VCC (23 pins) Total	P1-7	P2-19
	P1-19	P2-31
	P1-31	P2-43
	P1-43	P2-55
	P1-55	P2-67
	P1-67	P2-79
	P1-79	P2-91
	P1-91	P2-103
	P1-103	P2-115

	P1-115	P2-127
	P1-127	P2-135
	P1-139	-
VCC-RTC	P1-37	

3.23. Recommended power sequence

The CM-iTC has an automatic power button function that turns on the device immediately after the insertion of power and readiness of internal circuits.

The power-up sequence should be as follows:

1. Apply VCC5SBY
2. Wait for SUSP_S3 (P1-15, PM_EN_5VS# on the SB-iTC) low to enable VCC5 rail.

The power down/standby sequence:

1. SUSP_S3# high will disable VCC5 rail
2. Shut down VCC5SBY (or leave it connected and use PWRBTN# signal for next power up).

VCCRTC should always be connected for proper RTC operation.

4. Interface Connectors

4.1. Connector Type

The CM-iTC connects to the external world through P1 and P2 - 140-pin, 0.6 mm connectors.

Conn	Mfg.	CM-iTC Connector P/N	Mating Connector P/N
P1, P2	AMP	8-5353183-0	8-5353189-0

4.2. Standoffs

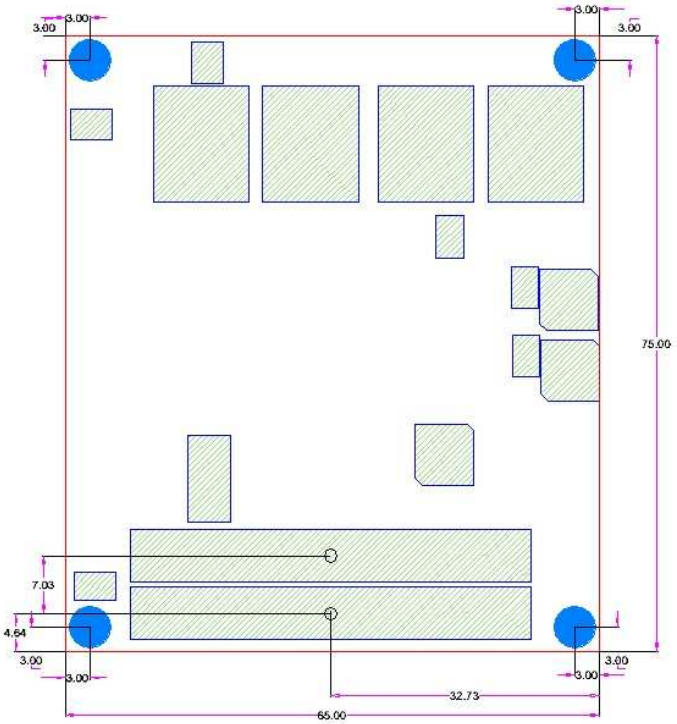
The CM-iTC has four mounting holes for standoffs. All of them are connected to GND. Refer to the mechanical drawing of the module with baseboard interface connectors. The developer is advised to connect the mating holes of the baseboard to GND in order to improve the EMC.

The standoff is implemented by three parts: a screw, a spacer and a nut.

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	FCI 95121-005 Acton InoxPro BF22102010 World Bridge Machinery 380J52080
Spacer	M2x.4 thread, 4.2 mm length	Hirosugi ASU-2004 MAC8 2SP-4 World Bridge Machinery M2, L=4.2mm
Nut	M2, 1.6-2.0mm width	FCI 92869-001 (or 002) Acton InoxPro BG12102000 Bossard 1241397 (DIN934-A2 M2) World Bridge Machinery 381A52000

Mating connectors and standoffs are available from manufacturer representatives or from CompuLab, see [prices] >> [accessories] in CompuLab's website.

4.3. Connectors Layout



Bottom side image, viewed from the top side of the module

Board-to-board mating height is 4 mm.
Hatched green areas indicate height constraints - don't locate components beneath.

Connectors' and mechanical layout is available in DXF format from CompuLab's website, following [http://www.compulab.co.il/iTC/html/iTC-developer.py - Dimensions and Connector Location links.

4.4. Connectors Pinout

Note: gray-colored signals are not available. They are either not implemented or are routed through other pins of the connector (i.e., mixed with another function). Grayed signals are displayed in order to clarify standard baseboard interface pin assignment.

	P1-A
P1-02	MDI1_0+
P1-04	MDI1_0-
P1-06	ETH_LED1_0#
P1-08	**GND**
P1-10	MDI1_2+
P1-12	MDI1_2-
P1-14	**GND**
P1-16	PWRGOOD
P1-18	SPDIF_OUT
P1-20	HDA_SDIN1
P1-22	SENSE_A
P1-24	MIC_IN_R
P1-26	**GND**
P1-28	SDVO_BCLK-
P1-30	SDVO_BCLK+
P1-32	SDVO_CTRL_DAT
P1-34	SDVO_INT-
P1-36	SDVO_INT+
P1-38	**GND**
P1-40	SDVO_RED-
P1-42	SDVO_RED+
P1-44	GPIO14
P1-46	STRAP_EN
P1-48	LVDS_BLT_CTR
P1-50	**GND**
P1-52	LVDS_A0-
P1-54	LVDS_A0+
P1-56	LVDS_BLEN
P1-58	LVDS_A2-
P1-60	LVDS_A2+
P1-62	**GND**
P1-64	GPIO6

	P1-B
P1-01	MDI1_1+
P1-03	MDI1_1-
P1-05	ETH_LED1_1#
P1-07	**VCC5**
P1-09	MDI1_3+
P1-11	MDI1_3-
P1-13	ETH_LED1_2#
P1-15	SUS_S3
P1-17	GPIO13
P1-19	**VCC5**
P1-21	SDVO_TVCLKIN-
P1-23	SDVO_TVCLKIN+
P1-25	SDVO_CTRL_CLK
P1-27	SDVO_GREEN-
P1-29	SDVO_GREEN+
P1-31	**VCC5**
P1-33	SDVO_BLUE-
P1-35	SDVO_BLUE+
P1-37	VCC_RTC
P1-39	SDVO_FLDSTALL-
P1-41	SDVO_FLDSTALL+
P1-43	**VCC5**
P1-45	GPIO12
P1-47	LVDS_DID_CLK
P1-49	LVDS_DID_DAT
P1-51	LVDS_A1-
P1-53	LVDS_A1+
P1-55	**VCC5**
P1-57	LVDS_A3-
P1-59	LVDS_A3+
P1-61	LVDS_PPEN
P1-63	LVDS_CLK-

	P1-A
P1-66	GPIO7
P1-68	GPIO8
P1-70	GPIO9
P1-72	GPIO10
P1-74	**GND**
P1-76	LCD_R1
P1-78	LCD_R3
P1-80	**VCC_SBY**
P1-82	LCD_R5
P1-84	LCD_R7
P1-86	**GND**
P1-88	LCD_G2
P1-90	LCD_G4
P1-92	LCD_G5
P1-94	LCD_G7
P1-96	LCD_B1
P1-98	**GND**
P1-100	LCD_B4
P1-102	LCD_B6
P1-104	LCD_B7
P1-106	LCD_PWREN
P1-108	LCD_CLK
P1-110	**GND**
P1-112	COM2_RX
P1-114	COM2_TX
P1-116	DEBUG0
P1-118	DEBUG1
P1-120	DEBUG2
P1-122	**GND**
P1-124	COM1_RI#
P1-126	GPIO14
P1-128	USB_OC0_1#
P1-130	USB0-
P1-132	USB0+
P1-134	**GND**
P1-136	USB1-
P1-138	USB1+
P1-140	**VCC_SBY**

	P1-B
P1-65	LVDS_CLK+
P1-67	**VCC5**
P1-69	GPIO4
P1-71	GPIO5
P1-73	GPIO11
P1-75	LCD_R0
P1-77	LCD_R2
P1-79	**VCC5**
P1-81	LCD_R4
P1-83	LCD_R6
P1-85	LCD_G0
P1-87	LCD_G1
P1-89	LCD_G3
P1-91	**VCC5**
P1-93	LCD_G6
P1-95	LCD_B0
P1-97	LCD_B2
P1-99	LCD_B3
P1-101	LCD_B5
P1-103	**VCC5**
P1-105	LCD_DE
P1-107	LCD_VSYNC
P1-109	LCD_HSYNC
P1-111	COM1_DSR#
P1-113	COM1_DCD#
P1-115	**VCC5**
P1-117	COM1_RX
P1-119	COM1_TX
P1-121	COM1_RTS#
P1-123	COM1_CTS#
P1-125	COM1_DTR#
P1-127	**VCC5**
P1-129	USB2-
P1-131	USB2+
P1-133	USB_OC2_3#
P1-135	USB3-
P1-137	USB3+
P1-139	**VCC5**

	P2-A
P2-02	MDI2_0+
P2-04	MDI2_0-
P2-06	ETH_LED2_0#
P2-08	**GND**
P2-10	MDI2_2+
P2-12	MDI2_2-
P2-14	**GND**
P2-16	GPIO0
P2-18	GPIO1
P2-20	RESET#
P2-22	TIMER_SPKR
P2-24	SMB_ALRT
P2-26	**GND**
P2-28	GPIO2
P2-30	GPIO3
P2-32	NC
P2-34	NC
P2-36	DEBUG3
P2-38	**GND**
P2-40	DEBUG4
P2-42	SPARE4
P2-44	SPARE5
P2-46	BIOS_WP#
P2-48	SPARE6
P2-50	SPARE7
P2-52	**GND**
P2-54	SDA_D0
P2-56	SDA_D1
P2-58	SDA_D2
P2-60	SDA_D3
P2-62	**GND**
P2-64	SPI_MISO
P2-66	SPI_MOSI
P2-68	SPI_CLK

	P2-B
P2-01	MDI2_1+
P2-03	MDI2_1-
P2-05	ETH_LED2_1#
P2-07	**GND**
P2-09	MDI2_3+
P2-11	MDI2_3-
P2-13	ETH_LED2_2#
P2-15	PCIE_CLK1E#
P2-17	NC
P2-19	**VCC5**
P2-21	SMB_CLK
P2-23	SMB_DAT
P2-25	I2C_CLK
P2-27	I2C_DAT
P2-29	NC
P2-31	**VCC5**
P2-33	RSTIN#
P2-35	PWRBTN#
P2-37	NC
P2-39	NC
P2-41	NC
P2-43	**VCC5**
P2-45	NC
P2-47	NC
P2-49	NC
P2-51	NC
P2-53	NC
P2-55	**VCC5**
P2-57	SDB_WP
P2-59	COM4_RX
P2-61	COM4_TX
P2-63	NC
P2-65	CAN_TX
P2-67	**VCC5**

	P2-A
P2-70	SPI_SSN
P2-72	SDA_CD#
P2-74	**GND**
P2-76	SDA_CLK
P2-78	SDA_CMD
P2-80	SDA_LED
P2-82	SDA_WP
P2-84	SDA_PWEN#
P2-86	**GND**
P2-88	LPC_CLK
P2-90	LPC_AD0
P2-92	LPC_AD1
P2-94	LPC_AD2
P2-96	LPC_AD3
P2-98	**GND**
P2-100	SATA1_RX-
P2-102	SATA1_RX+
P2-104	PCIE_RST#
P2-106	PCIE0_RX-
P2-108	PCIE0_RX+
P2-110	**GND**
P2-112	PCIE0_TX-
P2-114	PCIE0_TX+
P2-116	**VCC_SBY**
P2-118	SATA0_RX-
P2-120	SATA0_RX+
P2-122	**GND**
P2-124	SATA0_TX-
P2-126	SATA0_TX+
P2-128	SATA_LED
P2-130	USB4-
P2-132	USB4+
P2-134	**GND**
P2-136	USB_OC4_5#
P2-138	USB5-
P2-140	USB5+

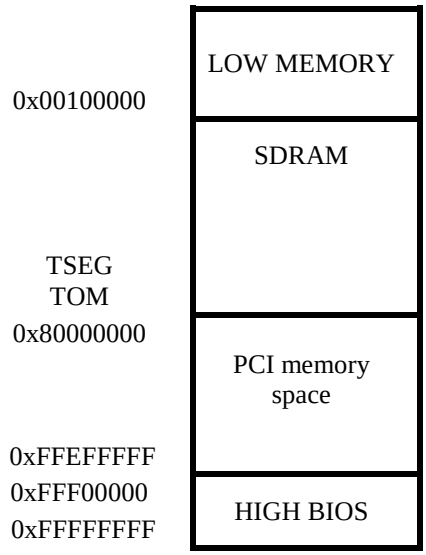
	P2-B
P2-69	CAN_RX
P2-71	**VCC_SBY**
P2-73	COM3_RX
P2-75	COM3_TX
P2-77	SATA1_LED
P2-79	**VCC5**
P2-81	PCIE_CLK1-
P2-83	PCIE_CLK1+
P2-85	NC
P2-87	LPC_FRM#
P2-89	LPC_SERIRQ
P2-91	**VCC5**
P2-93	SATA1_TX-
P2-95	SATA1_TX+
P2-97	**VCC_SBY**
P2-99	USB_DEVN
P2-101	USB_DEVP
P2-103	**VCC5**
P2-105	PCIE1_RX-
P2-107	PCIE1_RX+
P2-109	PCI_WAKE#
P2-111	PCIE1_TX-
P2-113	PCIE1_TX+
P2-115	**VCC5**
P2-117	HDA_SDIN0
P2-119	HDA_BCLK
P2-121	HDA_RST#
P2-123	HDA_SDO
P2-125	HDA_SYNC
P2-127	**VCC5**
P2-129	MIC_IN_L
P2-131	AIN_R
P2-133	AIN_L
P2-135	**VCC5**
P2-137	AOUT_R
P2-139	AOUT_L

5. MEMORY and I/O mapping

5.1. Memory space usage in the first 1MB

0000:0 - 9FFF:F	Standard Low memory
A000:0 - BFFF:F	Graphic Memory Will be forwarded to PCIE if graphic disabled
C000:0 - DFFF:F	VGA BIOS expansion area
E000:0 - FFFF:F	BIOS

5.2. Memory space usage above first 1MB



TSEG is a 1-MB, 2-MB or 8-MB memory region located below Intel Graphics Media Adapter stolen memory, which is at the top of the physical memory (TOM). It is used for System Management Mode accesses by the processor.

5.3. I/O Space Usage

TBD

5.4. BIOS Flash Mapping

TBD

5.5. PCI Resource Map

TBD

5.6. Interrupt Channel Mapping

TBD

6. Power Consumption

The current consumption measurements specified below were performed on a system with the following configurations:

- CM-iTC-D1G-C1300-L-E2-A-H (CONFIG1)
- CM-iTC-D1G-C1000-L-E2-A-H (CONFIG2)
- CM-iTC-D05G-C600-L-E2-A-H (CONFIG3) -TBD
- SB-iTC-M-P-A

The configuration also includes a USB mouse and USB keyboard powered from 5VSBY. Current consumption is specified for both boards; however, 90% of the total current is consumed by the CM-iTC module. Max load was simulated using the SiSoft Sandra Burn-in Test.

CPU Speed	Activity	Current 5V	Current 5VSBY
1300 MHz CONFIG1	Standby	~0(1.1mA)	0.13A
	Average	0.92A	0.52A
	Max load	1.14A	0.89A
1000 MHz CONFIG2	Standby	~0(1.1mA)	0.13A
	Average	0.88A	0.52A
	Max load	1.05A	0.88A

Average power consumption

- CPU clock - 1300 MHz (CONFIG1)/1000MHz(CONFIG2)
- Average

[5V * (0.88A+0.52A)]*0.9(90%) = 6.3 watt (CONFIG2)
[5V * (0.92A+0.52A)] *0.9(90%) = 6.5 watt (CONFIG1)

Maximum power consumption

- CPU clock - 1300 MHz (CONFIG1)/1100MHz (CONFIG2)
- Max load

[5V * (1.05A+0.88A)]*0.9(90%) = 8.7 watt (CONFIG2)
[5V * (1.14A+0.89A)] *0.9(90%) = 9.2 watt (CONFIG1)

Standby power consumption

[5V * 0.13A] *0.9(90%)= 0.6 watt (CONFIG2)

7. Performance Benchmarks

Measured with CPU E660@ 1300 MHz, using SiSoft Sandra bench test under Windows.

Drystone (integer)	4162 MIPS
Whetstone (floating point)	1437 MFLOPS
Whetstone (iSSE2)	1879 MFLOPS
DDR bandwidth	2318 MB/s

Measured with CPU E640@ 1000 MHz, using SiSoft Sandra bench test under Windows.

Drystone (integer)	3203 MIPS
Whetstone (floating point)	1099 MFLOPS
Whetstone (iSSE2)	1456 MFLOPS
DDR bandwidth	2130 MB/s

8. Operating Temperature Ranges

The CM-iTC is available with three operating temperature range options:

Range	Temp.	Description
Commercial	0^o to 70^o C	Sample cards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20^o to 70^o C	Every card is individually tested for the lower limit (-20^o C) qualification.
Industrial	-40^o to 85^o C	Every card is individually tested for both lower and upper limits and at several midpoints.

* Temp - maximum temperature measured on hottest spot of heatsink.

For more information regarding the availability of a specific card configuration for Industrial grade, please refer to [Products] >> [Industrial Temperature] links in CompuLab's web-site.

9. Heat Dissipation

TBD