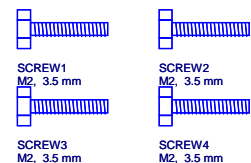
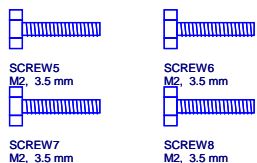
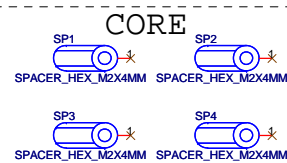
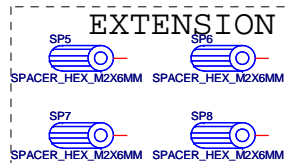
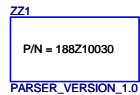
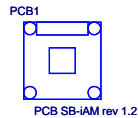
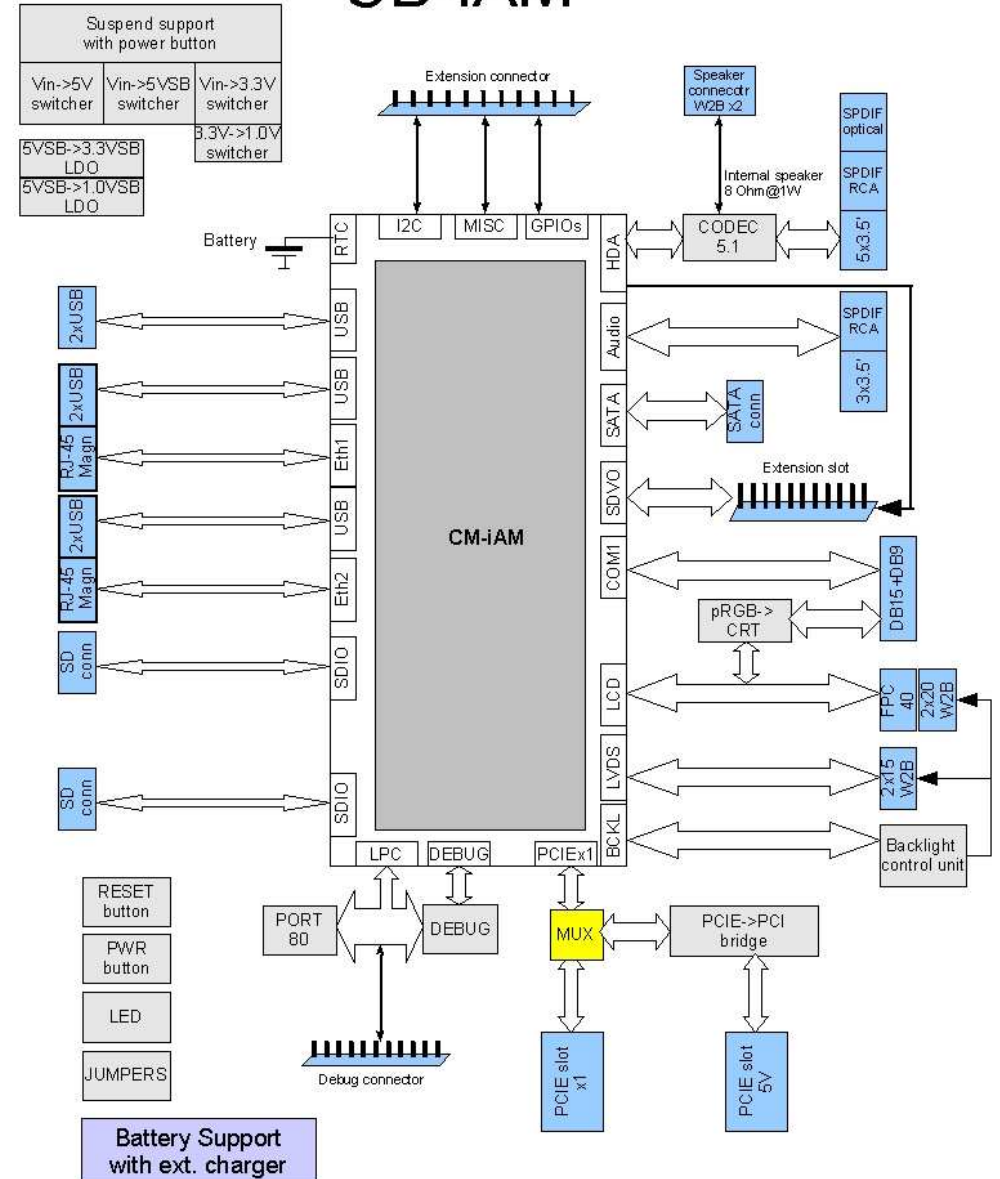


PAGE	FUNCTION
01	INDEX
02	CAMI CONNECTORS
03	POWER
04	ETHERNET & USB
05	AUDIO
06	SDIO & SATA
07	LCD & LVDS
08	CRT & COM
09	SDVO slot
10	PCIE MUX & PCIE connector
11	PCIE to PCI bridge
12	PCI slot
13	PORT80
14	DEBUG
15	MISC

Rev 1.2

SB-iAM



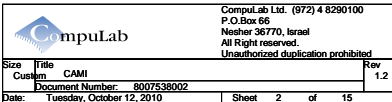
Revision notes

Rev. 1.1
Initial public release

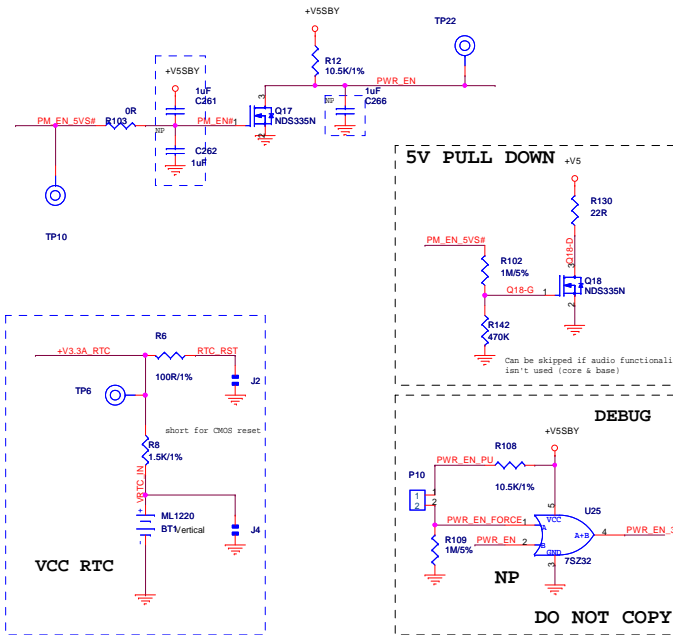
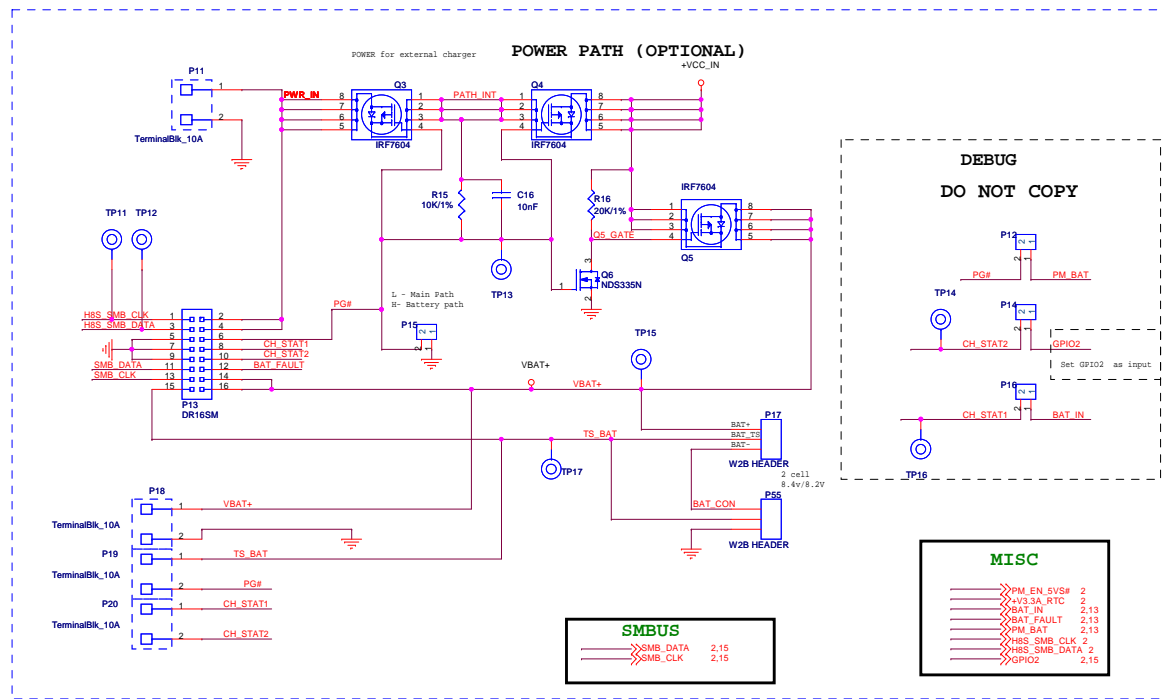
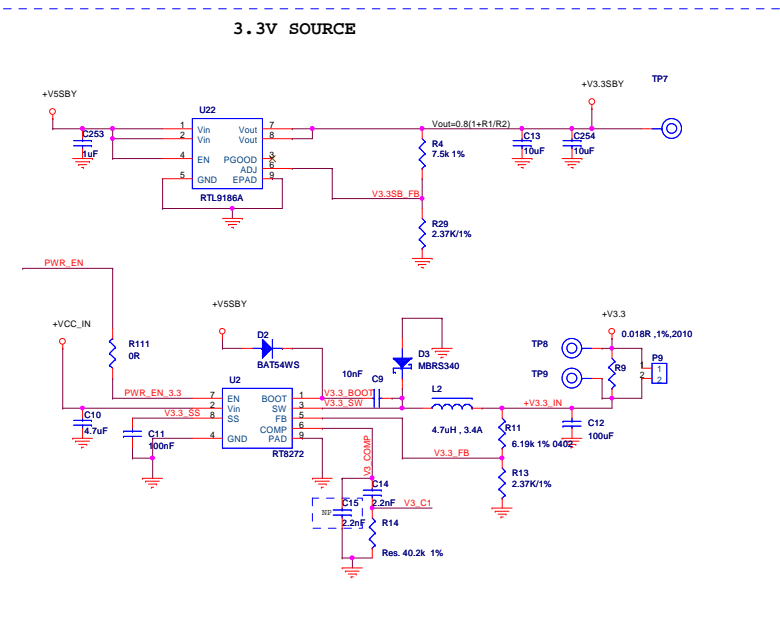
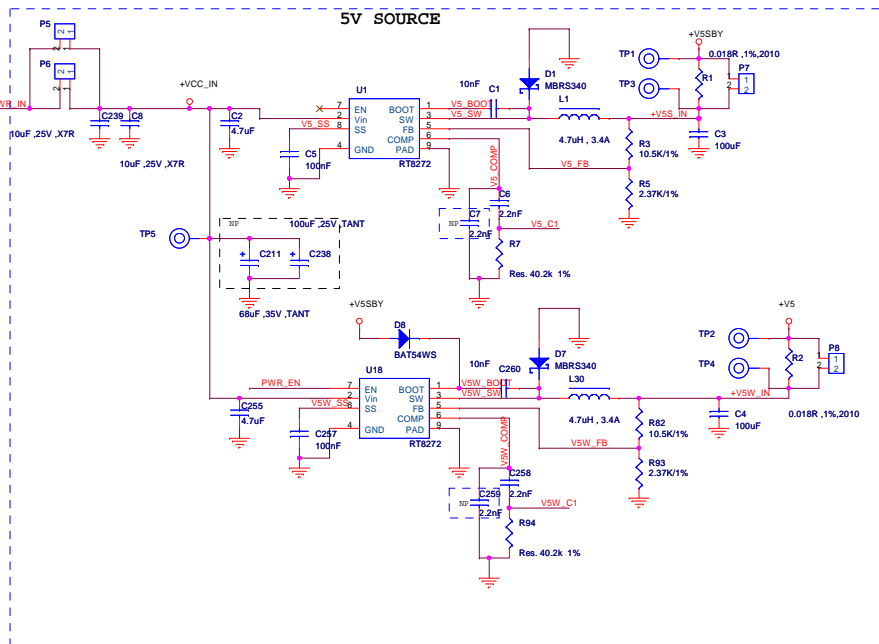
Rev. 1.2

1. Page 4 - P3 & P4 layout and pin changes (pin 11,12,13,14)
2. Page 5 - added provision for rev 1.2 new audio codec
3. Page 6 - slot1_wp pull up was changed to 1k
4. Added some provisions for DEBUG and PORT80

5. Added J4 for ext. RTC battery connection
6. Page 15 - added FIALBOOT pin and A_VIN (SPARE4) - for rev. 1.2 (CM-iAM) and above
7. Sdk changes on the P50 to reflect new core SIO GPIOs
8. Page3 - added note regarding RTC battery

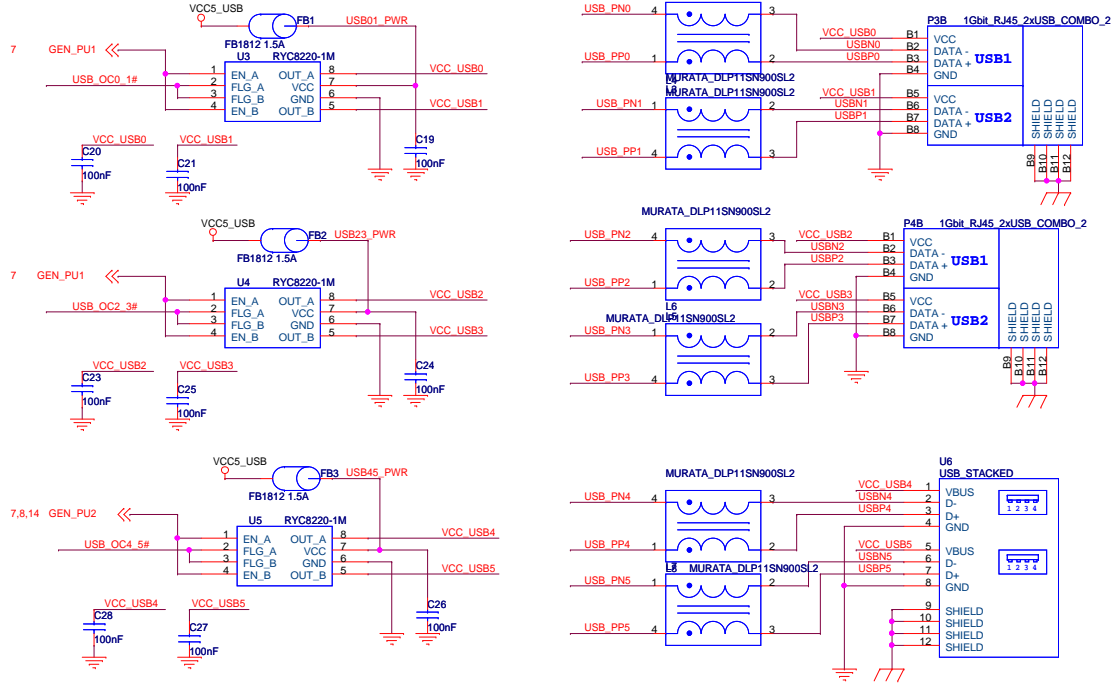


Vin: 7-20V



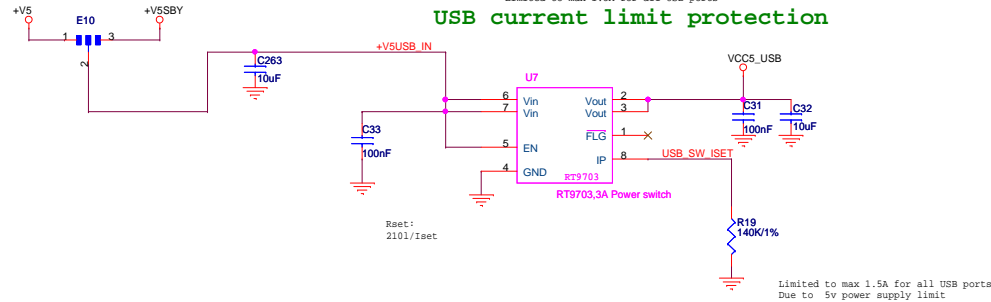
NOTE:
Schematic shows rechargeable ML1220 battery for the RTC circuit
External diode should be placed between R8 and R6 when using non-rechargeable battery to prevent charging

USB CONNECTORS & POWER

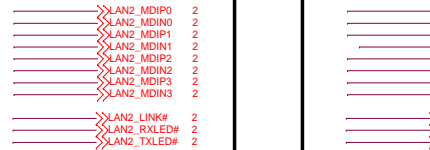


USB current limit protection

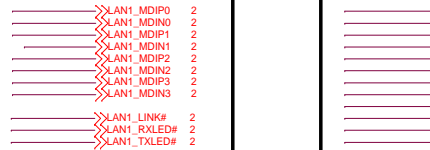
Limited to max 1.5A for all USB ports



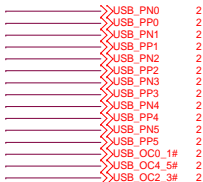
Ethernet2 Gbit



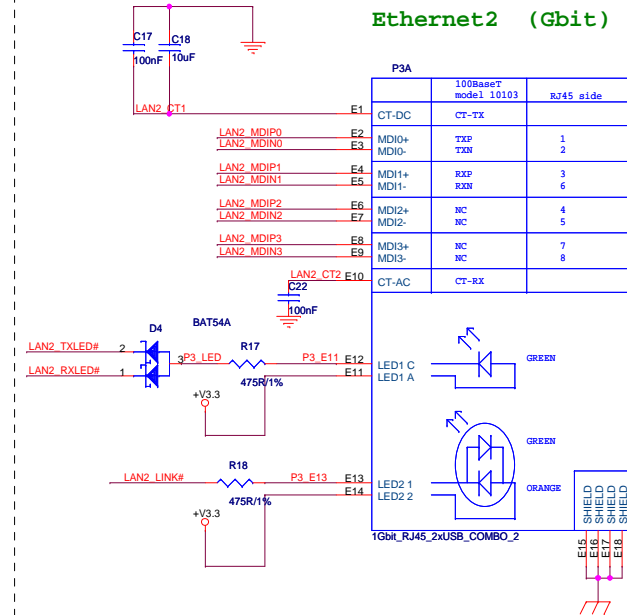
Ethernet1 (Gbit)



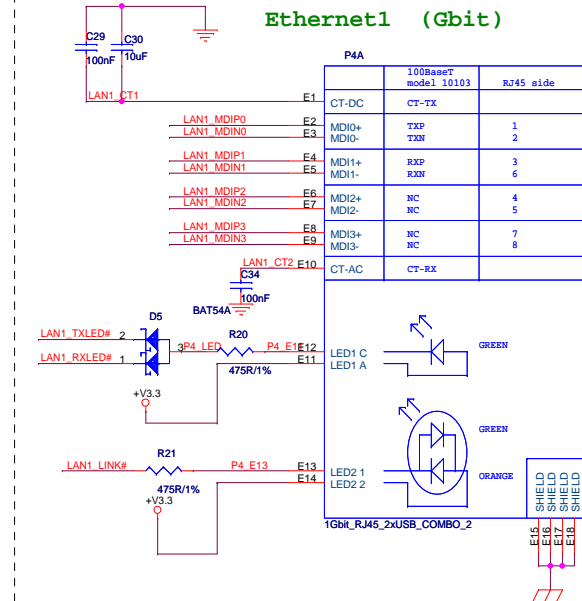
USB



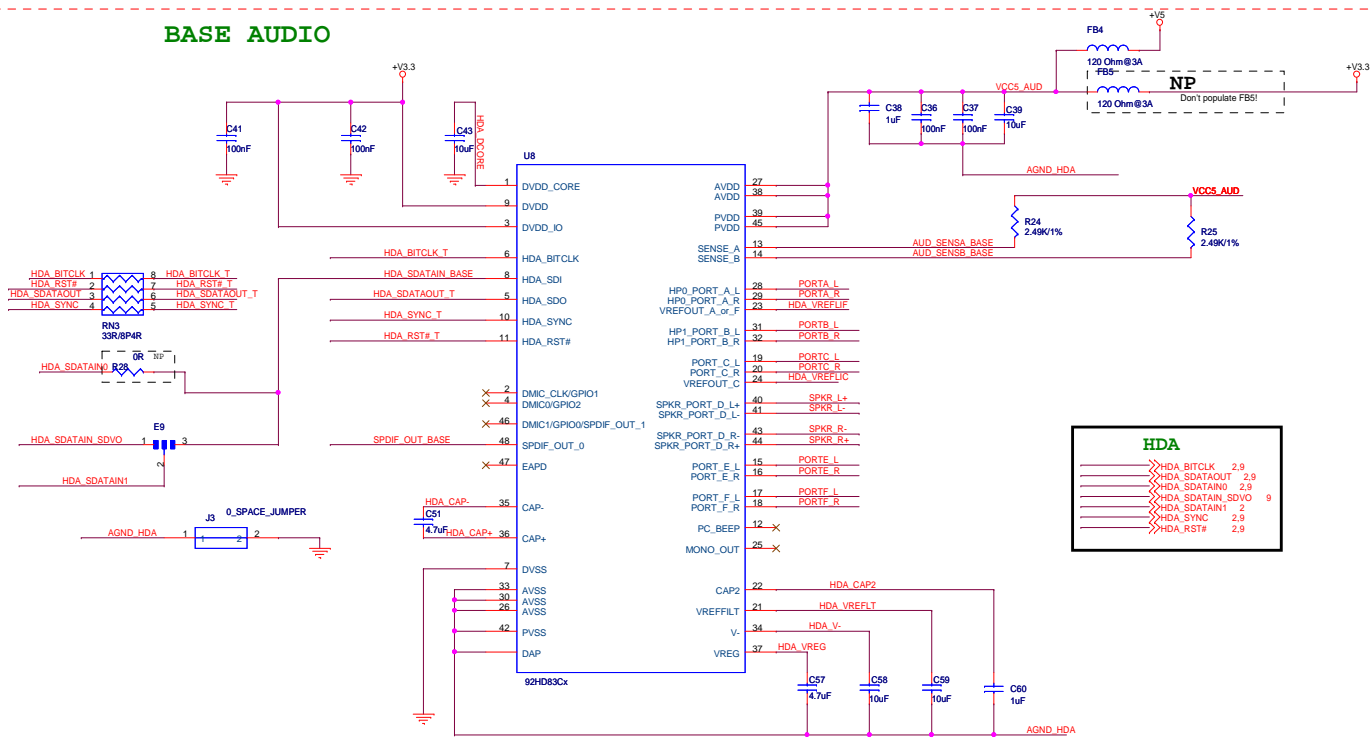
Ethernet2 (Gbit)



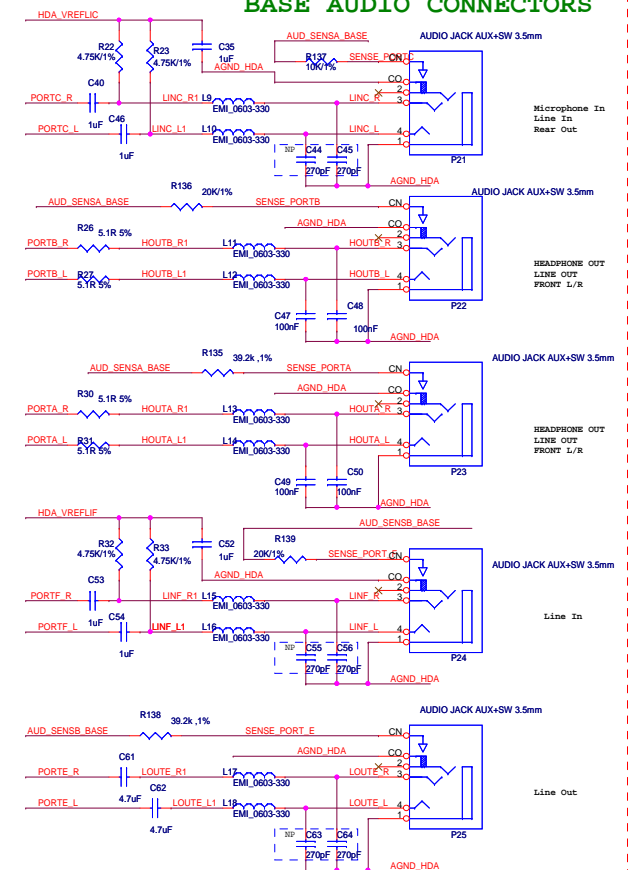
Ethernet1 (Gbit)



BASE AUDIO

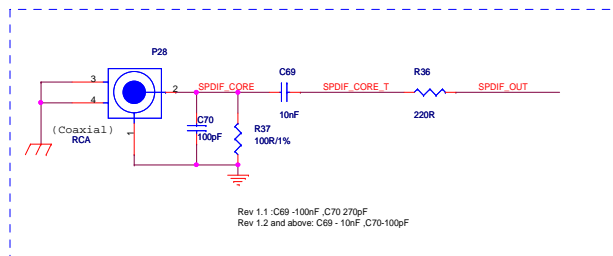


BASE AUDIO CONNECTORS

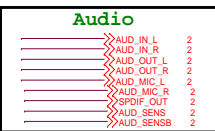


CORE AUDIO CONNECTORS

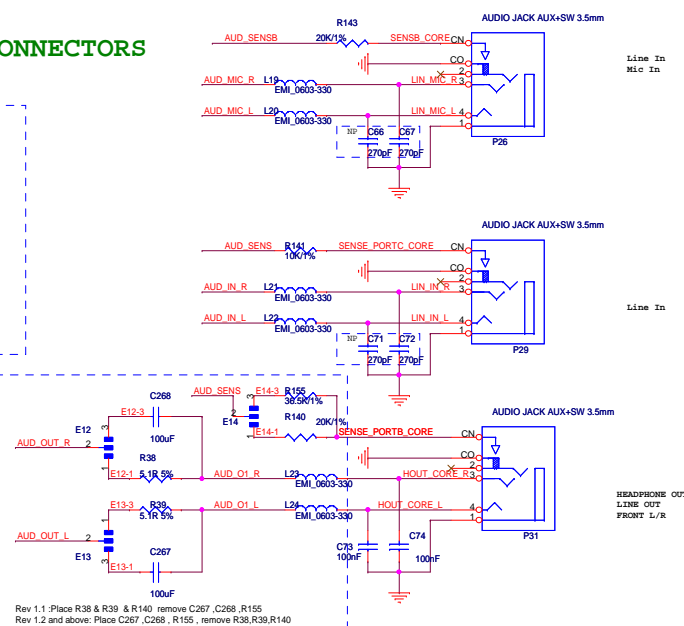
S/PDIF (CORE): Coaxial



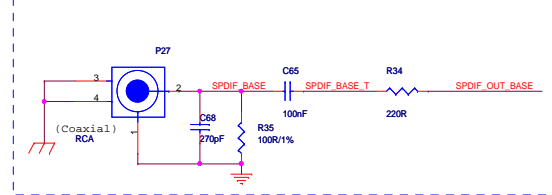
Audio



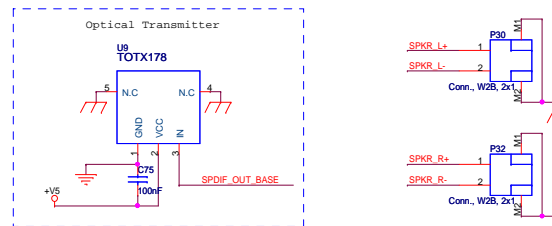
Rev	E12	E13	E14
1.1	1-2	1-2	1-2
1.2	2-3	2-3	2-3

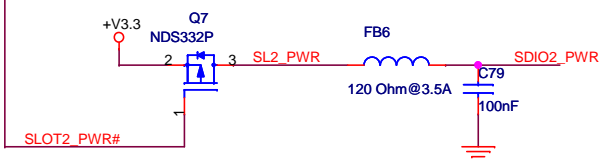
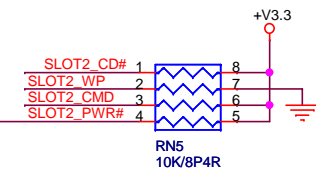
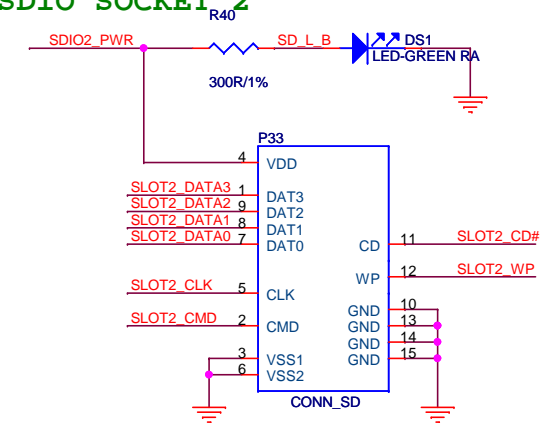


S/PDIF module option 2(BASE): Coaxial

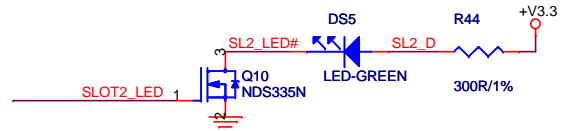


S/PDIF module option 1(BASE): Optical

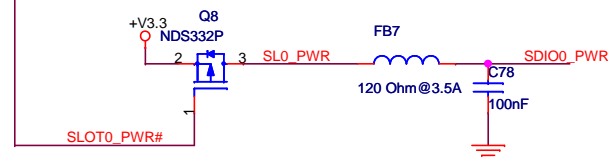
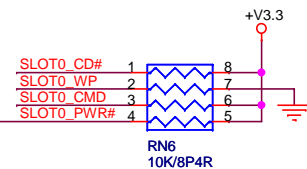
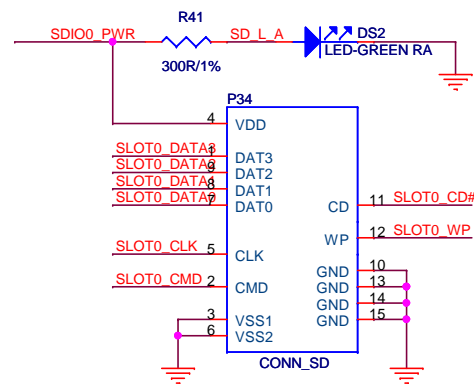


SDIO SOCKET 2 B40

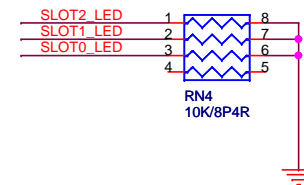
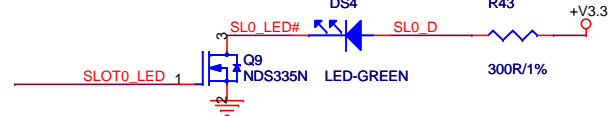
SDIO2 ACTIVITY



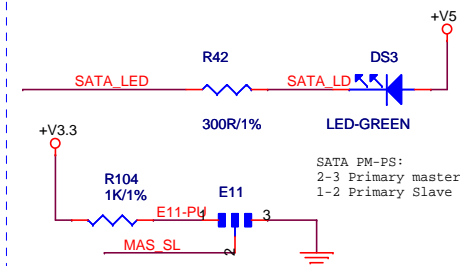
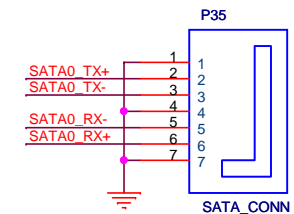
SDIO SOCKET 0



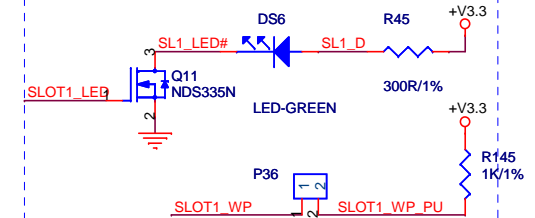
SDIO0 ACTIVITY



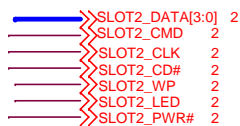
SATA CONNECTOR



SDIO1 (MODULE) ACTIVITY



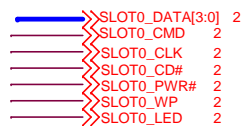
SDIO2



SDIO1



SDIO0

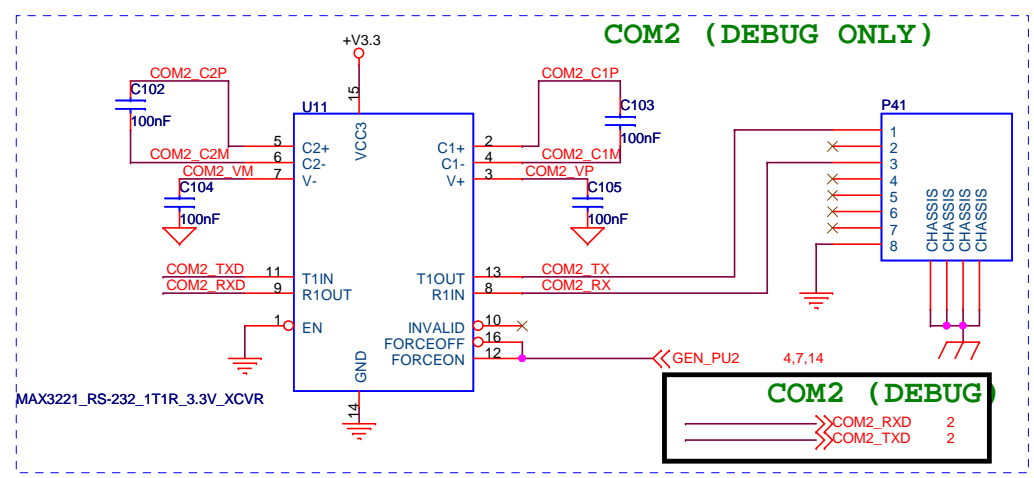
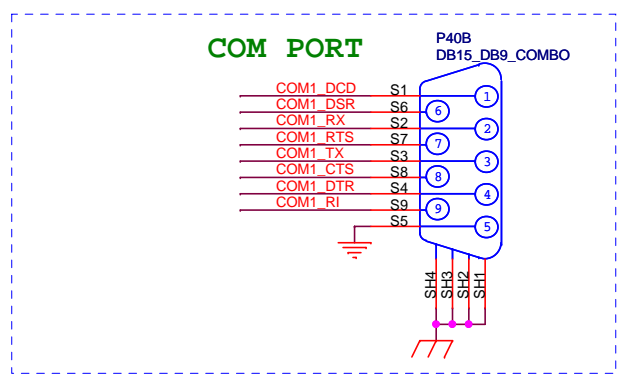
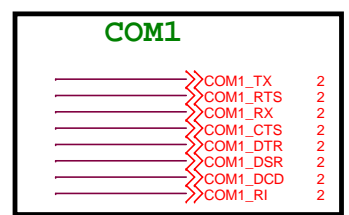
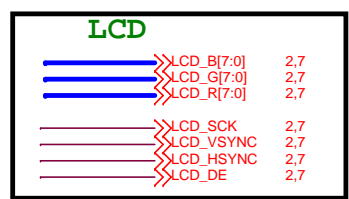
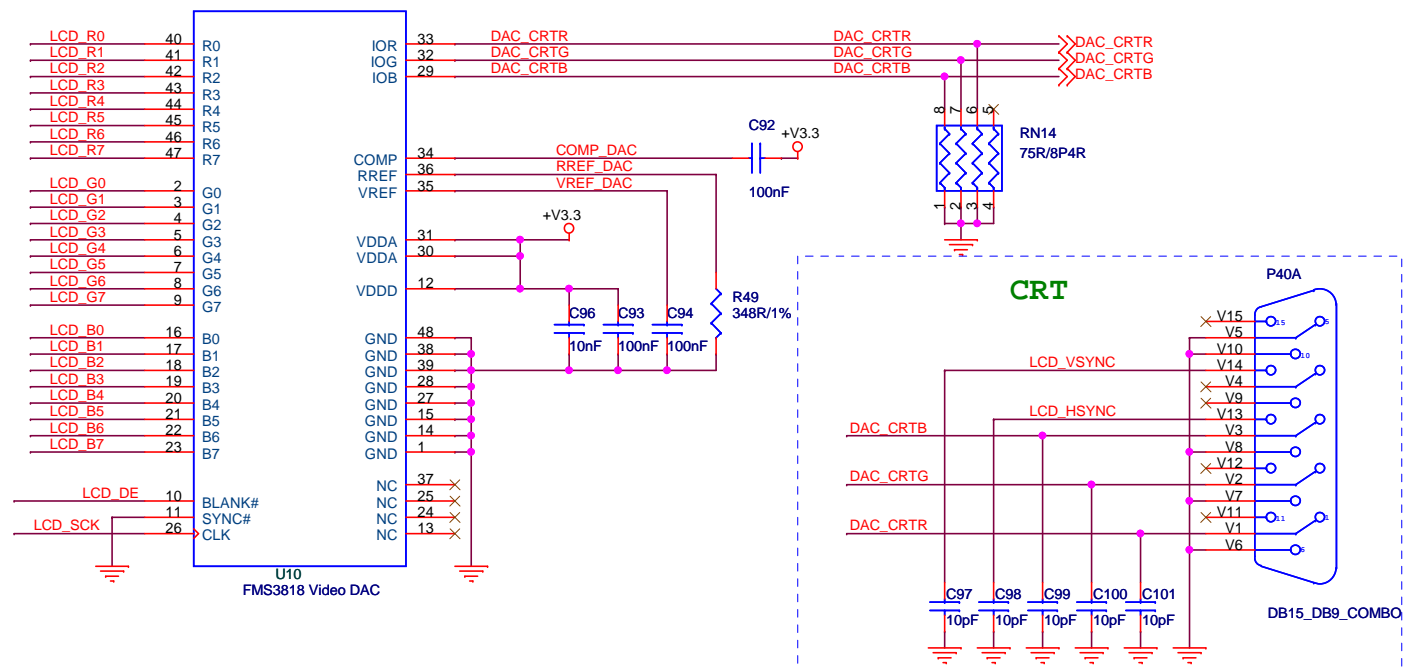


SATA

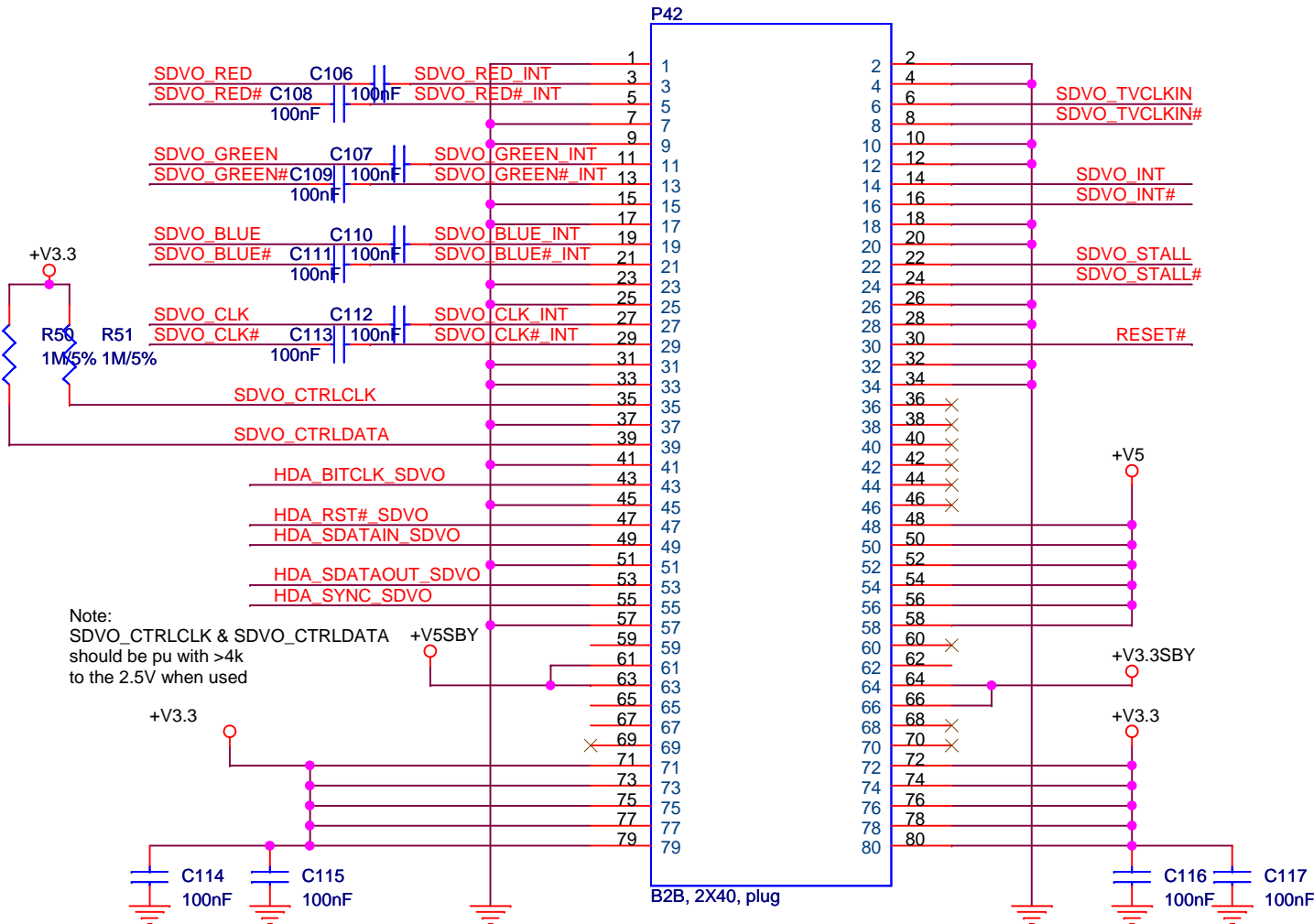


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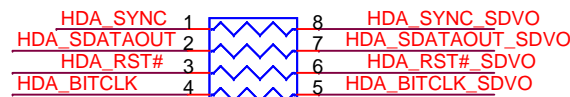
Size		Title		Rev	
Custom		SDIO & SATA		1.2	
		Document Number: 8007538002			
Date:		Wednesday, June 15, 2011		Sheet 6 of 15	



EXTENSION SLOT



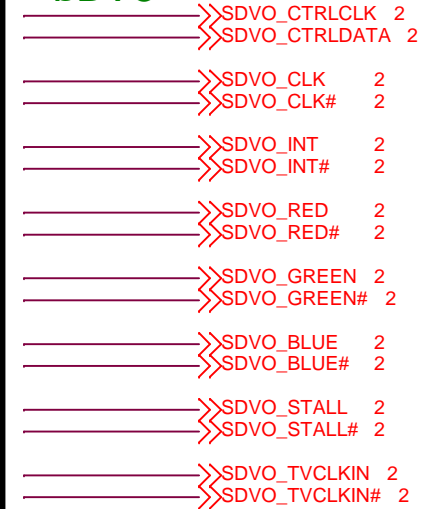
Note:
SDVO_CTRLCLK & SDVO_CTRLDATA
should be pu with >4k
to the 2.5V when used



RN22
33R/8P4R

HDA_SDATAIN0 OR NP HDA_SDATAIN_SDVO

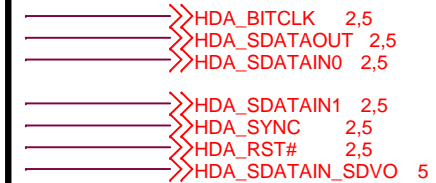
SDVO



MISC

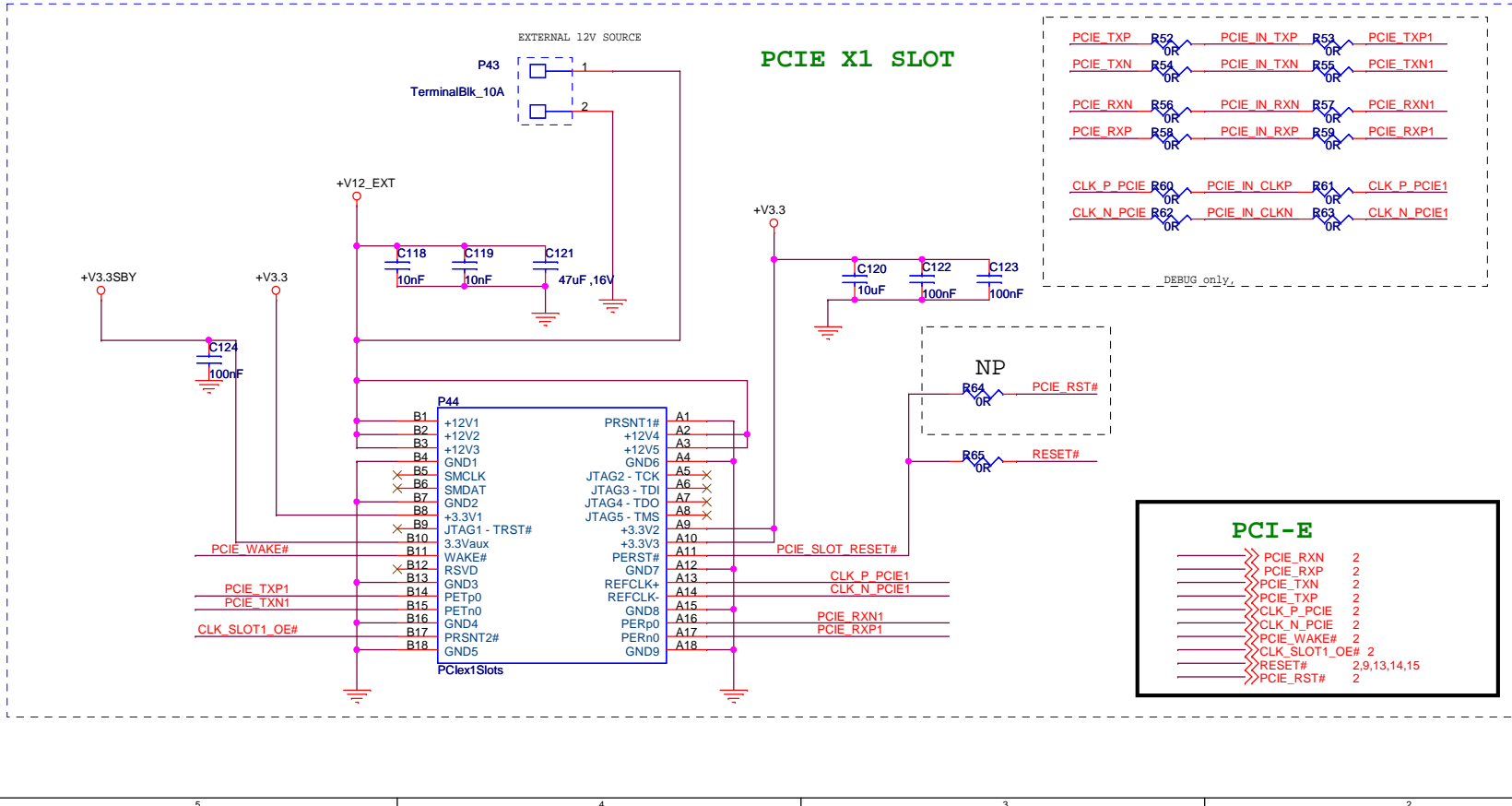
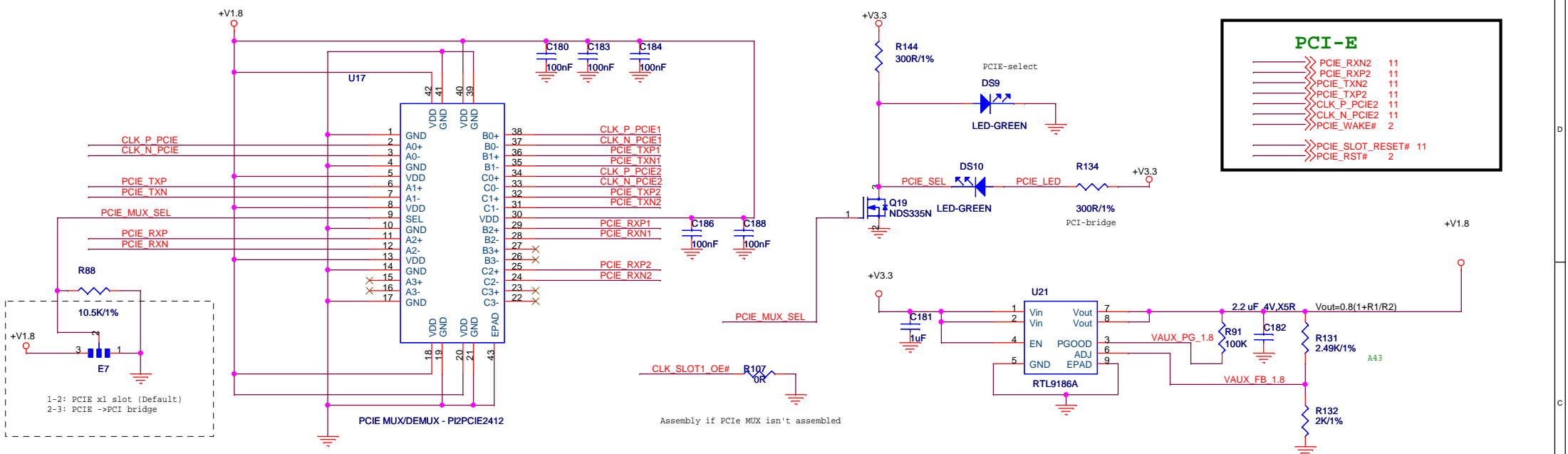


HDA



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Size A	Title SDVO slot	Document Number: 8007538002	Rev 1.2
Date: Tuesday, October 12, 2010	Sheet 9	of 15	



PCI-E

PCIE_RXN2	11
PCIE_RXP2	11
PCIE_TXN2	11
PCIE_TXP2	11
CLK_P_PCIE2	11
CLK_N_PCIE2	11
PCIE_WAKE#	2
PCIE_SLOT_RESET#	11
PCIE_RST#	2

PCIE X1 SLOT

PCIE_TXP	R52	PCIE_IN_TXP	R53	PCIE_TXP1
PCIE_TXN	R54	PCIE_IN_TXN	R55	PCIE_TXN1
PCIE_RXN	R56	PCIE_IN_RXN	R57	PCIE_RXN1
PCIE_RXP	R58	PCIE_IN_RXP	R59	PCIE_RXP1
CLK_P_PCIE	R60	PCIE_IN_CLKP	R61	CLK_P_PCIE1
CLK_N_PCIE	R62	PCIE_IN_CLKN	R63	CLK_N_PCIE1

DEBUG only

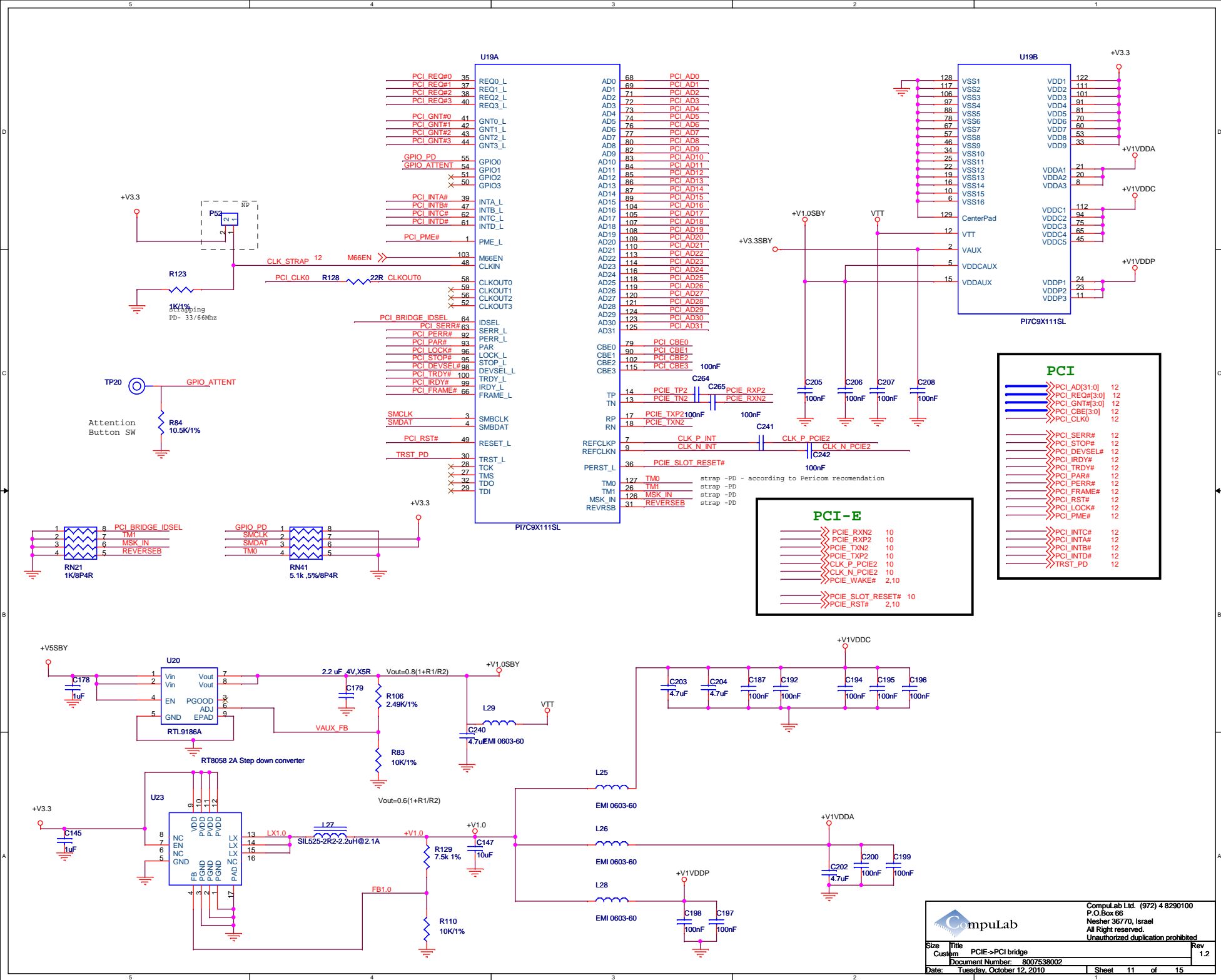
PCIE_WAKE#	B12
PCIE_TXP1	B14
PCIE_TXN1	B15
CLK_SLOT1_OE#	B17

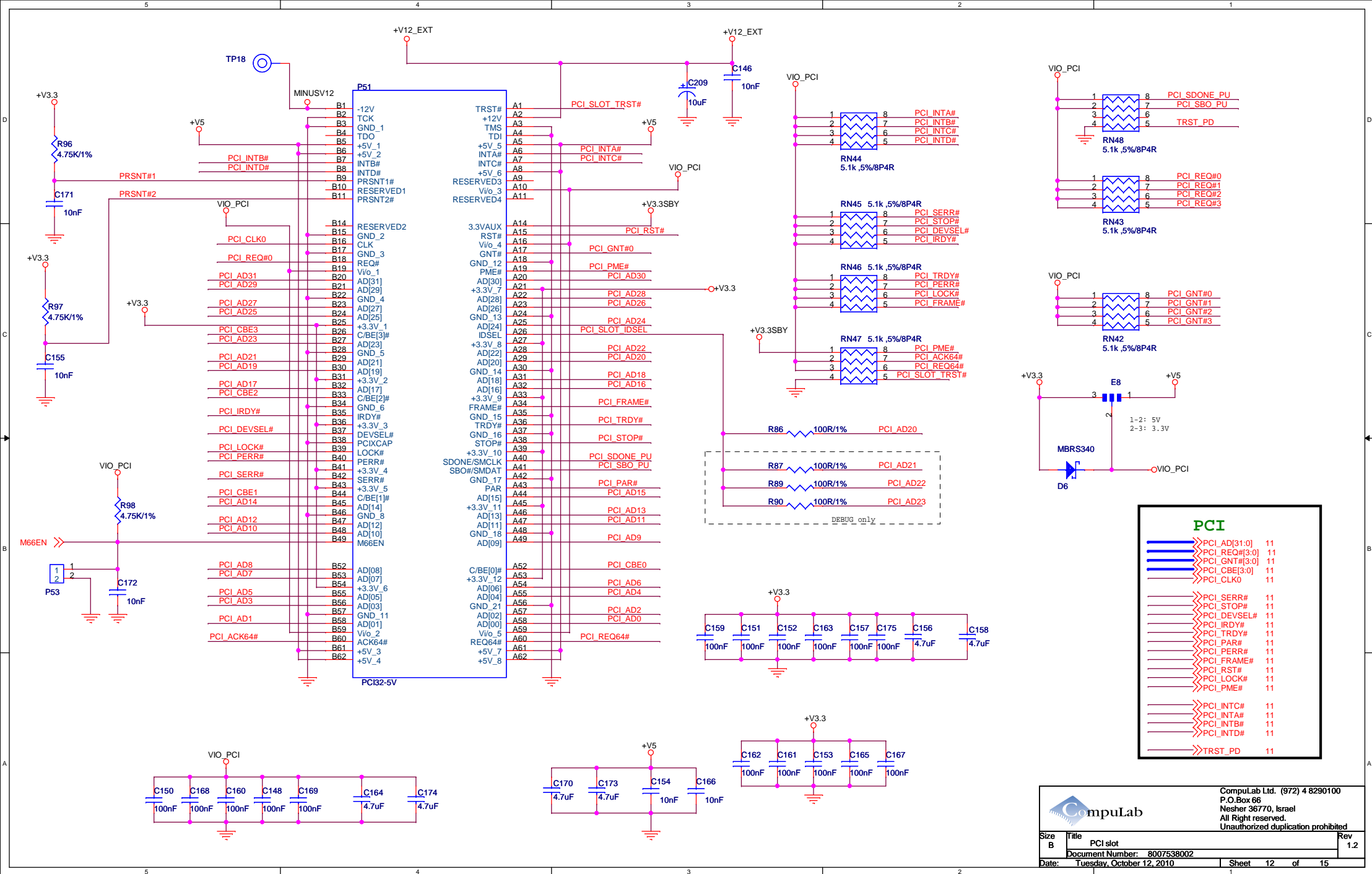
PCI-E

PCIE_RXN	2
PCIE_RXP	2
PCIE_TXN	2
PCIE_TXP	2
CLK_P_PCIE	2
CLK_N_PCIE	2
PCIE_WAKE#	2
CLK_SLOT1_OE#	2
RESET#	2,9,13,14,15
PCIE_RST#	2

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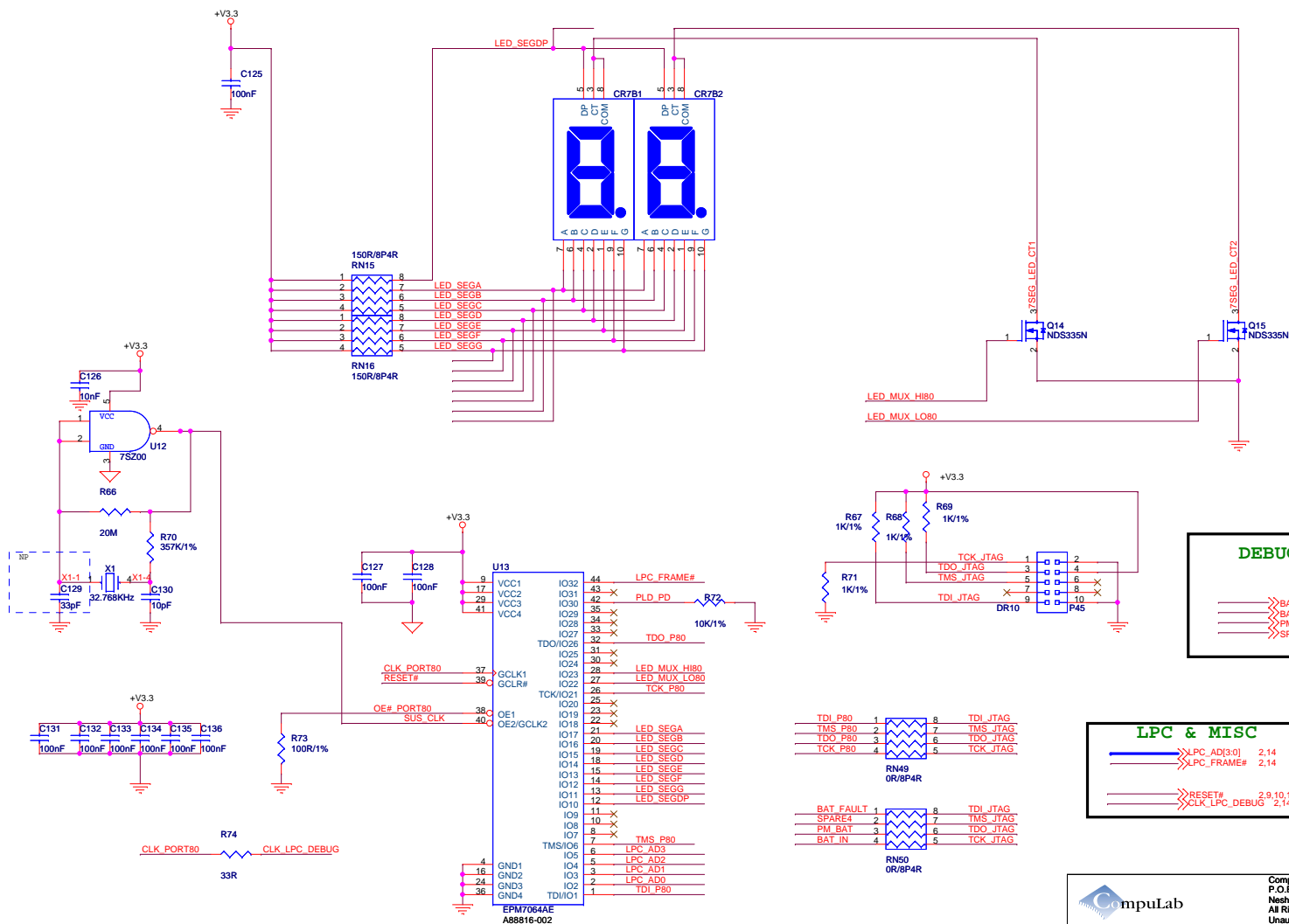
Size	Title	Rev
Custom	PCIE MUX & PCIE slot	1.2
Document Number: 8007538002		
Date:	Tuesday, October 12, 2010	Sheet 10 of 15





DEBUG (DON'T COPY THIS PAGE)

PORT 80 DISPLAY



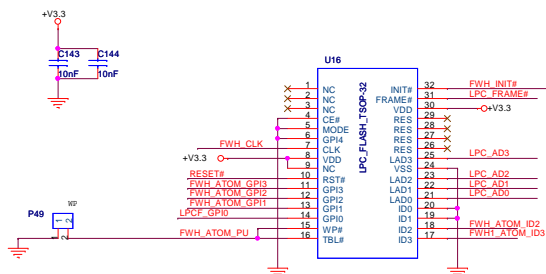
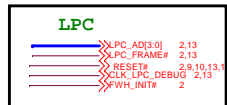
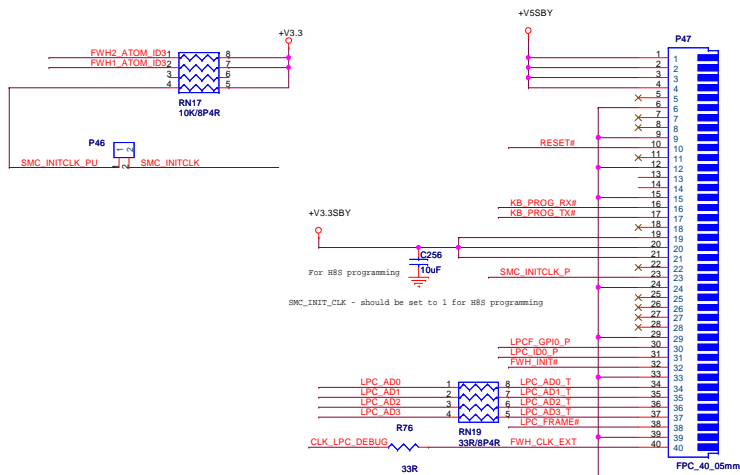
DEBUG2

BAT_IN 2,3
BAT_FAULT 2,3
PM_BAT 2,3
SPARE4 2

LPC & MISC

LPC_AD[3:0] 2,14
LPC_FRAME# 2,14
RESET# 2,9,10,14,15
CLK_LPC_DEBUG 2,14

DEBUG (DON'T COPY THIS PAGE)



Size Title Custom DEBUG (DON'T COPY THIS PAGE) Document Number: 8007538002 Date: Thursday, November 25, 2010 Sheet 14 of 15

