CM-T3517 CoM

Reference Guide

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Table 1 Revision Notes

Date	Description
August 2010	First release
December 2010	Table 25 fixed. CAN bus pins are on Connector P2 and not P1.
May 2011	Table 23 fixed. MMC3_CMD is available at P2-51 and not at P1-51. Table 48 fixed. USB OTG ESD performance changed to ±1 kV using HBM instead of ±8 kV
May 2012	Introduction of CM-T3517 board rev 1.2. Chapter 2.1 revised: WLAN now supports 802.11n. Chapter 2.1 revised: Bluetooth standard v4.0 is now supported. Chapter 2.1 revised: Optional onboard micro-SD socked support added. Figure 1 revised: Block diagram now corresponds with CM-T3517 board rev1.2. Table 3 revised: Added support for onboard bootable miro-SD storage Table 4 revised: WiFi & Bluetooth Interface section. Chapter 3.3.2 renamed and revised: A micro-SD card can now be used as main CM-T3517 boot and storage device. Table 6 revised: GPMC_nCS5 availability changed. Table 6 revised: GPMC_WAIT1 signal type corrected Chapter 4.4.2 revised: a note on TI USB2.0 host ports added. Chapter 4.5 and all related tables revised: Description conforms with WIFI+BT solution used with CM-T3517 board rev1.2. Table 19 revised: UART2 availability changed. Table 23 revised: MMC1 signals availability changed. Table 26 revised: GPIO 11, 31, 56, 120, 121, 122, 123, 124, 125 140, 141, 142, and 143 signals availability changed. Table 26 revised: GPIO_99 and GPIO_100 signals cannot be used as outputs. Table 29 revised: SPI2 signals availability changed. Table 30 revised: McBSP3 signals availability changed Chapter 4.20 revised: A note on WIFI/BT added. Chapter 5.4.1 revised: Availability note added. Figure 4 updated to correspond with CM-T3517 board revision 1.2 Figure 5 updated to correspond with CM-T3517 board revision 1.2
August 2012	Figure 1 revised: Minor changes to block diagram to improve readability. Chapter 1.2 revised – ordering information & webpage link updated. Table 3 revised - Revised options column (storage). Chapter 6.3 revised – DXF formatted mechanical drawings availability note changed. Table 40 fixed – P1-83: UART3_RTS changed to UART3_CTS, no functionality changes, only a documentation bug fix.

Please check for a newer revision of this manual at CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-T3517 Computer-on-Module.

1.2 CM-T3517 Part Number Legend

Please refer to the CompuLab website 'Ordering Information' section to decode the CM-T3517 part number: http://compulab.co.il/products/computer-on-modules/cm-t3517/#ordering

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-T3517 Product Developer Resources	http://www.compulab.co.il/
Sitara AM3517/05 Technical Reference Manual	http://www.ti.com/

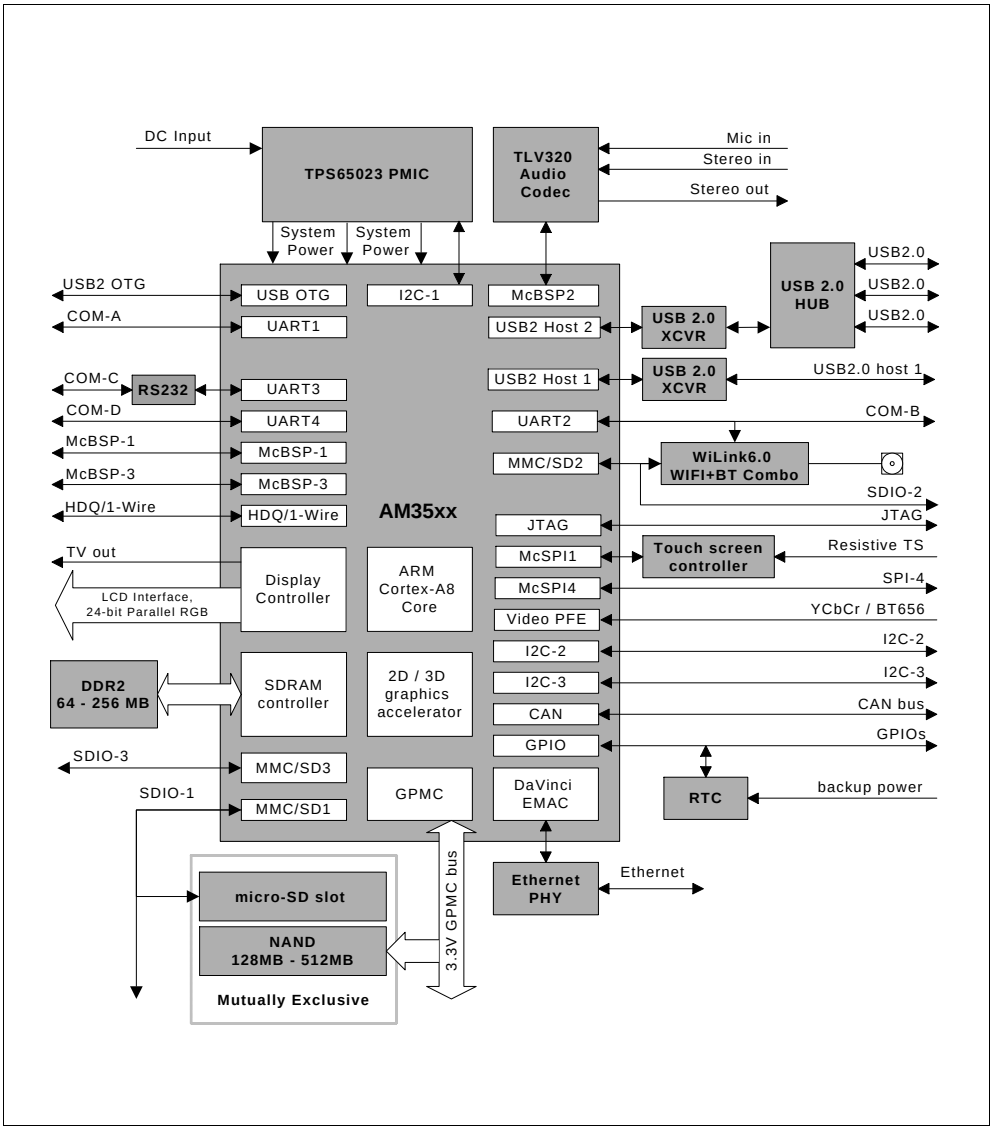
2 OVERVIEW

2.1 Highlights

• Cortex-A8 Sitara AM3505 or AM3517 CPU, up to 600 MHz • Up to 256 Mbyte DDR 2 • Up to 512 Mbyte Flash Disk, including filesystem protection • Optional onboard micro-SD socket for bootloader and storage. • WLAN / WiFi 802.11b/g/n Interface • Bluetooth 4.0 interface • Graphics controller supporting STN and TFT panels with 1400 x 1050 max resolution • PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support • General purpose bus • SDIO / MMC interface • Camera interface port • Audio codec with speaker and microphone support • Touch-screen Controller • USB Slave / Host / OTG ports • Serial ports, GPIO, SPI, I2C, CAN bus • 100 Mbps Ethernet port • Tiny size: 66 x 44 x 7 mm • Interchangeable with other modules via CAMI connectors • SB-T35 carrier board turns the CM-T3517 module into ***SBC-T3517*** - a tiny single board computer	The CM-T3517 is a small Computer-on-Module board designed to serve as a building block in embedded applications. The CM-T3517 includes all the peripherals to run operating systems such as Linux and Windows CE. Ready packages for these operating systems are available from CompuLab. The small size and low power consumption of the CM-T3517 allow its integration into portable and space-constrained designs, while its low price makes it an ideal selection for cost-sensitive applications. The CM-T3517 features Texas Instruments' Sitara AM3517/05 system-on-chip based on the advanced Cortex-A8 ARM CPU with a PowerVR SGX GPU providing 2D / 3D graphics acceleration. For embedded applications, the CM-T3517 provides a general-purpose local bus, 100Mbit Ethernet, CAN bus, serial ports, I/O lines and other essential functions, while the integrated WLAN and Bluetooth interfaces implement industry standard wireless connectivity. The standardized CAMI ("CompuLab's Aggregated Module Interface") connectors of the CM-T3517 module allow interchangeability with other Computer-On-Module's available from CompuLab, enabling the flexibility required by a dynamic market in which application requirements can change rapidly.

2.2 Block Diagram

Figure 1 CM-T3517 Block Diagram



2.3 CM-T3517 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available.

Table 3 CPU, Memory and Busses

Feature	Specifications	Option
CPU	Texas Instruments Sitara AM3505 / AM3517 CPU 600 MHz, NEON™ SIMD Coprocessor L1 cache: 32 KB L2 cache: 256 KB DMA, Interrupt controllers, Timers	C600/C600G
RAM	64 - 256 MB, DDR2-333 MHz, 32/16-bit	D64/D128/D256
Onboard Storage	An onboard micro-SD socket.	NS0
	An onboard micro-SD socket, incl. an 8GB pre-flashed micro-SD card	NS8
	Onboard 128Mbytes bootable SLC NAND Flash	N128
	Onboard 512Mbytes bootable SLC NAND Flash	N512
External local bus	16-bit, variable rate up to 83 MHz, 3.3V levels	+

Table 4 Peripherals

Feature	Specifications	Option
Graphics Controller	1/2/4/8/12/16/24 bpp, resolution up to 1400 x 1050, HD 720p resolution support @ 60fps. Remote frame buffer support. Display types support: TFT (parallel RGB), STN, composite video - PAL / NTSC	+
2D / 3D graphics	PowerVR SGX GPU providing 2D / 3D graphics acceleration with OpenGL-ES and OpenVG support. Part of Sitara AM3517 CPU	C600G
VPFE Interface	REC656/CCIR-656 standard support YCbCr 4:2:2 support 8-bit interface. Pixel clock up to 75MHz. DMA support	+
USB	- Host / Slave (OTG) USB2 high-speed port, 480 Mbps	+
	- One, two or four additional USB2 host ports, 480 Mbps, EHCI/OHCI compliant	U2/U3/U5
Serial Ports (UART's)	Up to 4 UART ports, 16C750 compatible: COM-A – 3.3V interface, partial modem controls, 3.6 Mbps COM-B – 3.3V interface, partial modem controls, 3.6 Mbps COM-C - RS232 interface, Rx / Tx only, 250 Kbps COM-D – 3.3V interface, partial modem controls, 3.6 Mbps	+
General Purpose I/O	Up to 134 lines shared with other functions. Can also be used as interrupt inputs	+
Keyboard & mouse	USB, or redirection from COM port	+
Ethernet	Sitara integrated EMAC & PHY, 10/100BaseT, Activity LED's	E
MMC / SD /SDIO	MMC / SD / SDIO support including SDHC up to 32GB	+
Audio codec	I2S/McBSP compliant audio codec, stereo output, electret mic input, mic bias output.	A
Touchscreen ctrl.	TSC2046 touchscreen controller. Support 4-wire resistive panels	I
RTC	Real Time Clock, powered by external lithium battery	+
WiFi & Bluetooth Interface	Implements 802.11b/g/n wireless connectivity standard. Based on TI WiLink6.0 WL1271 solution. Bluetooth 4.0 (also compliant with Bluetooth 2.1 + EDR) On-board connector for external antenna.	W

NOTE: A valid configuration must contain one "CPU" option, one "RAM" option and one "Onboard Storage" option

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 3.6V or Lithium-ion polymer battery
Active power consumption	0.2 - 2 W, depending on configuration and CPU speed
Dimensions	66 x 44 x 7 mm
Weight	16 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C Extended: -20° to 70° C Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 CORE SYSTEM COMPONENTS

3.1 Sitara AM3517/05 CPU

The Sitara AM3517/05 family of high-performance application processors is based on the enhanced OMAP™ 3 architecture and is integrated on Texas Instruments' 65-nm process technology.

The architecture is designed to provide video, image, graphics and processing power sufficient to support the following:

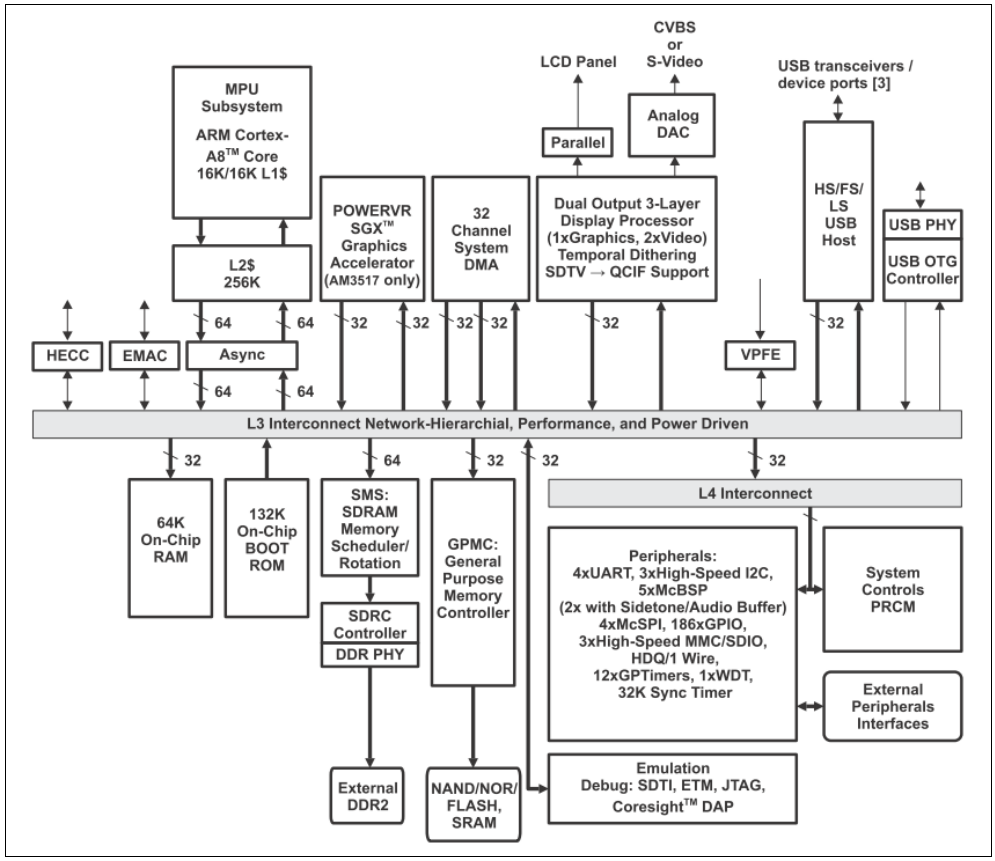
- Home and Industrial automation
- Test and measurement
- Digital Signage
- Medical instrumentation
- Remote monitoring
- Motion control
- Point-of-Sale
- Single Board Computers

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 microprocessor
- SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects
- Display subsystem with multiple concurrent image manipulation support, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- Level 3 (L3) and level 4 (L4) interconnects providing high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals

The device also offers a comprehensive power and clock-management scheme enabling high-performance and low-power operation features.

Figure 2 Sitara AM3517/05 Block Diagram



3.2 Multimedia System

3.2.1 Multimedia Accelerator

The Sitara AM3517 2D and 3D graphics accelerator (SGX) provides support for the following imaging and video features:

- 2D and 3D graphics, vector graphics, and programming support for GP-GPU functions
- Tile-based architecture
- An advanced shader feature set in excess of Microsoft VS3.0, PS3.0 and OGL2.0
- Industry standard API supports Direct3D mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0.1 and OpenMax
- Fine-grained task switching, load balancing and power management
- Programmable high-quality image anti-aliasing
- Advanced geometry DMA driven operation for minimum CPU interaction
- POWERVR SGX core MMU for address translation from the core virtual address to the external physical address (up to 4GB address range).
- Fully virtualized memory addressing for OS operation in a unified memory architecture
- Advanced and standard 2D operations (that is, vector graphics, BLT's, ROP's, etc.)

NOTE: Multimedia features are available only with the 'C600G' configuration option.

3.3 Memory

3.3.1 DRAM

The CM-T3517 board is assembled with 128 or 256 Mbytes of DDR2 SDRAM. The DDR2 interface is 32/16-bits wide and runs with a 166 MHz clock.

3.3.2 Onboard Storage

The CM-T3517 is equipped with one of the following onboard storage solutions:

- Either 128 or 512 Mbytes of SLC NAND Flash pre-loaded with boot-loader software.
- Onboard micro-SD socket. An 8GB micro-SD card, pre-loaded with boot-loader software is available with the NS8 option.

The onboard storage solution of choice, serves as the main non-volatile memory device of the CM-T3517. This non-volatile storage is used for storing the boot-loader and the OS.

NOTE: Ordering an Extended/Industrial temperature version of the CM-T3517 precludes the NS8 (8GB micro-SD) option. For detailed instructions on bootable micro-SD preparation, please refer to the CompuLab website.

4 PERIPHERAL INTERFACES

The CM-T3517 implements a number of peripheral interfaces through the CAMI connectors (P1 and P2). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the CM-T3517. Each signal's availability is noted in the "Signals description" table of each interface.
- Most CAMI pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to chapter 5.5.
- Certain signals are available on more than one CAMI pin. Only one CAMI pin can be used for each signal.
- All of the CM-T3517 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal
- **"Pin#" –** The pin number on the CAMI connector
- **"Type" –** Signal type
- **"Description" –** Signal description
- **"Availability" –** Certain signals are not available with/without certain configuration options. This column summarizes configuration requirements for each signal.

Each CAMI signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal

- **"O"** – Digital output
- **"I"** – Digital input
- **"IO"** – Digital Input/Output
- **"AO"** – Analog Output
- **"AI"** – Analog Input
- **"OD"** – Open Drain Signal (not pulled up on the CM-T3517 unless otherwise noted)
- **"IPU"** – Open Drain Signal (pulled up on the CM-T3517 unless otherwise noted)

4.1 Local Bus

The CM-T3517 local bus is derived from the Sitara AM3517/05 general-purpose memory controller (GPMC) bus.

The GPMC is dedicated to interfacing with the following external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous and page mode (only available in non-muxed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For additional details, please refer to section 9.1 of the "Sitara AM3517/05 Technical Reference Manual".

Table 6 Local bus signal descriptions

Signal Name	Pin #	Type	Description	Availability
GPMC_A1	P1-71*	O	Address bit 1	Always available
GPMC_A2	P1-70*	O	Address bit 2	Always available
GPMC_A3	P1-73*	O	Address bit 3	Always available
GPMC_A4	P1-72*	O	Address bit 4	Always available
GPMC_A5	P1-75*	O	Address bit 5	Always available
GPMC_A6	P1-76*	O	Address bit 6	Always available
GPMC_A7	P1-77*	O	Address bit 7	Always available
GPMC_A8	P1-78*	O	Address bit 8	Always available
GPMC_A9	P1-81*	O	Address bit 9	Always available
GPMC_A10	P1-80*	O	Address bit 10	Always available
GPMC_D0	P1-94	IO	Data bit 0	Always available
GPMC_D1	P1-95	IO	Data bit 1	Always available
GPMC_D2	P1-96	IO	Data bit 2	Always available
GPMC_D3	P1-97	IO	Data bit 3	Always available
GPMC_D4	P1-100	IO	Data bit 4	Always available
GPMC_D5	P1-99	IO	Data bit 5	Always available
GPMC_D6	P1-102	IO	Data bit 6	Always available
GPMC_D7	P1-101	IO	Data bit 7	Always available
GPMC_D8	P1-104*	IO	Data bit 8	Always available
GPMC_D9	P1-105*	IO	Data bit 9	Always available
GPMC_D10	P1-106*	IO	Data bit 10	Always available
GPMC_D11	P1-107*	IO	Data bit 11	Always available
GPMC_D12	P1-108*	IO	Data bit 12	Always available
GPMC_D13	P1-109*	IO	Data bit 13	Always available
GPMC_D14	P1-112*	IO	Data bit 14	Always available
GPMC_D15	P1-111*	IO	Data bit 15	Always available
GPMC_nCS1	P1-118*	O	Chip select bit 1	Only available **without** 'E' option.
GPMC_nCS3	P1-92*	O	Chip select bit 3	Always available
GPMC_nCS4	P1-93*	O	Chip select bit 4	Always available
GPMC_nCS5	P1-58*	O	Chip select bit 5	Only available **without** 'W' option.
GPMC_nCS7	P1-85*	O	Chip select bit 7	Always available
GPMC_IODIR			IO direction control for use with external transceivers	
GPMC_CLK	P1-88*	O	Clock	Always available
GPMC_nADV	P1-90	O	Address valid	Always available
GPMC_ALE			Address latch enable for NAND protocol memories	
GPMC_nWE	P1-84	O	Write enable	Always available
GPMC_nBE0	P1-82	O	Lower byte enable	Always available
GPMC_CLE			Command latch enable for NAND protocol memories	
GPMC_nBE1	P1-87*	O	Upper byte enable	Always available

Signal Name	Pin #	Type	Description	Availability
GPMC_WAIT3	P1-83*	I	External wait signal for NOR and NAND protocol memories	Always available
GPMC_nOE	P1-89	O	Output enable	Always available
GPMC_nRE			Read enable for NAND protocol memories	
GPMC_WAIT1	P2-76*	I	External wait signal for NOR and NAND protocol memories	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.2 Display Interface

The CM-T3517 display subsystem is based on the display interface of the Sitara AM3517/05.

The display subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on either a liquid-crystal display (LCD) panel or a TV set.

The display subsystem supports the following main features:

Display controller

- Programmable pixel display modes (1, 2, 4, 8, 12, 16 and 24 bits-per-pixel)
- Programmable panel size up to 2048 (lines) x 2048 (pixels)
- 256 x 24-bit entries palette in red, green and blue (RGB)
- Programmable pixel rate up to 75 MHz
- Four types of displays are supported: passive (STN) and active (TFT) colors, passive (STN) and active (TFT) monochromes
- Overlay support for graphics
- Programmable video re-sizer independent horizontal and vertical re-sampling
- Rotation of 90-, 180- and 270-degrees

Video encoder

- NTSC/PAL encoder outputs with the following standards:
  - NTSC-J, M
  - PAL-B, D, G, H, I
  - PAL-M
  - CGMS-A as described in the CEA-608-x standard
- Composite video (CVBS)
- Separate video (S-video)

For additional details, please refer to section 12 of the "Sitara AM3517/05 Technical Reference Manual".

Table 7 Display interface signals

Signal Name	Pin #	Type	Description	Availability
LCD Interface				
LCD_PCLK	P2-112*	O	Pixel clock	Always available
LCD_HSYNC	P2-96*	O	Horizontal synchronization	Always available
LCD_VSYNC	P2-111*	O	Vertical synchronization	Always available
LCD_ACBIAS LCD_DE	P2-114*	O	AC bias control (STN) Pixel data enable (TFT)	Always available
LCD_D0	P2-95*	O	Pixel data bit 0	Always available
	P2-94*			Always available
LCD_D1	P2-97*	O	Pixel data bit 1	Always available
	P2-123*			Always available
LCD_D2	P2-100*	O	Pixel data bit 2	Always available
	P2-126*			Always available
LCD_D3	P2-99*	O	Pixel data bit 3	Always available
	P2-121*			Always available
LCD_D4	P2-102*	O	Pixel data bit 4	Always available
	P2-124*			Always available
LCD_D5	P2-101*	O	Pixel data bit 5	Always available
	P2-93*			Always available
LCD_D6	P2-104*	O	Pixel data bit 6	Always available
LCD_D7	P2-106*	O	Pixel data bit 7	Always available
LCD_D8	P2-105*	O	Pixel data bit 8	Always available
LCD_D9	P2-108*	O	Pixel data bit 9	Always available

LCD_D10	P2-107*	O	Pixel data bit 10	Always available
LCD_D11	P2-109*	O	Pixel data bit 11	Always available
LCD_D12	P2-113*	O	Pixel data bit 12	Always available
LCD_D13	P2-116*	O	Pixel data bit 13	Always available
LCD_D14	P2-118*	O	Pixel data bit 14	Always available
LCD_D15	P2-117*	O	Pixel data bit 15	Always available
LCD_D16	P2-120*	O	Pixel data bit 16	Always available
LCD_D17	P2-119*	O	Pixel data bit 17	Always available
LCD_D18	P2-124*	O	Pixel data bit 18	Always available
LCD_D19	P2-121*	O	Pixel data bit 19	Always available
LCD_D20	P2-126*	O	Pixel data bit 20	Always available
LCD_D21	P2-123*	O	Pixel data bit 21	Always available
LCD_D22	P2-94*	O	Pixel data bit 22	Always available
LCD_D23	P2-93*	O	Pixel data bit 23	Always available
Video Encoder				
TV_OUT1	P2-1	AO	TV analog output composite	Always available
TV_OUT2	P2-3	AO	TV analog output S-VIDEO	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.3 Ethernet

The CM-T3517 incorporates a single full-featured 10/100 Ethernet interface, implemented with the Sitara AM3517/05 integrated multimedia access controller (DaVinci EMAC) coupled with an on-board 10/100 PHY.

The CM-T3517 Ethernet interface supports the following main features:

- Fully compliant with IEEE 802.3u standard
- 10BASE-T and 100BASE-TX
- Full- and Half-duplex
- HP auto MDI/MDI-X
- Activity and speed indicator LED controls

For additional details regarding the DaVinci EMAC, please refer to section 22 of the "Sitara AM3517/05 Technical Reference Manual".

Table 8 Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
CM_ETH_TXP	P1-1	AO	Transmit positive output	Only available **with** 'E' option.
CM_ETH_TXN	P1-3	AO	Transmit negative output	Only available **with** 'E' option.
CM_ETH_RXP	P1-4	AI	Receive positive input	Only available **with** 'E' option.
CM_ETH_RXN	P1-2	AI	Receive negative input	Only available **with** 'E' option.
CM_ETH_LED1	P1-6	OD	Activity indicator LED output. Active low (pulled up).	Only available **with** 'E' option.
CM_ETH_LED2	P1-5	OD	Speed indicator LED output. Active (100Mbs) low (pulled up).	Only available **with** 'E' option.

NOTE: For magnetics selection recommendations, please refer to section *8.3* of this document.

4.4 USB 2.0

4.4.1 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the Sitara AM3517/05 USB 2.0 OTG controller. The interface provides the following features:

- Supports USB 2.0 peripheral at High Speed (480 Mbps) and Full Speed (12 Mbps)
- Supports USB 2.0 host or OTG at High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps)
- Supports all modes of transfers (control, bulk, interrupt and isochronous).
- Supports 16 transmit (TX) and 16 receive (RX) endpoints including endpoint 0

For additional details on USB2.0 OTG, please refer to section 20.1 of the "Sitara AM3517/05 Technical Reference Manual".

Table 9 USB 2.0 OTG interface signals

Signal Name	Pin #	Type	Description	Availability
USB0_DP*	P1-136	AOI	USB OTG positive data	Always available
USB0_DN*	P1-138	AOI	USB OTG negative data	Always available
USB0_ID	P1-137	AI	USB OTG ID	Always available
USB0_5V_OUT	P1-140	P	USB OTG VBUS power rail	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.4.2 USB 2.0 Host

The CM-T3517 high-speed USB2.0 host interface is implemented with the Sitara AM3517/05 high-speed USB host subsystem. It provides up to two USB2.0 host ports and supports the following features:

- Complies with EHCI (high-speed host controller)
- Complies with OHCI (low-speed/full-speed host controller)
- Complies with the USB 2.0 standard for high-speed (480M bit/s) functions

In addition to the AM3517/05 integrated USB2.0 host subsystem, the CM-T3517 is equipped with a USB2.0 hub, providing three downstream host ports.

For additional details on USB2.0 host controllers of the Sitara AM3517/05, please refer to section 20.2 of the "Sitara AM3517/05 Technical Reference Manual".

Figure 3 CM-T3517 USB2.0 host sub-system

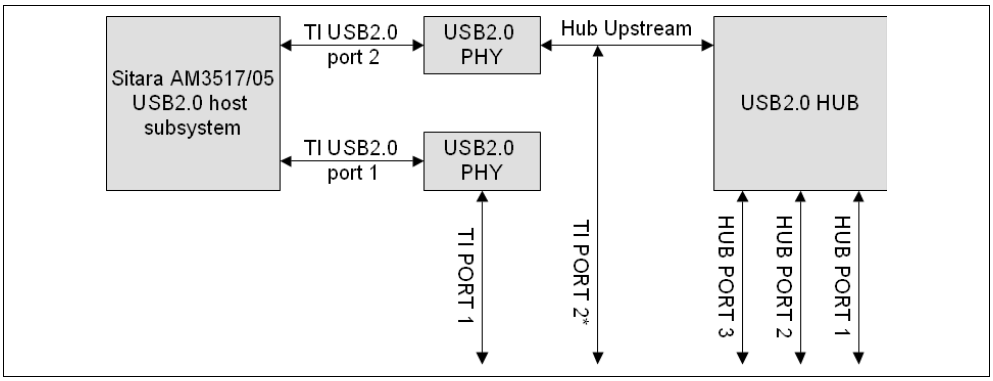


Table 10 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
TI Port 1				
USB1_DP	P2-138	AOI	USB host port 1 positive data	Only available **with** 'U3', or 'U5' option.
USB1_DM	P2-140	AOI	USB host port 1 negative data	Only available **with** 'U3', or 'U5' option.
USB1_CPEN	P2-6	O	USB host port 1 external 5V supply enable. Active high.	Only available **with** 'U3', or 'U5' option.
USB1_VBUS	P2-8	AI	USB host port 1 external 5V supply sense input.	Only available **with** 'U3', or 'U5' option.
TI Port 2				
USB2_DP	P2-137	AOI	USB host port 2 positive data	Only available **with** 'U2' or 'U3' option.
USB2_DM	P2-139	AOI	USB host port 2 negative data	Only available **with** 'U2' or 'U3' option.
USB2_CPEN	P2-9	O	USB host port 2 external 5V supply enable. Active high.	Only available **with** 'U2' or 'U3' option.
USB2_VBUS	P2-11	AI	USB host port 2 external 5V supply sense input.	Only available **with** 'U2' or 'U3' option.
HUB Port 1				
HUBP1_DP	P2-137	AOI	USB hub port 1 positive data	Only available **with** 'U5' option.
HUBP1_DM	P2-139	AOI	USB hub port 1 negative data	Only available **with** 'U5' option.
HUBP1_CPEN	P2-9	O	USB hub port 1 external 5V supply enable. Active high.	Only available **with** 'U5' option.
HUBP1_nOVC	P1-51	IPU	USB hub port 1 Over-current sense input, active LOW	Only available **with** 'U5' option.

Signal Name	Pin #	Type	Description	Availability
HUB Port 2				
HUBP2_DP	P2-40	AOI	USB hub port 2 positive data	Only available **with** 'U5' option.
HUBP2_DM	P2-42	AOI	USB hub port 2 negative data	Only available **with** 'U5' option.
HUBP2_CPEN	P2-36	O	USB hub port 2 external 5V supply enable. Active high.	Only available **with** 'U5' option.
HUBP2_nOVC	P1-59	IPU	USB hub port 2 Over-current sense input, active LOW	Only available **with** 'U5' option.
HUB Port 3				
HUBP3_DP	P2-33	AOI	USB hub port 3 positive data	Only available **with** 'U5' option.
HUBP3_DM	P2-35	AOI	USB hub port 3 negative data	Only available **with** 'U5' option.
HUBP3_CPEN	P2-41	O	USB hub port 3 external 5V supply enable. Active high.	Only available **with** 'U5' option.
HUBP3_ nOVC	P1-69	IPU	USB hub port 3 Over-current sense input, active LOW	Only available **with** 'U5' option.

NOTE: The TI USB 2.0 host ports ("TI port 1" and "TI port 2") do not support low-speed and full-speed operation modes. External USB hub is recommended in order to enable these operation modes. Please refer to the SB-T35 design package for a comprehensive reference design.

4.5 WLAN & Bluetooth

The CM-T3517 incorporates full-featured 802.11b/g/n and Bluetooth 4.0 capabilities, implemented with the Murata LBEH59XUHC WLAN + Bluetooth combo controller module. The LBEH59XUHC is based on the TI WiLink6.0 WL1271 chipset.

WLAN Standards supported:

- 802.11b data rates of 1, 2, 5.5 and 11 Mbps.
- 802.11g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps.
- 802.11n-2.4G data rates of 6.5, 13, 19.5, 26, 39, 52, 58.5 and 65 Mbps.

Bluetooth standards supported:

- Bluetooth 4.0
- Bluetooth Power Class 1

The LBEH59XUHC SiP is interfaced with the Sitara AM3517/05 SoC using the MMC-2 and UART-2 ports. MMC-2 is used for WLAN data while UART-2 is used for Bluetooth data.

Antenna Connection

The LBEH59XUHC requires a single 2.45GHz antenna. The antenna is connected via the onboard UFL high frequency connector J1. Any type of 2.45GHz antenna can be used. Please refer to section 6.3 for connector location.

Table 11 J1 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 12 Test Conditions (Tables 13, 14, 15 and 16)

Parameter	Value
Temperature	25˚C
VCC_CM	3.6V

Table 13 802.11b (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	14	16	18	dBm
Spectrum Mask				
1st side lobes		-40	-30	dBr
2nd side lobes		-55	-50	dBr
Power-on and Power-down ramp		0.1	2	µSec
RF Carrier Suppression	15	37		dB
Modulation Accuracy (EVM)		10	35	%
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-60	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
11Mbps (FER ≤ 8%)		-87	-76	dBm
Maximum Input Level (FER ≤ 8%)	-10	0		dBm

Table 14 802.11g (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	11	13	15	dBm
Spectrum Mask				
at fc +/- 11MHz		-30	-20	dBr
at fc +/- 20MHz		-33	-28	dBr
at fc +/- 30MHz		-45	-40	dBr
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-65	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
Constellation Error (EVM)		-30	-25	dB
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
54Mbps (PER ≤ 10%)		-73	-65	dBm
Maximum Input Level (PER ≤ 10%)	-20	-4		dBm

Table 15 802.11n (WLAN) RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Power Levels	10	12	14	dBm
Spectrum Mask				
at fc +/- 11MHz		-30	-20	dBr
at fc +/- 20MHz		-35	-28	dBr
at fc +/- 30MHz		-50	-45	dBr
Spurious Emissions				
30MHz to 1GHz		-80	-36	dBm
1GHz to 12.75GHz		-65	-30	dBm
1.8GHz to 1.9GHz		-80	-47	dBm
5.15GHz to 5.3GHz		-80	-47	dBm
Constellation Error (EVM)		-30	-28	dB
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Minimum Input Level Sensitivity				
54Mbps (PER ≤ 10%)		-67	-64	dBm
Maximum Input Level (PER ≤ 10%)	-20	-5		dBm

Table 16 Bluetooth RF system specifications

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Output Power	4.5	8.0		dBm
Frequency range (Rx/Tx)	2400 – 2483.5			MHz
-20db bandwidth		0.8	1	MHz
Adjacent Channel Power (Up to 3 spurious responses within Bluetooth limits are allowed)				
[M-N] = 2		-45	-20	dBm
[M-N] ≥ 3		-46	-40	dBm
Modulation Characteristics				
Modulation δf1avg	140	158	175	kHz
Modulation δf2max	115	132		kHz
Modulation δf2avg/δf1avg	0.8	0.9		kHz
Carrier Frequency Drift				
1 slot	-25		+25	kHz
3 slot	-40		+40	kHz
5 slot	-40		+40	kHz
Maximum drift rate	-20		+20	kHz/ 50µS

TX Characteristics				
Parameter	Min	Typ	Max	Unit
Out-of Band Spurious Emissions				
30-1000MHz (Operation mode)		-58	36	dBm
1000-12750MHz (Operation mode)		-40	-30	dBm
1800-1900MHz (Operation mode)		-80	-47	dBm
5150-5300MHz (Operation mode)		-80	-47	dBm
EDR Relative Power (π/4-DQPSK and 8DPSK)	-4	-0.2	1	
EDR Carrier Frequency Stability and Modulation Accuracy				
ωi (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
ω0 (Pi/4-DQPSK and 8DPSK)	-10	0	10	kHz
ωi+ω0 (Pi/4-DQPSK and 8DPSK)	-75	0	75	kHz
RMS DEVM (Pi/4-DQPSK)		6	20	%
99% DEVM (Pi/4-DQPSK)		10	30	%
Peak DEVM (Pi/4-DQPSK)		14	35	%
RMS DEVM (8DPSK)		6	13	%
99% DEVM (8DPSK)		10	20	%
Peak DEVM (8DPSK)		15	25	%
RX Characteristics				
Parameter	Min	Typ	Max	Unit
Sensitivity (BER < 0.1%)				
2402MHz		-90	-70	dBm
2441MHz		-90	-70	dBm
2480MHz		-90	-70	dBm
C/I Performance (BER < 0.1%) (Up to 5 spurious responses within Bluetooth limits are allowed.)				
co-channel ratio (-60dBm input)		7	11	dB
1MHz ratio (-60dBm input)		-9	0	dB
2MHz ratio (-60dBm input)		-46	-30	dB
3MHz ratio (-67dBm input)		-48	-40	dB
image +/- 1MHz ratio (-67dBm input)		-30	-20	dB
Blocking performance (BER < 0.1%) (Up to 24 spurious responses within Bluetooth limits are allowed.)				
30MHz-2000MHz	-10	-8		dBm
2000MHz-2400MHz	-27	0		dBm
2500MHz-3000MHz	-27	0		dBm
3000MHz-12750MHz	-10	-5		dBm
Intermodulation performance (BER < 0.1%, -64dBm input)	-39	-30		dBm
Maximum Input Level	-20	10		dBm
EDR Sensitivity (at 0.01% BER)				
π/4-DQPSK		-90	-70	dBm
8DPSK		-84	-70	dBm

For additional details, please refer to the Murata LBEH59XUHC datasheet.

NOTE: The WLAN & Bluetooth module is available only with the 'W' configuration option.

4.6 Audio

The CM-T3517 audio subsystem is implemented with the Texas Instruments TLV320AIC23b audio codec. The audio subsystem supports the following features:

- Single ended stereo-line output
- Single ended stereo-line input
- Integrated total electret-microphone biasing and buffering solution
- 8-kHz – 96-kHz Sampling-Frequency Support
- 100-dB SNR Multibit Sigma-Delta DAC (A-weighted at 48 kHz)
- 90-dB SNR Multibit Sigma-Delta ADC (A-weighted at 48 kHz)

Table 17 Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		
	Rload = 16Ω			40		
Signal-to-noise ratio, A-weighted (see Note 2)			90	97		dB
Total harmonic distortion	1kHz output	Pout = 10mW			0.1	%
		Pout = 20mW			1.0	%
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
Programmable gain	1 kHz output		-73		6	
Programmable-gain step size				1		
Mute attenuation	1 kHz output			80		
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 1 and 2)	Fsample = 48 kHz.		85	90		dB
Dynamic range, A-weighted, −60-dB full-scale input (see Note 2)			85	90		dB
Total harmonic distortion, −1-dB input, 0-dB gain				-80		dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain step size	Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10		20	kΩ
	0 dB input gain		30	35		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 1 and 2)			80	85		dB
Dynamic range, A-weighted, −60-dB full-scale input (see Note 2)			80	85		dB
Total harmonic distortion, −1-dB input, 0-dB gain				-60		dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
Mute attenuation	0dB, 1 kHz input tone		60	80		dB
Input resistance			8		14	kΩ
Input capacitance				10		pF
Microphone BIas						
Bias voltage			2.375	2.475	2.575	V
Bias-current source					3	mA

For additional details, please refer to the TLV320AIC23B datasheet, available from Texas Instruments.

Table 18 Audio signals

Signal Name	Pin #	Type	Description	Availability
AUDIO_OUT_R	P2-136	AO	Right stereo mixer-channel amplified headphone output	Only available **with** the 'A' option.
AUDIO_OUT_L	P2-130	AO	Left stereo mixer-channel amplified headphone output	Only available **with** the 'A' option.
AUDIO_IN_R	P2-132	AI	Right stereo-line input channel	Only available **with** the 'A' option.
AUDIO_IN_L	P2-128	AI	Left stereo-line input channel	Only available **with** the 'A' option.
MIC_IN_ELECTRET	P2-131	AI	Buffered amplifier input suitable for use with electret-microphone capsules	Only available **with** the 'A' option.
MIC_BIAS	P2-129	O	Microphone bias output, suitable for electret-microphone-capsule biasing, 2.475V nominal.	Only available **with** the 'A' option.
AGND	P2-125	P	Dedicated analog audio ground	Only available **with** the 'A' option.

4.7 UART

The CM-T3517 incorporates four general-purpose UART interfaces. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 3.6M bit/s
- Configurable data format

For additional details on UART interfaces of the Sitara AM3517/05, please refer to section 14 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Some UART signals are available on more than one CAMI pin. Only one pin can be used for each signal.

NOTE: Using the UART-3 port on CAMI precludes the use of the RS-232, IRDA and CIR ports.

Table 19 UART signals

Signal Name	Pin #	Type	Description	Availability
UART-1				
UART1_TX	P1-24*	O	UART1 serial data out	Always available
	P2-104*			Always available
UART1_RX	P1-22*	I	UART1 serial data in	Always available
	P2-106*			Always available
UART1_CTS	P1-27*	I	UART1 clear to send	Always available
	P2-95*			Always available
UART1_RTS	P1-29*	O	UART1 request to send	Always available
	P2-97*			Always available
UART-2				
UART2_TX	P1-32*	O	UART2 serial data out	Only available **without** 'W' option.
UART2_RX	P1-34*	I	UART2 serial data in	Only available **without** 'W' option.
UART2_CTS	P1-33*	I	UART2 clear to send	Only available **without** 'W' option.
	P1-25*			Only available **without** 'W' option.
UART2_RTS	P1-35*	O	UART2 request to send	Only available **without** 'W' option.
UART-3**				
UART3_TX	P2-101*	O	UART3 serial data out	Always available
	P1-138*			Always available
UART3_RX	P2-102*	I	UART3 serial data in	Always available
	P2-44*			Always available
	P1-136*			Always available
UART3_CTS	P1-83*	I	UART3 clear to send	Always available
UART3_RTS	P2-46*	O	UART3 request to send	Always available
	P1-42*			Always available
UART-4				
UART4_TX	P1-46*	O	UART4 serial data out	Only available **without** 'W' option.
	P2-76*			Always available
	P2-78*			Always available
UART4_RX	P1-47*	I	UART4 serial data in	Only available **without** 'W' option.

Signal Name	Pin #	Type	Description	Availability
	P2-70*			Always available
UART4_CTS	P1-48*	I	UART4 clear to send	Only available **without** 'W' option.
	P2-68*			Always available
UART4_RTS	P1-41*	O	UART4 request to send	Only available **without** 'W' option.
	P2-80*			Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.8 IRDA interface

The CM-T3517 integrated IRDA port is based on the Sitara AM3517/05 UART-3 port IRDA communication support. The CM-T3517 includes the following key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications
- Uplink/downlink cyclic redundancy check (CRC) generation/detection
- Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

For additional details on IRDA interface of the Sitara AM3517/05, please refer to section 14 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Using the IRDA port on CAMI precludes the use of RS-232, CIR and UART-3 ports.

Table 20 IRDA signals

Signal Name	Pin #	Type	Description	Availability
UART3_IRRX	P2-102*	I	Serial data input	Always available
	P2-44*			Always available
	P1-136*			Always available
UART3_IRTX	P2-101*	O	Serial data output in SIR, MIR, and FIR modes	Always available
	P1-138*			Always available
UART3_RTS_SD	P2-46*	O	SD mode is used to configure the transceivers.	Always available
	P1-42*			Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.9 CIR interface

The CM-T3517 integrated CIR support is based on the Sitara AM3517/05 UART-3 port. It uses a variable pulse-width modulation (PWM) technique to encompass the various formats of infrared encoding for remote-control applications. CIR logic transmits data packets based on a user-definable frame structure and packet content.

CIR logic supports the following features:

- Transmit mode only (receive mode is not supported)
- Free data format (supports any remote-control private standards)
- Configurable carrier frequency
- Selectable bit rate
- 1/2, 5/12, 1/3 or 1/4 carrier duty cycle

For additional details on the CIR interface of the Sitara AM3517/05, please refer to section 14 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Using the CIR port on CAMI precludes the use of RS-232, IRDA and UART-3 ports.

Table 21 CIR signals

Signal Name	Pin #	Type	Description	Availability
UART3_IRRX	P2-102*	I	Serial data input	Always available
	P2-44*			Always available
	P1-136*			Always available
UART3_RCTX	P1-83*	O	Serial data output in CIR mode	Always available
UART3_RTS_SD	P2-46*	O	SD mode is used to configure the transceivers	Always available
	P1-42*			Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.10 RS232

The CM-T3517 incorporates a single RS232 port. The following features are supported:

- 16C750 compatibility
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter
- Programmable baud rate of up to 250 kbit/s
- Configurable data format
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART-3 port of the Sitara AM3517/05 SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

NOTE: Using the RS-232 port precludes the use of UART-3, IRDA and CIR ports.

Table 22 RS232 signals

Signal Name	Pin #	Type	Description	Availability
RS232_TXD	P1-30	O	RS232 serial data out	Always available
RS232_RXD	P1-28	I	RS232 serial data in	Always available

4.11 MMC / SD / SDIO

The CM-T3517 features three multimedia card high-speed/secure data/secure digital I/O (MMC / SD / SDIO) host interfaces. The following main features are supported:

- Full compliance with MMC command/response sets as defined in the Multimedia Card System Specification v4.2, including high-capacity (size >2GB) cards HC MMC
- Full compliance with SD command/response sets as defined in the SD Memory Card Specifications v2.0, including high-capacity cards SDHC up to 32 GB
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10
- Compliance with sets as defined in the SD Card Specification, Part A2, SD Host Controller Standard Specification, v1.00
- Full compliance with MMC bus testing procedure as defined in the Multimedia Card System Specification, v4.2
- Full compliance with CE-ATA command/response sets as defined in the CE-ATA Standard Specification

Each MMC/SD/SDIO host controller can support one client (MMC card, SD card or SDIO device) only.

The first controller (MMC-1) integrates an internal transceiver that allows a direct connection to the MMC/SD/SDIO card without an external transceiver. It also allows using 1, 4 or 8 bit transfer modes for MMC/SD/SDIO cards.

The second controller (MMC-2) allows connecting MMC/SD/SDIO cards or an external device that uses the MMC/SD/SDIO interface (a WLAN device for example). It also allows using 1, 4 or 8 bit transfer modes for MMC/SD/SDIO cards.

The third controller (MMC-3) allows connecting MMC/SD/SDIO cards or an external device that uses the MMC/SD/SDIO interface (a Wireless USB card for example). It also allows using 1 or 4 bit transfer modes for MMC/SD/SDIO cards.

For additional details on the MMC/SD/SDIO host controller, please refer to section 19 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Some MMC/SD/SDIO signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 23 MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description	Availability
MMC-1				
MMC1_CLK	P1-12*	O	Output clock	Only available **without** 'NS8' & 'NS0' options
MMC1_CMD	P1-13*	IO	Command signal	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT0	P1-15*	IO	Card data bit 0	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT1	P1-16*	IO	Card data bit 1	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT2	P2-4*	IO	Card data bit 2	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT3	P1-18*	IO	Card data bit 3	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT4	P1-9*	IO	Card data bit 4	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT5	P1-17*	IO	Card data bit 5	Only available **without** 'NS8' &

Signal Name	Pin #	Type	Description	Availability
				'NS0' options
MMC1_DAT6	P1-21*	IO	Card data bit 6	Only available **without** 'NS8' & 'NS0' options
MMC1_DAT7	P1-23*	IO	Card data bit 7	Only available **without** 'NS8' & 'NS0' options
VCC_MMC	P1-10	P	MMC1 dedicated output voltage (3.3V) enabled/disabled by software	Only available **without** 'NS8' & 'NS0' options
MMC-2				
MMC2_CLK	P1-48*	O	Output clock	Only available **without** 'W' option.
MMC2_CMD	P1-41*	IO	Command signal	Only available **without** 'W' option.
MMC2_DAT0	P1-46*	IO	Card data bit 0	Only available **without** 'W' option.
MMC2_DAT1	P1-47*	IO	Card data bit 1	Only available **without** 'W' option.
MMC2_DAT2	P1-52*	IO	Card data bit 2	Only available **without** 'W' option.
MMC2_DAT3	P1-49*	IO	Card data bit 3	Only available **without** 'W' option.
MMC2_DAT4	P1-54*	IO	Card data bit 4	Always available
	P2-64*			Only available **without** 'I' option.
MMC2_DAT5	P1-39*	IO	Card data bit 5	Always available
	P1-113*			Only available **without** 'I' option.
MMC2_DAT6	P1-56*	IO	Card data bit 6	Always available
	P1-129*			Only available **without** 'I' option.
MMC2_DAT7	P1-45*	IO	Card data bit 7	Always available
MMC-3				
MMC3_CLK	P1-123*	O	Output clock	Only available **without** 'U3' & 'U5' options.
	P2-5*			Always available
MMC3_CMD	P1-125*	IO	Command signal	Only available **without** 'U3' & 'U5' options.
	P2-51*			Always available
MMC3_DAT0	P1-120*	IO	Card data bit 0	Only available **without** 'U3' & 'U5' options.
	P1-54*			Always available
MMC3_DAT1	P1-124*	IO	Card data bit 1	Only available **without** 'U3' & 'U5' options.
	P1-39*			Always available
MMC3_DAT2	P1-126*	IO	Card data bit 2	Only available **without** 'U3' & 'U5' options.
	P1-56*			Always available
MMC3_DAT3	P1-45*	IO	Card data bit 3	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

NOTE: MMC-1 signals are pulled-up to 3.3V onboard CM-T3517. If other MMC interfaces are utilized, relevant signals should be pulled up on the base board.

4.12 Touch-Screen

The CM-T3517 features a resistive touch-screen interface. The interface supports 4-wire touch panels.

Table 24 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_X+	P1-53	AI	Touch screen X+ (right)	Only available **with** 'I' option.
TS_X-	P1-57	AI	Touch screen X- (left)	Only available **with** 'I' option.
TS_Y+	P2-71	AI	Touch screen Y+ (top)	Only available **with** 'I' option.
TS_Y-	P2-73	AI	Touch screen Y- (bottom)	Only available **with** 'I' option.

4.13 CAN controller

The CM-T3517 features a CAN controller, based on the Sitara AM3517/05 integrated HECC/SCC controller. The CAN controller supports the following main features:

- CAN, version 2.0B compliant
- Common CAN protocol kernel (CPK) to perform protocol tasks
- Standard CAN controller (SCC) for standard CAN applications (16 message-object acceptance-filtering)
- High-end CAN controller (HECC) for complex applications (32 message objects full-mask acceptance-filtering)
- Automatic reply to a remote request
- Automatic retransmission in case of error

For additional details, please refer to section 23 of the "Sitara AM3517/05 Technical Reference Manual".

Table 25 CAN controller signals

Signal Name	Pin #	Type	Description	Availability
CAN_TX_3V3*	P2-44	O	CAN Transmit serial data pin	Always available
CAN_RX_3V3*	P2-46	I	CAN Receive serial data pin	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

NOTE: HECC signals should be connected to both a matching external physical level translator and a galvanic isolator. For a reference design, please refer to the latest SB-T35 schematics.

4.14 GPIO

The CM-T3517 provides up to 133 GPIO signals. These signals can be configured for the following applications:

- Data input / output
- Keyboard interface with a debounce cell
- Interrupt generation
- Wake-up request

For additional details, please refer to section 21 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Some GPIO signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 26 GPIO signal availability

CM-T3517 signal	Sitara AM3517/05 signal	Availability
P1-133*	GPIO_10	Available with all configurations.
P2-18*	GPIO_11	Only available **without** 'W' option
P1-123*	GPIO_12	Only available **without** 'U3' & 'U5' options
P1-125*	GPIO_13	Only available **without** 'U3' & 'U5' options
P1-128*	GPIO_14	Only available **without** 'U3' & 'U5' options
P1-119*	GPIO_15	Only available **without** 'U3' & 'U5' options
P1-130*	GPIO_16	Only available **without** 'U3' & 'U5' options
P1-120*	GPIO_18	Only available **without** 'U3' & 'U5' options
P1-124*	GPIO_19	Only available **without** 'U3' & 'U5' options
P1-126*	GPIO_20	Only available **without** 'U3' & 'U5' options
P1-121*	GPIO_21	Only available **without** 'U3' & 'U5' options
P1-117*	GPIO_23	Only available **without** 'U3' & 'U5' options
P1-116*	GPIO_30	Available with all configurations
P2-20*	GPIO_31	Only available **without** 'W' option
P1-71*	GPIO_34	Available with all configurations
P1-70*	GPIO_35	Available with all configurations
P1-73*	GPIO_36	Available with all configurations
P1-72*	GPIO_37	Available with all configurations
P1-75*	GPIO_38	Available with all configurations
P1-76*	GPIO_39	Available with all configurations
P1-77*	GPIO_40	Available with all configurations
P1-78*	GPIO_41	Available with all configurations
P1-81*	GPIO_42	Available with all configurations
P1-80*	GPIO_43	Available with all configurations
P1-104*	GPIO_44	Available with all configurations
P1-105*	GPIO_45	Available with all configurations
P1-106*	GPIO_46	Available with all configurations
P1-107*	GPIO_47	Available with all configurations
P1-108*	GPIO_48	Available with all configurations
P1-109*	GPIO_49	Available with all configurations
P1-112*	GPIO_50	Available with all configurations
P1-111*	GPIO_51	Available with all configurations
P1-118*	GPIO_52	Only available **without** 'E' option
P1-92*	GPIO_54	Available with all configurations
P1-93*	GPIO_55	Available with all configurations
P1-58*	GPIO_56	Only available **without** 'W' option
P1-85*	GPIO_58	Available with all configurations
P1-88*	GPIO_59	Available with all configurations
P1-87*	GPIO_61	Available with all configurations
P2-76*	GPIO_63	Available with all configurations
P1-83*	GPIO_65	Available with all configurations

CM-T3517 signal	Sitara AM3517/05 signal	Availability
P2-112*	GPIO_66	Available with all configurations
P2-96*	GPIO_67	Available with all configurations
P2-111*	GPIO_68	Available with all configurations
P2-114*	GPIO_69	Available with all configurations
P2-95*	GPIO_70	Available with all configurations
P2-97*	GPIO_71	Available with all configurations
P2-100*	GPIO_72	Available with all configurations
P2-99*	GPIO_73	Available with all configurations
P2-102*	GPIO_74	Available with all configurations
P2-101*	GPIO_75	Available with all configurations
P2-104*	GPIO_76	Available with all configurations
P2-106*	GPIO_77	Available with all configurations
P2-105*	GPIO_78	Available with all configurations
P2-108*	GPIO_79	Available with all configurations
P2-107*	GPIO_80	Available with all configurations
P2-109*	GPIO_81	Available with all configurations
P2-113*	GPIO_82	Available with all configurations
P2-116*	GPIO_83	Available with all configurations
P2-118*	GPIO_84	Available with all configurations
P2-117*	GPIO_85	Available with all configurations
P2-120*	GPIO_86	Available with all configurations
P2-119*	GPIO_87	Available with all configurations
P2-124*	GPIO_88	Available with all configurations
P2-121*	GPIO_89	Available with all configurations
P2-126*	GPIO_90	Available with all configurations
P2-123*	GPIO_91	Available with all configurations
P2-94*	GPIO_92	Available with all configurations
P2-93*	GPIO_93	Available with all configurations
P2-77*	GPIO_94	Available with all configurations
P2-78*	GPIO_95	Available with all configurations
P2-80*	GPIO_96	Available with all configurations
P2-68*	GPIO_97	Available with all configurations
P2-70*	GPIO_98	Available with all configurations
P2-81*	GPIO_99	Available with all configurations, **Can only be used as INPUT**
P2-82*	GPIO_100	Available with all configurations, **Can only be used as INPUT**
P2-83*	GPIO_101	Available with all configurations
P2-84*	GPIO_102	Available with all configurations
P2-85*	GPIO_103	Available with all configurations
P2-88*	GPIO_104	Available with all configurations
P2-87*	GPIO_105	Available with all configurations
P2-90*	GPIO_106	Available with all configurations
P1-12*	GPIO_120	Only available **without** 'NS8' & 'NS0' options
P1-13*	GPIO_121	Only available **without** 'NS8' & 'NS0' options
P1-15*	GPIO_122	Only available **without** 'NS8' & 'NS0' options
P1-16*	GPIO_123	Only available **without** 'NS8' & 'NS0' options
P2-4*	GPIO_124	Only available **without** 'NS8' & 'NS0' options
P1-18*	GPIO_125	Only available **without** 'NS8' & 'NS0' options
P1-9*	GPIO_126	Available with all configurations
P1-17*	GPIO_127	Available with all configurations
P1-21*	GPIO_128	Available with all configurations
P1-23*	GPIO_129	Available with all configurations
P1-48*	GPIO_130	Only available **without** 'W' option
P2-44*	GPIO_130	Available with all configurations
P1-41*	GPIO_131	Only available **without** 'W' option
P2-46*	GPIO_131	Available with all configurations
P1-46*	GPIO_132	Only available **without** 'W' option
P1-47*	GPIO_133	Only available **without** 'W' option
P1-52*	GPIO_134	Only available **without** 'W' option
P1-49*	GPIO_135	Only available **without** 'W' option
P1-54*	GPIO_136	Available with all configurations
P1-39*	GPIO_137	Available with all configurations
P1-56*	GPIO_138	Available with all configurations
P1-45*	GPIO_139	Available with all configurations
P1-33*	GPIO_140	Only available **without** 'W' option
P1-35*	GPIO_141	Only available **without** 'W' option

CM-T3517 signal	Sitara AM3517/05 signal	Availability
P1-32*	GPIO_142	Only available **without** 'W' option
P1-34*	GPIO_143	Only available **without** 'W' option
P1-25*	GPIO_144	Available with all configurations
P1-24*	GPIO_148	Available with all configurations
P1-29*	GPIO_149	Available with all configurations
P1-27*	GPIO_150	Available with all configurations
P1-22*	GPIO_151	Available with all configurations
P2-28*	GPIO_156	Available with all configurations
P2-30*	GPIO_157	Available with all configurations
P2-32*	GPIO_158	Available with all configurations
P2-34*	GPIO_159	Available with all configurations
P2-27*	GPIO_161	Available with all configurations
P2-29*	GPIO_162	Available with all configurations
P2-42*	GPIO_164	Available with all configurations
P1-61*	GPIO_168	Available with all configurations
P1-36*	GPIO_170	Available with all configurations
P2-64*	GPIO_171	Only available **without** 'I' option
P1-113*	GPIO_172	Only available **without** 'I' option
P1-129*	GPIO_173	Only available **without** 'I' option
P2-51*	GPIO_175	Available with all configurations
P2-5*	GPIO_176	Available with all configurations
P2-45*	GPIO_178	Only available **without** 'U2', 'U3' & 'U5' options.
P2-39*	GPIO_179	Only available **without** 'U2', 'U3' & 'U5' options.
P2-49*	GPIO_180	Only available **without** 'U2', 'U3' & 'U5' options.
P2-47*	GPIO_181	Only available **without** 'U2', 'U3' & 'U5' options.
P2-37*	GPIO_182	Only available **without** 'U2', 'U3' & 'U5' options.
P1-60*	GPIO_183	Available with all configurations
P1-63*	GPIO_184	Available with all configurations
P1-64*	GPIO_185	Available with all configurations

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.15 Video input Interface

The video processing subsystem of the CM-T3517 is based on the video processing front-end (VPFE) of the Sitara AM3517/05 SoC. The VPFE controller receives input video/image data from external capture devices and stores it in the CM-T3517 memory. The CPU will process the image data based on application requirements.

The VPFE controller supports the following features:

- Bayer pattern and Foveon sensor formats support
- Progressive and interlaced sensors support
- REC656/CCIR-656 standard support
- YcbCr 422 format support
- Supports up to 16K pixels (image size) in both the horizontal and vertical directions

For additional details, please refer to section 10 of the "Sitara AM3517/05 Technical Reference Manual".

Table 27 Camera interface signals

Signal Name	Pin #	Type	Description	Availability
CAM_PCLK	P2-77*	I	Parallel interface pixel clock	Always available
CAM_HS	P2-80*	I	Line trigger input/output signal	Always available
CAM_VS	P2-68*	I	Frame trigger input/output signal	Always available
CAM_FLD	P2-78*	I	Field identification input/output signal	Always available
CAM_D8			Parallel input data line 8	
CAM_WEN	P2-70*	I	External write-enable signal	Always available
CAM_D9			Parallel input data line 9	
CAM_D0	P2-81*	I	Parallel input data line 0	Always available
CAM_D1	P2-82*	I	Parallel input data line 1	Always available
CAM_D2	P2-83*	I	Parallel input data line 2	Always available
CAM_D3	P2-84*	I	Parallel input data line 3	Always available
CAM_D4	P2-85*	I	Parallel input data line 4	Always available
CAM_D5	P2-88*	I	Parallel input data line 5	Always available
CAM_D6	P2-87*	I	Parallel input data line 6	Always available
CAM_D7	P2-90*	I	Parallel input data line 7	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.16 I²C

The CM-T3517 features two general-purpose high-speed I²C interfaces. The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Support for HS mode for transfer up to 3.4M bits/s

The I²C interfaces are implemented with the I²C-2 and I²C-3 controller modules of the Sitara AM3517/05 SoC.

NOTE: Some I2C signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 28 I²C signals

Signal Name	Pin #	Type	Description	Availability
I2C-2				
I2C2_SDA	P1-60*	IPU	I2C serial data line. Open drain buffer. Pulled up to 3.3V	Always available
I2C2_SCL	P1-61*	IPU	I2C serial clock line. Open drain buffer. Pulled up to 3.3V	Always available
I2C-3				
I2C3_SDA	P1-64*	OD	I2C serial data line. Open drain buffer. Pulled up to 3.3V	Always available
	P1-81*		I2C serial data line. Open drain buffer.	Always available
I2C3_SCL	P1-63*	OD	I2C serial clock line. Open drain buffer. Pulled up to 3.3V	Always available
	P2-78*		I2C serial clock line. Open drain buffer.	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.17 SPI

CM-T3517 features four multi-channel serial port interfaces (SPI). The following main features are supported:

- Serial clock with programmable frequency, polarity and phase for each channel
- A wide selection of SPI word lengths ranging from 4 bits to 32 bits

NOTE: Some SPI signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 29 SPI signals

Signal Name	Pin #	Type	Description	Availability
SPI-1				
SPI1_CLK	P2-64*	IO	Serial clock	Only available **without** 'I' option.
SPI1_CS1	P2-51*	IO	Chip select 0	Always available
SPI1_CS2	P2-5*	IO	Chip select 1	Always available
SPI1_SIMO	P1-113*	O	Serial data master out	Only available **without** 'I' option.
SPI1_SOMI	P1-129*	I	Serial data master input	Only available **without** 'I' option.
SPI-2				
SPI2_CLK	P2-45*	IO	Serial clock	Only available **without** 'U2', 'U3' & 'U5' options
	P1-15*			Only available **without** 'NS8' & 'NS0' options
SPI2_CS0	P2-47*	IO	Chip select 0	Only available **without** 'U2', 'U3' & 'U5' options
	P1-18*			Only available **without** 'NS8' & 'NS0' options
SPI2_CS1	P2-37*	IO	Chip select 1	Only available **without** 'U2', 'U3' & 'U5' options
SPI2_SIMO	P2-39*	O	Serial data master out	Only available **without** 'U2', 'U3' & 'U5' options
	P1-16*			Only available **without** 'NS8' & 'NS0' options
SPI2_SOMI	P2-49*	I	Serial data master input	Only available **without** 'U2', 'U3' & 'U5' options
	P2-4*			Only available **without** 'NS8' & 'NS0' options
SPI-3				
SPI3_CLK	P2-124*	IO	Serial clock	Always available
	P1-48*			Only available **without** W' option.
SPI3_CS0	P2-123*	IO	Chip select 0	Always available
	P1-49*			Only available **without** W' option.
	P1-130*			Only available **without** 'U3' & 'U5' options.
SPI3_CS1	P2-94*	IO	Chip select 1	Always available
	P1-52*			Only available **without** W' option.
	P1-121*			Only available **without** 'U3' & 'U5' options.
SPI3_SIMO	P2-121*	O	Serial data master out	Always available
	P1-41*			Only available **without** W' option.
	P1-128*			Only available **without** 'U3' & 'U5' options.
SPI3_SOMI	P2-126*	I	Serial data master input	Always available
	P1-46*			Only available **without** W' option.
	P1-119*			Only available **without** 'U3' & 'U5' options.
SPI-4				
SPI4_CLK	P2-28*	IO	Serial clock	Always available

Signal Name	Pin #	Type	Description	Availability
	P1-22*			Always available
SPI4_CS0	P2-27*	IO	Chip select 0	Always available
SPI4_SIMO	P2-32*	O	Serial data master out	Always available
SPI4_SOMI	P2-34*	I	Serial data master input	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.18 McBSP

The CM-T3517 features three multi-channel buffered serial port (McBSP) interfaces. The following main features are supported:

- L4 interconnect slave interface supporting:
  - 32-bit data bus width
  - 32-bit access supported
  - 16- /8-bit access not supported
  - 10-bit address bus width
  - Write non-posted transaction mode supported
- 128 x 32-bit words (512 bytes) for each buffer for transmit/receive operations
- Interrupts configurable in legacy mode (2 requests) or PRCM compliant (1 request)
- Transmit and receive DMA requests triggered with programmable FIFO thresholds

For additional details, please refer to section 18 of the "Sitara AM3517/05 Technical Reference Manual".

NOTE: Some McBSP signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 30 McBSP signals

Signal Name	Pin #	Type	Description	Availability
McBSP-1				
McBSP1_DR	P2-34*	I	Received serial data	Always available
McBSP1_CLKR	P2-28*	IO	Receive Clock	Always available
	P1-22*			Always available
McBSP1_FSR	P2-30*	IO	Receive frame synchronization	Always available
McBSP1_DX	P2-32*	IO	Transmitted serial data	Always available
McBSP1_CLKX	P2-29*	IO	Transmit clock	Always available
McBSP1_FSX	P2-27*	IO	Transmit frame synchronization	Always available
McBSP-3				
McBSP3_DR	P1-35*	I	Received serial data	Only available **without** 'W' option
	P2-34*			Always available
McBSP3_DX	P1-33*	IO	Transmitted serial data	Only available **without** 'W' option
	P1-25*			Always available
	P2-32*			Always available
McBSP3_CLKX	P1-32*	IO	Transmit clock	Only available **without** 'W' option
	P2-29*			Always available
McBSP3_FSX	P1-34*	IO	Transmit frame synchronization	Only available **without** 'W' option
	P2-27*			Always available
McBSP-5				
McBSP5_DR	P1-120*	I	Received serial data	Only available **without** 'U3' & 'U5' options
McBSP5_DX	P1-126*	IO	Transmitted serial data	Only available **without** 'U3' & 'U5' options
McBSP5_CLKX	P1-123*	IO	Transmit clock	Only available **without** 'U3' & 'U5' options
McBSP5_FSX	P1-124*	IO	Transmit frame synchronization	Only available **without** 'U3' & 'U5' options

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.19 HDQ / 1-Wire

The HDQ/1-Wire interface implements the hardware protocol of the master functions of the Benchmark HDQ and the Dallas Semiconductor 1-Wire® protocols.

The following main features are supported:

- Benchmark HDQ protocol
- Dallas Semiconductor 1-Wire® protocol
- Power-down mode

For additional details, please refer to section 17 of the "Sitara AM3517/05 Technical Reference Manual".

Table 31 HDQ / 1-Wire signals

Signal Name	Pin #	Type	Description	Availability
HDQ_SIO	P1-36*	IO	Serial data input/output	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

4.20 JTAG

The CM-T3517 JTAG interface is derived from the Sitara AM3517/05 SoC JTAG port.

The Sitara AM3517/05 target debug interface uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI and TDO) and a return clock (RTCK) to meet the clocking requirements of the ARM968 processor and the two instrumentations pins (EMU0 and EMU1).

For additional details, please refer to section 24.5 of the "Sitara AM3517/05 Technical Reference Manual".

Table 32 JTAG signals

Signal Name	Pin #	Type	Description	Availability
JTAG_TCK	P2-24	I	Test clock	Always available
JTAG_TDO	P2-17	O	Test data output	Always available
JTAG_TDI	P2-21	I	Test data input	Always available
JTAG_TMS	P2-23	IO	Test mode select	Always available
JTAG_nTRST	P2-25	I	Test logic reset	Always available
JTAG_RTCK	P2-22	O	Returned test clock	Always available
JTAG_EMU0	P2-18*	IO	Channel 0 trigger	Always available
JTAG_EMU1	P2-20*	IO	Channel 1 trigger	Always available

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

NOTE: WiFi and Bluetooth functions are not available while the system is in JTAG operation modes

5 SYSTEM LOGIC

The following notes apply to system signals:

- Most CAMI pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to chapter 5.5.
- Certain signals are available on more than one CAMI pin. Only one CAMI pin can be connected to each signal.
- All of the CM-T3517 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each Interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal
- **"Pin#" –** The pin number on the CAMI connector
- **"Type" –** Signal type
- **"Description" –** Signal description

Each CAMI signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal.

- **"I"** – Digital input
- **"IO"** – Digital input/output
- **"P"** – Power input/output

5.1 Power Management

5.1.1 Power Rails

The CM-T3517 supports two power supply options:

- Regulated DC 3.6V
- Lithium-ion polymer battery

The CM-T3517 does not feature an onboard Lithium-ion polymer battery charger. If required, such a charger must be implemented on the baseboard. Please refer to the SB-T35 schematics for a reference design.

Table 33 Power signals

Signal Name	Type	Description
VCC_CM	P	Main power supply. Typical voltage – 3.6V
BKBAT	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave unconnected if RTC back-up is not required.
GND	P	Common ground.

5.2 Reset

CM-T3517 supports two reset signals: cold reset input (nRST_IN) and warm reset input/output (SYS_nRESWARM).

Cold reset is generated at power up by the TPS65023 PMIC to reset the full logic of the CM-T3517. It may also be asserted by the nRST_IN input signal. Cold reset is a global reset that affects every module on the device. The cold reset assertion also causes SYS_nRESWARM assertion.

Warm reset is also a global reset, but it does not affect all the modules on the device. Usually, the device does not require a complete reboot on a warm reset.

The nRST_IN signal should be used as the main system reset.

For additional details, please refer to section 4 of the "Sitara AM3517/05 Technical Reference Manual".

Table 34 Reset signals

Signal Name	Pin #	Type	Description
nRST_IN	P1-11	I	Cold reset. Active low. Pulled up to 3.3V. Input only.
SYS_nRESWARM	P1-116*	IO	Warm reset. Active low. Pulled up to 3.3V.

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

5.3 Boot Options

The CM-T3517 supports two boot sequences providing the following boot options:

- Boot from onboard NAND flash
- Boot from external SD card connected to MMC-1 interface
- Boot from external PC host via USB OTG port
- Boot from external PC host via RS232 port

The boot sequence is selected with the BOOT_SOURCE signal. The standard boot sequence is designed for normal system operation with the onboard NAND flash acting as the boot media. The alternate boot sequences are mainly intended for system debug and production, but can also be used for normal operation with an SD memory device (connected to the MMC-1 interface) acting as the boot media.

For additional details, please refer to section 24 of the "Sitara AM3517/05 Technical Reference Manual".

Table 35 Boot sequences

Boot sequence	BOOT_SOURCE(0) signal input	First device	Second device	Third device	Forth device
Default	Unconnected.	NAND	USB	RS232	MMC-1
Alternate	Pulled to 3.3V with 1k resistance.	USB	RS232	MMC-1	NAND

Table 36 Boot selection signals

Signal Name	Pin #	Type	Description
BOOT_SOURCE0	P1-65	I	Boot selection 0. Pulled down with 10.5k. Leave disconnected for default boot sequence.
BOOT_SOURCE1	P1-37	I	Boot selection 1. Reserved for production. Leave disconnected.

5.4 System and Miscellaneous Signals

5.4.1 External DMA Requests

The CM-T3517 provides four optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the Sitara AM3517/05 SDMA controller. A logical channel can be configured to respond to an external synchronization request.

For additional details, please refer to section 7 of the "Sitara AM3517/05 Technical Reference Manual".

Table 37 System signals

Signal Name	Pin #	Type	Description
nDMAREQ0	P1-92*	I	External AM35x DMA request 0.
nDMAREQ1	P1-93*	I	External AM35x DMA request 1.
	P1-83*		
nDMAREQ2	P1-81*	I	External AM35x DMA request 2.
	P1-58*^		
nDMAREQ3	P1-80*	I	External AM35x DMA request 3.

NOTE: Pins denoted by "*" may be used for other interfaces. For details, please refer to section *5.5* of this document.

NOTE: Pins denoted by "^" are only available without "W" option.

5.4.2 Miscellaneous

Table 38 Miscellaneous

Signal Name	Pin #	Type	Description
SYS_CLKOUT1	P1-133*	O	Configurable output clock1. Can output main oscillator clock (26MHz).
RESERVED	P2-12	-	Reserved for debug and production. Leave unconnected. Pulled-up to 3.3V.
RESERVED	P1-66	-	Reserved for debug and production. Leave unconnected.
RESERVED	P1-40	-	Reserved for debug and production. Leave unconnected.
RESERVED	P1-44	-	Reserved for debug and production. Leave unconnected.
RESERVED	P1-114	-	Reserved for debug and production. Leave unconnected.

5.5 Signal Multiplexing Characteristics

Sitara AM3517/05 pins can have up to eight alternate function modes. The table below provides a description of signal multiplexing. Function names marked with gray shading denote the default function intended in the CM-T3517 design.

NOTE: Some signals are available on more than one CAMI pin. Only one pin can be used for each signal.

Table 39 Signal multiplexing

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-22	uart1_rx		mcbsp1_clkr	mcspi4_clk	gpio151			safe_mode
P1-24	uart1_tx				gpio148			safe_mode
P1-27	uart1_cts				gpio150			safe_mode
P1-29	uart1_rts				gpio149			safe_mode
P1-32	mcbsp3_clkx	uart2_tx			gpio142			safe_mode
P1-33	mcbsp3_dx	uart2_cts			gpio140			safe_mode
P1-34	mcbsp3_fsx	uart2_rx			gpio143			safe_mode
P1-35	mcbsp3_dr	uart2_rts			gpio141			safe_mode
P1-36	hdq_sio	sys_altclk	i2c2_sccbe	i2c3_sccbe	gpio170			safe_mode
P1-39	mmc2_dat5	mmc2_dir_dat1		mmc3_dat1	gpio137		mm_fsusb3_rxdp	safe_mode
P1-41	mmc2_cmd	mcspi3_simo	uart4_rts		gpio131			safe_mode
P1-42	uart3_rts_sd				gpio164			safe_mode
P1-45	mmc2_dat7	mmc2_clkin		mmc3_dat3	gpio139		mm_fsusb3_rxdm	safe_mode
P1-46	mmc2_dat0	mcspi3_somi	uart4_tx		gpio132			safe_mode
P1-47	mmc2_dat1		uart4_rx		gpio133			safe_mode
P1-48	mmc2_clk	mcspi3_clk	uart4_cts		gpio130			safe_mode
P1-49	mmc2_dat3	mcspi3_cs0			gpio135			safe_mode
P1-52	mmc2_dat2	mcspi3_cs1			gpio134			safe_mode
P1-54	mmc2_dat4	mmc2_dir_dat0		mmc3_dat0	gpio136			safe_mode
P1-56	mmc2_dat6	mmc2_dir_cmd		mmc3_dat2	gpio138			safe_mode
P1-58	gpmc_ncs5	sys_ndmareq2		gpt10_pwm_evt	gpio56			safe_mode
P1-60	i2c2_sda				gpio183			safe_mode
P1-61	i2c2_scl				gpio168			safe_mode
P1-63	i2c3_scl				gpio184			safe_mode
P1-64	i2c3_sda				gpio185			safe_mode
P1-68	gpmc_wait1	uart4_tx			gpio63			safe_mode
P1-70	gpmc_a2				gpio35			safe_mode
P1-71	gpmc_a1				gpio34			safe_mode
P1-72	gpmc_a4				gpio37			safe_mode
P1-73	gpmc_a3				gpio36			safe_mode
P1-75	gpmc_a5				gpio38			safe_mode
P1-76	gpmc_a6				gpio39			safe_mode
P1-77	gpmc_a7				gpio40			safe_mode
P1-78	gpmc_a8				gpio41			safe_mode
P1-80	gpmc_a10	sys_ndmareq3			gpio43			safe_mode
P1-81	gpmc_a9	sys_ndmareq2			gpio42			safe_mode
P1-82	gpmc_nbe0_cle				gpio60			
P1-83	gpmc_wait3	sys_ndmareq1	uart3_cts_rctx		gpio65			safe_mode
P1-85	gpmc_ncs7	gpmc_io_dir		gpt8_pwm_evt	gpio58			safe_mode
P1-87	gpmc_nbe1				gpio61			safe_mode
P1-88	gpmc_clk				gpio59			
P1-90	gpmc_nadv_ale							
P1-92	gpmc_ncs3	sys_ndmareq0	gpt10_pwm_evt		gpio54			safe_mode
P1-93	gpmc_ncs4	sys_ndmareq1		gpt9_pwm_evt	gpio55			safe_mode
P1-104	gpmc_d8				gpio44			
P1-105	gpmc_d9				gpio45			
P1-106	gpmc_d10				gpio46			
P1-107	gpmc_d11				gpio47			
P1-108	gpmc_d12				gpio48			
P1-109	gpmc_d13				gpio49			
P1-111	gpmc_d15				gpio51			
P1-112	gpmc_d14				gpio50			
P1-113	mcspi1_simo	mmc2_dat5			gpio172			safe_mode
P1-114	gpmc_ncs2		gpt9_pwm_evt		gpio53			safe_mode

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1-117	etk_d9	sys_secure_ indicator	mmc3_dat5	hsusb1_nxt	gpio23	mm_fsusb1_ rxdm	hsusb1_tll_ nxt	hw_dbg11
P1-118	gpmc_ncs1				gpio52			
P1-119	etk_d1	mcspi3_somi		hsusb1_ data1	gpio15	mm_fsusb1_ txse0	hsusb1_tll_ data1	hw_dbg3
P1-120	etk_d4	mcbsp5_dr	mmc3_dat0	hsusb1_ data4	gpio18		hsusb1_tll_ data4	hw_dbg6
P1-121	etk_d7	mcspi3_cs1	mmc3_dat7	hsusb1_ data3	gpio21	mm_fsusb1_ txen_n	hsusb1_tll_ data3	hw_dbg9
P1-123	etk_clk	mcbsp5_clkx	mmc3_clk	hsusb1_ stp	gpio12		hsusb1_tll_ stp	hw_dbg0
P1-124	etk_d5	mcbsp5_fsx	mmc3_dat1	hsusb1_ data5	gpio19		hsusb1_tll_ data5	hw_dbg7
P1-125	etk_ctl		mmc3_cmd	hsusb1_ clk	gpio13	mm_fsusb1_ rxdp	hsusb1_tll_ clk	hw_dbg1
P1-126	etk_d6	mcbsp5_dx	mmc3_dat2	hsusb1_ data6	gpio20		hsusb1_tll_ data6	hw_dbg8
P1-128	etk_d0	mcspi3_simo	mmc3_dat4	hsusb1_ data0	gpio14	mm_fsusb1_ rxrcv	hsusb1_tll_ data0	hw_dbg2
P1-129	mcspi1_somi	mmc2_dat6			gpio173			safe_mode
P1-130	etk_d2	mcspi3_cs0		hsusb1_ data2	gpio16	mm_fsusb1_ txdat	hsusb1_tll_ data2	hw_dbg4
P1-133	sys_clkout1				gpio10			safe_mode
P2-27	mcbsp1_fsx	mcspi4_cs0	mcbsp3_fsx		gpio161			safe_mode
P2-28	mcbsp1_clkr	mcspi4_clk			gpio156			safe_mode
P2-29	mcbsp1_clkx		mcbsp3_clkx		gpio162			safe_mode
P2-30	mcbsp1_fsr				gpio157			safe_mode
P2-32	mcbsp1_dx	mcspi4_simo	mcbsp3_dx		gpio158			safe_mode
P2-34	mcbsp1_dr	mcspi4_somi	mcbsp3_dr		gpio159			safe_mode
P2-37	mcspi2_cs1	gpt8_pwm_ evt	hsusb2_tll_ data3	hsusb2_ data3	gpio182	mm_fsusb2_ txen_n		safe_mode
P2-39	mcspi2_simo	gpt9_pwm_ evt	hsusb2_tll_ data4	hsusb2_ data4	gpio179			safe_mode
P2-44	hecc1_txd		uart3_rx_irrx		gpio130			safe_mode
P2-45	mcspi2_clk		hsusb2_tll_ data7	hsusb2_ data7	gpio178			safe_mode
P2-46	hecc1_rxd		uart3_rts_sd		gpio131			safe_mode
P2-47	mcspi2_cs0	gpt11_pwm_ evt	hsusb2_tll_ data6	hsusb2_ data6	gpio181			safe_mode
P2-49	mcspi2_somi	gpt10_pwm_ evt	hsusb2_tll_ data5	hsusb2_ data5	gpio180			safe_mode
P2-5	mcspi1_cs2			mmc3_clk	gpio176			safe_mode
P2-51	mcspi1_cs1			mmc3_cmd	gpio175			safe_mode
P2-64	mcspi1_clk	mmc2_dat4			gpio171			safe_mode
P2-68	ccdc_vd		uart4_cts		gpio97	hw_dbg2		safe_mode
P2-70*	ccdc_wen	ccdc_data9	uart4_rx		gpio98	hw_dbg3		safe_mode
P2-76	gpmc_wait1				gpio63			safe_mode
P2-77	ccdc_pclk				gpio94	hw_dbg0		safe_mode
P2-78*	ccdc_field	ccdc_data8	uart4_tx	i2c3_scl	gpio95	hw_dbg1		safe_mode
P2-80	ccdc_hd		uart4_rts		gpio96			safe_mode
P2-81	ccdc_data0			i2c3_sda	gpio99			safe_mode
P2-82	ccdc_data1				gpio100			safe_mode
P2-83	ccdc_data2				gpio101	hw_dbg4		safe_mode
P2-84	ccdc_data3				gpio102	hw_dbg5		safe_mode
P2-85	ccdc_data4				gpio103	hw_dbg6		safe_mode
P2-87	ccdc_data6				gpio105			safe_mode
P2-88	ccdc_data5				gpio104	hw_dbg7		safe_mode
P2-89*	ccdc_field	ccdc_data8	uart4_tx	i2c3_scl	gpio95	hw_dbg1		safe_mode
P2-90	ccdc_data7				gpio106			safe_mode
P2-92*	ccdc_wen	ccdc_data9	uart4_rx		gpio98	hw_dbg3		safe_mode
P2-93	dss_data23			dss_data5	gpio93			safe_mode
P2-94	dss_data22		mcspi3_cs1	dss_data0	gpio92			safe_mode
P2-95	dss_data0		uart1_cts		gpio70			safe_mode
P2-96	dss_hsync				gpio67	hw_dbg13		safe_mode
P2-97	dss_data1		uart1_rts		gpio71			safe_mode
P2-99	dss_data3				gpio73			safe_mode
P2-100	dss_data2				gpio72			safe_mode
P2-101	dss_data5		uart3_tx_irtx		gpio75			safe_mode

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P2-102	dss_data4		uart3_rx_irrx		gpio74			safe_mode
P2-104	dss_data6		uart1_tx		gpio76	hw_dbg14		safe_mode
P2-105	dss_data8				gpio78	hw_dbg16		safe_mode
P2-106	dss_data7		uart1_rx		gpio77	hw_dbg15		safe_mode
P2-107	dss_data10				gpio80			safe_mode
P2-108	dss_data9				gpio79	hw_dbg17		safe_mode
P2-109	dss_data11				gpio81			safe_mode
P2-111	dss_vsync				gpio68			safe_mode
P2-112	dss_pclk				gpio66	hw_dbg12		safe_mode
P2-113	dss_data12				gpio82			safe_mode
P2-114	dss_acbias				gpio69			safe_mode
P2-116	dss_data13				gpio83			safe_mode
P2-117	dss_data15				gpio85			safe_mode
P2-118	dss_data14				gpio84			safe_mode
P2-119	dss_data17				gpio87			safe_mode
P2-120	dss_data16				gpio86			safe_mode
P2-121	dss_data19		mcspi3_simo	dss_data3	gpio89			safe_mode
P2-123	dss_data21		mcspi3_cs0	dss_data1	gpio91			safe_mode
P2-124	dss_data18		mcspi3_clk	dss_data4	gpio88			safe_mode
P2-126	dss_data20		mcspi3_somi	dss_data2	gpio90			safe_mode

5.6 RTC

The CM-T3517 RTC is implemented with the EM MICROELECTRONIC V3020. The RTC provides time and calendar information. The TI TPS65023 powers the RTC when system power is present.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. The backup battery should be connected to the BKBAT power input.

For additional RTC functional information, please refer to the “EM MICROELECTRONIC V3020 Datasheet”.

5.7 General Purpose LED

The CM-T3517 features a single general purpose green LED controlled by GPIO186 of the Sitara AM3517/05 SoC. The LED is ON when GPIO186 is set high.

6 BASEBOARD INTERFACE

The CM-T3517 connects to the baseboard through P1 and P2 - 0.6 mm pitch 140-pin connectors. The following notes apply to signals available through those connectors.

General notes:

- Some interfaces/signals are available only with/without certain configuration options. Each signal's availability is noted in the "Signal Descriptions" table of each interface.
- Some signals are available on more than one CAMI pin. Only one CAMI pin can be connected to each signal.

6.1 Connector Pinout

Table 40 Connector P1

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P1-01	CM_ETH_TXP	4.3	P1-02	CM_ETH_RXN	4.3
P1-03	CM_ETH_TXN	4.3	P1-04	CM_ETH_RXP	4.3
P1-05	CM_ETH_LED2	4.3	P1-06	CM_ETH_LED1	4.3
P1-07	VCC_CM	5.1	P1-08	GND	5.1
P1-09	MMC1_DAT4 GPIO126	4.11 4.14	P1-10	VCC_MMC	4.11
P1-11	nRST_IN	5.2	P1-12	MMC1_CLK GPIO120	4.11 4.14
P1-13	MMC1_CMD GPIO121	4.11 4.14	P1-14	GND	5.1
P1-15	MMC1_DAT0 SPI2_CLK GPIO122	4.11 4.17 4.14	P1-16	MMC1_DAT1 SPI2_SIMO GPIO123	4.11 4.17 4.14
P1-17	MMC1_DAT5 GPIO127	4.11 4.14	P1-18	MMC1_DAT3 SPI2_CS0 GPIO125	4.11 4.17 4.14
P1-19	VCC_CM	5.1	P1-20	BKBAT	5.1
P1-21	MMC1_DAT6 GPIO128	4.11 4.14	P1-22	McBSP1_CLKR SPI4_CLK UART1_RX GPIO151	4.18 4.17 4.7 4.14
P1-23	MMC1_DAT7 GPIO129	4.11 4.14	P1-24	UART1_TX GPIO148	4.7 4.14
P1-25	McBSP3_DX UART2_CTS GPIO144	4.18 4.7 4.14	P1-26	GND	5.1
P1-27	UART1_CTS GPIO150	4.7 4.14	P1-28	RS232_RXD	4.10
P1-29	UART1_RTS GPIO149	4.7 4.14	P1-30	RS232_TXD	4.10
P1-31	VCC_CM	5.1	P1-32	McBSP3_CLKX UART2_TX GPIO142	4.18 4.7 4.14
P1-33	McBSP3_DX UART2_CTS GPIO140	4.18 4.7 4.14	P1-34	McBSP3_FSX UART2_RX GPIO143	4.18 4.7 4.14
P1-35	McBSP3_DR UART2_RTS GPIO141	4.18 4.7 4.14	P1-36	HDQ_SIO GPIO170	4.19 4.14
P1-37	BOOT_SOURCE (1)	5.3	P1-38	GND	5.1
P1-39	MMC2_DAT5 MMC3_DAT1 GPIO137	4.11 4.11 4.14	P1-40	RESERVED	5.4.2

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P1-41	MMC2_CMD SPI3_SIMO UART4_RTS GPIO131	4.11 4.17 4.7 4.14	P1-42	UART3_RTS UART3_RTS_SD UART3_RTS_SD GPIO164	4.7 4.8 4.9 4.14
P1-43	VCC_CM	5.1	P1-44	RESERVED	5.4.2
P1-45	MMC2_DAT7 MMC3_DAT3 GPIO139	4.11 4.11 4.14	P1-46	MMC2_DAT0 SPI3_SOMI UART4_TX GPIO132	4.11 4.17 4.7 4.14
P1-47	MMC2_DAT1 UART4_RX GPIO133	4.11 4.7 4.14	P1-48	MMC2_CLK SPI3_CLK UART4_CTS GPIO130	4.11 4.17 4.7 4.14
P1-49	MMC2_DAT3 SPI3_CS0 GPIO135	4.11 4.17 4.14	P1-50	GND	5.1
P1-51	HUBP1_nOVC	4.4.2	P1-52	MMC2_DAT2 SPI3_CS1 GPIO134	4.11 4.17 4.14
P1-53	TS_X+	4.12	P1-54	MMC2_DAT4 MMC3_DAT0 GPIO136	4.11 4.11 4.14
P1-55	VCC_CM	5.1	P1-56	MMC2_DAT6 MMC3_DAT2 GPIO138	4.11 4.11 4.14
P1-57	TS_X-	4.12	P1-58	GPMC_nCS5 nDMAREQ2 GPIO56	4.1 5.4.1 4.14
P1-59	HUBP2_nOVC	4.4.2	P1-60	I2C2_SDA GPIO183	4.16 4.14
P1-61	I2C2_SCL GPIO168	4.16 4.14	P1-62	GND	5.1
P1-63	I2C3_SCL GPIO184	4.16 4.14	P1-64	I2C3_SDA GPIO185	4.16 4.14
P1-65	BOOT_SOURCE (0)	5.3	P1-66	RESERVED	5.4.2
P1-67	VCC_CM	5.1	P1-68	N.C.	
P1-69	HUBP3_nOVC	4.4.2	P1-70	GPMC_A2 GPIO35	4.1 4.14
P1-71	GPMC_A1 GPIO34	4.1 4.14	P1-72	GPMC_A4 GPIO37	4.1 4.14
P1-73	GPMC_A3 GPIO36	4.1 4.14	P1-74	GND	5.1
P1-75	GPMC_A5 GPIO38	4.1 4.14	P1-76	GPMC_A6 GPIO39	4.1 4.14
P1-77	GPMC_A7 GPIO40	4.1 4.14	P1-78	GPMC_A8 GPIO41	4.1 4.14
P1-79	VCC_CM	5.1	P1-80	GPMC_A10 nDMAREQ3 GPIO43	4.1 5.4.1 4.14
P1-81	GPMC_A9 nDMAREQ2 GPIO42	4.1 5.4.1 4.14	P1-82	GPMC_nBE0 GPMC_CLE	4.1 4.1
P1-83	GPMC_WAIT3 nDMAREQ1 UART3_RCTX UART3_CTS GPIO65	4.1 5.4.1 4.9 4.7 4.14	P1-84	GPMC_nWE	4.1
P1-85	GPMC_nCS7 GPMC_IODIR GPIO58	4.1 4.1 4.14	P1-86	GND	5.1
P1-87	GPMC_nBE1 GPIO61	4.1 4.14	P1-88	GPMC_CLK GPIO59	4.1 4.14
P1-89	GPMC_nOE	4.1	P1-90	GPMC_nADV GPMC_ALE	4.1 4.1
P1-91	VCC_CM	5.1	P1-92	GPMC_nCS3 nDMAREQ0 GPIO54	4.1 5.4.1 4.14

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P1-93	GPMC_nCS4 nDMAREQ1 GPIO55	4.1 5.4.1 4.14	P1-94	GPMC_D0	4.1
P1-95	GPMC_D1	4.1	P1-96	GPMC_D2	4.1
P1-97	GPMC_D3	4.1	P1-98	GND	5.1
P1-99	GPMC_D5	4.1	P1-100	GPMC_D4	4.1
P1-101	GPMC_D7	4.1	P1-102	GPMC_D6	4.1
P1-103	VCC_CM	5.1	P1-104	GPMC_D8 GPIO44	4.1 4.14
P1-105	GPMC_D9 GPIO45	4.1 4.14	P1-106	GPMC_D10 GPIO46	4.1 4.14
P1-107	GPMC_D11 GPIO47	4.1 4.14	P1-108	GPMC_D12 GPIO48	4.1 4.14
P1-109	GPMC_D13 GPIO49	4.1 4.14	P1-110	GND	5.1
P1-111	GPMC_D15 GPIO51	4.1 4.14	P1-112	GPMC_D14 GPIO50	4.1 4.14
P1-113	MMC2_DAT5 SPI1_SIMO GPIO172	4.11 4.17 4.14	P1-114	RESERVED	5.4.2
P1-115	VCC_CM	5.1	P1-116	SYS_nRESWARM GPIO30	5.2 4.14
P1-117	GPIO23	4.14	P1-118	GPMC_nCS1 GPIO52	4.1 4.14
P1-119	SPI3_SOMI GPIO15	4.17 4.14	P1-120	MMC3_DAT0 McBSP5_DR GPIO18	4.11 4.18 4.14
P1-121	SPI3_CS1 GPIO21	4.17 4.14	P1-122	GND	5.1
P1-123	MMC3_CLK McBSP5_CLKX GPIO12	4.11 4.18 4.14	P1-124	MMC3_DAT1 McBSP5_FSX GPIO19	4.11 4.18 4.14
P1-125	MMC3_CMD GPIO13	4.11 4.14	P1-126	MMC3_DAT2 McBSP5_DX GPIO20	4.11 4.18 4.14
P1-127	VCC_CM	5.1	P1-128	SPI3_SIMO GPIO14	4.17 4.14
P1-129	MMC2_DAT6 SPI1_SOMI GPIO173	4.11 4.17 4.14	P1-130	SPI3_CS0 GPIO16	4.17 4.14
P1-131	N.C.		P1-132	N.C.	
P1-133	SYS_CLKOUT1 GPIO10	5.4.2 4.14	P1-134	GND	5.1
P1-135	N.C		P1-136	USB0_DP UART3_RX UART3_IRRX UART3_IRRX	4.4.1 4.7 4.8 4.9
P1-137	USB0_ID	4.4.1	P1-138	USB0_DN UART3_TX UART3_IRTX	4.4.1 4.7 4.8
P1-139	VCC_CM	5.1	P1-140	USB0_5V_OUT	4.4.1

Table 41 Connector P2

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P2-01	TV_OUT1	4.2	P2-02	GND	5.1
P2-03	TV_OUT2	4.2	P2-04	MMC1_DAT2 SPI2_SOMI GPIO124	4.11 4.17 4.14
P2-05	MMC3_CLK SPI1_CS2 GPIO176	4.11 4.17 4.14	P2-06	USB1_CPEN	4.4.2
P2-07	VCC_CM	5.1	P2-08	USB1_VBUS	4.4.2
P2-09	USB2_CPEN HUBP1_CPEN	4.4.2	P2-10	N.C.	
P2-11	USB2_VBUS	4.4.2	P2-12	RESERVED	5.4.2

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P2-13	N.C.		P2-14	GND	5.1
P2-15	N.C.		P2-16	N.C.	
P2-17	JTAG_TDO	4.20	P2-18	JTAG_EMU0 GPIO11	4.20 4.14
P2-19	VCC_CM	5.1	P2-20	JTAG_EMU1 GPIO31	4.20 4.14
P2-21	JTAG_TDI	4.20	P2-22	JTAG_RTCK	4.20
P2-23	JTAG_TMS	4.20	P2-24	JTAG_TCK	4.20
P2-25	JTAG_nTRST	4.20	P2-26	GND	5.1
P2-27	McBSP1_FSX McBSP3_FSX SPI4_CS0 GPIO161	4.18 4.18 4.17 4.14	P2-28	McBSP1_CLKR SPI4_CLK GPIO156	4.18 4.17 4.14
P2-29	McBSP1_CLKX McBSP3_CLKX GPIO162	4.18 4.18 4.14	P2-30	McBSP1_FSR GPIO157	4.18 4.14
P2-31	VCC_CM	5.1	P2-32	McBSP1_DX McBSP3_DX SPI4_SIMO GPIO158	4.18 4.18 4.17 4.14
P2-33	HUBP3_DP	4.4.2	P2-34	McBSP1_DR McBSP3_DR SPI4_SOMI GPIO159	4.18 4.18 4.17 4.14
P2-35	HUBP3_DN	4.4.2	P2-36	HUBP2_CPEN	4.4.2
P2-37	SPI2_CS1 GPIO182	4.17 4.14	P2-38	GND	5.1
P2-39	SPI2_SIMO GPIO179	4.17 4.14	P2-40	HUBP2_DP	4.4.2
P2-41	HUBP3_CPEN	4.4.2	P2-42	HUBP2_DM	4.4.2
P2-43	VCC_CM	5.1	P2-44	CAN_TX UART3_RX UART3_IRRX UART3_IRRX GPIO130	4.13 4.7 4.8 4.9 4.14
P2-45	SPI2_CLK GPIO178	4.17 4.14	P2-46	CAN_RX UART3_RTS UART3_RTS_SD UART3_RTS_SD GPIO131	4.13 4.7 4.8 4.9 4.14
P2-47	SPI2_CS0 GPIO181	4.17 4.14	P2-48	N.C.	
P2-49	SPI2_SOMI GPIO180	4.17 4.14	P2-50	GND	5.1
P2-51	MMC3_CMD SPI1_CS1 GPIO175	4.11 4.17 4.14	P2-52	N.C.	
P2-53	N.C.		P2-54	N.C.	
P2-55	VCC_CM	5.1	P2-56	N.C.	
P2-57	N.C.		P2-58	N.C.	
P2-59	N.C.		P2-60	N.C.	
P2-61	N.C.		P2-62	GND	5.1
P2-63	N.C.		P2-64	MMC2_DAT4 SPI1_CLK GPIO171	4.11 4.7 4.14
P2-65	N.C.		P2-66	N.C.	
P2-67	VCC_CM	5.1	P2-68	CAM_VS UART4_CTS GPIO97	4.15 4.16 4.14
P2-69	N.C.		P2-70	CAM_WEN CAM_D9 UART4_RX GPIO98	4.15 4.15 4.7 4.14
P2-71	TS_Y+	4.12	P2-72	N.C.	
P2-73	TS_Y-	4.12	P2-74	GND	5.1

Pin #	CM-T3517 Signal Name	Reference Section	Pin #	CM-T3517 Signal Name	Reference Section
P2-75	N.C.		P2-76	GPMC_WAIT1 UART4_TX GPIO63	4.1 4.7 4.14
P2-77	CAM_PCLK GPIO94	4.15 4.14	P2-78	CAM_D8 CAM_FLD I2C3_SCL UART4_TX GPIO95	4.15 4.15 4.16 4.7 4.14
P2-79	VCC_CM	5.1	P2-80	CAM_HS UART4_RTS GPIO96	4.15 4.16 4.14
P2-81	CAM_D0 I2C3_SDA GPIO99	4.15 4.16 4.14	P2-82	CAM_D1 GPIO100	4.15 4.14
P2-83	CAM_D2 GPIO101	4.15 4.14	P2-84	CAM_D3 GPIO102	4.15 4.14
P2-85	CAM_D4 GPIO103	4.15 4.14	P2-86	GND	5.1
P2-87	CAM_D6 GPIO105	4.15 4.14	P2-88	CAM_D5 GPIO104	4.15 4.14
P2-89	N.C.		P2-90	CAM_D7 GPIO106	4.15 4.14
P2-91	VCC_CM	5.1	P2-92	N.C.	
P2-93	LCD_D23 LCD_D5 GPIO93	4.2 4.2 4.14	P2-94	LCD_D22 LCD_D0 SPI3_CS1 GPIO92	4.2 4.2 4.17 4.14
P2-95	LCD_D0 UART1_CTS GPIO70	4.2 4.7 4.14	P2-96	LCD_HSYNC GPIO67	4.2 4.14
P2-97	LCD_D1 UART1_RTS GPIO71	4.2 4.7 4.14	P2-98	GND	5.1
P2-99	LCD_D3 GPIO73	4.2 4.14	P2-100	LCD_D2 GPIO72	4.2 4.14
P2-101	LCD_D5 UART3_TX UART3_IRTX GPIO75	4.2 4.7 4.8 4.14	P2-102	LCD_D4 UART3_RX UART3_IRRX UART3_IRRX GPIO74	4.2 4.7 4.8 4.9 4.14
P2-103	VCC_CM	5.1	P2-104	LCD_D6 UART1_TX GPIO76	4.2 4.7 4.14
P2-105	LCD_D8 GPIO78	4.2 4.14	P2-106	LCD_D7 UART1_RX GPIO77	4.2 4.7 4.14
P2-107	LCD_D10 GPIO80	4.2 4.14	P2-108	LCD_D9 GPIO79	4.2 4.14
P2-109	LCD_D11 GPIO81	4.2 4.14	P2-110	GND	5.1
P2-111	LCD_VSYNC GPIO68	4.2 4.14	P2-112	LCD_PCLK GPIO66	4.2 4.14
P2-113	LCD_D12 GPIO82	4.2 4.14	P2-114	LCD_ACBIAS LCD_DE GPIO69	4.2 4.2 4.14
P2-115	VCC_CM	5.1	P2-116	LCD_D13 GPIO83	4.2 4.14
P2-117	LCD_D15 GPIO85	4.2 4.14	P2-118	LCD_D14 GPIO84	4.2 4.14
P2-119	LCD_D17 GPIO87	4.2 4.14	P2-120	LCD_D16 GPIO86	4.2 4.14
P2-121	LCD_D19 LCD_D3 SPI3_SIMO GPIO89	4.2 4.2 4.17 4.14	P2-122	GND	5.1
P2-123	LCD_D21 LCD_D1 SPI3_CS0 GPIO91	4.2 4.2 4.17 4.14	P2-124	LCD_D18 LCD_D4 SPI3_CLK GPIO88	4.2 4.2 4.17 4.14

Pin #	CM-T3517 Signal Name	Reference Section		Pin #	CM-T3517 Signal Name	Reference Section
P2-125	AGND	4.6		P2-126	LCD_D20 LCD_D2 SPI3_SOMI GPIO90	4.2 4.2 4.17 4.14
P2-127	VCC_CM	5.1		P2-128	AUDIO_IN_L	4.6
P2-129	MIC_BIAS	4.6		P2-130	AUDIO_OUT_L	4.6
P2-131	MIC_IN_ELECTRET	4.6		P2-132	AUDIO_IN_R	4.6
P2-133	N.C.			P2-134	GND	5.1
P2-135	VCC_CM	5.1		P2-136	AUDIO_OUT_R	4.6
P2-137	USB2_DP HUBP1_DP	4.4.2 4.4.2		P2-138	USB1_DP	4.4.2
P2-139	USB2_DM HUBP1_DM	4.4.2 4.4.2		P2-140	USB1_DM	4.4.2

6.2 Connector Type

Table 42 Connector type

Part Reference	Mfg.	CM-T3517 connector P/N	Baseboard (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab, see [prices] >> [accessories] links at CompuLab's website.

CompuLab's P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 4 CM-T3517 top view

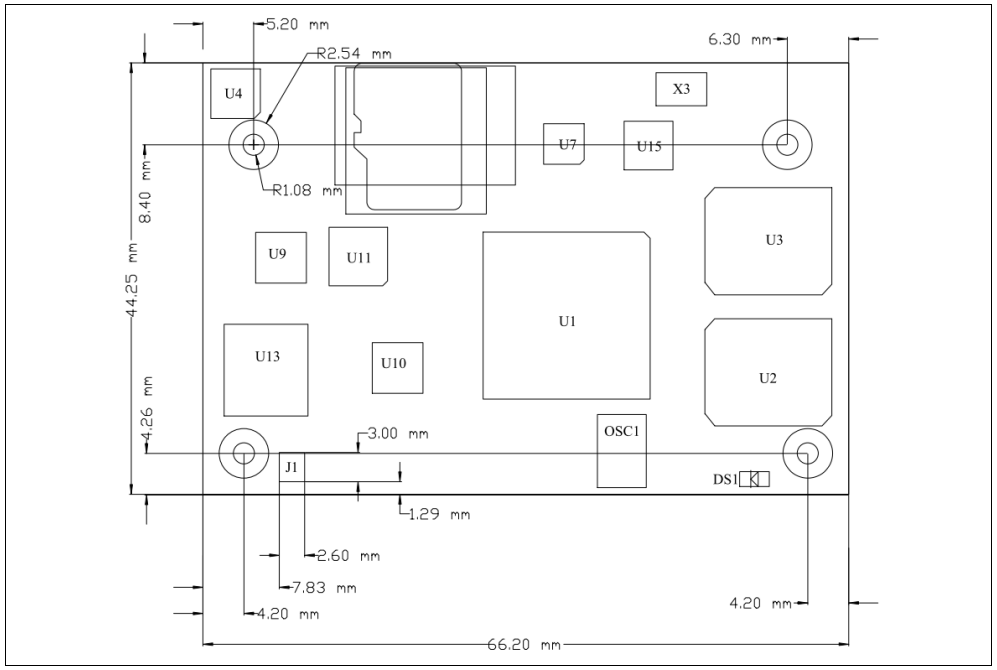
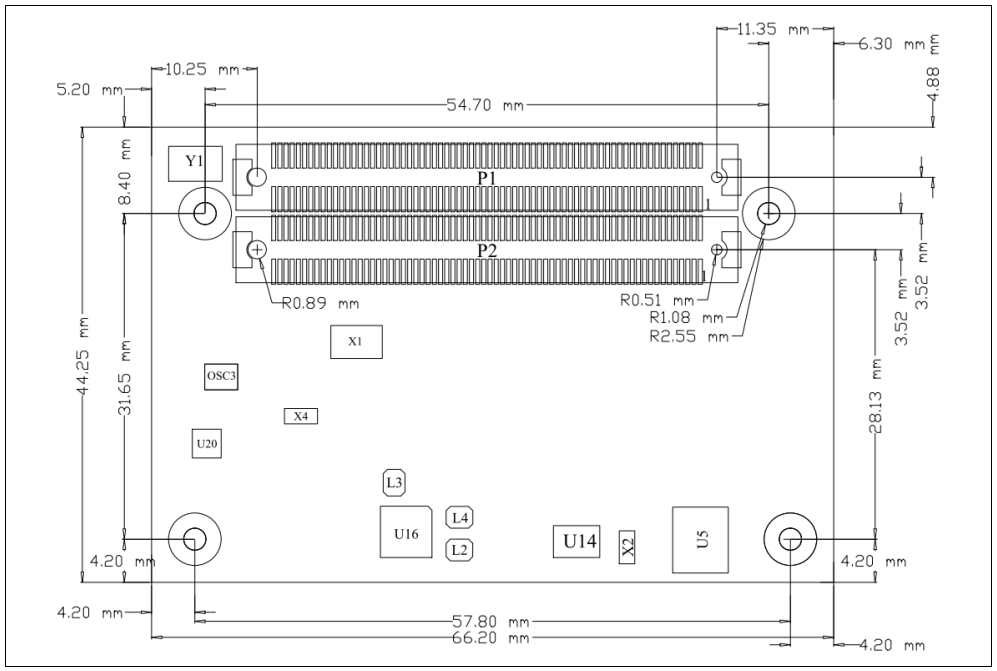


Figure 5 CM-T3517 bottom (X-Ray view - as seen from top side)



1. All dimensions are in millimeters.
2. Height of all components is <2mm.
3. Baseboard connectors provide 4mm board-to-board clearance.
4. Board thickness is 1.6mm.

Mechanical drawings are available for download in DXF format the CompuLab website, by opening the "Development Resources" tab of the CM-T3517 product page and downloading the "CM-T3517 dimensions and connector locations" file.

6.4 Standoffs

The CM-T3517 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 43 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 44 Absolute Maximum ratings

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	2.1		4.5	V

7.2 Recommended Operating Conditions

Table 45 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VCC_CM)	3.3	3.6	4.2	V
Main power supply voltage (VCC_CM) **without** 'W' option	3.0	3.6	4.2	V
RTC backup battery voltage (BKBAT)	1.8	3.2	3.3	V

7.3 DC Electrical Characteristics

Table 46 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
Digital I/O interfaces					
V_{IH}		2.0		3.6	V
V_{IL}		TBD		0.6	
V_{OH}		2.475			
V_{OL}		TBD		0.412	
I^2C (open drain with internal pull up to 3.3V)					
V_{IH}		TBD		TBD	V
V_{IL}		TBD		0.6	V
V_{OL}		TBD		TBD	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V

7.4 Power Output Characteristics

Table 47 Power Output Characteristics

Parameter	Min	Typ	Max	Unit
VCC_MMC				
Output voltage	3.135	3.3	3.465	V
Rated output current			200	mA
USB0_5V_OUT				
Output voltage		4.8		V
Rated output current		100		mA

7.5 Power Consumption

To be added in a future revision of this document.

7.6 ESD Performance

Table 48 ESD Performance

Interface	ESD Performance
USB OTG	±1 kV ESD using HBM
USB host 1 & 2	±8 kV ESD using HBM
USB hub	±4 kV ESD using HBM
RS232	±15 kV ESD using HBM

7.7 Operating Temperature Ranges

The CM-T3517 is available with three options of operating temperature range.

Table 49 CM-T3517 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual cards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Baseboard Design Guidelines

- Ensure that all VCC_CM and GND power pins are connected.
- Major power rails - VCC_CM and GND must be implemented by planes, rather than by traces. Using at least two planes is essential to ensure the system's signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VCC_CM and GND near the mating connectors.
- It is recommended to connect the standoff holes of the baseboard to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-T3517 operation. All power-up circuitry and all required pullups/pulldowns are found on the module.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIO's), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet and USB signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
  - Local bus signals must be buffered in most cases.
- Be careful when placing components under the CM-T3517 module. The baseboard interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-T3517. Maximum allowable height for components placed under the CM-T3517 is 1.0mm.
- Refer to the SB-T35 baseboard reference design schematics.

8.2 Baseboard Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the baseboard. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VCC_CM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module, then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module's on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the baseboard, shorting them on the connectors can disable the module's operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector's body. Note that solder shorts are the most frequent factor inhibiting a module's start.
- Check possible signal's shorting due to errors of baseboard PCB design or assembly.
- Improper functioning of a customer baseboard can accidentally delete boot-up code from the CM-T3517, or even damage the module's hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab's SB-T35 baseboard.
- It is recommended to assemble more than one baseboard for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Isolation Transformer and Qualified Magnetics

The CM-T3517 provides a physical 10/100 Ethernet interface. This interface is based on the KSZ8041 physical layer transceiver from Micrel.

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements. Refer to the table below for recommended transformer characteristics.

Table 50 Recommended Transformer Characteristics

Parameter	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350µH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4µH	1MHz (min.)
Inter-Winding Capacitance (typ.)	12pF	
DC resistance (typ.)	0.9Ω	
Insertion Loss (max.)	-1.0dB	0 MHz – 65 MHz
HIPOT (min.)	1500Vrms	

Refer to the table below for qualified single port magnetics.

Table 51 Qualified Magnetics

Vendor	P/N	Auto MDI-X
Bel Fuse	S558-5999-U7	YES
Bel Fuse (Mag Jack)	SI-46001	YES
Bel Fuse (Mag Jack)	SI-50170	YES
Delta	LF8505	YES
LanKom	LF-H41S	YES
Pulse	H1102	YES
Pulse (low-cost)	H1260	YES
Transpower	HB726	YES
TDK (Mag Jack)	TLA-6T718	YES
UDE	RTA-1D4B8V1A	YES

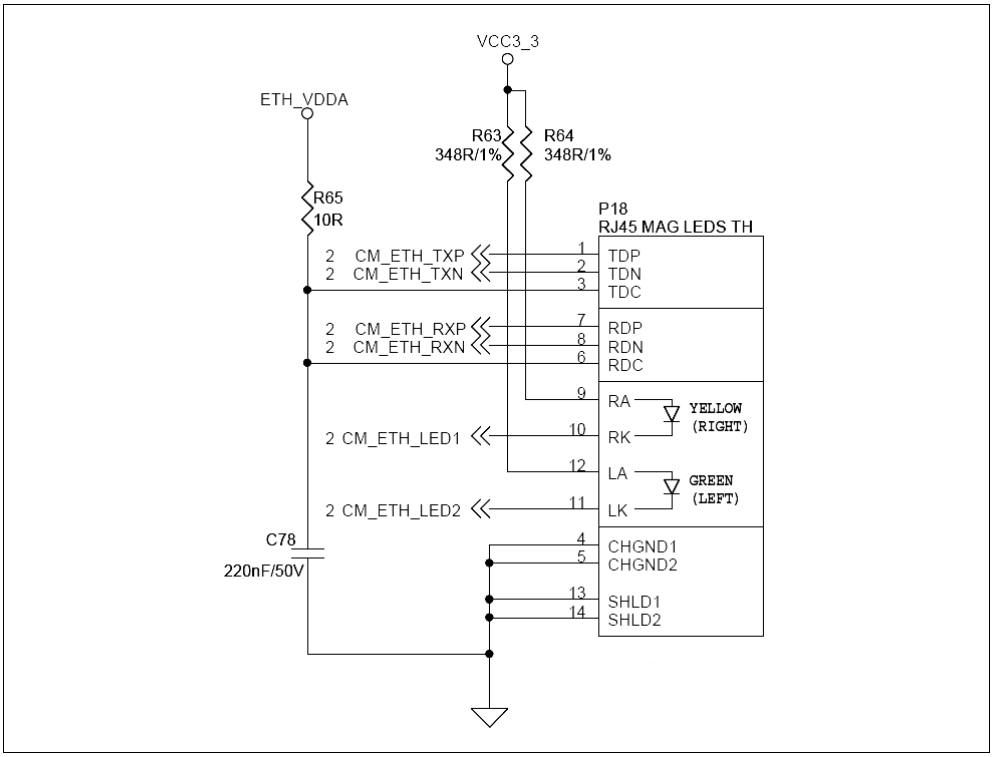
8.3.2 Magnetics Connection

The center tap connection on the CM-T3517 side for the transmit channel must be connected to a 3.3V analog power rail (can be created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. Decouple the 3.3V voltage with at least one large and one small capacitor (10uF and 0.1uF respectively). The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

The center tap connection on the CM-T3517 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 µF capacitor is required from the receive channel center tap of the magnetics to digital ground.

The figure below shows an implementation example with a magnetic embedded in the RJ-45 socket with integrated LED's.

Figure 6 Magnetics connection example



8.4 Battery Powered Design

The power management sub-system of the CM-T3517 is designed for direct operation with a Lithium ion Polymer battery. Battery charging and supervision functions must be implemented on the baseboard. Please refer to SB-T35 design package for a comprehensive reference design.