CM-iGT CoM

Reference Guide

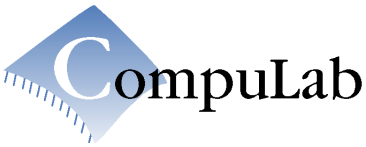

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Table 1 Revision Notes

Date	Description
February 2013	First release

Please check for a newer revision of this manual at CompuLab web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site to those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CM-iGT Computer-on-Module.

1.2 CM-iGT Part Number Legend

For CM-iGT part number legend, please refer to the 'Pricing and Ordering Info' section at CompuLab website: https://compulab.co.il/products/computer-on-modules/cm-igt/#ordering .

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-iGT Developer Resources	https://compulab.co.il/products/computer-on-modules/cm-igt/#devres

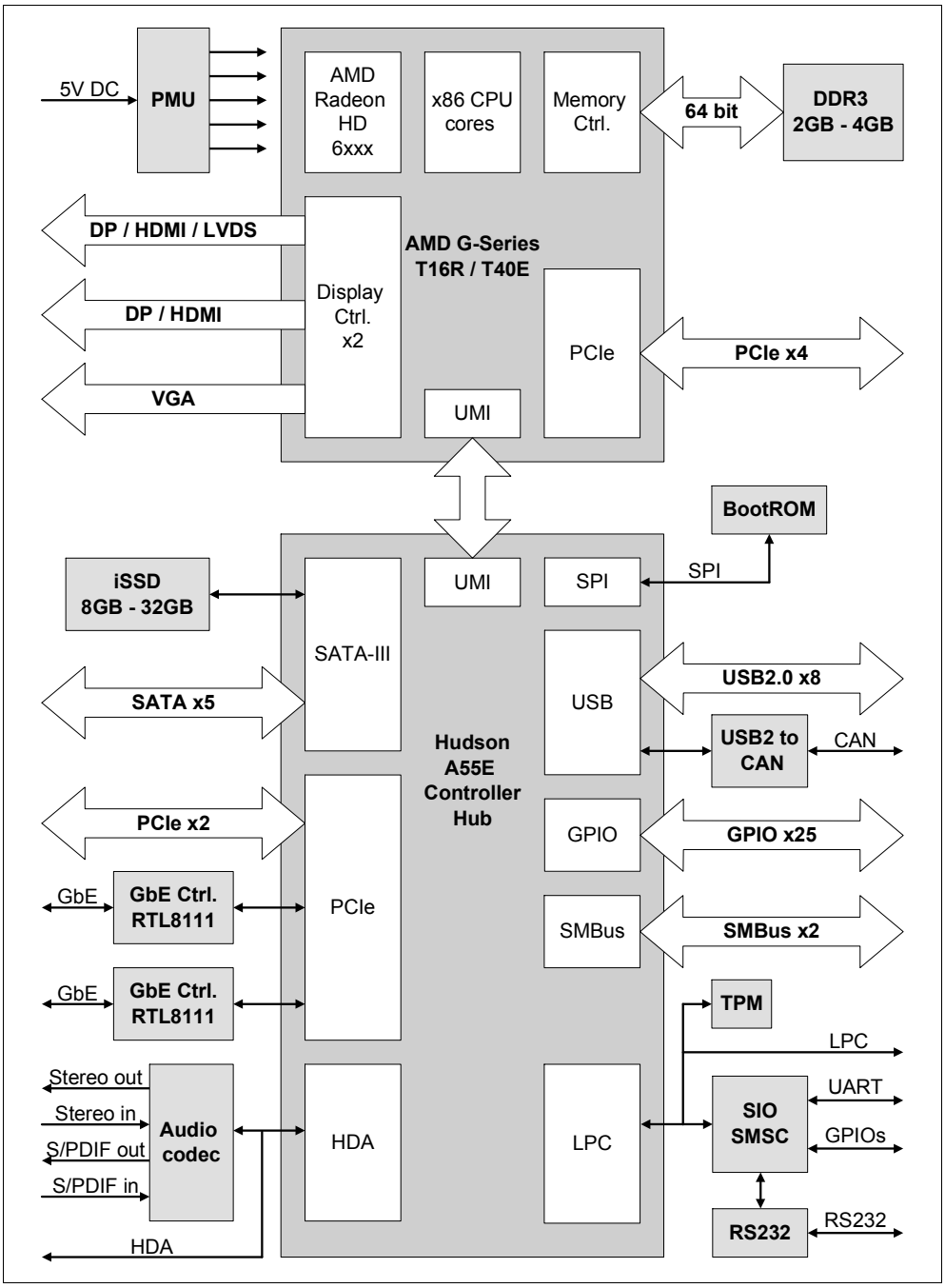
2 OVERVIEW

2.1 Highlights

- AMD G-Series Fusion dual-core 64 bit x86 CPU, up to 1.65GHz
- Up to 4GB DDR3
- Up to 32GB on-board SSD storage
- AMD Radeon HD 6250 GPU
- Universal Video Decoder, 1080p Blu-Ray playback support
- Graphics controller with dual-head support. Up to 1920x1200 at 60 Hz resolution
- HDMI, DisplayPort, LVDS and VGA interfaces
- GbE x 2, PCIe x 6, SATA x 5, USB x 9, RS232, UART, CAN, GPIO x 29, SMBus x 2, LPC
- Linux, Windows Embedded 7
- Miniature size: 75 x 65 x 8 mm
- SB-iGT carrier board turns the CM-iGT module into SBC-iGT - a single board computer

2.2 Block Diagram

Figure 1 CM-iGT Block Diagram



2.3 CM-iGT Features

The "Option" column specifies the configuration code required for a particular feature. "+" means that the feature is always available.

Table 3 System and Graphics

Feature	Specifications	Option
CPU	AMD G-Series Processor: G-T16R single-core 600MHz / G-T40E dual-core 1GHz / G-T56N dual-core 1.65GHz*	C
RAM	2GB - 4GB DDR3-1066, 64-bit	D
Storage	On-board BIOS flash, 1MB, reprogrammable	+
	On-board SSD, up to 32GB, through SATA interface	ND
Video Processing Unit	UVD 3 engine with native H.264, VC-1, MPEG2, and DivX 1080p Blu-Ray playback support	+

* The G-T56N CPU option requires an extended cooling solution, which is not provided by CompuLab.

Table 4 I/O

Feature	Specifications	Option
Display	Two configurable display interfaces support simultaneous operation with the following configurations: • Up to two DisplayPort interfaces, up to 1920x1200 at 60Hz • Up to two HDMI 1.4 interfaces, stereo-3D support, up to 1920x1200 at 60Hz • Up to one LVDS interface • Up to one VGA interface	+
PCI Express	Up to 6 PCI Express Gen 2.0 ports	+
USB	Up to 9 USB2.0 high-speed host ports, 3 EHCI/OHCI USB2 high/full-speed hubs USB2.0 full-speed port, OHCI full speed hub	+
SATA	Up to 5 SATA III ports, 6.0 Gbps, integrated controller and PHY	+
Serial Ports	COM1 - RS-232, rx/tx & flow control, RS-232 levels, up to 460 Kbps	S
	UART2 - UART, rx/tx, or IrDA v1.2, 3.3V levels, up to 4 Mbps	S
CAN bus	CAN bus interface (CAN V2.0B at 1 Mb/s), 3.3V levels	Y
Gigabit Ethernet	Up to two 1000Base-T Ethernet ports. Implemented with Realtek RT8111F 802.3 compliant controllers	E
Audio	Onboard audio codec with analog stereo output, stereo input and stereo microphone support	A
	S/PDIF input / output	A
	HDMI audio	+
	Azalia HD audio compliant interface	+
LPC Bus	Host, 33 MHz, Intel LPC v1.0 compatible	+
I2C/SMBus	Up to 2 I2C buses, up to 400Kbps	+
TPM	Trusted Platform Manager ver 1.2 of TCG by Atmel AT97SC3204	J
General Purpose I/O	Up to 21 GPIO's implemented with the FCH chipset	+
	Up to 8 GPIO's implemented with SuperIO	S
General Event Inputs	Up to 3 software programmable general purpose input signals	+

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 5V DC
Active power consumption	TBD
Standby/Sleep consumption	TBD
Dimensions	75 x 65 x 8 mm
Weight	37 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C Extended: -20° to 70° C Industrial: -40° to 85° C
Storage temperature	-40° to 85° C

Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 CORE SYSTEM COMPONENTS

3.1 AMD Embedded G-Series APU

3.1.1 CPU Core

The AMD embedded G-Series APU x86 core supports the following key features:

- Single or dual x86 Processor
- AMD64 64-bit ISA
- Advanced Branch Prediction
- Out-of-Order Instruction Execution
- 64-bit floating-point unit
- SSE1,2,3, SSSE3 ISA, SSE4A, MMX
- AMD Virtualization technology

3.1.2 GPU Core

The AMD embedded G-Series APU integrated GPU core supports the following key features:

- Dedicated graphics memory controller
  - High efficiency ring bus memory controller
  - Direct connection to memory
- 2D Acceleration
  - Highly-optimized 128-bit engine, capable of processing multiple pixels per clock
- 3D Acceleration
  - Full DirectX 11 support, including full speed 32-bit floating point per component operations
  - Shader Model 5
  - OpenCL 1.1 support
  - OpenGL 4.0 support
- Motion Video Acceleration
  - Dedicated hardware (UVD 3) for H.264, VC-1 and MPEG2 decode
  - HD HQV and SD HQV support: noise removal, detail enhancement, color enhancement, cadence detection, sharpness, and advanced de-interlacing
  - Super up-conversion for SD to HD resolutions

3.2 DRAM

CM-iGT incorporates 2GB - 4GB of DDR3. The DRAM interface is 64-bits wide and runs with a 533MHz clock.

3.3 SPI Flash or Boot ROM

CM-iGT features 16 Mbits of SPI flash used for BIOS.

3.4 iSSD

CM-iGT features up to 32GB of on-board iSSD storage.

4 PERIPHERAL INTERFACES

CM-iGT implements a number of peripheral interfaces through the interface connectors (P1 and P18). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options. Each signal's availability is noted in the "Signal description" table of each interface.
- Certain interface pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to "Signal description" in the table of each interface.
- All of the CM-iGT digital interfaces operate at 3.3V CMOS voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal.
- **"Pin#" –** The pin number on the interface connector.
- **"Type" –** Signal type.
- **"Description" –** Signal description.
- **"Availability" –** Certain signals are not available with/without certain configuration options. This column summarizes configuration requirements for each signal.

Each interface signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal

- **"O"** – Digital output
- **"I"** – Digital input
- **"IO"** – Digital Input/Output
- **"AO"** – Analog Output
- **"AI"** – Analog Input
- **"OD"** – Open Drain Signal, not pulled up on the CM-iGT
- **"ODP"** – Open Drain Signal, pulled up on the CM-iGT
- **"IPU"** – Open Drain Input Signal, pulled up on the CM-iGT
- **"IPD"** – Open Drain Input Signal, pulled down on the CM-iGT
- **"P"** – Power signal

4.1 Display Interface

The CM-iGT display sub-system is based on the display controller of the APU.

The display sub-system incorporates two independent display controllers supporting dual-head operation and features three separate display interfaces:

- DP0 – configurable as DisplayPort, eDP, HDMI, single link DVI, single link LVDS
- DP1 – configurable as DisplayPort, eDP, HDMI, single link DVI
- Analog VGA, cloned with DP1.

When DP0 is configured for Display Port / eDP / single link DVI operating modes, maximal resolution is 1920x1200@60Hz. When DP0 is configured as single link LVDS maximal resolution is 1024x600@60Hz.

In dual-head operation mode, maximal resolution for DP1 is 1920x1200@60Hz.

Table 6 Display interface signals

Signal Name	Pin #	Type	Description	Availability
Display Port#0				Always available
DP0_TX0_P	P1-60	O	DP0 - Lane#0	
DP0_TX0_N	P1-58	O		
DP0_TX1_P	P1-53	O	DP0 - Lane#1	
DP0_TX1_N	P1-51	O		
DP0_TX2_P	P1-54	O	DP0 - Lane#2	
DP0_TX2_N	P1-52	O		
DP0_TX3_P	P1-65	O	DP0 - Lane#3	
DP0_TX3_N	P1-63	O		
DP0_AUX_P	P1-47	IO	DP0 - Auxiliary lane, Used as DDC lines for HDMI/DVI/LVDS	
DP0_AUX_N	P1-49	IO		
DP0_HPD	P1-44	I	DP0 - Hot plug detection. 100K PD on Base is needed	
LVDS Support Signals				
LVDS_AUX_EN#	P1-46	O	Control to Power LCD Logic Circuits	
LVDS_VARY_BL	P1-48	O	LCD Backlight Intensity	
LVDS_BLON	P1-56	O	LCD Backlight Inverter ON	
Display Port#1				
DP1_TX0_P	P1-29	O	DP1 - Lane#0	
DP1_TX0_N	P1-27	O		
DP1_TX1_P	P1-35	O	DP1 - Lane#1	
DP1_TX1_N	P1-33	O		
DP1_TX2_P	P1-42	O	DP1 - Lane#2	
DP1_TX2_N	P1-40	O		
DP1_TX3_P	P1-30	O	DP1 - Lane#3	
DP1_TX3_N	P1-28	O		
DP1_AUX_P	P1-23	IO	DP1 - Auxiliary lane, Used as DDC lines for HDMI/DVI	
DP1_AUX_N	P1-21	IO		
DP1_HPD	P1-32	I	DP1 - Hot plug detection. 100K PD on Base is needed	
VGA				
VGA_R	P1-93	AO	Red video signal	
VGA_G	P1-101	AO	Green video signal	
VGA_B	P1-105	AO	Blue video signal	
VGA_VSYNC	P1-107	O	Vertical synchronization	
VGA_HSYNC	P1-109	O	Horizontal synchronization	
VGA_SDA	P1-99	IO	EDID Data Line	
VGA_SCL	P1-95	O	EDID Clock Line	

4.2 Gigabit Ethernet

CM-iGT incorporates up to two full-featured Gigabit Ethernet interfaces.

4.2.1 Primary Gigabit Ethernet

CM-iGT primary Gigabit Ethernet interface is implemented with the RTL8111F Gigabit Ethernet controller with integrated PHY. The interface supports the following main features:

- Fully compliant with IEEE 802.3 standard
- 1000 Mbps operation – full duplex
- 10 / 100 Mbps operation – half and full duplex
- Crossover Detection and Auto-Correction, Polarity Correction
- Auto-negotiation, adaptive equalization, cross-talk and echo cancellation
- Timing recovery and Error correction
- Activity and speed indicator LED controls

Table 7 Primary Gigabit Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
LAN0_MDIP0	P1-2	IO	First pair in 1000Base-T / transmit pair in 10Base-T and 100Base-T	Only available **with** either 'E1' or 'E2' configuration options
LAN0_MDIN0	P1-4	IO		
LAN0_MDIP1	P1-1	IO	Second pair in 1000Base-T / receive pair in 10Base-T and 100Base-T	
LAN0_MDIN1	P1-3	IO		
LAN0_MDIP2	P1-10	IO	Third pair in 1000Base-T	
LAN0_MDIN2	P1-12	IO		
LAN0_MDIP3	P1-9	IO	Forth pair in 1000Base-T	
LAN0_MDIN3	P1-11	IO		
LAN0_EESK_L1	P1-6	O	Activity LED output. Active low	
LAN0_EEDI_L2	P1-5	O	10 / 100 / 1000 LED output	
LAN0_TXLED#	P1-13	O	10 / 100 / 1000 + activity LED output	

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

4.2.2 Secondary Gigabit Ethernet

CM-iGT secondary Gigabit Ethernet interface is implemented with the RTL8111F Gigabit Ethernet controller with integrated PHY. The interface supports the following main features:

- Fully compliant with IEEE 802.3 standard
- 1000 Mbps operation – full duplex
- 10 / 100 Mbps operation – half and full duplex
- Crossover Detection and Auto-Correction, Polarity Correction
- Auto-negotiation, adaptive equalization, cross-talk and echo cancellation
- Timing recovery and Error correction
- Activity and speed indicator LED controls

Table 8 Secondary Gigabit Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
LAN1_MDIP0	P18-2	IO	First pair in 1000Base-T / transmit pair in 10Base-T and 100Base-T	Only available **with** either 'E2' configuration options
LAN1_MDIN0	P18-4	IO		
LAN1_MDIP1	P18-1	IO	Second pair in 1000Base-T / receive pair in 10Base-T and 100Base-T	
LAN1_MDIN1	P18-3	IO		
LAN1_MDIP2	P18-10	IO	Third pair in 1000Base-T	
LAN1_MDIN2	P18-12	IO		
LAN1_MDIP3	P18-9	IO	Forth pair in 1000Base-T	
LAN1_MDIN3	P18-11	IO		
LAN1_EESK_L1	P18-6	O	Activity LED output. Active low	
LAN1_EEDI_L2	P18-5	O	10 / 100 / 1000 LED output	
LAN1_TXLED#	P18-13	O	10 / 100 / 1000 + activity LED output	

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

4.3 PCI Express

CM-iGT features up to six PCI Express Gen2 ports. Two ports are implemented with the Fusion Controller Hub (FCH) and additional four ports with the APU. PCIe interface derived from the APU can be configured as 4 x PCIe-single lane or 2 x PCIe-x2 lane or 1 x PCIe-x4 lane.

Table 9 PCI Express interface signals

Signal Name	Pin #	Type	Description	Availability
PCIE Interface APU				
PCIE_APU_RX0_N	P1-34	I	receive data pair Lane#0	Always available
PCIE_APU_RX0_P	P1-36	I		
PCIE_APU_TX0_N	P1-78	O	transmit data pair Lane#0	
PCIE_APU_TX0_P	P1-76	O		
PCIE_APU_RX1_N	P1-39	I	receive data pair Lane#1	
PCIE_APU_RX1_P	P1-41	I		
PCIE_APU_TX1_N	P1-84	O	transmit data pair Lane#1	
PCIE_APU_TX1_P	P1-82	O		
PCIE_APU_RX2_N	P1-83	I	receive data pair Lane#2	
PCIE_APU_RX2_P	P1-81	I		
PCIE_APU_TX2_N	P1-90	O	transmit data pair Lane#2	
PCIE_APU_TX2_P	P1-88	O		
PCIE_APU_RX3_N	P1-89	I	receive data pair Lane#3	
PCIE_APU_RX3_P	P1-87	I		
PCIE_APU_TX3_N	P1-96	O	transmit data pair Lane#3	
PCIE_APU_TX3_P	P1-94	O		
PCIE Interface FCH				
PCIE_FCH_RX2_N	P18-106	I	receive data pair	Always available
PCIE_FCH_RX2_P	P18-108	I		
PCIE_FCH_TX2_N	P18-112	O	transmit data pair	
PCIE_FCH_TX2_P	P18-114	O		
PCIE_FCH_RX3_N	P18-105	I	receive data pair	
PCIE_FCH_RX3_P	P18-107	I		
PCIE_FCH_TX3_N	P18-111	O	transmit data pair	
PCIE_FCH_TX3_P	P18-113	O		
PCIE reference clock and misc. signals				
XA_PCIE_CLK_N	P18-81	O	clock pair A	Always available
XA_PCIE_CLK_P	P18-83	O		
XA_PCIe_CLKREQ#	P18-17	IPU	clock request input	
XB_PCIE_CLK_N	P18-99	IO	clock pair B	
XB_PCIE_CLK_P	P18-101	O		
XB_PCIe_CLKREQ#	P18-15	IPU	clock request input	
PCIE_WAKE_UP#	P18-109	IPU	PCIE wake-up input	

4.4 SATA

CM-iGT incorporates five SATA-III ports implemented with the FCH. The interface supports the following main features:

- Backward compatible with Second and First generation devices
- Complies with SATA 2.6 specification
- Supports two modes of operation: (a) IDE emulation mode ; (b) AHCI mode (compliant with AHCI specification revision 1.2)
- Device or Host Initiated Power Management (DIPM /HIPM) support
- Hot plug support
- Native Command Queuing (NCQ)

Table 10 SATA interface signals

Signal Name	Pin #	Type	Description	Availability
SB_SATA_RX0_N	P18-118	I	receive data pair#1	Always available
SB_SATA_RX0_P	P18-120	I		
SB_SATA_TX0_N	P18-124	O	transmit data pair#1	
SB_SATA_TX0_P	P18-126	O		
SB_SATA_RX1_N	P18-100	I	receive data pair#2	
SB_SATA_RX1_P	P18-102	I		
SB_SATA_TX1_N	P18-93	O	transmit data pair#2	
SB_SATA_TX1_P	P18-95	O		
eSATA_RX0_N	P1-118	I	receive data pair#3	
eSATA_RX0_P	P1-120	I		
eSATA_TX0_N	P1-102	O	transmit data pair#3	
eSATA_TX0_P	P1-100	O		
eSATA_RX1_N	P18-58	I	receive data pair#4	
eSATA_RX1_P	P18-60	I		
eSATA_TX1_N	P18-56	O	transmit data pair#4	
eSATA_TX1_P	P18-54	O		
eSATA_RX2_N	P18-82	I	receive data pair#5	
eSATA_RX2_P	P18-84	I		
eSATA_TX2_N	P18-78	O	transmit data pair#5	
eSATA_TX2_P	P18-76	O		
HDD_ACT#	P18-128	OD	HDD activity indicator	

4.5 USB

CM-iGT provides up to 9 USB 2.0 ports and one USB1.0 implemented with the FCH. USB 2.0 interface provides the following features:

- Complies with EHCI (high-speed host controller)
- Complies with OHCI (low-speed/full-speed host controller)
- Complies with the USB 2.0 standard for high-speed (480M bit/s) functions

Table 11 USB interface signals

Signal Name	Pin #	Type	Description	Availability	HUB
USB_FS1_N	P1-77	IO	USB Full speed pair#0	Always available.	OHCI3
USB_FS1_P	P1-75	IO			
USB_HS0_N	P1-59	IO	USB High Speed pair#0		OHCI0 EHCI0
USB_HS0_P	P1-57	IO			
USB_HS1_N	P18-41	IO	USB High Speed pair#1		OHCI0 EHCI0
USB_HS1_P	P18-39	IO			
USB_HS3_N	P18-75	IO	USB High Speed pair#3		OHCI0 EHCI0
USB_HS3_P	P18-77	IO			
USB_HS4_N	P1-130	IO	USB High Speed pair#4		OHCI0 EHCI0
USB_HS4_P	P1-132	IO			
USB_HS5_N	P18-138	IO	USB High Speed pair#5		OHCI1 EHCI1
USB_HS5_P	P18-140	IO			
USB_HS7_N	P1-129	IO	USB High Speed pair#7		OHCI1 EHCI1
USB_HS7_P	P1-131	IO			
USB_HS8_N	P1-135	IO	USB High Speed pair#8		OHCI1 EHCI1
USB_HS8_P	P1-137	IO			
USB_HS12_N	P1-136	IO	USB High Speed pair#12		OHCI2 EHCI2
USB_HS12_P	P1-138	IO			
USB_HS13_N	P18-130	IO	USB High Speed pair#13		OHCI2 EHCI2
USB_HS13_P	P18-132	IO			
USBOC2#	P1-128	IPU	USB Over Current indicator #2		
USBOC6#	P18-136	IPU	USB Over Current indicator #6		
USBOC3#	P1-133	IPU	USB Over Current indicator #3		

4.6 CAN Bus

CM-iGT incorporates CAN bus interface implemented with the Microchip MCP2515 IC. The CAN bus implements the CAN specification, version 2.0B. It is capable of transmitting and receiving both standard and extended data and remote frames. It features two acceptance masks and six acceptance filters that are used to filter out unwanted messages, thereby reducing the host processor overhead.

Table 12 CAN BUS

Signal Name	Pin #	Type	Description	Availability
CAN_RX	P18-69	I	CAN BUS Receive signal 3.3V level	Only available with the '**Y**' configuration option
CAN_TX	P18-65	O	CAN BUS Transmit signal 3.3V level	

4.7 Audio

4.7.1 Analog and Digital Audio

The CM-iGT analog audio subsystem is implemented with the Realtek ALC886-GR audio codec. The audio sub-system supports the following features:

- Single ended stereo-line output
- Single ended stereo-line input
- Digital input and output (S/PDIF)

Table 13 Audio signals

Signal Name	Pin #	Type	Description	Availability
LIN1_L	P18-133	AI	Left stereo line input	Only available with the '**A**' configuration option
LIN1_R	P18-131	AI	Right stereo line input	
LOUT_L	P18-139	AO	Left stereo line output	
LOUT_R	P18-137	AO	Right stereo line output	
MIN1_L	P18-129	AI	Left stereo microphone input	
MIN1_R	P1-24	AI	Right stereo microphone input	
SPDIFI	P1-20	I	Audio digital Input	
SPDIFO	P1-18	O	Audio digital Output	
AUD_SENSA	P1-22	I	Jack detection pin, see SB-iGT manual	
SPKR	P18-22	AO	Computer speaker output	Always available

4.7.2 High Definition Audio Interface

The CM-iGT High Definition Audio (HDA) interface is implemented with the FCH Azalia controller compliant with HD Audio 1.0 specification.

Table 14 HDA signals

Signal Name	Pin #	Type	Description	Availability
AZ_BITCLK	P18-119	O	HDA clock	Always available
AZ_RST#	P18-121	O	HDA reset	
AZ_SYNC	P18-125	O	HDA sync	
AZ_SDOUT	P18-123	O	HDA digital output	
AZ_SDATA_IN0	P18-117	I	HDA digital input #0	Only available **without** the '**A**' configuration option
AZ_SI2_GPIO169	P18-73	IO	HDA digital input #2	Always available
AZ_SI3_GPIO170	P18-85	IO	HDA digital input #3	

4.8 LPC - Low Pin Count Interface

CM-iGT features an LPC Interface compliant with the LPC 1.1 specification. The LPC bus provides a functional replacement for interfacing legacy ISA functions.

Table 15 LPC signals

Signal Name	Pin #	Type	Description	Availability
PCI_CLK3	P18-72	O	LPC clock#1 (33 Mhz)	Always available
LPC_CLK0	P18-88	O	LPC clock#2 (33 Mhz)	
LAD0	P18-90	IO	LPC Multiplexed command, address, data	
LAD1	P18-92	IO		
LAD2	P18-94	IO		
LAD3	P18-96	IO		
SERIRQ_GPIO48	P18-89	OD	Serial Interrupt Request	
LFRAME#	P18-87	O	LPC Frame	
FCH_PCIE_RST#	P18-104	ODP	LPC Device reset (active low)	

4.9 Serial Ports

4.9.1 UART

CM-iGT provides one general purpose UART interface implemented with the SMSC SIO1007 SuperIO. The UART interface supports the following features:

- High Speed 16C550A compatible with Send/Receive 16 byte FIFO
- Supports 50 to 460.8K baud rates with programmable baud rate generator

Table 16 UART Signals

Signal Name	Pin #	Type	Description	Availability
SIO_IR_RXD	P1-112	I	Serial Data In	Only available with the '**S**' configuration option
SIO_IR_TXD	P1-114	O	Serial Data Out	

4.9.2 RS232

CM-iGT incorporates one RS232 port implemented with the SMSC SIO1007 SuperIO. The following features are supported:

- High Speed 16C550A compatible with Send/Receive 16 byte FIFO
- Programmable baud rate of up to 250 Kbps
- Full modem control circuitry

Table 17 UART/RS232 Signals

Signal Name	Pin #	Type	Description	Availability
COM1_CTS	P1-123	I	Clear To Send	Only available with the '**S**' configuration option
COM1_DCD	P1-113	I	Data Carrier Detect	
COM1_DSR	P1-111	I	Data Set Ready	
COM1_DTR	P1-125	O	Data Terminal Ready	
COM1_RI	P1-124	I	Ring Indicate	
COM1_RTS	P1-121	O	Request To Send	
COM1_RX	P1-117	I	Serial Data In	
COM1_TX	P1-119	O	Serial Data Out	

4.10 GPIO and GEVENT

CM-iGT provides 26 general purpose I/O pins (GPIO) and 3 general event inputs (GEVET).

Table 18 GPIO signals

Signal Name	Pin #	Type	Description	Availability
GPIO by Super IO				
SIO_GPIO16	P1-64	IO	Each SIO_GPIOxx corresponds to the GPIOxx of SIO1007 SuperIO chip	Available with **S** option
SIO_GPIO17	P1-66	IO		
SIO_GPIO30	P1-68	IO		
SIO_GPIO31	P1-70	IO		
SIO_GPIO32	P1-72	IO		
SIO_GPIO33	P1-69	IO		
SIO_GPIO34	P1-71	IO		
SIO_GPIO35	P1-73	IO		
Regular GPIO by FCH				
GPIO202_FCS#	P18-42	IO	Each GPIOxx corresponds to the GPIOxx of FCH. Active in S0 power state	Always available
GPIO205_FCK	P18-44	IO		
FCH_GPIO13	P18-57	IO		
FCH_GPIO11	P1-17	IO		
FN2PWM_GPIO54	P18-16	IO		
FNTH1_GPIO57	P18-80	IO		
FNTH2_GPIO58	P18-29	IO		
TIN2_GPIO173	P1-85	IO		
TMR0_GPIO197	P18-28	IO		
TMR1_GPIO198	P18-30	IO		
FNTH_GPIO56	P1-104	IO		
Open Drain GPIO by FCH				
FCH_GPIOD145	P1-45	IO	Each GPIOxx corresponds to the Open Drain GPIOxx of FCH. Active in S0 power state	Always available
FCH_GPIOD146	P1-92	IO		
FCH_GPIOD147	P1-108	IO		
FCH_GPIOD147	P1-116	IO		
FCH_GPIOD149	P1-97	IO		
Regular GPIO by FCH available in Stand-by / Hibernate modes				
FCH_GPIO201_S5	P18-18	IO	GPIO201/204 by FCH Active in S0 and S5 power states.	Always available
FCH_GPIO204_S5	P18-46	IO		

Table 19 GEVENT signals

Signal Name	Pin #	Type	Description	Availability
IRRX0_GEVENT16#	P18-59	I		Always available
IRRX1_GEVENT20#	P18-37	I		
IRTX0_GEVENT17#	P18-61	I		

4.11 SMBUS

CM-iGT features up to two SMBUS interfaces with Alert Input. One of the interfaces is available in Sleep/Hibernate modes. This interface is compatible with I2C devices. SMBus supports operating frequencies of 10-100 kHz.

Table 20 SMBUS signals

Signal Name	Pin #	Type	Description	Availability
SCLK0	P18-21	ODP	SMBUS#0 CLK and Data, active in S0 power state	Always Available
SDATA0	P18-23	ODP		
SCLK2	P18-27	ODP	SMBUS#1 CLK and Data, active in S3/S5 power state	
SDATA2	P18-25	ODP		
SMBALERT#	P18-24	IPU	SMBUS Alert	

5 SYSTEM LOGIC

5.1 Power Management

5.1.1 Power Rails

CM-iGT is powered with 5V_S0 and 5V_S5 power rails:

- 5V_S0 - Main power supply. Typical voltage – 5V. Current consumption requirements: 3A for C600 and C1000D configuration options and 5A for C1650D configuration option.
- 5V_S5 - Sleep/Hibernate power supply. Typical voltage – 5V. Always present. Current consumption requirements: 2A for C600 and C1000D configuration options and 3A for C1650D configuration option.
- A_VBAT - RTC back-up battery power input. A_VBAT should always be present for proper RTC operation. It is recommended to connect this rail to a 3V coin-cell lithium battery.
- GND - Common ground.

5.1.2 System Signals and Power Sequence

CM-iGT features an automatic power-on function that turns on the device immediately after the power is applied and internal circuits are stabilized. The power-up sequence should be as follows:

- Apply 5V_S5
- FCH initiates SLP_S3B5V low to enable 5V_S0 rail.

The power down/standby sequence:

- Apply PWRBTN#_HW (short pulse for standby / more than 4sec for power down)
- FCH initiates SLP_S3B5V high that disables the 5V_S0 rail
- Shut down 5V_S5 (or leave it connected and use PWRBTN# signal for next power up).

Table 21 System signals

Signal Name	Pin #	Type	Description	Availability
SLP_S3B5V	P1-15	OD	Go to (high)/Exit Off (low) standby/hibernate signal	Always available
SYS_RST#	P18-33	IPU	System reset	
SB_PG	P1-16	IPU	Carrier board Power Good	
FCH_PCIE_RST#	P18-20	ODP	Devices reset	
INTRUDER_ALERT#	P18-63	IPU	Intruder detection	
PROCHOT#	P1-106	ODP	APU is overheated and going to shut-down	
PWRBTN#_HW	P18-35	IPD	Power Button signal	

SYS_RST# signal is the main system reset (should be asserted for at least 50msec) that invokes a global reset that affects every functional module on CM-iGT.

FCH_PCIE_RST# signal should be used to reset peripheral devices on CM-iGT and on the carrier board.

5.2 Unconnected Pins

The pins listed below are reserved for future use and must be left unconnected.

Table 22 Reserved Signals

Signal Name	Pin #	Type	Description	Availability
Reserved	P18-40		Leave unconnected	Unavailable
Reserved	P18-68			
Reserved	P18-36			
Reserved	P18-34			
Reserved	P18-70			
Reserved	P18-64			
Reserved	P18-66			
Reserved	P18-32			
Reserved	P18-49			
Reserved	P18-47			
Reserved	P18-53			
Reserved	P18-48			
Reserved	P18-50			
Reserved	P18-45			

5.3 System Boot Options

Following devices can serve as a bootable device for operating system:

- Onboard iSSD
- External hard drive connected to the SATA interface
- USB storage device

The boot order is determined by BIOS setup menu.

5.4 TPM

CM-iGT features an optional TMP module implemented with Atmel AT97SC3204.

6 BASEBOARD INTERFACE

CM-iGT connects to the carrier board through P1 and P18 - 0.6 mm pitch 140-pin connectors.

6.1 Connector Pin-out

Table 23 Connector P1

Pin #	CM-iGT Signal Name	Reference Section		Pin #	CM-iGT Signal Name	Reference Section
P1-1	LAN0_MDIP1	4.2.1		P1-2	LAN0_MDIP0	4.2.1
P1-3	LAN0_MDIN1	4.2.1		P1-4	LAN0_MDIN0	4.2.1
P1-5	LAN0_EEDI_L2	4.2.1		P1-6	LAN0_EESK_L1	4.2.1
P1-7	5V_S0	5.1.1		P1-8	GND	5.1.1
P1-9	LAN0_MDIP3	4.2.1		P1-10	LAN0_MDIP2	4.2.1
P1-11	LAN0_MDIN3	4.2.1		P1-12	LAN0_MDIN2	4.2.1
P1-13	LAN0_TXLED#	4.2.1		P1-14	GND	5.1.1
P1-15	SLP_S3B5V	5.1.2		P1-16	SB_PG	5.1.2
P1-17	FCH_GPIO11	4.10		P1-18	SPDIFO	4.7.1
P1-19	5V_S0	5.1.1		P1-20	SPDIFI	4.7.1
P1-21	DP1_AUX_N	4.1		P1-22	AUD_SENSA	4.7.1
P1-23	DP1_AUX_P	4.1		P1-24	MIN1_R	4.7.1
P1-25	NC			P1-26	GND	5.1.1
P1-27	DP1_TX0_N	4.1		P1-28	DP1_TX3_N	4.1
P1-29	DP1_TX0_P	4.1		P1-30	DP1_TX3_P	4.1
P1-31	5V_S0	5.1.1		P1-32	DP1_HPD	4.1
P1-33	DP1_TX1_N	4.1		P1-34	PCIE_APU_RX0_N	4.3
P1-35	DP1_TX1_P	4.1		P1-36	PCIE_APU_RX0_P	4.3
P1-37	A_VBAT	5.1.1		P1-38	GND	5.1.1
P1-39	PCIE_APU_RX1_N	4.3		P1-40	DP1_TX2_N	4.1
P1-41	PCIE_APU_RX1_P	4.3		P1-42	DP1_TX2_P	4.1
P1-43	5V_S0	5.1.1		P1-44	DP0_HPD	4.1
P1-45	FCH_GPIOD145	4.10		P1-46	LVDS_AUX_EN#	4.1
P1-47	DP0_AUX_P	4.1		P1-48	LVDS_VARY_BL	4.1
P1-49	DP0_AUX_N	4.1		P1-50	GND	5.1.1
P1-51	DP0_TX1_N	4.1		P1-52	DP0_TX2_N	4.1
P1-53	DP0_TX1_P	4.1		P1-54	DP0_TX2_P	4.1
P1-55	5V_S0	5.1.1		P1-56	LVDS_BLON	4.1
P1-57	USB_HS0_P	4.5		P1-58	DP0_TX0_N	4.1
P1-59	USB_HS0_N	4.5		P1-60	DP0_TX0_P	4.1
P1-61	LVDS_DIGON	4.1		P1-62	GND	5.1.1
P1-63	DP0_TX3_N	4.1		P1-64	SIO_GPIO16	4.10
P1-65	DP0_TX3_P	4.1		P1-66	SIO_GPIO17	4.10
P1-67	5V_S0	5.1.1		P1-68	SIO_GPIO30	4.10
P1-69	SIO_GPIO33	4.10		P1-70	SIO_GPIO31	4.10
P1-71	SIO_GPIO34	4.10		P1-72	SIO_GPIO32	4.10
P1-73	SIO_GPIO35	4.10		P1-74	GND	5.1.1
P1-75	USB_FS1_P	4.5		P1-76	PCIE_APU_TX0_P	4.3
P1-77	USB_FS1_N	4.5		P1-78	PCIE_APU_TX0_N	4.3
P1-79	5V_S0	5.1.1		P1-80	5V_S5	5.1.1
P1-81	PCIE_APU_RX2_P	4.3		P1-82	PCIE_APU_TX1_P	4.3
P1-83	PCIE_APU_RX2_N	4.3		P1-84	PCIE_APU_TX1_N	4.3
P1-85	TIN2_GPIO173	4.10		P1-86	GND	5.1.1
P1-87	PCIE_APU_RX3_P	4.3		P1-88	PCIE_APU_TX2_P	4.3
P1-89	PCIE_APU_RX3_N	4.3		P1-90	PCIE_APU_TX2_N	4.3
P1-91	5V_S0	5.1.1		P1-92	FCH_GPIOD146	4.10
P1-93	VGA_R	4.1		P1-94	PCIE_APU_TX3_P	4.3
P1-95	VGA_SCL	4.1		P1-96	PCIE_APU_TX3_N	4.3
P1-97	FCH_GPIOD149	4.10		P1-98	GND	5.1.1
P1-99	VGA_SDA	4.1		P1-100	eSATA_TX0_P	4.4
P1-101	VGA_G	4.1		P1-102	eSATA_TX0_N	4.4
P1-103	5V_S0	5.1.1		P1-104	FNTH_GPIO56	4.10
P1-105	VGA_B	4.1		P1-106	PROCHOT#	5.1.2

P1-107	VGA_VSYNC	4.1		P1-108	FCH_GPIOD147	4.10
P1-109	VGA_HSYNC	4.1		P1-110	GND	5.1.1
P1-111	COM1_DSR	4.9		P1-112	SIO_IR_RXD	4.9
P1-113	COM1_DCD	4.9		P1-114	SIO_IR_TXD	4.9
P1-115	5V_S0	5.1.1		P1-116	FCH_GPIOD147	4.10
P1-117	COM1_RX	4.9		P1-118	eSATA_RX0_N	4.4
P1-119	COM1_TX	4.9		P1-120	eSATA_RX0_P	4.4
P1-121	COM1_RTS	4.9		P1-122	GND	5.1.1
P1-123	COM1_CTS	4.9		P1-124	COM1_RI	4.9
P1-125	COM1_DTR	4.9		P1-126	AZ_SI1_FCH_PG	4.10
P1-127	5V_S0	5.1.1		P1-128	USBOC2#	4.5
P1-129	USB_HS7_N	4.5		P1-130	USB_HS4_N	4.5
P1-131	USB_HS7_P	4.5		P1-132	USB_HS4_P	4.5
P1-133	USBOC3#	4.5		P1-134	GND	5.1.1
P1-135	USB_HS8_N	4.5		P1-136	USB_HS12_N	4.5
P1-137	USB_HS8_P	4.5		P1-138	USB_HS12_P	4.5
P1-139	5V_S0	5.1.1		P1-140	5V_S5	5.1.1

Table 24 Connector P18

Pin #	CM-iGT Signal Name	Reference Section	Pin #	CM-iGT Signal Name	Reference Section
P18-1	LAN1_MDIP1	4.2.2	P18-2	LAN1_MDIP0	4.2.2
P18-3	LAN1_MDIN1	4.2.2	P18-4	LAN1_MDIN0	4.2.2
P18-5	LAN1_EEDI_L2	4.2.2	P18-6	LAN1_EESK_L1	4.2.2
P18-7	GND	5.1.1	P18-8	GND	5.1.1
P18-9	LAN1_MDIP3	4.2.2	P18-10	LAN1_MDIN2	4.2.2
P18-11	LAN1_MDIN3	4.2.2	P18-12	LAN1_MDIN2	4.2.2
P18-13	LAN1_TXLED#	4.2.2	P18-14	GND	5.1.1
P18-15	XB_PCIe_CLKREQ#	4.3	P18-16	FN2PWM_GPIO54	4.10
P18-17	XA_PCIe_CLKREQ#	4.3	P18-18	FCH_GPIO201_S5	4.10
P18-19	5V_S0	5.1.1	P18-20	FCH_PCIE_RST#	5.1.2
P18-21	SCLK0	4.11	P18-22	SPKR	4.7.1
P18-23	SDATA0	4.11	P18-24	SMBALERT#	4.11
P18-25	SDATA2	4.11	P18-26	GND	5.1.1
P18-27	SCLK2	4.11	P18-28	TMR0_GPIO197	4.10
P18-29	FNTH2_GPIO58	4.10	P18-30	TMR1_GPIO198	4.10
P18-31	5V_S0	5.1.1	P18-32	Reserved	5.2
P18-33	SYS_RST#	5.1.2	P18-34	Reserved	5.2
P18-35	PWRBTN#_HW	5.1.2	P18-36	Reserved	5.2
P18-37	IRRX1_GEVENT20#	4.10	P18-38	GND	5.1.1
P18-39	USB_HS1_P	4.5	P18-40	Reserved	5.2
P18-41	USB_HS1_N	4.5	P18-42	GPIO202_FCS#	4.10
P18-43	5V_S0	5.1.1	P18-44	GPIO205_FCK	4.10
P18-45	Reserved	5.2	P18-46	FCH_GPIO204_S5	4.10
P18-47	Reserved	5.2	P18-48	Reserved	5.2
P18-49	Reserved	5.2	P18-50	Reserved	5.2
P18-51	Reserved	5.2	P18-52	GND	5.1.1
P18-53	Reserved	5.2	P18-54	eSATA_TX1_P	4.4
P18-55	5V_S0	5.1.1	P18-56	eSATA_TX1_N	4.4
P18-57	FCH_GPIO13	4.10	P18-58	eSATA_RX1_N	4.4
P18-59	IRRX0_GEVENT16#	4.10	P18-60	eSATA_RX1_P	4.4
P18-61	IRTX0_GEVENT17#	4.10	P18-62	GND	5.1.1
P18-63	INTRUDER_ALERT#	5.1.2	P18-64	Reserved	5.2
P18-65	CAN_TX	4.6	P18-66	Reserved	5.2
P18-67	5V_S0	5.1.1	P18-68	Reserved	5.2
P18-69	CAN_RX	4.6	P18-70	Reserved	5.2
P18-71	5V_S5	5.1.1	P18-72	PCI_CLK3	4.8
P18-73	AZ_SI2_GPIO169	4.10, 4.7.2	P18-74	GND	5.1.1
P18-75	USB_HS3_N	4.5	P18-76	eSATA_TX2_P	4.4
P18-77	USB_HS3_P	4.5	P18-78	eSATA_TX2_N	4.4
P18-79	5V_S0	5.1.1	P18-80	FNTH1_GPIO57	4.10
P18-81	XA_PCIE_CLK_N	4.3	P18-82	eSATA_RX2_N	4.4
P18-83	XA_PCIE_CLK_P	4.3	P18-84	eSATA_RX2_P	4.4
P18-85	AZ_SI3_GPIO170	4.10, 4.7.2	P18-86	GND	5.1.1
P18-87	LFRAME#	4.8	P18-88	LPC_CLK0	4.8
P18-89	SERIRQ_GPIO48	4.8	P18-90	LAD0	4.8
P18-91	5V_S0	5.1.1	P18-92	LAD1	4.8
P18-93	SB_SATA_TX1_N	4.4	P18-94	LAD2	4.8

P18-95	SB_SATA_TX1_P	4.4	P18-96	LAD3	4.8
P18-97	5V_S5	5.1.1	P18-98	GND	5.1.1
P18-99	XB_PCIE_CLK_N	4.3	P18-100	SB_SATA_RX1_N	4.4
P18-101	XB_PCIE_CLK_P	4.3	P18-102	SB_SATA_RX1_P	4.4
P18-103	5V_S0	5.1.1	P18-104	FCH_PCIE_RST#	5.1.2
P18-105	PCIE_FCH_RX3_N	4.3	P18-106	PCIE_FCH_RX2_N	4.3
P18-107	PCIE_FCH_RX3_P	4.3	P18-108	PCIE_FCH_RX2_P	4.3
P18-109	PCIE_WAKE_UP#	4.3	P18-110	GND	5.1.1
P18-111	PCIE_FCH_TX3_N	4.3	P18-112	PCIE_FCH_TX2_N	4.3
P18-113	PCIE_FCH_TX3_P	4.3	P18-114	PCIE_FCH_TX2_P	4.3
P18-115	5V_S0	5.1.1	P18-116	5V_S5	5.1.1
P18-117	AZ_SDATA_IN0	4.7.2	P18-118	SB_SATA_RX0_N	4.4
P18-119	AZ_BITCLK	4.7.2	P18-120	SB_SATA_RX0_P	4.4
P18-121	AZ_RST#	4.7.2	P18-122	GND	5.1.1
P18-123	AZ_SDOUT	4.7.2	P18-124	SB_SATA_TX0_N	4.4
P18-125	AZ_SYNC	4.7.2	P18-126	SB_SATA_TX0_P	4.4
P18-127	5V_S0	5.1.1	P18-128	HDD_ACT#	4.4
P18-129	MIN1_L	4.7.1	P18-130	USB_HS13_N	4.5
P18-131	LIN1_R	4.7.1	P18-132	USB_HS13_P	4.5
P18-133	LIN1_L	4.7.1	P18-134	GND	5.1.1
P18-135	5V_S0	5.1.1	P18-136	USBOC6#	4.5
P18-137	LOUT_R	4.7.1	P18-138	USB_HS5_N	4.5
P18-139	LOUT_L	4.7.1	P18-140	USB_HS5_P	4.5

6.2 Connector Type

Table 25 Connector type

Part Reference	Mfg.	CM-iGT connector P/N	Baseboard (mating) connector P/N
P1, P18	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab. For further details, please refer to http://compulab.co.il/support/cables-connectors-accessories/.

CompuLab P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 2 CM-iGT Top (dimensions are in mm)

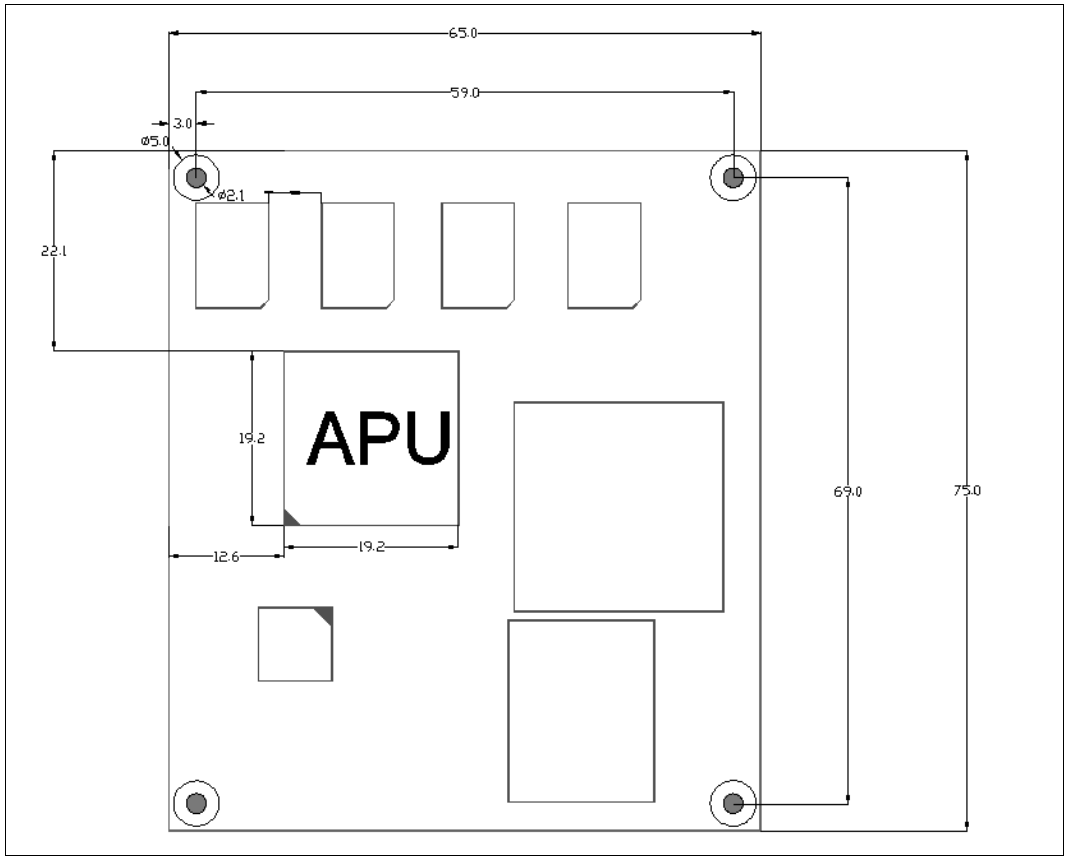
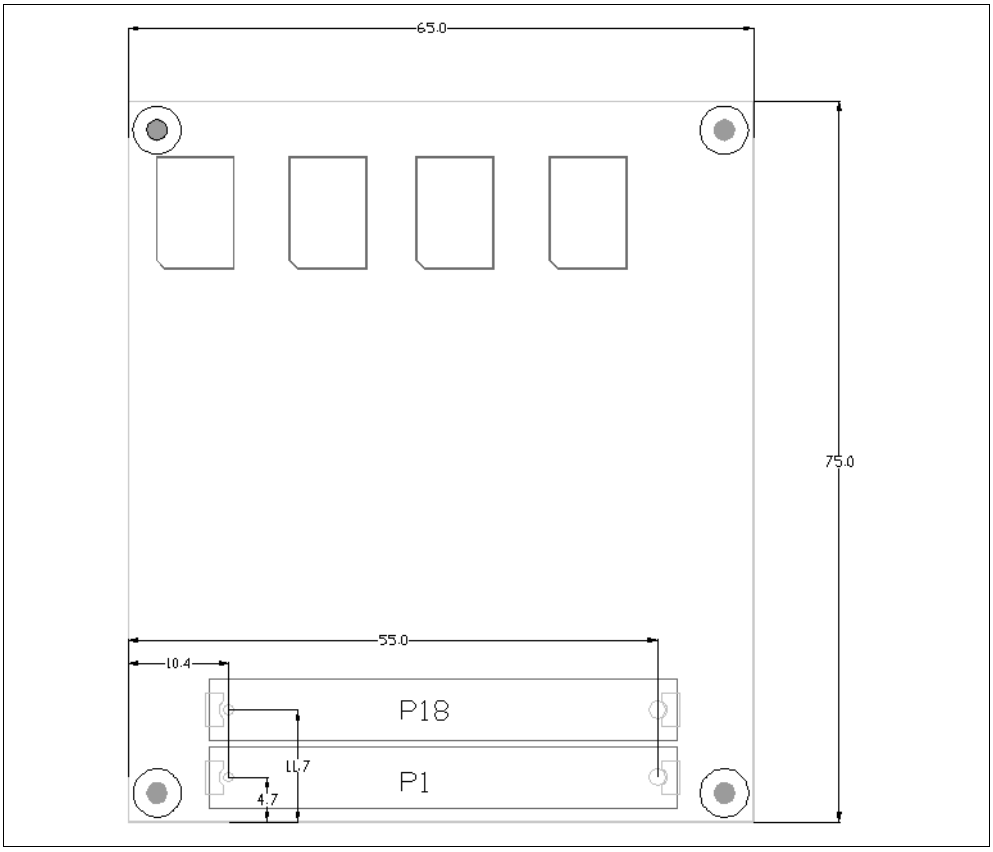


Figure 3 CM-iGT bottom (in mm; X-Ray view - as seen from top side)



1. All dimensions are in millimeters.
2. Height of all components is <3mm.
3. Baseboard connectors provide 4mm board-to-board clearance.
4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format at https://compulab.co.il/products/computer-on-modules/cm-igt/#devres.

6.4 Standoffs

CM-iGT features four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 26 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 27 Absolute Maximum ratings

Parameter	Min	Typ	Max	Unit
Main power supply voltage (5V_S0 / 5V_S5)	-0.3		6.0	V
A_VBAT	-0.3		4.0	V

7.2 Recommended Operating Conditions

Table 28 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (5V_S0 / 5V_S5)	4.75	5.0	5.25	V
RTC backup battery voltage (VCC_RTC)	2.2	3.3	3.45	V

7.3 DC Electrical Characteristics

Table 29 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
3.3V Digital I/O					
V_{IH}		2		3.6	V
V_{IL}		-0.3		0.8	V
V_{OH}		2.4			V
V_{OL}				0.4	V
I^2C (open drain with internal pull up to 3.3V)					
V_{IH}		2.3		3.8	V
V_{IL}		-0.5		1.0	V
V_{OL}	IOL = 3 mA	-		0.4	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing				±25	V

7.4 Power Consumption

To be added in a future revision of this document.

7.5 ESD Performance

Table 30 ESD Performance

Interface	ESD Performance
RS232	±15 kV ESD using HBM

7.6 Thermal Characteristics

To be added in a future revision of this document.

7.7 Operating Temperature Ranges

The CM-iGT is available with three options of operating temperature range.

Table 31 CM-iGT Temperature Range Options

Range	Temp.	Description
Commercial	0° to 70° C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20° to 70° C	Every board undergoes a short test for the lower limit (-20° C) qualification.
Industrial	-40° to 85° C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Baseboard Design Guidelines

- Ensure that all 5V_S0, 5V_S5 and GND power pins are connected.
- Major power rails - 5V_S0, 5V_S5 and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system's signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between 5V_S0 and GND and 5V_S5and GND near the mating connectors.
- It is recommended to connect the standoff holes of the baseboard to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-iGT operation. All power-up circuitry and all required pull-ups/pull-downs are present on the module.
- If for some reason you decide to place an external pull-up or pull-down resistor on a certain signal (for example - on the GPIO's), first check the documentation of that signal provided in this manual. Certain signals have on-board pull-up/pull-down resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
    - PCI Express, SATA, Ethernet and USB signals must be routed in differential pairs and by a controlled impedance trace.
    - Audio input must be decoupled from possible sources of baseboard noise.
- Be careful when placing components under the CM-iGT module. The baseboard interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-iGT. Maximum allowable height for components placed under the CM-iGT is 1mm.
- Refer to the SB-iGT baseboard reference design schematics.

8.2 Baseboard Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the baseboard. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the 5V_S0 and 5V_S5 power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
    - Devices improperly driving the local bus

- External pull-up/pull-down resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the baseboard, shorting them on the connectors can disable the module. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often, solder bridges are deep beneath the connector's body. Note that solder shorts are the most frequent factor disabling module operation.
- Check possible signal shorts due to errors of baseboard PCB design or assembly.
- Improper functioning of a custom baseboard can accidentally delete the CM-iGT boot-up code or even damage the module hardware permanently. Before each activation attempt, check that your module is still functional with a CompuLab SB-iGT baseboard.
- It is recommended to assemble more than one baseboard for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetic modules. Designers should test and qualify magnetic modules before using them in an application.

Table 32 Compatible Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
Speed Tech	P65-101-[1|2]AK9	Integrated RJ45
Pulse Engineering	H5007	16-pin SOIC
Pulse Engineering	H1251	16-pin SOIC

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-iGT reference design schematics.

8.4 Heat-plate Integration

To be added in a future revision of this document.