SBC-QS600

Technical Reference Manual

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Table 1 Document Revision Notes

Date	Description
September 2014	• First release
November 2014	• Added description for RTC backup battery connector (P15)

1 INTRODUCTION

1.1 About This Document

This document is part of a set of documents providing information necessary to operate and program Compulab SBC-QS600.

1.2 Related Documents

For additional information not covered in this manual, please refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
SBC-QS600 Resources	https://compulab.co.il/products/sbcs/sbc-qs600/

2 OVERVIEW

2.1 Highlights

SBC-QS600 is a fully functional miniature computer based on the Qualcomm® Snapdragon™ 600 processor (APQ8064) SoC – a quad-core Krait™ 300 CPU with an Adreno™ 320 GPU, products of Qualcomm Technologies Inc., and integrated multimedia acceleration engines.

The device enables versatile connectivity through a variety of peripheral interfaces – Gigabit Ethernet port, 802.11n WiFi, Bluetooth 4.0, I2C, SPI, UART and high-speed USB.

SBC-QS600 is designed into a miniature form-factor with unprecedentedly low-power envelope, while providing rich multimedia capabilities and PC-like user experience.

High performance, low-power, rich I/O and miniature rugged design, position SBC-QS600 as an attractive solution for a wide range of applications – media player, IPTV, infotainment system, signage, gaming or even desktop replacement.

2.2 Specifications

Table 3 System

Feature	Specifications
CPU	Qualcomm Snapdragon 600 APQ8064 quad-core Krait 300, 1.7GHz NEON SIMD and VFPv4
Memory	Up to 2 GB, DDR3-1066, 64 bit bus width
Storage	mSATA SSD, up to 512GB
	Micro-SD SDXC, up to 128GB
	eMMC up to 32GB

Table 4 Display and Graphics

Feature	Specifications
GPU	Adreno 320 GPU compliant with OpenGL ES 1.1 / 2.0 / 3.0 and OpenCL 1.2 and DirectX11
Primary Display	HDMI 1.4 up to 1920 x 1200 @ 60Hz
Secondary Display	LVDS, up to 2048x1536@ 60Hz, FPC connector

Table 5 Network

Feature	Specifications
LAN	1000 BaseT Ethernet port
WiFi	802.11b/g/n Wi-Fi, dual band, dual antenna
Bluetooth	Bluetooth 4.0 (low power)

Table 6 I/O

Feature	Specifications
Audio	Stereo line-out, stereo line-in and microphone, 3.5mm audio jacks
USB	Four USB 2.0 high-speed ports, standard A-type connectors, max current 1A per port
	USB OTG micro-USB connector
Serial	Two UART ports, one USB CDC port on mini USB connector and one UART port on 100 mil header.
I2C	Thee I2C port over 100 mil header
SPI	One SPI port over 100 mil header
GPIO	6 GPIOs over 100 mil header

Table 7 Mechanical and Environmental

Supply Voltage	Unregulated 8V to 15V High efficiency switched power supply
Power consumption	3W to 9W in full activity, depending on system configuration and load
Dimensions	81mm x 81mm x 24mm
Weight	
Operation temperature	0C – 70C

3 CORE SYSTEM COMPONENTS

3.1 Snapdragon 600 processor (APQ8064)

3.1.1 Quad core Krait CPU

Snapdragon 600 (APQ8064) based SoC is a multimedia application device featuring Snapdragon 600 processor, video, image and graphics processing for a broad range of multimedia-rich applications. The device is composed of the following major subsystems:

- Four Krait application processors – advanced CPU architecture for high-end multimedia applications:
  - Up to 1.7 GHz core speed
  - 2 MB L2 cache (combined)
  - ARM v7 compliant
  - TrustZone support
  - VeNum 128-bit SIMD multimedia coprocessor and VFPv4
- Adreno 320 GPU
- Video playback and capture sub-system
- QDSP6 core (500 MHz) for application support
- ARM9 for WLAN/BT/FM processing
- ARM7 for smart peripheral sub-system processing

3.1.2 Video subsystems

The SBC-QS600 video graphics subsystem consists of the following APQ8064 sub-blocks.

- MDP 4.4
- 1080p encode and decode at up to 60 fps
- H.263, H.264, MP4

3.1.3 Graphics subsystems

SBC-QS600 incorporates powerful Adreno 320 GPU, optimized specifically for a mobile applications screen size and color depth using low-power, high-performance processing

- 200 M peak triangles/second
- 6.4 B vector shader instructions/second
- 3.2 BP/second; 3.2 B texel/second
- APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
- Direct 3D mobile, flash10-pixel blender acceleration
- 325 MHz and 400 MHz turbo mode

3.2 System Memory

3.2.1 DRAM

SBC-QS600 features up to a 2GB of on-board dual-channel DDR3 memory. Each DDR channel is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

3.3 System Storage

3.3.1 mSATA

SBC-QS600 features an internal mSATA socket supporting standard mSATA SSD devices of up-to 512GB. mSATA functionality is implemented with the APQ8064 integrated SATA controller and PHY. The following main features are supported:

- SATA 1.5 Gb/s
- Power management features including automatic partial-to-slumber transition
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries

3.3.2 Micro-SD

SBC-QS600 features micro-SD socket supporting SDXC cards of up-to 128GB on APQ8064 SDC-3 interface.

3.3.3 eMMC

SBC-QS600 features eMMC storage up to 32GB on APQ8064 SDC-1 interface.

3.4 Display Subsystem

3.4.1 HDMI

SBC-QS600 HDMI output is based on the HDMI TX & HDMI PHY integrated into the APQ8064 SoC. APQ8064 HDMI subsystem features a dedicated HDMI DDC. HDMI_DETECT signal is connected to the APQ8064 HDMI_HPD input. HDMI signals are routed to the primary display output HDMI connector J1. The HDMI output supports resolutions of up to 1920 x 1080 @ fps.

3.4.2 LVDS

SBC-QS600 is equipped with LVDS display interface. The LVDS display interface is derived from the APQ8064 MDP4.4 subsystem. LVDS interface and routed to the FPC connector P8. LVDS output supports resolutions of up to 2048x1536.

3.5 Audio Subsystem

3.5.1 Analog Audio

SBC-QS600 analog audio functionality is implemented by interfacing the Qualcomm WCD9311 audio codec with APQ8064 slimBUS port. The Qualcomm WCD9311 supports the following features:

- Stereo output –headphone left and right
- 110 dB (typical) headphone SNR
- Stereo single-ended headphone outputs (16 or 32 Ω): Capless, class G, 63 mW into 16Ω (each)
- 4 mW stereo playback at a 48 kHz sample rate
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz

For more information please refer to WCD9311 Device Specification 80-N1764-1 document. Analog line output is routed to the audio jack P4. Analog line input is routed to the audio jack P6.

Table 8 Analog Audio Characteristics

Parameter		Comments	Min	Typ	Max	Unit
Stereo Headphone Output - 8 kHz; 16 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	68	72		dB
	PCMI=-60 dBFS		36	38		
Stereo Headphone Output - 48 kHz; 16 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	84	89		dB
	PCMI=-60 dBFS		38	40		
Stereo Headphone Output - 48 or 192 kHz; 24 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	84	89		dB
	PCMI=-60 dBFS		38	44		

Parameter		Comments	Min	Typ	Max	Unit
Stereo Headphone Output - Other characteristics						
Full-scale output voltage		f = 1.02 kHz, 0 dB FS; 16 Ω load	0.65	0.69	0.73	Vrms
Output power f = 1.02 kHz, 0 dB FS		16 Ω load	26.4	29.7	33.3	mW
		32 Ω load	25.8	29.4	33.1	
Output load		16 Ω nominal	13	16	50000	Ω
		32 Ω nominal	26	32	50000	
Power supply rejection:	0 kHz < f < 1 kHz	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS	80	90		dB
	1 kHz < f < 5 kHz		70	80		
	5 kHz < f < 20 kHz		60	70		
Output DC offset			-0.81	0	0.81	mV
Line Input to ADC						
Full-scale input voltage			-0.5	0	0.5	dBv
Absolute gain error		-20 dBv input level, 1.02 kHz	-0.5		0.5	dB
Power supply rejection:	0 kHz < f < 1 kHz	100 mVpp square wave imposed on power supply; analog input = 0 Vrms	51	56		dB
	1 kHz < f < 5 kHz		51	56		
	5 kHz < f < 20 kHz		51	56		
Interchannel isolation		20 < f < 20 kHz; IN_1 terminated with 1 k Ω; IN_2 = -5 dBFS at 1 kHz	90	100		dB
Rx to Tx cross-talk attenuation		Tx path measurement with -5 dBFS Rx path signal. f = 1 kHz	90	100		dB
Mute attenuation		0dB, 1 kHz input tone		80		dB
Input resistance		All gain modes	16	20	24	kΩ
Input capacitance				15		pF
Microphone Input to ADC						
Input referred noise				9.2	11.5	uVrms
SNR			90	93		dB
Dynamic range, (see Note 3)		A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion		Input level = -1 dBV		86	91	dB
		Input level = -60 dBV		34	41	
Microphone Bias						
Bias voltage			1.7		2.85	V
Bias-current source					3	mA
Output noise		0.1 µF bypass	0.5	2.0	3.0	uVrms

3.6 USB Subsystem

3.6.1 USB 2.0 Host

SBC-QS600 high-speed USB interfaces are implemented with APQ8064 high-speed USB host ports 3 and 4. The interface supports the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation
- Complies with EHCI (high-speed host controller)

SBC-QS600 enables 5 USB Host ports by utilizing an on-board USB2.0 hub connected to APQ6084 USB port 3. Three of the HUB's USB2 ports are routed to the P13 to P14 dual head connectors. APQ8064 USB 2 host port 4 is routed directly to P13 lower socket. The fourth port of the USB 2 hub is routed to mini-PCIe socket P12.

3.6.2 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the APQ8064 USB 2.0 port 1 and OTG controller. USB OTG is routed to P17 connector. The interface provides the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation in host mode
- Supports USB 2.0 High Speed (480 Mbps) and Full Speed (12 Mbps) operation in peripheral mode.
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol

The USB selector path is controlled with the APQ8064 USB1_HS_ID signal.

3.7 Wireless Interfaces

SBC-QS600 features 802.11b/g/n and Bluetooth 4.0 wireless connectivity solution, implemented by interfacing the Qualcomm QCA6234X WLAN + Bluetooth combo controller module with the APQ8064 WLSDIO (SDC-4) interface.

Two stream (2x2) 802.11n provides highest throughput and superior RF performance for handheld devices:

- 40MHz channels at 5GHz
- Half Guard Interval for high throughput
- Frame Aggregation for high throughput
- Space Time Block Coding (STBC) Rx for improved downlink robustness over range
- Low Density Parity Check (LDPC) encoding for improved uplink and downlink robustness over range
- Maximum Ratio Combining (MRC)
- Maximum Likelihood (ML) Decoder
- Frame Aggregation (A-MPDU) processing
- De-capsulation of the 802.11 frame to 802.3 frame
- Bluetooth low energy (BT4.0) ready
- Class 1.5 Bluetooth with integrated Tx/Rx switch.
- Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence

3.8 Ethernet

SBC-QS600 features a single Gigabit Ethernet port.

3.8.1 Ethernet Controller

SBC-QS600 incorporates a full-featured Gigabit Ethernet interface. The interface is implemented with Atheros AR8151-B controller connected to the APQ8064 PCIe interface. The Gigabit interface is routed to connector P3.

The SBC-QS600 Ethernet interface supports the following main features:

- Integrated PHY for 10/100/1000 Mbps
- IEEE 802.3 Auto-Negotiation support.
- IEEE 802.3ab PHY compliance and compatibility
- Supports automatic MDI/MDIX functions
- Cable Diagnostic Test (CDT) for open, short cable, cable length detection, and incorrect or mismatched impedance
- IEEE 802.3az support
- IEEE 802.3x compliant flow control support
- Interrupt coalescing
- PHY support for HP Auto-MDIX
- Activity and speed indicator LED controls
- Descriptor ring management for Tx/Rx
- IPv4 and IPv6 support
- 802.3u support
- IEEE 802.1Q VLAN feature
- Jumbo frame support
- Automatic polarity correction
- Media Access Control

3.9 UART

The SBC-QS600 features up to a two UART ports.

UART7 port is used as a debug interface. It's derived from the APQ8064 GSBI7 interface and converted to USB CDC via UART2USB bridge. The USB CDC debug port is routed to P16.

UART4 port is featured on APQ8064 GSBI4 interface, and routed to 100 mil header P9.

The UART ports support the following features:

- High-speed UART operation up to 4 Mbps and medium data-rate IrDA operation up to 1.152 Mbps.
- Rate-controlled data mover with separate CRCI channels for Rx and Tx
- Larger Rx and Tx FIFOs that are implemented in one SRAM
- EIA RS232-C standard

3.10 I2C

SBC-QS600 features up to three general purpose I^2C interfaces via GSBI3, GSBI4 and GSBI5 ports. The following features are supported:

- Two-wire bus for inter-IC communications supporting any IC fabrication process
- Each device is recognized by a unique address, and can operate as either a transmitter or receiver, depending on the device function
- The I2C controller provides an interface between the CPSS fast peripheral bus (FPB), an advanced high-performance bus (AHB), and the industry-standard I2C serial bus
- It is I2C-compliant, high-speed mode (HS-mode)-compliant, and a master-only device
- Clock speed is 384 kHz
- I2C pins use GPIOs configured as open-drain outputs; the pullup resistor is provided by the slave
- Camera auto-focus control via I2C originates with the aDSP; a separate hardware request port is required at the I2C controller.

The I2C ports are routed to 100-mil header P9

3.11 SPI

SBC-QS600 features an SPI port over APQ8064 GSBI4 interface. SPI port supports the following main features:

- 4-bit synchronous serial data link.
- Master and slave mode supported
- Up to 52 MHz in both master and slave mode
- Master device initiates data transfers; multiple slave devices are supported by using chip selects
- No explicit communication framing, error checking, or defined data word lengths, so the transfers are strictly at the raw bit level
- As SPI master, the core supports several SPI system configurations (as defined by the SPI protocol):
  - Configurations 1, 2, 4, and 5 are supported, though configurations 4 and 5 are software dependent
  - Configuration 3 and the multi-master configuration are not supported

The SPI ports are routed to 100-mil header P9

3.12 GSBI

SBC-QS600 features an APQ8064 GSBI4 port over P9 100-mil header. GSBI is a connectivity port that can function as UART, SPI, I2C or GPIO. GSBI4 is four bits wide: GSBI4 [3:0] and can be configured by software.

GSBI3 and GSBI5 ports are dedicated to I2C interfaces in SBC-QS600 and should not be alternated by software.

Table 9 GSBI Options

#	Configuration	GSBI bit 3	GSBI bit 2	GSBI bit 1	GSBI bit 0
1	4-pin UART	UART_TX O	UART_RX I	UART_CTS I	UART_RFR O
2	4-pin SPI	SPI_DATA_MOSI IO	SPI_DATA_MISO IO	SPI_CS_N IO	SPI_CLK IO
3	3-pin UIM + 1 GPIO	UIM_DATA IO UIM data	UIM_CLK O UIM clock	UIM_RESET_N O UIM reset	GPIO_XX IO Configurable I/O
4	2-pin I2C + 2-pin UART	UART_TX O 2-pin UART TX	UART_RX I 2-pin UART RX	I2C_SDA IO I2C serial data	I2C_SCL IO I2C serial clock
5	UIM + I^2C	UIM_DATA IO UIM data	UIM_CLK O UIM clock	I2C_SDA IO I2C serial data	I2C_SCL IO I2C serial clock
6	4 GPIOs	GPIO_XX	GPIO_XX IO	GPIO_XX IO	GPIO_XX IO

4 SYSTEM LOGIC

4.1 Power Subsystem

4.1.1 Power Rails

SBC-QS600 is powered with a single 12V power supply.

Table 10 Power signals

Signal Name	Type	Description
+12V	P	Main power supply. Typical voltage – 12V.
5V	P	Core components power supply
3V3	P	Peripherals power supply
1V8	P	Core logic reference power supply
V3_COIN	P	RTC back-up battery power input. Connected to a 3V coin-cell lithium battery.
GND	P	Common ground.

4.1.2 Power Modes

The SBC-QS600 supports three hardware power modes.

Table 11 Power modes

Power Mode	Description
ON	All internal power rails are enabled. Mode entered automatically when main power supply is connected.
LPM	TBD
OFF	All internal power rails except those required for the power management logic are switched off.

4.1.3 RTC Back-Up Battery

The SBC-QS600 features an external 38mAh coin cell lithium battery, which maintains the SBC-QS600 RTC whenever the main power supply is not present. The battery is connected to connector P15.

4.2 Firmware Boot Options

The SBC-QS600 standard boot sequence provides the following boot options:

- Boot from the on-board eMMC using the SDC-1 interface – default boot device.
- Boot from an external SD card using the SDC-3 interface – alternative boot device.

The standard boot sequence is designed for normal system operation with the on-board eMMC flash as the boot media. If an external SD card presents in the Micro SD P5 socket, the system will try to boot from the card. Such configuration allowing to perform recovery/upgrade routine of the on-board boot media.

NOTE: The recovery-boot only affects the boot process. O/S and file-system boot configuration is determined by the boot-loader settings.

4.3 Real Time Clock

The SBC-QS600 RTC is implemented with the PMM8920 (PM8921) RTC subsystem that provides clock and calendar information to the system. PMM8920 is connected to the SSBI_PMIC1 port of the APQ8064 SoC. The RTC backup battery keeps the RTC running to maintain clock and time information whenever the main SBC-QS600 power supply is not present.

5 INTERFACES AND CONNECTORS

5.1 HDMI Connector (J1)

The primary HDMI display output is provided through the standard HDMI socket (J1).

For additional details, please refer to section 3.4.1 of this document.

Table 12 J1 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	HDMI_TXD2+	11	GND
2	GND	12	HDMI_TXC-
3	HDMI_TXD2-	13	NC
4	HDMI_TXD1+	14	NC
5	GND	15	HDMI_DDC_SCL
6	HDMI_TXD1-	16	HDMI_DDC_SDA
7	HDMI_TXD0+	17	GND
8	GND	18	HDMI_5V
9	HDMI_TXD0-	19	HDMI_DETECT
10	HDMI_TXC+		

5.2 LVDS Connector (P8)

The LVDS display output is provided through the FPC connector P8.

For additional details, please refer to section 3.4.2 of this document.

Table 13 J1 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	GND	13	GND
2	LVDS_TX0_N	14	LVDS_TX3_N
3	LVDS_TX0_P	15	LVDS_TX3_P
4	GND	16	3V3
5	LVDS_TX1_N	17	3V3
6	LVDS_TX1_P	18	NC
7	GND	19	NC
8	LVDS_TX2_N	20	PMIC_MPP_8821_9
9	LVDS_TX2_P	21	3V3
10	GND	22	3V3
11	CLK_170M_0_LVDS_P	23	100K PD
12	CLK_170M_0_LVDS_N	24	3V3

5.3 DC Power Jack (J3)

DC power input connector.

Table 14 J3 connector pin-out

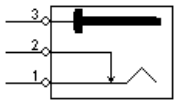
Pin	Signal Name	
1	GND	
2	GND	
3	VIN_12V	

Table 15 J3 connector data

Manufacturer	Mfg. P/N
Contact Technology	DC-022

The connector is compatible with the SBC-QS600 power supply unit available from CompuLab.

5.4 Micro-SD Socket (P5)

The micro-SD socket (P5) is connected directly to the APQ8064 SDC-3 port.

For additional details, please refer to section 3.3.2 of this document.

Table 16 P5 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	SDIO3_DAT2	5	SDIO3_CLK
2	SDIO3_DAT3	6	GND
3	SDIO3_CMD	7	SDIO3_DAT0
4	VDD_3V3	8	SDIO3_DAT1

5.5 uSIM Socket (P11)

The uSIM slot (P11) is connected to mPCIe socket's (P12) pins 8, 10, 12, 14 and 16. On board uSIM slot can be utilized to host uSIM, card when the used mPCIe data modem lacks such slot.

Table 17 P9 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	SIM_VCC	5	GND
2	SIM_RST	6	SIM_VPP
3	SIM_CLK	7	SIM_IO
4	NC	8	NC

5.6 Audio Jacks (P4, P6)

The SBC-QS600 features two 3.5mm jacks. The analog audio signal pin-outs are compatible with standard 3-pole audio cables. CDC_IN2_P signal on P4-2 pin is used for microphone input. For additional details, please refer to section 3.5.1 of this document.

Table 18 P4 connector pin-out

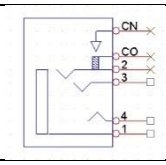
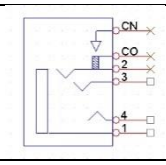
Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	CDC_IN2_P		
3	AUDIO_OUT_R		
4	AUDIO_OUT_L		

Table 19 P6 connector pin-out

Pin	Signal Name	Jack pin-out	Mating plug
1	AUDIO_GND		
2	NC		
3	AUDIO_IN_R		
4	AUDIO_IN_L		

5.7 USB Host Connectors (P13, P14)

The SBC-QS600 external USB2.0 host ports are available through four standard dual head type-A USB connectors (P13 and 14). For additional details, please refer to section 3.6.1 of this document.

Table 20 P13 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	VCC_USB_3	3	USBHUB_P3_DP
2	USBHUB_P3_DM	4	GND
5	VCC_USB_4	7	USBHUB_P4_DP
6	USBHUB_P4_DM	8	GND

Table 21 P14 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	VCC_USB_1	3	USBHUB_P1_DP
2	USBHUB_P1_DM	4	GND
5	VCC_USB_2	7	USBHUB_P2_DP
6	USBHUB_P2_DM	8	GND

5.8 USB OTG Connector (P7)

The APQ8064 USB OTG port is routed to the micro-USB connector P7. For additional details, please refer to section 3.6.2 of this document.

Table 22 P7 connector pin-out

Pin	Signal Name
1	VBUS_OTG
2	USB_DEV_DM
3	USB_DEV_DP
4	OTG_ID
5	GND

5.9 Primary Gigabit Ethernet Connector (P3)

The SBC-QS600 Gigabit Ethernet port is routed to the standard RJ-45 connector (P3). For additional details, please refer to section 3.8.1 of this document.

Table 23 P3 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	LAN_MDIP0	7	LAN_MDIP2
2	LAN_MDIN0	8	LAN_MDIN2
3	LAN_MDIP1	9	LAN_MDIP3
4	LAN_MDIN1	10	LAN_MDIN3
5	LAN_CT1		
6	LAN_CT2		

5.10 mSATA Socket (P2)

The SATA output signals are routed to mSATA connector P2. The mSATA connector is utilized for the SBC-QS600 internal SATA storage. For additional details, please refer to section 3.3.1 of this document.

Table 24 P2 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	GND	27	GND
2	3V3	28	NC
3	NC	29	GND
4	GND	30	VDD_5V
5	NC	31	SATA_TXN
6	NC	32	NC
7	NC	33	SATA_TXP
8	NC	34	GND
9	GND	35	GND
10	NC	36	NC
11	NC	37	GND
12	NC	38	NC
13	NC	39	3V3
14	NC	40	GND
15	GND	41	3V3
16	NC	42	NC
17	NC	43	NC
18	GND	44	NC

19	NC	45	NC
20	NC	46	NC
21	GND	47	NC
22	NC	48	NC
23	SATA_RXP	49	NC
24	3V3	50	GND
25	SATA_RXN	51	NC
26	GND	52	3V3

5.11 mini-PCIe Socket (P12)

The USB2 hub downstream port #4 and uSIM signals are routed to mini-PCIe connector P2. The mini-PCIe connector can be used to host cellular data modem with USB interface, or any other mini-PCIe card with USB interface.

Table 25 P12 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	RESERVED	27	GND
2	3V3	28	RESERVED
3	NC	29	GND
4	GND	30	I2C5_SCL
5	NC	31	RESERVED
6	NC	32	I2C5_SDA
7	RESERVED	33	RESERVED
8	SIM_VCC	34	GND
9	GND	35	GND
10	SIM_IO	36	USB_DM
11	RESERVED	37	GND
12	SIM_CLK	38	USB_DP
13	RESERVED	39	3V3
14	SIM_RST	40	GND
15	GND	41	3V3
16	SIM_VPP	42	NC
17	NC	43	NC
18	GND	44	NC
19	NC	45	NC
20	NC	46	NC
21	GND	47	NC
22	RESERVED	48	RESERVED
23	RESERVED	49	NC
24	3V3	50	GND
25	RESERVED	51	NC
26	GND	52	3V3

5.12 Expansion 100-mil header (P9)

Table 26 P9 connector pin-out

Pin	Signal Name	Pin	Signal Name
1	GSBI4_0	2	I2C5_SCL
3	GSBI4_1	4	I2C5_SDA
5	GSBI4_2	6	I2C3_SCL
7	GSBI4_3	8	I2C3_SDA

5.13 Power Button (SW2)

SBC-QS600 power button SW2 controls the system power state. The table below describes the button functions.

Table 27 Power button functions

User action	System state	System behavior
Short press	OFF	Power on.
Short press	Sleep	Wake Up
Short press	ON	Notify the O/S of a shut-down request / Screen off
Mid press (> 5sec)	ON	Android power button menu
Long press (>15 sec)	ON	System reset

For additional details, please refer to section 4.1.2 of this document.

5.14 RTC Backup Battery Connector (P15)

Connector P15 is used to connect the RTC backup battery to SBC-QS600. The RTC backup battery is required to maintain RTC timekeeping whenever the main SBC-QS600 power supply is not present.

Table 28 P15 connector pin-out

Pin	Signal Name
1	GND
2	3V

Table 29

Manufacturer	Mfg. P/N
Molex	53261-0271

5.15 Indicator LED (DS1)

The table below describes SBC-QS600 indicator LED.

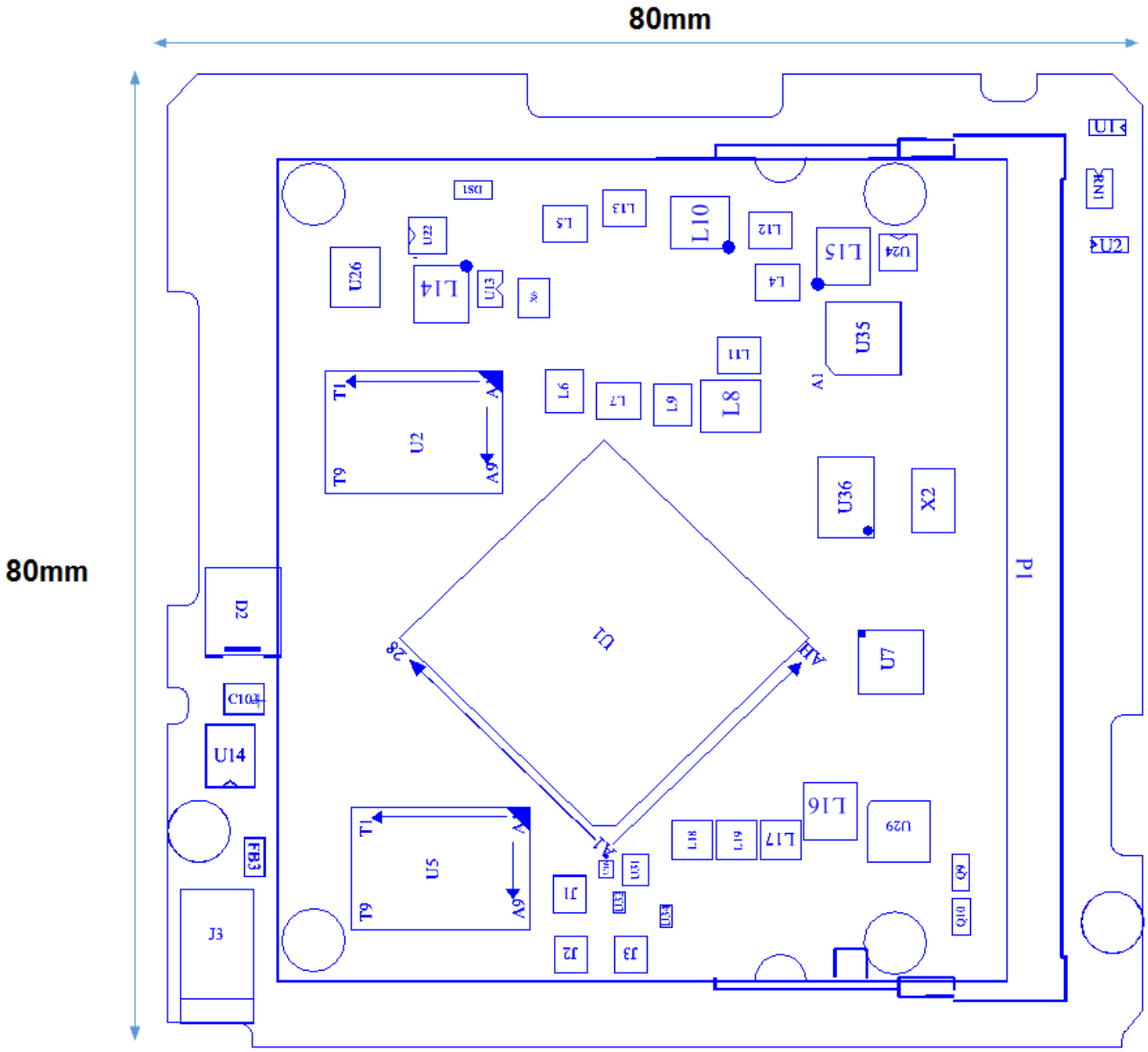
Table 30 DS1 Dual Color LED description

Power state	Color	
	Green	Orange
On	TBD	TBD
Standby	TBD	TBD
Off	TBD	TBD

6 MECHANICAL DRAWINGS

6.1 Dimensions

Top



Bottom


80mm
80mm
P6
P7
P14
P5
SW2
SP1
F13
Q7
Q16
P8
F10
F9
SW1
SW3
P2
E1
P11
U16
P12
P9
L23
P15
P16
L22
C110
F6
FB2
P3
FB4
J1
J4
P4
P13

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 31 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	-0.3	12	16	V

NOTE: Stress beyond Absolute Maximum Ratings may cause permanent damage to the device.

7.2 Recommended Operating Conditions

Table 32 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	9.5	12	15	V

7.3 DC Electrical Characteristics

Table 33 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
1.8V Digital I/O					
V_{IH}		1.17		2.1	V
V_{IL}		-0.3		0.63	V
V_{OH}		1.35		1.8	V
V_{OL}		0		0.45	V
3.3V Digital I/O					
V_{IH}		2.31		3.3	V
V_{IL}		0		0.99	V
V_{OH}		3.15			V
V_{OL}				0.15	V