UCM-iMX7

Reference Guide

Compulab Ltd.
P.O. Box 687 Yokneam Illit
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.com
Fax: +972 (4) 8325251

Table of Contents

Table 1 Revision Notes

Date	Description
May 2017	First release

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.com/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab UCM-iMX7 Computer-on-Module.

1.2 UCM-iMX7 Part Number Legend

Please refer to the CompuLab website 'Pricing and Ordering' section to decode the UCM-iMX7 part number: http://www.compulab.com/products/computer-on-modules/ucm-imx7/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
UCM-iMX7 Developer Resources	http://www.compulab.com/
i.MX7 Reference Manual	http://www.nxp.com/
i.MX7 Datasheet	http://www.nxp.com/

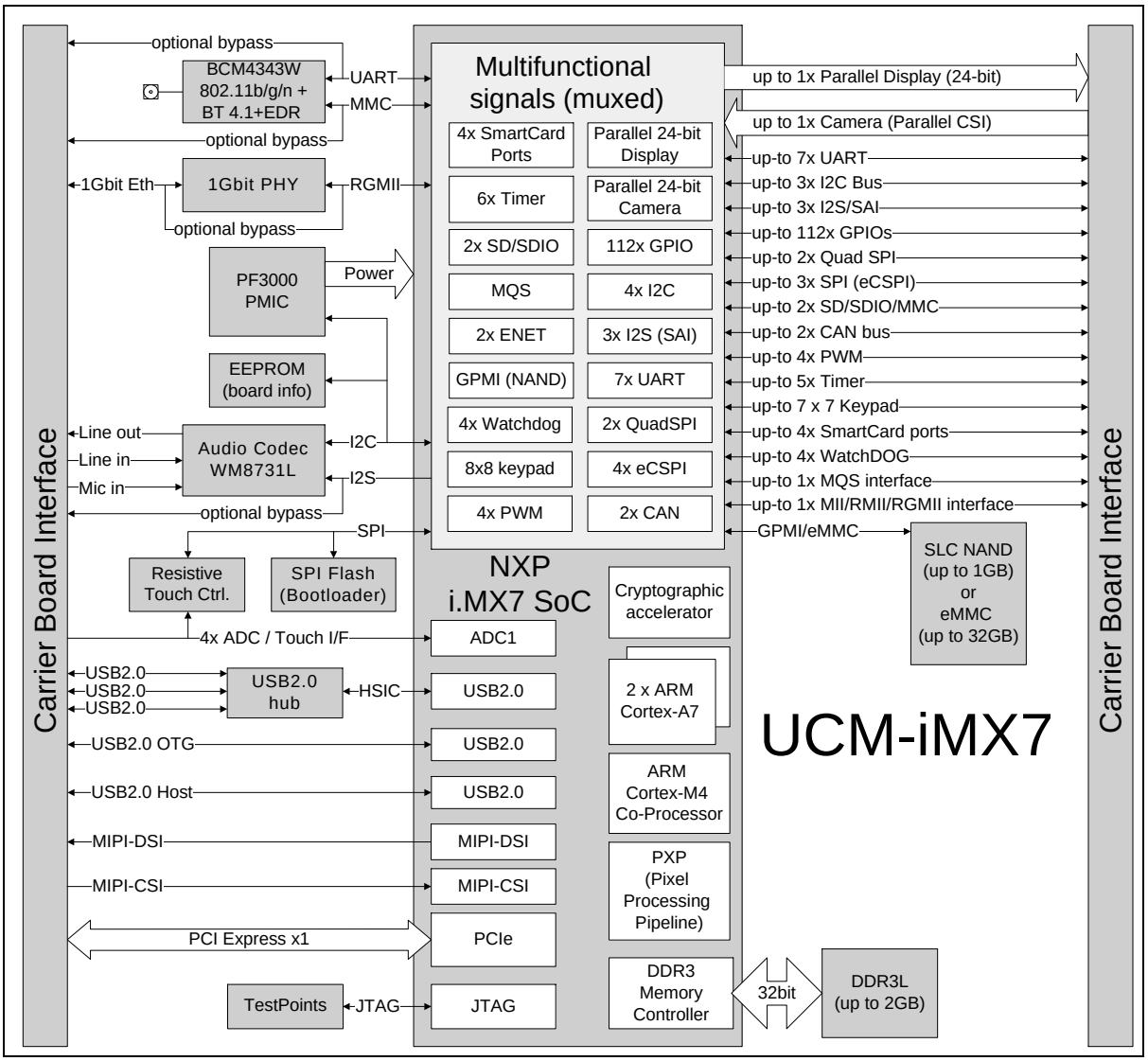
2 OVERVIEW

2.1 Highlights

- NXP i.MX7 Dual / Single core Cortex-A7 SoC, up to 1GHz
- Up to 2GB DDR3L-1066 with 32-bit data bus.
- Up to 32GB on-board eMMC storage.
- 802.11b/g/n WiFi and Bluetooth 4.1 BLE
- PCIe, GbE, 5x USB2, 7x UART, 2x CAN, 112x GPIO
- LVDS, MIPI-DSI, Parallel RGB, up to 1920 x 1080
- ARM Cortex-M4, 200Mhz Co-Processor dedicated for real-time tasks

2.2 Block Diagram

Figure 1 UCM-iMX7 Block Diagram



2.3 UCM-iMX7 Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX 7Solo ARM Cortex-A7, 800MHz NEON SIMD and VFPv4	C800
	NXP i.MX 7Dual ARM Cortex-A7, 1GHz NEON SIMD and VFPv4	C1000D
Real-Time Coprocessor	ARM Cortex-M4, 200Mhz	+
Memory and Storage		
RAM	256MB – 2GB, DDR3L-1066	D
Storage	SLC NAND flash, 128MB - 1GB	N
	eMMC flash, 4GB - 32GB	
Display and Camera		
Display	Parallel 24-bit display interface, up to 1920 x 1080 @60Hz	+
	MIPI-DSI, 2 data lanes, up to 1400 x 1050 @60Hz	+
Touchscreen	On-board 4-wire resistive touch-screen controller	I
	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	Parallel camera interface, up to 24-bit	+
	MIPI-CSI, 2 data lanes	+
Network		
Gigabit Ethernet	1x 10/100/1000Mbps Ethernet port (MAC+PHY)	E
	MII/RMII/RGMII Interface Ethernet port (MAC only)	~~E~~
WiFi	802.11b/g/n WiFi interface Cypress (Broadcom) BCM4343W chipset	WB
Bluetooth	Bluetooth 4.1 BLE	WB
Audio		
Analog Audio	Audio codec with analog stereo output, stereo input and electret microphone support	A
Digital Audio	I2S compliant digital audio interface	+
	MQS audio interface	+
I/O		
PCI Express	PCIe x1 Gen. 2.1	C1000D
USB	1x USB2.0 OTG port	+
	Additional 1x USB2.0 host ports	C1000D
	Additional 3x USB2.0 host ports	UH
Serial Ports (UARTs)	Up to 7x UART ports, up to 4 Mbps	+
CAN bus	Up to 2x CAN bus, 3.3V levels	+
MMC/SD/SDIO	Up to 2x MMC/SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 112x GPIO (multifunctional signals shared with other functions)	+
Timers	Up to 6x Timer outputs	+
ADC	4x general-purpose ADC channels	~~I~~
System Logic		
RTC	Real time clock, powered by external battery	+

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	3.5V to 4.5V / Li-Ion battery
Digital I/O voltage	3.3V
Active power consumption	0.5 - 3 W, depending on configuration and system load
Mechanical Specifications	
Dimensions	30 x 27 x 8 mm
Weight	5.9 gram
Connectors	2 x 100 pin, 0.4mm pitch
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

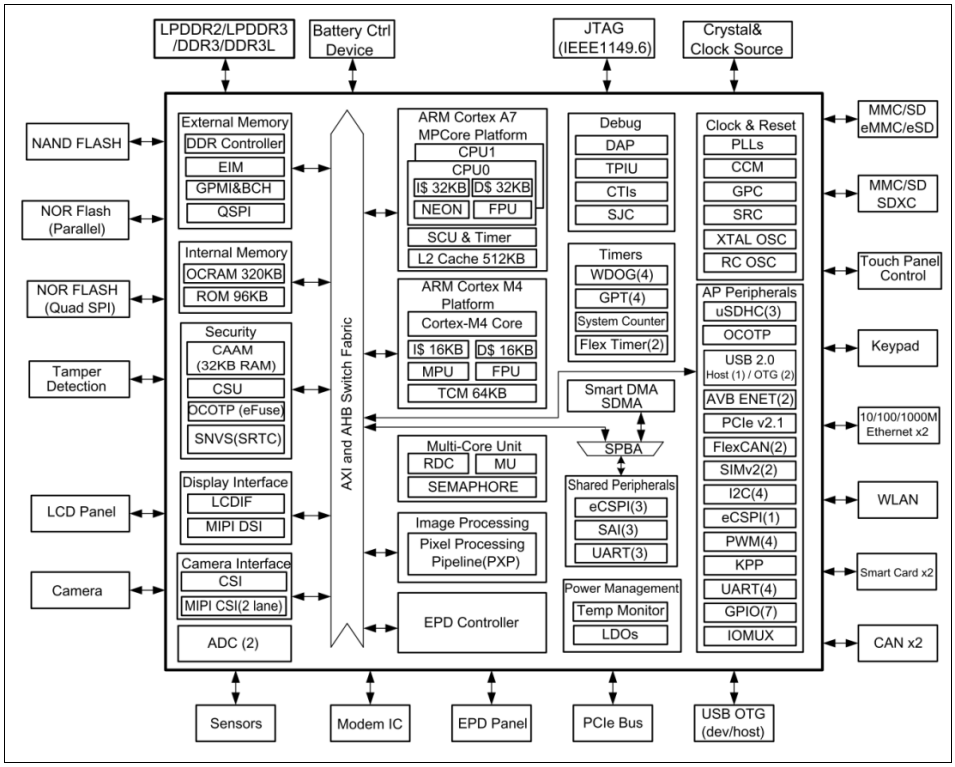
3 CORE SYSTEM COMPONENTS

3.1 i.MX7 SoC

The i.MX7 family of processors combines an implementation of two ARM® Cortex®-A7 cores intended for high level O/S, with an ARM® Cortex®-M4 core dedicated for real-time tasks. The i.MX7 has the following main features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology), each core includes:
  - Up to 1GHz operation frequency
  - 32 KByte L1 Instruction Cache, 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - NEON MPE coprocessor
- One ARM Cortex-M4 Core dedicated for real-time tasks, with the following features:
  - 200MHz operation frequency
  - MPU, FPU
  - 16 KByte instruction cache, 16 KByte data cache
  - 64 KByte TCM (tightly-coupled memory)
- Cryptographic acceleration and assurance module, containing cryptographic and hash engines supporting DPA (differential power analysis) protection, 32 KB secure RAM, and true and pseudo random number generator (NIST certified)
- PXP—PiXel processing pipeline for imagine resize, rotation, overlay and CSC. Offloading key pixel processing operations are required to support the display applications

Figure 2 i.MX 7Dual Block Diagram



3.2 Memory

3.2.1 DRAM

UCM-iMX7 is equipped with up to 2GB of onboard DDR3L memory. The DDR3L data bus is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

NOTE: UCM-iMX7 boards with 256MB of DRAM (D256 option) feature a 16-bit wide DDR3 data bus.

3.2.2 Bootloader Storage

The UCM-iMX7 is assembled with 2MBytes of SPI NOR flash. The SPI NOR flash is the primary non-volatile memory device of UCM-iMX7, used for the boot-loader and configuration blocks storage.

3.2.3 General Purpose Storage

UCM-iMX7 is available with optional secondary on-board storage designed to store the operating system and user data. One of the following on-board non-volatile memory devices can be used as the secondary on-board storage.

- On-board eMMC flash (up to 32GBytes).
- On-board raw SLC NAND Flash (up to 1GBytes).

The secondary storage device is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

UCM-iMX7 implements a variety of peripheral interfaces through the UCM carrier board connectors. The following notes apply to interfaces available through the UCM interface:

- Some interfaces/signals are available only with/without certain configuration options of UCM-iMX7. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Many of the UCM-iMX7 carrier board interface pins are multifunctional. Up-to 8 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5 of this document.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the UCM-iMX7 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on UCM-iMX7 Configuration options, certain carrier board interface pins are physically disconnected (floating) from the carrier board interface connector on-board UCM-iMX7. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Signal Input
- **"AO"** – Analog Signal Output
- **"AIO"** – Analog Signal Input/Output
- **"APO"** – Analog Power Output
- **"API"** – Analog Power Input
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"IOD"** – Open Drain Signal (not pulled up on-board UCM-iMX7 unless otherwise noted).
- **"PI"** – Power Input
- **"PO"** – Power Output
- "**SPU" –** Software controlled pull up to 3.3V
- "**SPD" –** Software controlled pull down to GND
- **"PU18**" – Always pulled up to 1.8V on-board UCM-iMX7, (typ. 5KΩ-15KΩ).

- **"PU33"** – Always pulled up to 3.3V on-board UCM-iMX7, (typ. 5KΩ-15KΩ).
- **"PUSUPPLY"** – Always pulled up to 3.3V - 4.5V on-board UCM-iMX7, (typ. 5KΩ-15KΩ).
- **"PD" -** Always pulled down on-board UCM-iMX7, (typ. 5KΩ-15KΩ).

4.1 Parallel Display interface

UCM-iMX7 Parallel display interface is derived from the i.MX7 integrated Enhanced LCD interface (eLCDIF) designed to drive a wide range of display devices varying in size and capabilities. eLCDIF supports the following main features:

- Support for parallel LCD displays (up to 24-bit) with resolutions up to 1920x1080 at 60Hz.
- Support for both synchronous and asynchronous "smart" displays.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode, including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the Parallel display interface signals

Table 5 Parallel display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LCDIF.BUSY	P2-69*	I	Busy Signal	Always
LCDIF.CLK	P2-33*	O	Clock Signal	Always
LCDIF.CLK	P2-93*	O	Clock Signal	Always
LCDIF.CS	P2-57*	O	Chip Select	Always
LCDIF.CS	P2-20*	O	Chip Select	Always
LCDIF.DATA[0]	P2-93*	IO	Data Signal	Always
LCDIF.DATA[0]	P2-87^*	IO; PD	Data Signal	Always
LCDIF.DATA[0]	P2-65*	IO	Data Signal	Always
LCDIF.DATA[1]	P2-89*	IO	Data Signal	Always
LCDIF.DATA[1]	P2-85^*	IO; PD	Data Signal	Always
LCDIF.DATA[1]	P2-61*	IO	Data Signal	Always
LCDIF.DATA[10]	P1-42^*	IO; PD	Data Signal	Always
LCDIF.DATA[10]	P2-63*	IO	Data Signal	Always
LCDIF.DATA[11]	P1-56^*	IO; PD	Data Signal	Always
LCDIF.DATA[11]	P1-77*	IO	Data Signal	Always
LCDIF.DATA[11]	P2-61*	IO	Data Signal	Always
LCDIF.DATA[12]	P1-68^*	IO; PD/PU33	Data Signal. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[12]	P2-59*	IO	Data Signal	Always
LCDIF.DATA[12]	P2-22*	IO	Data Signal	Always
LCDIF.DATA[13]	P1-64^*	IO; PU33/PD	Data Signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[13]	P2-90*	IO	Data Signal	Always
LCDIF.DATA[13]	P2-57*	IO	Data Signal	Always
LCDIF.DATA[14]	P2-88*	IO	Data Signal	Always
LCDIF.DATA[14]	P1-66^*	IO; PU33/PD	Data Signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[14]	P2-53*	IO	Data Signal	Always
LCDIF.DATA[15]	P1-60^*	IO; PD	Data Signal	Always
LCDIF.DATA[15]	P2-72*	IO	Data Signal	Always
LCDIF.DATA[15]	P2-51*	IO	Data Signal	Always
LCDIF.DATA[16]	P1-50^*	IO; PD	Data Signal	Always
LCDIF.DATA[17]	P2-47^*	IO; PU33	Data Signal	Always
LCDIF.DATA[18]	P1-52^*	IO; PD	Data Signal	Always
LCDIF.DATA[19]	P1-54^*	IO; PD	Data Signal	Always
LCDIF.DATA[2]	P2-95*	IO	Data Signal	Always
LCDIF.DATA[2]	P2-83^*	IO; PD	Data Signal	Always
LCDIF.DATA[20]	P1-62*	IO	Data Signal	Always
LCDIF.DATA[21]	P2-59*	IO	Data Signal	Always
LCDIF.DATA[21]	P2-37*	IO	Data Signal	Always
LCDIF.DATA[22]	P1-44*	IO	Data Signal	Always
LCDIF.DATA[22]	P2-53*	IO	Data Signal	Always
LCDIF.DATA[23]	P1-40*	IO	Data Signal	Always
LCDIF.DATA[3]	P2-97*	IO	Data Signal	Always
LCDIF.DATA[3]	P2-81^*	IO; PD	Data Signal	Always

Signal Name	Pin #	Type	Description	Availability
LCDIF.DATA[4]	P2-66^*	IO; PD	Data Signal	Always
LCDIF.DATA[4]	P2-77*	IO	Data Signal	Always
LCDIF.DATA[5]	P2-64^*	IO; PD	Data Signal	Always
LCDIF.DATA[5]	P2-75*	IO	Data Signal	Always
LCDIF.DATA[6]	P2-35*	IO	Data Signal	Always
LCDIF.DATA[6]	P2-78^*	IO; PD	Data Signal	Always
LCDIF.DATA[6]	P2-73*	IO	Data Signal	Always
LCDIF.DATA[7]	P2-71*	IO	Data Signal	Always
LCDIF.DATA[7]	P2-45^*	IO; PD	Data Signal	Always
LCDIF.DATA[7]	P2-20*	IO	Data Signal	Always
LCDIF.DATA[8]	P2-69*	IO	Data Signal	Always
LCDIF.DATA[8]	P1-11^*	IO; PD	Data Signal	Always
LCDIF.DATA[9]	P2-65*	IO	Data Signal	Always
LCDIF.DATA[9]	P2-63*	IO	Data Signal	Always
LCDIF.DATA[9]	P1-13^*	IO; PD	Data Signal	Always
LCDIF.ENABLE	P1-28*	IO	Enable Signal	Always
LCDIF.ENABLE	P2-35*	IO	Enable Signal	Always
LCDIF.ENABLE	P2-89*	IO	Enable Signal	Always
LCDIF.HSYNC	P1-48*	I	HSYNC enable	Always
LCDIF.HSYNC	P1-77*	I	HSYNC enable	Always
LCDIF.HSYNC	P2-97*	I	HSYNC enable	Always
LCDIF.RESET	P2-80*	IO	LCD reset Signal	Always
LCDIF.RESET	P2-70*	IO	LCD reset Signal	Always
LCDIF.VSYNC	P2-41*	I	VSYNC Signal	Always
LCDIF.VSYNC	P2-95*	I	VSYNC Signal	Always
LCDIF.VSYNC	P2-22*	I	VSYNC Signal	Always
LCDIF.WR_RWN	P2-51*	IO	WR Signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.2 MIPI-DSI Interface

The MIPI-DSI interface available with UCM-iMX7 is based on the two-lane MIPI display interface available with the i.MX7 SoC. The following main features are supported:

- Up-to two data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Complies to MIPI DSI Standard Specification V1.01r11.
- Maximum resolution ranges up to SXGA+(1400 x 1050 @ 60 Hz, 24 bpp).
- Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24bpp

NOTE: UCM-iMX7 MIPI-DSI interface is available only without the 'L' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_DSI_CLK_N	P1-73	AO	Negative part of MIPI-DSI clock diff-pair	Always
MIPI_DSI_CLK_P	P1-71	AO	Positive part of MIPI-DSI clock diff-pair	Always
MIPI_DSI_D0_N	P1-61	AO	Negative part of MIPI-DSI data diff-pair 0	Always
MIPI_DSI_D0_P	P1-59	AO	Positive part of MIPI-DSI data diff-pair 0	Always
MIPI_DSI_D1_N	P1-67	AO	Negative part of MIPI-DSI data diff-pair 1	Always
MIPI_DSI_D1_P	P1-65	AO	Positive part of MIPI-DSI data diff-pair 1	Always

4.3 Parallel Camera Interface

The UCM-iMX7 parallel camera interface is derived from the i.MX7 integrated CSI IP. The CSI block enables direct connection between UCM-iMX7 and external CMOS image sensors. The capabilities of CSI include:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
- Up to 133 MHz operation frequency.
- Configurable master clock frequency output to sensor.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the Parallel camera interface signals

Table 7 Parallel camera Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI1.DATA[0]	P2-47^*	I; PU33	CMOS Sensor data	Always
CSI1.DATA[1]	P1-50^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[10]	P1-40*	I	CMOS Sensor data	Always
CSI1.DATA[11]	P1-44*	I	CMOS Sensor data	Always
CSI1.DATA[12]	P2-37*	I	CMOS Sensor data	Always
CSI1.DATA[13]	P1-62*	I	CMOS Sensor data	Always
CSI1.DATA[14]	P1-54^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[15]	P1-52^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[16]	P2-33*	I	CMOS Sensor data	Always
CSI1.DATA[17]	P1-28*	I	CMOS Sensor data	Always
CSI1.DATA[18]	P1-48*	I	CMOS Sensor data	Always
CSI1.DATA[19]	P2-41*	I	CMOS Sensor data	Always
CSI1.DATA[2]	P1-60^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[20]	P2-87^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[21]	P2-85^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[22]	P2-83^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[23]	P2-81^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[3]	P1-66^*	I; PU33/PD	CMOS Sensor data. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[4]	P1-64^*	I; PU33/PD	CMOS Sensor data. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[5]	P1-68^*	I; PD/PU33	CMOS Sensor data. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[6]	P1-56^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[6]	P2-90*	I	CMOS Sensor data	Always
CSI1.DATA[7]	P1-42^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[7]	P2-88*	I	CMOS Sensor data	Always
CSI1.DATA[8]	P2-72*	I	CMOS Sensor data	Always
CSI1.DATA[8]	P1-13^*	I; PD	CMOS Sensor data	Always
CSI1.DATA[9]	P2-70*	I	CMOS Sensor data	Always
CSI1.DATA[9]	P1-11^*	I; PD	CMOS Sensor data	Always
CSI1.FIELD	P2-80*	I	CSI Field Signal	Always
CSI1.HSYNC	P2-96*	I	Horizontal Sync (Blank Signal)	Always
CSI1.HSYNC	P2-64^*	I; PD	Horizontal Sync (Blank Signal)	Always
CSI1.MCLK	P2-29*	O	CMOS Sensor Master Clock	Always
CSI1.MCLK	P2-45^*	O; PD	CMOS Sensor Master Clock	Always
CSI1.PIXCLK	P2-27*	I	Pixel Clock	Always
CSI1.PIXCLK	P2-78^*	I; PD	Pixel Clock	Always
CSI1.VSYNC	P2-94*	I	Vertical Sync (Start Of Frame)	Always
CSI1.VSYNC	P2-66^*	I; PD	Vertical Sync (Start Of Frame)	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.4 MIPI-CSI Camera Interface

The MIPI-CSI interface available with UCM-iMX7 is derived from the two-lane MIPI CSI2 host controller (MIPI_CSI2) integrated into the i.MX7 SoC. The CSI2 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between UCM-iMX7 and a MIPI CSI-2 compliant camera sensor. The following main features are supported:

- Up-to two data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Compliant to MIPI CSI2 Standard Specification V1.01r06.
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits.
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 8 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_CSI_CLK_N	P1-55	AI	Negative part of MIPI-CSI clock diff-pair 1	Always
MIPI_CSI_CLK_P	P1-53	AI	Positive part of MIPI-CSI clock diff-pair	Always
MIPI_CSI_D0_N	P1-43	AI	Negative part of MIPI-CSI data diff-pair 0	Always
MIPI_CSI_D0_P	P1-41	AI	Positive part of MIPI-CSI data diff-pair 0	Always
MIPI_CSI_D1_N	P1-49	AI	Negative part of MIPI-CSI data diff-pair 1	Always
MIPI_CSI_D1_P	P1-47	AI	Positive part of MIPI-CSI data diff-pair 1	Always

4.5 Ethernet

4.5.1 Copper Ethernet Interface

UCM-iMX7 incorporates a full-featured 10/100/1000 (copper) ethernet port implemented with the MAC built into the i.MX7 SoC, coupled with two AR8033 RGMII Ethernet PHYs from Atheros. The following main features are supported:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover .
- Automatic polarity correction.
- Activity and speed indicator LED controls.

NOTE: UCM-iMX7 primary Ethernet port is available only with the 'E' ordering option.

Please refer to the i.MX7 and the Atheros AR8033 respective reference manuals for additional details. The table below summarizes the ethernet interface signals

Table 9 Ethernet1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH1_LED_ACT	P1-10^	IO; PD	Active High, activity LED driver. 2.5V signal	"E"
ETH1_LED1_SPD	P1-38^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal	"E"
ETH1_LED3	P1-19	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	"E"
ETH1_MDI0N	P1-12	AIO	Negative part of 100ohm diff-pair 0	"E"
ETH1_MDI0P	P1-14	AIO	Positive part of 100ohm diff-pair 0	"E"
ETH1_MDI1N	P1-20	AIO	Negative part of 100ohm diff-pair 1	"E"
ETH1_MDI1P	P1-18	AIO	Positive part of 100ohm diff-pair 1	"E"
ETH1_MDI2N	P1-26	AIO	Negative part of 100ohm diff-pair 2	"E"
ETH1_MDI2P	P1-24	AIO	Positive part of 100ohm diff-pair 2	"E"
ETH1_MDI3N	P1-32	AIO	Negative part of 100ohm diff-pair 3	"E"
ETH1_MDI3P	P1-30	AIO	Positive part of 100ohm diff-pair 3	"E"

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.5.2 MII/RMII/RGMII Interface

UCM-iMX7 incorporates a full-featured MII/RMII/RGMII port implemented with the MAC built into the i.MX7 SoC. The i.MX7 integrated MAC supports the following main features:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking.
- Dynamically configurable to support 10/100-Mbit/s and gigabit operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Supports gigabit full-duplex operation
- Seamless interface to commercial ethernet PHY devices
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames providing for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Supports legacy FEC buffer descriptors
- Interrupt coalescing reduces the number of interrupts generated by the MAC, reducing CPU loading
- Supports all IEEE 1588 frames.
- Provides a 4-channel IEEE 1588 timer. Each channel supports input capture and output compare using the 1588 counter (up to 3 with UCM-iMX7)

NOTE: UCM-iMX7 MII/RMII/RGMII port is available only without the 'E' ordering option.

Please refer to the i.MX7 reference manual for additional details. The table below summarizes the MII/RMII/RGMII interface signals

Table 10 MII/RMII/RGMII1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET1.1588_EVENT1_IN	P1-95*	I	Capture/compare block input	not "WB"
ENET1.1588_EVENT1_OUT	P1-91*	O	Capture/compare block output	not "WB"
ENET1.1588_EVENT2_IN	P2-33*	I	Capture/compare block input	Always
ENET1.1588_EVENT2_OUT	P1-62*	O	Capture/compare block output	Always

Signal Name	Pin #	Type	Description	Availability
ENET1.1588_EVENT3_IN	P1-28*	I	Capture/compare block input	Always
ENET1.1588_EVENT3_OUT	P2-37*	O	Capture/compare block output	Always
ENET1.COL	P1-92*	I	Collision detect signal (MII mode)	not "A"
ENET1.CRS	P1-88*	I	Carrier sense signal (MII mode)	not "A"
ENET1.MDC	P1-74*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	not "E"
ENET1.MDC	P2-82*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always
ENET1.MDC	P2-3*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always
ENET1.MDIO	P2-76*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	not "E"
ENET1.MDIO	P2-84*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always
ENET1.MDIO	P2-1*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always
ENET1.RGMII_RD0	P1-19*	I	Ethernet input data from the PHY	not "E"
ENET1.RGMII_RD1	P1-10*	I	Ethernet input data from the PHY	not "E"
ENET1.RGMII_RD2	P1-26*	I	Ethernet input data from the PHY	not "E"
ENET1.RGMII_RD3	P1-24*	I	Ethernet input data from the PHY	not "E"
ENET1.RGMII_RX_CTL	P1-30*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode).	not "E"
ENET1.RGMII_RXC	P1-32*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	not "E"
ENET1.RGMII_TD0	P1-38*	O	controlled)	not "E"
ENET1.RGMII_TD1	P1-20*	O	Serial output Ethernet data to PHY	not "E"
ENET1.RGMII_TD2	P1-57*	O	Serial output Ethernet data to PHY	not "E"
ENET1.RGMII_TD3	P1-18*	O	Serial output Ethernet data to PHY	not "E"
ENET1.RGMII_TX_CTL	P1-12*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode).	not "E"
ENET1.RGMII_TXC	P1-14*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	not "E"
ENET1.RX_CLK	P1-94*	I	Timing reference for RX_DATA[3:0] and RX_ER in MII MODE	not "A"
ENET1.RX_ER	P1-32*	I	When asserted with RXDV, indicates the PHY detects an error in the current frame. (MII/RMII mode)	not "E"
ENET1.TX_CLK	P1-86*	O	Timing reference for TX_DATA[3:0] and TX_ER in MII MODE	not "A"
ENET1.TX_ER	P1-14*	O	When asserted for one or more clock cycles while TXEN is also asserted, PHY sends one or more illegal symbols (MII/RMII mode)	not "E"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.6 WLAN + Bluetooth

The UCM-iMX7 WLAN + Bluetooth capabilities are based on the Murata LBEE5KL1DX module populated onboard. LBEE5KL1DX is based on the Cypress (Broadcom) BCM4343W chipset enabling Wi-Fi and Bluetooth functionality with UCM-iMX7. LBEE5KL1DX supports the following features:

- FCC certified with chip antennas.
- Support of IEEE Std 802.11b, 802.11g and 802.11n.
- Bluetooth 4.1/EDR + BLE
- AP & STA dual mode network topologies support
- Power Class 1 (10dBm max) + BLE

When populated, LBEE5KL1DX is interfaced with the i.MX7 through the following interfaces:

- i.MX7 MMC/SD/SDIO2 interface is used for WLAN data.
- i.MX7 UART3 and SAI2 interfaces are employed for Bluetooth and A2DP data.
- J1 U.FL connector is available for external antenna connection.

Please refer to the i.MX7 and the Murata respective documentation for additional details.

NOTE: UCM-iMX7 WiFi and Bluetooth functionality is available only with the 'WB' ordering option.

Table 11 J1 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

4.7 Analog Audio

The UCM-iMX7 analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with the i.MX7 SAI1 port. The WM8731L codec supports the following main features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

NOTE: UCM-iMX7 Analog audio interface is available only with the 'A' ordering option.

Table 12 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB

Parameter	Test conditions	Min	Typ	Max	Unit
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVp-p		45		
Programmable gain	1 kHz output	-73	0	6	dB
Programmable-gain step size	1 kHz		1		dB
Mute attenuation	1 kHz output, 0dB		80		dB
Line Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio	A-weighted, 0dB gain, Fsample = 48 kHz.	85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.		90		
Dynamic range	A-weighted, −60-dB full-scale input	85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain		-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVp-p		45		
ADC Channel Separation	1 kHz input tone		90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω	-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic		1.5		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance	12 dB input gain	10	15		kΩ
	0 dB input gain	20	30		
Input capacitance			10		pF
Microphone Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio	A-weighted, 0-dB gain		85		dB
Dynamic range,	A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion,	0dB input, 0dB gain		-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVp-p		45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,		14		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance			10		kΩ
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

Please refer to the Wolfson Microelectronics WM8731L datasheet for additional details. The table below summarizes the analog audio interface signals

Table 13 Analog Audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
LHPOUT	P1-100	AO	Left channel headphone output	"A"
LLINEIN	P1-94	AI	Left channel line input	"A"
MICBIAS	P1-88	APO	Electret microphone bias supply	"A"
MICIN	P1-86	AI	Microphone input	"A"
RHPOUT	P1-98	AO	Right channel headphone output	"A"
RLINEIN	P1-92	AI	Right channel line input	"A"

4.8 Digital Audio (SAI)

UCM-iMX7 enables access to all 3 of the i.MX7 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.

- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for first word and remaining words in frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

NOTE: UCM-iMX7 SAI1 interface is available only without the 'A' ordering option.

NOTE: UCM-iMX7 SAI2 interface is available only without the 'WAB' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SAI interface signals

Table 14 SAI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1.MCLK	P2-68*	IO	Audio master clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.RX_BCLK	P1-14*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "E"
SAI1.RX_BCLK	P1-100*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.RX_DATA[0]	P1-86*	I	Receive data, sampled synchronously by the bit clock	not "A"
SAI1.RX_SYNC	P1-12*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "E"
SAI1.RX_SYNC	P1-98*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"
SAI1.TX_BCLK	P1-94*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.TX_DATA[0]	P1-92*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "A"
SAI1.TX_SYNC	P1-88*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"

Table 15 SAI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2.MCLK	P2-100*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI2.RX_BCLK	P1-37*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "WB"
SAI2.RX_BCLK	P1-100*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI2.RX_DATA[0]	P1-21*	I	Receive data, sampled synchronously by the bit clock	not "WB"
SAI2.RX_DATA[0]	P1-25*	I	Receive data, sampled synchronously by the bit clock	not "WB"
SAI2.RX_SYNC	P1-29*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "WB"
SAI2.RX_SYNC	P1-98*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"
SAI2.TX_BCLK	P1-23*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "WB"

Signal Name	Pin #	Type	Description	Availability
SAI2.TX_BCLK	P1-31*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "WB"
SAI2.TX_DATA[0]	P1-17*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "WB"
SAI2.TX_DATA[0]	P1-35*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "WB"
SAI2.TX_SYNC	P1-15*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "WB"
SAI2.TX_SYNC	P1-33*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "WB"

Table 16 SAI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI3.MCLK	P2-92*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.MCLK	P2-82*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.MCLK	P2-18~*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.RX_BCLK	P2-12~*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	Always
SAI3.RX_DATA[0]	P2-16*~	I	Receive data, sampled synchronously by the bit clock	Always
SAI3.RX_SYNC	P2-4~*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always
SAI3.TX_BCLK	P2-24*~	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	Always
SAI3.TX_DATA[0]	P2-8*~	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always
SAI3.TX_DATA[0]	P1-95*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "WB"
SAI3.TX_SYNC	P2-10*~	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always
SAI3.TX_SYNC	P1-91*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "WB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.9 Medium Quality Sound module (MQS)

The i.MX7 integrated medium-quality sound module (MQS) is used to generate 2-channel, medium-quality, PWM-like audio, via two standard digital GPIO pins, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. The MQS block accepts valid signals from SAI1 and provides up-to 20dB output SNR for signals below 10kHz. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided. Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MQS interface signals

Table 17 MQS Interface Signals

Signal Name	Pin #	Type	Description	Availability
MQS.LEFT	P1-37*	O	Left signal output	not "WB"
MQS.LEFT	P1-100*	O	Left signal output	not "A"
MQS.RIGHT	P1-29*	O	Right signal output	not "WB"
MQS.RIGHT	P1-98*	O	Right signal output	not "A"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.10 USB 2.0

4.10.1 Native USB2.0 ports

The i.MX7 SoC is equipped with two high-speed OTG controller modules and integrated high-speed analog USB PHYs. UCM-iMX7 enables full access to both ports trough the carrier board interface connector. The USB ports support the following main features:

- High speed, full speed and low speed operation in host mode.
- High speed and full speed operation in peripheral mode.
- Up to 8 bidirectional endpoints.
- UCM-iMX7 USB port 0 (i.MX7 port 1) supports for OTG signaling, session request protocol (SRP), host negotiation protocol (HNP), and attach detection protocol (ADP). ADP support includes dedicated timer hardware and register interface.
- UCM-iMX7 USB port 1 (i.MX7 port 2) is configured to operate in host only mode onboard UCM-iMX7.
- Supports charger detection with USB_OTG1_CHD_B pin (i.MX7 port 1 only) and register interface (both i.MX7 ports)

NOTE: UCM-iMX7 USB port 1 (i.MX7 port 2) is available only with the 'C1000D' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the native USB interface signals

Table 18 Native USB port 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB.OTG1_ID	P2-27*	I	OTG1 ID Signal (MUXED)	Always
USB.OTG1_ID	P1-74*	I	OTG1 ID Signal (MUXED)	not "E"
USB.OTG1_ID	P2-100*	I	OTG1 ID Signal (MUXED)	Always
USB.OTG1_PWR	P2-6*	O	external USB_OTG1_VBUS power supply control signal	Always
USB_OTG1_CHD_B	P2-56	IO	OTG1 Charge detect signal	Always
USB_OTG1_DN	P2-34	AIO	Negative part of i.MX7 OTG port1 diff pair	Always
USB_OTG1_DP	P2-36	AIO	Positive part of i.MX7 OTG port1 diff pair	Always
USB_OTG1_ID	P2-5	AI	OTG1 ID Signal (non-muxed)	Always
USB_OTG1_VBUS	P2-44	PI	VBUS input for USB_OTG1	Always

Table 19 Native USB port 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB.OTG2_ID	P2-29*	I	OTG2 ID Signal (MUXED)	"C1000D"
USB.OTG2_ID	P2-92*	I	OTG2 ID Signal (MUXED)	"C1000D"
USB.OTG2_OC	P1-95	I	Input for USB_OTG2_VBUS overcurrent detection signal.	"C1000D" and not "WB"
USB.OTG2_PWR	P1-91	O	external USB_OTG2_VBUS power supply control signal	"C1000D" and not "WB"

Signal Name	Pin #	Type	Description	Availability
USB_OTG2_DN	P2-30	AIO	Negative part of i.MX7 OTG port2 diff pair	"C1000D"
USB_OTG2_DP	P2-28	AIO	Positive part of i.MX7 OTG port2 diff pair	"C1000D"
USB_OTG2_VBUS	P2-32	PI	VBUS input for USB_OTG2	"C1000D"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.10.2 Onboard USB2.0 Hub

UCM-iMX7 is equipped with an optional onboard USB2.0 hub supporting three downstream USB2.0 host ports. The 3 additional ports are implemented through a combination of the i.MX7 on-chip HSIC high-speed host-only port with the Microchip USB3503 USB hub. The USB hub supports the following main features:

- Three USB 2.0 High Speed (480Mbps) compatible downstream ports
- Supports either Single-TT or Multi-TT configurations for Full-Speed (12Mbps) and Low-Speed (1.5Mbps) connections

NOTE: UCM-iMX7 onboard USB hub is available only with the 'UH' ordering option.

Please refer to the Microchip USB3503 datasheet for additional information. The table below summarizes the USB Hub interface signals

Table 20 USB Hub Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_H1_DN	P2-21	AIO	Negative part of USB hub port1 diff pair.	"UH"
USB_H1_DP	P2-23	AIO	Positive part of USB hub port1 diff pair.	"UH"
USB_H2_DN	P2-9	AIO	Negative part of USB hub port2 diff pair.	"UH"
USB_H2_DP	P2-11	AIO	Positive part of USB hub port2 diff pair.	"UH"
USB_H3_DN	P2-15	AIO	Negative part of USB hub port3 diff pair.	"UH"
USB_H3_DP	P2-17	AIO	Positive part of USB hub port3 diff pair.	"UH"
VBUS_EN_REQ	P2-25	O	external VBUS power supply control signal for onboard USB2.0 Hub ports	"UH"
VBUS_NOVERCURRENT	P2-13	I	Input for USB2.0 Hub ports VBUS overcurrent detection signal.	"UH"

4.11 PCI-Express

The i.MX7Dual SoC is equipped with a single lane PCI Express port (PCIe) v2.1 port. UCM-iMX7 enables access to the i.MX7Dual PCI-Express port through the carrier board interface. The PCI Express port supports the following main features:

- Single lane compliant with PCI Express base specification v2.1 (6.0Gbps).
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface.
- Supports spread spectrum clocking in transmitter and receiver.

NOTE: UCM-iMX7 PCI-Express interface is available only with the 'C1000D' ordering option.

Please refer to the i.MX7 Dual Reference manual for additional details. The table below summarizes the PCI-Express interface signals

Table 21 PCI-Express Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_REFCLKIN_N	P2-42	AI	100 MHz negative-side reference clock differential input for PCIe (optional). Must not be left floating if used.	"C1000D"
PCIE_REFCLKIN_P	P2-40	AI	100 MHz positive-side reference clock differential input for PCIe (optional). Must not be left floating if used.	"C1000D"
PCIE_REFCLKOUT_N	P2-48	AO	100 MHz negative-side reference clock differential output for PCIe (optional). Must be pulled low through 49.9Ω resistor on carrier board if used.	"C1000D"
PCIE_REFCLKOUT_P	P2-46	AO	100 MHz positive-side reference clock differential output for PCIe (optional). Must be pulled low through 49.9Ω resistor on carrier board if used.	"C1000D"
PCIE_RX_N	P2-52	AI	Negative-side received differential input from the PHY	"C1000D"
PCIE_RX_P	P2-54	AI	Positive-side received differential input from the PHY	"C1000D"
PCIE_TX_N	P2-58	AO	Negative-side transmitted differential output from the PHY	"C1000D"
PCIE_TX_P	P2-60	AO	Positive-side transmitted differential output from the PHY	"C1000D"

4.12 MMC / SD /SDIO

Up to two MMC/SD/SDIO ports are available through the UCM-iMX7 carrier board interface. Both ports are derived from the i.MX7 on-chip MMC/SD/SDIO controller IPs (uSDHC). The uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS400 (8-bit transfer mode is only available on uSDHC port 1).
- Dedicated “card detection” and “write protection” signals and (hardware reset not supported).
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

NOTE: UCM-iMX7 MMC/SD/SDIO port 2 is available only without the ‘W’ and ‘WAB’ ordering options.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the MMC/SD/SDIO interface signals

Table 22 MMC/SD/SDIO1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC1.CD_B	P1-82*~	I	Card detection pin	Always
USDHC1.CLK	P2-4~*	O	Clock for MMC/SD/SDIO card	Always
USDHC1.CMD	P2-12~*	IO	CMD line connect to card	Always
USDHC1.DATA0	P2-16*~	IO	DATA0 line in all modes. Also used to detect busy state	Always
USDHC1.DATA1	P2-24*~	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always

Signal Name	Pin #	Type	Description	Availability
USDHC1.DATA2	P2-10*~	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always
USDHC1.DATA3	P2-8*~	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always
USDHC1.DATA4	P2-90*	IO	DATA4 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA5	P2-88*	IO	DATA5 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA6	P2-72*	IO	DATA6 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA7	P2-70*	IO	DATA7 line in 8-bit mode, not used in other modes	Always
USDHC1.LCTL	P1-69*	O	LED control used to drive an external LED	Always
USDHC1.RESET_B	P2-18~*	O	Card hardware reset signal, active LOW	Always
USDHC1.WP	P2-49*~	I	Card write protect detection	Always

Table 23 MMC/SD/SDIO2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC2.CD_B	P2-76*	I	Card detection pin	not "E"
USDHC2.CLK	P1-29*	O	Clock for MMC/SD/SDIO card	not "WB"
USDHC2.CMD	P1-37*	IO	CMD line connect to card	not "WB"
USDHC2.DATA0	P1-25*	IO	DATA0 line in all modes Also used to detect busy state	not "WB"
USDHC2.DATA1	P1-31*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	not "WB"
USDHC2.DATA2	P1-33*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	not "WB"
USDHC2.DATA3	P1-35*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	not "WB"
USDHC2.LCTL	P2-1*	O	LED control used to drive an external LED	Always
USDHC2.WP	P1-74*	I	Card write protect detection	not "E"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.13 UART

UCM-iMX7 enables access to all 7 of the i.MX7 universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX7 UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: The UART3 interface is used onboard UCM-iMX7 for bluetooth functionality. Using the UART3 interface signals available through the carrier board interface precludes onboard bluetooth operation.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the UART interface signals

Table 24 UART1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1.CTS_B	P1-19*	O	Clear to send	not "E"
UART1.CTS_B	P1-15*	O	Clear to send	not "WB"
UART1.RTS_B	P1-10*	I	Request to send	not "E"
UART1.RTS_B	P1-23*	I	Request to send	not "WB"
UART1.RX	P1-26*	I	Serial / infrared data receive	not "E"
UART1.RX	P2-84*	I	Serial / infrared data receive	Always
UART1.TX	P1-24*	O	Serial / infrared data transmit	not "E"
UART1.TX	P2-82*	O	Serial / infrared data transmit	Always

Table 25 UART2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2.CTS_B	P2-41*	O	Clear to send	Always
UART2.CTS_B	P1-21*	O	Clear to send	not "WB"
UART2.RTS_B	P1-48*	I	Request to send	Always
UART2.RTS_B	P1-17*	I	Request to send	not "WB"
UART2.RX	P2-33*	I	Serial / infrared data receive	Always
UART2.TX	P1-28*	O	Serial / infrared data transmit	Always

Table 26 UART3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3.CTS_B	P2-3*	O	Clear to send	Always
UART3.CTS_B	P1-91*	O	Clear to send	not "WB"
UART3.RTS_B	P2-1*	I	Request to send	Always
UART3.RTS_B	P1-95*	I	Request to send	not "WB"
UART3.RX	P1-45*	I	Serial / infrared data receive	Always
UART3.TX	P1-69*	O	Serial / infrared data transmit	Always

Table 27 UART4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4.CTS_B	P1-76*	O	Clear to send	Always
UART4.CTS_B	P1-21*	O	Clear to send	not "WB"
UART4.CTS_B	P1-33*	O	Clear to send	not "WB"
UART4.RTS_B	P1-72*	I	Request to send	Always
UART4.RTS_B	P1-17*	I	Request to send	not "WB"
UART4.RTS_B	P1-35*	I	Request to send	not "WB"
UART4.RX	P1-80*	I	Serial / infrared data receive	Always
UART4.RX	P1-15*	I	Serial / infrared data receive	not "WB"
UART4.RX	P1-25*	I	Serial / infrared data receive	not "WB"
UART4.TX	P1-78*	O	Serial / infrared data transmit	Always
UART4.TX	P1-23*	O	Serial / infrared data transmit	not "WB"
UART4.TX	P1-31*	O	Serial / infrared data transmit	not "WB"

Table 28 UART5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART5.CTS_B	P2-94*	O	Clear to send	Always
UART5.RTS_B	P2-96*	I	Request to send	Always
UART5.RTS_B	P2-6*	I	Request to send	Always
UART5.RX	P2-27*	I	Serial / infrared data receive	Always
UART5.TX	P2-29*	O	Serial / infrared data transmit	Always

Table 29 UART6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART6.CTS_B	P2-4~*	O	Clear to send	Always
UART6.CTS_B	P2-61*	O	Clear to send	Always
UART6.RTS_B	P2-63*	I	Request to send	Always
UART6.RTS_B	P2-18~*	I	Request to send	Always
UART6.RX	P1-82*~	I	Serial / infrared data receive	Always
UART6.RX	P2-69*	I	Serial / infrared data receive	Always
UART6.TX	P2-49*~	O	Serial / infrared data transmit	Always
UART6.TX	P2-65*	O	Serial / infrared data transmit	Always

Table 30 UART7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART7.CTS_B	P2-10*~	O	Clear to send	Always
UART7.CTS_B	P2-70*	O	Clear to send	Always
UART7.CTS_B	P2-51*	O	Clear to send	Always
UART7.RTS_B	P2-8*~	I	Request to send	Always
UART7.RTS_B	P2-72*	I	Request to send	Always
UART7.RTS_B	P2-53*	I	Request to send	Always
UART7.RX	P2-90*	I	Serial / infrared data receive	Always
UART7.RX	P2-16*~	I	Serial / infrared data receive	Always
UART7.RX	P2-59*	I	Serial / infrared data receive	Always
UART7.TX	P2-88*	O	Serial / infrared data transmit	Always
UART7.TX	P2-24*~	O	Serial / infrared data transmit	Always
UART7.TX	P2-57*	O	Serial / infrared data transmit	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.14 I2C

UCM-iMX7 is equipped with three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the I2C interface signals

Table 31 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1.SCL	P1-76*	IOD	Serial Clock	Always
I2C1.SCL	P2-84*	IOD	Serial Clock	Always
I2C1.SDA	P1-72*	IOD	Serial Data	Always
I2C1.SDA	P2-82*	IOD	Serial Data	Always
I2C1.SDA	P2-6*	IOD	Serial Data	Always

Table 32 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3.SCL	P2-94*	IOD	Serial Clock	Always
I2C3.SCL	P1-19*	IOD	Serial Clock	not "E"
I2C3.SCL	P1-45*	IOD	Serial Clock	Always
I2C3.SCL	P1-62*	IOD	Serial Clock	Always
I2C3.SDA	P1-10*	IOD	Serial Data	not "E"

Signal Name	Pin #	Type	Description	Availability
I2C3.SDA	P2-96*	IOD	Serial Data	Always
I2C3.SDA	P1-69*	IOD	Serial Data	Always
I2C3.SDA	P2-37*	IOD	Serial Data	Always

Table 33 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4.SCL	P2-27*	IOD	Serial Clock	Always
I2C4.SCL	P1-57*	IOD	Serial Clock	not "E"
I2C4.SCL	P1-44*	IOD	Serial Clock	Always
I2C4.SCL	P2-1*	IOD	Serial Clock	Always
I2C4.SCL	P1-98*	IOD	Serial Clock	not "A"
I2C4.SDA	P2-29*	IOD	Serial Data	Always
I2C4.SDA	P1-18*	IOD	Serial Data	not "E"
I2C4.SDA	P1-40*	IOD	Serial Data	Always
I2C4.SDA	P2-3*	IOD	Serial Data	Always
I2C4.SDA	P1-100*	IOD	Serial Data	not "A"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.15 SPI

Up-to three SPI interfaces are accessible through the UCM-iMX7 carrier board interface. The SPI interfaces are derived from i.MX7 integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SPI interface signals

Table 34 SPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2.MISO	P1-57*	IO	Master data in; slave data out	not "E"
ECSPI2.MISO	P2-72*	IO	Master data in; slave data out	Always
ECSPI2.MOSI	P1-24*	IO	Master data out; slave data in	not "E"
ECSPI2.MOSI	P2-88*	IO	Master data out; slave data in	Always
ECSPI2.RDY	P1-20*	I	SPI data ready signal	not "E"
ECSPI2.SCLK	P1-26*	IO	SPI clock signal	not "E"
ECSPI2.SCLK	P2-90*	IO	SPI clock signal	Always
ECSPI2.SS0	P1-18*	IO	Chip select signal	not "E"
ECSPI2.SS0	P2-70*	IO	Chip select signal	Always
ECSPI2.SS1	P1-30*	IO	Chip select signal	not "E"
ECSPI2.SS2	P1-32*	IO	indicates the PHY detects an error in	not "E"
ECSPI2.SS3	P1-38*	IO	Chip select signal	not "E"

Table 35 SPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3.MISO	P1-76*	IO	Master data in; slave data out	Always

Signal Name	Pin #	Type	Description	Availability
ECSPI3.MISO	P1-15*	IO	Master data in; slave data out	not "WB"
ECSPI3.MOSI	P1-72*	IO	Master data out; slave data in	Always
ECSPI3.MOSI	P1-23*	IO	Master data out; slave data in	not "WB"
ECSPI3.SCLK	P1-80*	IO	SPI clock signal	Always
ECSPI3.SCLK	P1-21*	IO	SPI clock signal	not "WB"
ECSPI3.SS0	P1-78*	IO	Chip select signal	Always
ECSPI3.SS0	P1-17*	IO	Chip select signal	not "WB"
ECSPI3.SS1	P2-8*~	IO	Chip select signal	Always
ECSPI3.SS2	P2-76*	IO	Chip select signal	not "E"
ECSPI3.SS3	P1-74*	IO	Chip select signal	not "E"

Table 36 SPI4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI4.MISO	P2-33*	IO	Master data in; slave data out	Always
ECSPI4.MISO	P1-82*~	IO	Master data in; slave data out	Always
ECSPI4.MOSI	P1-28*	IO	Master data out; slave data in	Always
ECSPI4.MOSI	P2-49*~	IO	Master data out; slave data in	Always
ECSPI4.RDY	P2-10*~	I	SPI data ready signal	Always
ECSPI4.SCLK	P1-48*	IO	SPI clock signal	Always
ECSPI4.SCLK	P2-18~*	IO	SPI clock signal	Always
ECSPI4.SS0	P2-41*	IO	Chip select signal	Always
ECSPI4.SS0	P2-4~*	IO	Chip select signal	Always
ECSPI4.SS1	P2-12~*	IO	Chip select signal	Always
ECSPI4.SS2	P2-16*~	IO	Chip select signal	Always
ECSPI4.SS3	P2-24*~	IO	Chip select signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.16 Quad SPI

UCM-iMX7 is equipped with two instances of the Quad SPI interface. The interface is implemented with the i.MX7 integrated QSPI controller. The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the QSPI interface signals

Table 37 QSPI Interface Signals

Signal Name	Pin #	Type	Description	Availability
QSPI.A_DATA[0]	P2-93*	IO	I/O data signal 1 port 0 for serial flash device A	Always
QSPI.A_DATA[1]	P2-89*	IO	I/O data signal 1 port 1 for serial flash device A	Always
QSPI.A_DATA[2]	P2-95*	IO	I/O data signal 1 port 2 for serial flash device A	Always
QSPI.A_DATA[3]	P2-97*	IO	I/O data signal 1 port 3 for serial flash device A	Always
QSPI.A_DQS	P2-77*	I	Data strobe signal 1 to serial flash device A	Always
QSPI.A_SCLK	P2-75*	O	Serial clock output 1 to serial flash device A	Always

Signal Name	Pin #	Type	Description	Availability
QSPI.A_SS0_B	P2-73*	O	Chip select 1 port 0 for serial flash device A	Always
QSPI.A_SS1_B	P2-71*	O	Chip select 1 port 1 for serial flash device A	Always
QSPI.B_DATA[0]	P2-69*	IO	I/O data signal 1 port 0 for serial flash device B	Always
QSPI.B_DATA[1]	P2-65*	IO	I/O data signal 1 port 1 for serial flash device B	Always
QSPI.B_DATA[2]	P2-63*	IO	I/O data signal 1 port 2 for serial flash device B	Always
QSPI.B_DATA[3]	P2-61*	IO	I/O data signal 1 port 3 for serial flash device B	Always
QSPI.B_DQS	P2-59*	I	Data strobe signal 1 to serial flash device B	Always
QSPI.B_SCLK	P2-57*	O	Serial clock output 1 to serial flash device B	Always
QSPI.B_SS0_B	P2-53*	O	Chip select 1 port 0 for serial flash device B	Always
QSPI.B_SS1_B	P2-51*	O	Chip select 1 port 1 for serial flash device B	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.17 CAN Bus

UCM-iMX7 is equipped with two instances of the CAN bus controller. Each interface is implemented with the i.MX7 integrated FlexCAN module. The following features are supported by the DCAN module:

- Supports CAN protocol version 2.0B.
- Programmable bit rate up to 1 Mbps.
- Flexible Mailboxes of eight bytes data length
- 100% backwards compatibility with previous FLEXCAN version

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the CAN bus interface signals

Table 38 CAN bus 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN1.RX	P1-26*	I	FLEXCAN receive pin	not "E"
CAN1.RX	P1-76*	I	FLEXCAN receive pin	Always
CAN1.TX	P1-24*	O	FLEXCAN transmit pin	not "E"
CAN1.TX	P1-72*	O	FLEXCAN transmit pin	Always

Table 39 CAN bus 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN2.RX	P2-94*	I	FLEXCAN receive pin	Always
CAN2.RX	P1-57*	I	FLEXCAN receive pin	not "E"
CAN2.TX	P1-18*	O	FLEXCAN transmit pin	not "E"
CAN2.TX	P2-96*	O	FLEXCAN transmit pin	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.18 ADC

UCM-iMX7 is equipped with a single instance of the 12-bit general purpose analog to digital converter module (ADC). The i.MX7 ADC module supports the following main features:

- 12-bit word size.
- Support single and continuous conversion.
- Support compare mode and channel auto disable if data match the requirement.
- Support average conversion and flexible 4, 8, 16, 32 number of conversion data.
- Configurable sample time and conversion speed / power. Sample rates up to 1MHz.

- Conversion complete, hardware average complete, compare, DMA, time out flag and interrupt.
- Automatic compare with interrupt for less than, greater than, and equal to, within range, or out-of-range, programmable value.

NOTE: UCM-iMX7 ADC port 2 is available only without the 'I' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the ADC interface signals

Table 40 ADC1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ADC1_IN0	P1-79	AI	Analog channel 1 input 0	not "I"
ADC1_IN1	P1-81	AI	Analog channel 1 input 1	not "I"
ADC1_IN2	P1-83	AI	Analog channel 1 input 2	not "I"
ADC1_IN3	P1-85	AI	Analog channel 1 input 3	not "I"

4.19 Resistive Touch Interface

UCM-iMX7 features an optional on-board Texas Instruments TSC2046 resistive touch-screen controller. The controller is communicating with the i.MX7 SoC over the SPI1 interface. The interface supports 4-wire touch panels and is available through the UCM-iMX7 carrier board interface.

NOTE: UCM-iMX7 Resistive touch interface is available only with the 'I' ordering option.

Please refer to Texas Instruments TSC2046 datasheet for additional details. The table below summarizes the resistive touch interface signals

Table 41 Resistive Touch Interface Signals

Signal Name	Pin #	Type	Description	Availability
RTOUCH_X-	P1-81	AIO	Touch screen X- (left)	"I"
RTOUCH_X+	P1-79	AIO	Touch screen X+ (right)	"I"
RTOUCH_Y-	P1-85	AIO	Touch screen Y- (bottom)	"I"
RTOUCH_Y+	P1-83	AIO	Touch screen Y+ (top)	"I"

4.20 PWM

Four PWM output signals are available at the UCM-iMX7 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the PWM interface signals

Table 42 PWM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1.OUT	P1-19*	O	PWM1 functional output	not "E"
PWM1.OUT	P1-45*	O	PWM1 functional output	Always

Signal Name	Pin #	Type	Description	Availability
PWM1.OUT	P2-68*	O	PWM1 functional output	not "A"

Table 43 PWM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM2.OUT	P1-10*	O	PWM2 functional output	not "E"
PWM2.OUT	P1-69*	O	PWM2 functional output	Always
PWM2.OUT	P2-100*	O	PWM2 functional output	Always

Table 44 PWM3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM3.OUT	P1-38*	O	PWM3 functional output	not "E"
PWM3.OUT	P2-92*	O	PWM3 functional output	Always
PWM3.OUT	P2-1*	O	PWM3 functional output	Always

Table 45 PWM4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM4.OUT	P1-20*	O	PWM4 functional output	not "E"
PWM4.OUT	P2-3*	O	PWM4 functional output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.21 General Purpose Timer

UCM-iMX7 features 3 instances of a general purpose timer module (GPT). The GPT is capable of generating an event on UCM-iMX7 carrier board interface and/or a system interrupt when the timer reaches a programmed value. Additional GPT functionality includes capturing the counter value in a register (this can be triggered by an event on the UCM-iMX7 carrier board interface). The following main features are supported with each GPT module:

- One 32-bit up-counter with clock source selection, including external clock.
- 12-bit prescaler for division of input clock frequency.
- Two “Capture Event” trigger inputs (2 channels) with a programmable trigger edge.
- Three “Compare Event Occurred” outputs (3 channels) with programmable “active” state. A "forced compare" feature is also available.
- Interrupt generation at capture, compare, and rollover events.
- Restart or free-run modes for counter operations.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the GPT interface signals

Table 46 GPT1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT1.CAPTURE1	P2-81^*	I; PD	Input pin for a capture event	Always
GPT1.CAPTURE2	P2-66^*	I; PD	Input pin for a capture event	Always
GPT1.CLK	P2-83^*	I; PD	Input pin for an option external clock to use with timer	Always
GPT1.COMPARE1	P2-80*	O	Output pin that indicates a "compare event" occurrence	Always
GPT1.COMPARE2	P2-87^*	O; PD	Output pin that indicates a "compare event" occurrence	Always
GPT1.COMPARE3	P2-85^*	O; PD	Output pin that indicates a "compare event" occurrence	Always

Table 47 GPT2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT2.CAPTURE1	P1-88*	I	Input pin for a capture event	not "A"
GPT2.CAPTURE2	P1-92*	I	Input pin for a capture event	not "A"
GPT2.CLK	P1-94*	I	Input pin for an option external clock to use with timer	not "A"
GPT2.COMPARE1	P1-12*	O	Output pin that indicates a "compare event" occurrence	not "E"
GPT2.COMPARE2	P1-14*	O	Output pin that indicates a "compare event" occurrence	not "E"
GPT2.COMPARE3	P1-86*	O	Output pin that indicates a "compare event" occurrence	not "A"

Table 48 GPT4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT4.CAPTURE1	P1-37*	I	Input pin for a capture event	not "WB"
GPT4.CAPTURE2	P1-25*	I	Input pin for a capture event	not "WB"
GPT4.CLK	P1-29*	I	Input pin for an option external clock to use with timer	not "WB"
GPT4.COMPARE1	P1-31*	O	Output pin that indicates a "compare event" occurrence	not "WB"
GPT4.COMPARE2	P1-33*	O	Output pin that indicates a "compare event" occurrence	not "WB"
GPT4.COMPARE3	P1-35*	O	Output pin that indicates a "compare event" occurrence	not "WB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.22 Watch dog Timers

UCM-iMX7 is equipped with four “Watchdog timers” (WDOG) derived from the i.MX7 SoC. The WDOG can be used to protect system from failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a timeout, the WDOG will assert the internal system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. WDOG supports the following main features:

- A configurable timeout counter with periods from 0.5 seconds up to 128 seconds.
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the WDOG interface signals

Table 49 WDOG Interface Signals

Signal Name	Pin #	Type	Description	Availability
WDOG.GLOBAL	P1-92*	IO	Global WDOG signal	not "A"
WDOG1.WDOG_B	P1-45*	IO	This signal will power down the system	Always
WDOG2.WDOG_B	P1-94*	IO	This signal will power down the system	not "A"
WDOG2.WDOG_RST_B_DEB	P1-88*	O	This signal is a reset source for the system	not "A"
WDOG3.WDOG_B	P1-80*	IO	This signal will power down the system	Always
WDOG3.WDOG_RST_B_DEB	P1-78*	O	This signal is a reset source for the system	Always
WDOG4.WDOG_B	P2-27*	IO	This signal will power down the system	Always
WDOG4.WDOG_RST_B_DEB	P2-29*	O	This signal is a reset source for the system	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.23 FlexTimer Module

External signals for two instances of the i.MX7 integrated flexible time module (FTM) are accessible through the UCM-iMX7 carrier board interface. The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The following features are supported:

- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128.
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode.
- In output compare mode the output signal can be set, cleared, or toggled on match.
- All channels can be configured for center-aligned PWM mode.
- Quadrature decoder with input filters, relative position counting, and interrupts on position count or capture of position count on external event.
- Backwards compatible with TPM.
- Software control of PWM outputs.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the flextimer interface signals

Table 50 FLEXTIMER1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXTIMER1.CH[0]	P1-82*~	IO	Flextimer channel 0	Always
FLEXTIMER1.CH[1]	P2-49*~	IO	Flextimer channel 1	Always
FLEXTIMER1.CH[2]	P2-18~*	IO	Flextimer channel 2	Always
FLEXTIMER1.CH[3]	P2-4~*	IO	Flextimer channel 3	Always
FLEXTIMER1.CH[4]	P1-50^*	IO; PD	Flextimer channel 4	Always
FLEXTIMER1.CH[5]	P2-47^*	IO; PU33	Flextimer channel 5	Always
FLEXTIMER1.CH[5]	P2-6*	IO	Flextimer channel 5	Always
FLEXTIMER1.CH[6]	P1-52^*	IO; PD	Flextimer channel 6	Always
FLEXTIMER1.CH[7]	P1-54^*	IO; PD	Flextimer channel 7	Always
FLEXTIMER1.PHA	P2-8*~	I	Quadrature decoder phase A input	Always
FLEXTIMER1.PHA	P2-1*	I	Quadrature decoder phase A input	Always
FLEXTIMER1.PHB	P2-76*	I	Quadrature decoder phase B input	not "E"
FLEXTIMER1.PHB	P2-3*	I	Quadrature decoder phase B input	Always

Table 51 FLEXTIMER2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXTIMER2.CH[0]	P2-12~*	IO	Flextimer channel 0	Always
FLEXTIMER2.CH[1]	P2-16*~	IO	Flextimer channel 1	Always
FLEXTIMER2.CH[2]	P2-24*~	IO	Flextimer channel 2	Always
FLEXTIMER2.CH[3]	P2-10*~	IO	Flextimer channel 3	Always
FLEXTIMER2.CH[4]	P1-15*	IO	Flextimer channel 4	not "WB"
FLEXTIMER2.CH[4]	P1-62*	IO	Flextimer channel 4	Always
FLEXTIMER2.CH[5]	P1-23*	IO	Flextimer channel 5	not "WB"
FLEXTIMER2.CH[5]	P2-37*	IO	Flextimer channel 5	Always
FLEXTIMER2.CH[6]	P1-44*	IO	Flextimer channel 6	Always
FLEXTIMER2.CH[6]	P1-21*	IO	Flextimer channel 6	not "WB"
FLEXTIMER2.CH[7]	P1-40*	IO	Flextimer channel 7	Always
FLEXTIMER2.CH[7]	P1-17*	IO	Flextimer channel 7	not "WB"
FLEXTIMER2.PHA	P1-77*	I	Quadrature decoder phase A input	Always
FLEXTIMER2.PHA	P1-100*	I	Quadrature decoder phase A input	not "A"
FLEXTIMER2.PHB	P2-22*	I	Quadrature decoder phase B input	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.24 Keypad interface

UCM-iMX7 carrier board interface allows access the i.MX7 integrated keypad port (KPP). The KPP is a 16-bit peripheral designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad. The KPP includes these distinctive features:

- Supports up to an 8 x 8 external key pad matrix. (up to 7x7 with UCM-iMX7)
- Open drain design.
- Glitch suppression circuit design.
- Multiple-key detection.
- Long key-press detection.
- Standby key-press detection.
- Synchronizer chain clear.
- Supports a 2-point and 3-point contact key matrix.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the KPP interface signals

Table 52 KPP Interface Signals

Signal Name	Pin #	Type	Description	Availability
KPP.COL[0]	P1-20*	IO	Column input or output	not "E"
KPP.COL[0]	P2-71*	IO	Column input or output	Always
KPP.COL[1]	P1-32*	IO	Column input or output	not "E"
KPP.COL[1]	P2-75*	IO	Column input or output	Always
KPP.COL[2]	P1-24*	IO	Column input or output	not "E"
KPP.COL[2]	P2-97*	IO	Column input or output	Always
KPP.COL[3]	P1-10*	IO	Column input or output	not "E"
KPP.COL[3]	P2-89*	IO	Column input or output	Always
KPP.COL[5]	P1-45*	IO	Column input or output	Always
KPP.COL[6]	P2-1*	IO	Column input or output	Always
KPP.COL[7]	P1-21*	IO	Column input or output	not "WB"
KPP.ROW[0]	P1-38*	IO	Row input or output	not "E"
KPP.ROW[0]	P2-73*	IO	Row input or output	Always
KPP.ROW[1]	P1-30*	IO	Row input or output	not "E"
KPP.ROW[1]	P2-77*	IO	Row input or output	Always
KPP.ROW[2]	P1-26*	IO	Row input or output	not "E"
KPP.ROW[2]	P2-95*	IO	Row input or output	Always
KPP.ROW[3]	P1-19*	IO	Row input or output	not "E"
KPP.ROW[3]	P2-93*	IO	Row input or output	Always
KPP.ROW[5]	P1-69*	IO	Row input or output	Always
KPP.ROW[6]	P2-3*	IO	Row input or output	Always
KPP.ROW[7]	P1-17*	IO	Row input or output	not "WB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.25 SmartCard interface (SIM)

The i.MX7 features two instances of the smart card identification module (SIM). The module is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards and compatible with ISO/IEC 7816-3. The UCM-iMX7 carrier board interface allows access to signals of both interfaces. Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SIM interface signals

Table 53 SIM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SIM1.PORT1_CLK	P2-65*	O	Clock for the smartcard	Always
SIM1.PORT1_PD	P2-59*	I	Card insertion detect	Always
SIM1.PORT1_PD	P1-98*	I	Card insertion detect	not "A"
SIM1.PORT1_RST_B	P2-63*	O	Reset signal	Always
SIM1.PORT1_SVEN	P2-61*	O	Vcc enable	Always
SIM1.PORT1_TRXD	P2-69*	IO	Transmit/receive data	Always
SIM1.PORT2_CLK	P2-89*	O	Clock for the smartcard	Always
SIM1.PORT2_PD	P2-77*	I	Card insertion detect	Always
SIM1.PORT2_RST_B	P2-95*	O	Reset signal	Always
SIM1.PORT2_SVEN	P2-97*	O	Vcc enable	Always
SIM1.PORT2_TRXD	P2-93*	IO	Transmit/receive data	Always

Table 54 SIM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SIM2.PORT1_CLK	P2-53*	O	Clock for the smartcard	Always
SIM2.PORT1_CLK	P1-25*	O	Clock for the smartcard	not "WB"
SIM2.PORT1_PD	P1-35*	I	Card insertion detect	not "WB"
SIM2.PORT1_RST_B	P2-51*	O	Reset signal	Always
SIM2.PORT1_RST_B	P1-31*	O	Reset signal	not "WB"
SIM2.PORT1_SVEN	P1-33*	O	Vcc enable	not "WB"
SIM2.PORT1_TRXD	P2-57*	IO	Transmit/receive data	Always
SIM2.PORT1_TRXD	P1-37*	IO	Transmit/receive data	not "WB"
SIM2.PORT2_CLK	P2-73*	O	Clock for the smartcard	Always
SIM2.PORT2_RST_B	P2-71*	O	Reset signal	Always
SIM2.PORT2_TRXD	P2-75*	IO	Transmit/receive data	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.26 GPIO

Up-to 112 of the i.MX7 general purpose input/output (GPIO) signals are available through the UCM-iMX7 carrier board interface. When configured as an output, it is possible to write to an i.MX7 register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX7 register. In addition GPIOs peripheral can produce interrupts.

NOTE: Not all GPIO signals supported by the i.MX7 SoC are available through the UCM-iMX7 carrier board interface.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the GPIO interface signals

Table 55 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1.IO[1]	P2-68*	IO	General purpose input/output	not "A"
GPIO1.IO[10]	P2-1*	IO	General purpose input/output	Always
GPIO1.IO[11]	P2-3*	IO	General purpose input/output	Always
GPIO1.IO[2]	P2-100*	IO	General purpose input/output	Always

Signal Name	Pin #	Type	Description	Availability
GPIO1.IO[3]	P2-92*	IO	General purpose input/output	Always
GPIO1.IO[5]	P2-6*	IO	General purpose input/output	Always
GPIO1.IO[8]	P1-45*	IO	General purpose input/output	Always
GPIO1.IO[9]	P1-69*	IO	General purpose input/output	Always
GPIO2.IO[0]	P2-93*	IO	General purpose input/output	Always
GPIO2.IO[1]	P2-89*	IO	General purpose input/output	Always
GPIO2.IO[10]	P2-63*	IO	General purpose input/output	Always
GPIO2.IO[11]	P2-61*	IO	General purpose input/output	Always
GPIO2.IO[12]	P2-59*	IO	General purpose input/output	Always
GPIO2.IO[13]	P2-57*	IO	General purpose input/output	Always
GPIO2.IO[14]	P2-53*	IO	General purpose input/output	Always
GPIO2.IO[15]	P2-51*	IO	General purpose input/output	Always
GPIO2.IO[2]	P2-95*	IO	General purpose input/output	Always
GPIO2.IO[28]	P2-20*	IO	General purpose input/output	Always
GPIO2.IO[29]	P2-35*	IO	General purpose input/output	Always
GPIO2.IO[3]	P2-97*	IO	General purpose input/output	Always
GPIO2.IO[30]	P1-77*	IO	General purpose input/output	Always
GPIO2.IO[31]	P2-22*	IO	General purpose input/output	Always
GPIO2.IO[4]	P2-77*	IO	General purpose input/output	Always
GPIO2.IO[5]	P2-75*	IO	General purpose input/output	Always
GPIO2.IO[6]	P2-73*	IO	General purpose input/output	Always
GPIO2.IO[7]	P2-71*	IO	General purpose input/output	Always
GPIO2.IO[8]	P2-69*	IO	General purpose input/output	Always
GPIO2.IO[9]	P2-65*	IO	General purpose input/output	Always
GPIO3.IO[0]	P2-33*	IO	General purpose input/output	Always
GPIO3.IO[1]	P1-28*	IO	General purpose input/output	Always
GPIO3.IO[10]	P2-64^*	IO; PD	General purpose input/output	Always
GPIO3.IO[11]	P2-78^*	IO; PD	General purpose input/output	Always
GPIO3.IO[12]	P2-45^*	IO; PD	General purpose input/output	Always
GPIO3.IO[13]	P1-11^*	IO; PD	General purpose input/output	Always
GPIO3.IO[14]	P1-13^*	IO; PD	General purpose input/output	Always
GPIO3.IO[15]	P1-42^*	IO; PD	General purpose input/output	Always
GPIO3.IO[16]	P1-56^*	IO; PD	General purpose input/output	Always
GPIO3.IO[17]	P1-68^*	IO; PD/PU33	General purpose input/output. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[18]	P1-64^*	IO; PU33/PD	General purpose input/output. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[19]	P1-66^*	IO; PU33/PD	General purpose input/output. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[2]	P1-48*	IO	General purpose input/output	Always
GPIO3.IO[20]	P1-60^*	IO; PD	General purpose input/output	Always
GPIO3.IO[21]	P1-50^*	IO; PD	General purpose input/output	Always
GPIO3.IO[22]	P2-47^*	IO; PU33	General purpose input/output	Always
GPIO3.IO[23]	P1-52^*	IO; PD	General purpose input/output	Always
GPIO3.IO[24]	P1-54^*	IO; PD	General purpose input/output	Always
GPIO3.IO[25]	P1-62*	IO	General purpose input/output	Always
GPIO3.IO[26]	P2-37*	IO	General purpose input/output	Always
GPIO3.IO[27]	P1-44*	IO	General purpose input/output	Always
GPIO3.IO[28]	P1-40*	IO	General purpose input/output	Always
GPIO3.IO[3]	P2-41*	IO	General purpose input/output	Always
GPIO3.IO[4]	P2-80*	IO	General purpose input/output	Always
GPIO3.IO[5]	P2-87^*	IO; PD	General purpose input/output	Always
GPIO3.IO[6]	P2-85^*	IO; PD	General purpose input/output	Always
GPIO3.IO[7]	P2-83^*	IO; PD	General purpose input/output	Always
GPIO3.IO[8]	P2-81^*	IO; PD	General purpose input/output	Always
GPIO3.IO[9]	P2-66^*	IO; PD	General purpose input/output	Always
GPIO4.IO[0]	P2-84*	IO	General purpose input/output	Always
GPIO4.IO[1]	P2-82*	IO	General purpose input/output	Always
GPIO4.IO[10]	P1-80*	IO	General purpose input/output	Always
GPIO4.IO[11]	P1-78*	IO	General purpose input/output	Always
GPIO4.IO[12]	P2-94*	IO	General purpose input/output	Always
GPIO4.IO[13]	P2-96*	IO	General purpose input/output	Always
GPIO4.IO[14]	P2-27*	IO	General purpose input/output	Always
GPIO4.IO[15]	P2-29*	IO	General purpose input/output	Always
GPIO4.IO[20]	P2-90*	IO	General purpose input/output	Always
GPIO4.IO[21]	P2-88*	IO	General purpose input/output	Always
GPIO4.IO[22]	P2-72*	IO	General purpose input/output	Always

Signal Name	Pin #	Type	Description	Availability
GPIO4.IO[23]	P2-70*	IO	General purpose input/output	Always
GPIO4.IO[6]	P1-95*	IO	General purpose input/output	not "WB"
GPIO4.IO[7]	P1-91*	IO	General purpose input/output	not "WB"
GPIO4.IO[8]	P1-76*	IO	General purpose input/output	Always
GPIO4.IO[9]	P1-72*	IO	General purpose input/output	Always
GPIO5.IO[0]	P1-82*~	IO	General purpose input/output	Always
GPIO5.IO[1]	P2-49*~	IO	General purpose input/output	Always
GPIO5.IO[10]	P1-74*	IO	General purpose input/output	not "E"
GPIO5.IO[12]	P1-29*	IO	General purpose input/output	not "WB"
GPIO5.IO[13]	P1-37*	IO	General purpose input/output	not "WB"
GPIO5.IO[14]	P1-25*	IO	General purpose input/output	not "WB"
GPIO5.IO[15]	P1-31*	IO	General purpose input/output	not "WB"
GPIO5.IO[16]	P1-33*	IO	General purpose input/output	not "WB"
GPIO5.IO[17]	P1-35*	IO	General purpose input/output	not "WB"
GPIO5.IO[2]	P2-18~*	IO	General purpose input/output	Always
GPIO5.IO[3]	P2-4~*	IO	General purpose input/output	Always
GPIO5.IO[4]	P2-12~*	IO	General purpose input/output	Always
GPIO5.IO[5]	P2-16*~	IO	General purpose input/output	Always
GPIO5.IO[6]	P2-24*~	IO	General purpose input/output	Always
GPIO5.IO[7]	P2-10*~	IO	General purpose input/output	Always
GPIO5.IO[8]	P2-8*~	IO	General purpose input/output	Always
GPIO5.IO[9]	P2-76*	IO	General purpose input/output	not "E"
GPIO6.IO[16]	P1-98*	IO	General purpose input/output	not "A"
GPIO6.IO[17]	P1-100*	IO	General purpose input/output	not "A"
GPIO6.IO[19]	P1-15*	IO	General purpose input/output	not "WB"
GPIO6.IO[20]	P1-23*	IO	General purpose input/output	not "WB"
GPIO6.IO[21]	P1-21*	IO	General purpose input/output	not "WB"
GPIO6.IO[22]	P1-17*	IO	General purpose input/output	not "WB"
GPIO7.IO[0]	P1-19*	IO	General purpose input/output	not "E"
GPIO7.IO[1]	P1-10*	IO	General purpose input/output	not "E"
GPIO7.IO[10]	P1-12*	IO	General purpose input/output	not "E"
GPIO7.IO[11]	P1-14*	IO	General purpose input/output	not "E"
GPIO7.IO[12]	P1-86*	IO	General purpose input/output	not "A"
GPIO7.IO[13]	P1-94*	IO	General purpose input/output	not "A"
GPIO7.IO[14]	P1-88*	IO	General purpose input/output	not "A"
GPIO7.IO[15]	P1-92*	IO	General purpose input/output	not "A"
GPIO7.IO[2]	P1-26*	IO	General purpose input/output	not "E"
GPIO7.IO[3]	P1-24*	IO	General purpose input/output	not "E"
GPIO7.IO[4]	P1-30*	IO	General purpose input/output	not "E"
GPIO7.IO[5]	P1-32*	IO	General purpose input/output	not "E"
GPIO7.IO[6]	P1-38*	IO	General purpose input/output	not "E"
GPIO7.IO[7]	P1-20*	IO	General purpose input/output	not "E"
GPIO7.IO[8]	P1-57*	IO	General purpose input/output	not "E"
GPIO7.IO[9]	P1-18*	IO	General purpose input/output	not "E"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.27 External DMA Requests

UCM-iMX7 provides two optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the i.MX7 internal SDMA controller. A logical channel can be configured to respond to an external synchronization request.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the SDMA interface signals

Table 56 SDMA Interface Signals

Signal Name	Pin #	Type	Description	Availability
SDMA.EXT_EVENT[0]	P2-94*	I	External DMA request 0	Always
SDMA.EXT_EVENT[0]	P2-76*	I	External DMA request 0	not "E"
SDMA.EXT_EVENT[1]	P2-96*	I	External DMA request 1	Always
SDMA.EXT_EVENT[1]	P1-74*	I	External DMA request 1	not "E"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.28 General Purpose clocks

The i.MX7 clock controller module (CCM) signals are fully accessible through the UCM-iMX7 carrier board interface. The CCM allows the i.MX7 SoC to utilize carrier board generated clocks as well as providing on-SoC generated clocks to the carrier board. Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the CCM interface signals

Table 57 CCM Interface Signals

Signal Name	Pin #	Type	Description	Availability
CCM.CLKO1	P1-82~*	O	SoC Clock 1 output for off-som devices	Always
CCM.CLKO1	P2-100*	O	SoC Clock 1 output for off-som devices	Always
CCM.CLKO2	P2-49~*	O	SoC Clock 2 output for off-som devices	Always
CCM.CLKO2	P2-92*	O	SoC Clock 2 output for off-som devices	Always
CCM.ENET1_REF_CLK_ROOT	P1-72*	O	ENET Reference Clock 1	Always
CCM.ENET1_REF_CLK_ROOT	P2-100*	O	ENET Reference Clock 1	Always
CCM.ENET1_REF_CLK_ROOT	P1-86*	O	ENET Reference Clock 1	not "A"
CCM.ENET2_REF_CLK_ROOT	P1-80*	O	ENET Reference Clock 2	Always
CCM.ENET2_REF_CLK_ROOT	P2-92*	O	ENET Reference Clock 2	Always
CCM.ENET2_REF_CLK_ROOT	P2-20*	O	ENET Reference Clock 2	Always
CCM.ENET3_REF_CLK_ROOT	P1-69*	O	ENET Reference Clock 3	Always
CCM.ENET3_REF_CLK_ROOT	P1-78*	O	ENET Reference Clock 3	Always
CCM.ENET3_REF_CLK_ROOT	P2-68*	O	ENET Reference Clock 3	not "A"
CCM.EXT_CLK1	P2-16~*	I	External Clock 1	Always
CCM.EXT_CLK1	P1-86*	I	External Clock 1	not "A"
CCM.EXT_CLK2	P2-24~*	I	External Clock 2	Always
CCM.EXT_CLK2	P1-94*	I	External Clock 2	not "A"
CCM.EXT_CLK3	P2-10~*	I	External Clock 3	Always
CCM.EXT_CLK3	P1-88*	I	External Clock 3	not "A"
CCM.EXT_CLK4	P2-8~*	I	External Clock 4	Always
CCM.EXT_CLK4	P1-92*	I	External Clock 4	not "A"
CCM.PMIC_READY	P1-69*	I	Signal coming from PMIC to indicate that the voltage started to change as result of hange in PMIC_STBY_REQ	Always
CCM.PMIC_READY	P2-84*	I	Signal coming from PMIC to indicate that the voltage started to change as result of hange in PMIC_STBY_REQ	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.29 Debug Interfaces

The UCM-iMX7 exposes both of the i.MX7 Cortex-A9 core debug interfaces. The core supports debug through real-time trace via ARM CoreSight PTM, ETB and TPIU modules and static debug via JTAG.

4.29.1 JTAG

The UCM-iMX7 JTAG interface is derived from the i.MX7 SoC integrated SJC module. The SJC module implements and manages the daisy-chained topology consisting of its' own TAP and those of the SDMA, and the ARM Debug Access Port (DAP). The SJC supports the following main features:

- IEEE P1149.1, 1149.6 (standard JTAG) interface to off-chip test and development equipment
- Debug-related control and status

For additional details, please refer to the SJC chapter of the "i.MX7 Reference Manual". The JTAG interface signals are accessible through onboard test points. Please contact Compulab for details.

4.29.2 Cortex-A9 Real Time Trace

The i.MX7 Cortex-A9 trace interface is accessible through the carrier board interface. The Cortex-A9 core platform supports static debug through logic internal to i.MX7. This includes the capability of real time trace via ARM CoreSight PTM, ETB and TPIU modules. The CTI and CTM modules allow cross-triggering of internal and external trigger sources.

For additional details, please refer to the ARM Cortex A9 MPCore Platform (ARM) chapter of the "i.MX7 Reference Manual". The table below summarizes the ARM CoreSight debug/Trace interface signals

Table 58 ARM CoreSight debug/Trace Interface Signals

Signal Name	Pin #	Type	Description	Availability
CORESIGHT.EVENTI	P2-80*	I	Input event signal	Always
CORESIGHT.EVENTO	P1-52^*	O; PD	Output event signal	Always
CORESIGHT.TRACE[0]	P2-87^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[1]	P2-85^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[10]	P1-42^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[11]	P1-56^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[12]	P1-68^*	O; PD/PU33	Trace signal. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
CORESIGHT.TRACE[13]	P1-64^*	O; PU33/PD	Trace signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CORESIGHT.TRACE[14]	P1-66^*	O; PU33/PD	Trace signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CORESIGHT.TRACE[15]	P1-60^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[2]	P2-83^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[3]	P2-81^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[4]	P2-66^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[5]	P2-64^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[6]	P2-78^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[7]	P2-45^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[8]	P1-11^*	O; PD	Trace signal	Always
CORESIGHT.TRACE[9]	P1-13^*	O; PD	Trace signal	Always
CORESIGHT.TRACE_CLK	P1-50^*	O; PD	Clock signal	Always
CORESIGHT.TRACE_CTL	P2-47^*	O; PU33	Control signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

5 SYSTEM LOGIC

UCM-iMX7 allows access to several system logic related signals through the carrier board interface. Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Supply

The UCM-iMX7 supports two power supply options:

- Regulated DC supply (3.7V Typical).
- Lithium-ion polymer battery

UCM-iMX7 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board. The table below summarizes the power interface signals

Table 59 POWER Interface Signals

Signal Name	Pin #	Type	Description	Availability
GND	P1-99	PI	Main Ground connection	Always
GND	P2-98	PI	Main Ground connection	Always
GND	P2-91	PI	Main Ground connection	Always
GND	P1-87	PI	Main Ground connection	Always
GND	P2-86	PI	Main Ground connection	Always
GND	P1-84	PI	Main Ground connection	Always
GND	P2-79	PI	Main Ground connection	Always
GND	P1-75	PI	Main Ground connection	Always
GND	P2-74	PI	Main Ground connection	Always
GND	P1-70	PI	Main Ground connection	Always
GND	P2-67	PI	Main Ground connection	Always
GND	P1-63	PI	Main Ground connection	Always
GND	P2-62	PI	Main Ground connection	Always
GND	P1-58	PI	Main Ground connection	Always
GND	P2-55	PI	Main Ground connection	Always
GND	P1-51	PI	Main Ground connection	Always
GND	P2-50	PI	Main Ground connection	Always
GND	P1-46	PI	Main Ground connection	Always
GND	P2-43	PI	Main Ground connection	Always
GND	P1-39	PI	Main Ground connection	Always
GND	P2-38	PI	Main Ground connection	Always
GND	P1-34	PI	Main Ground connection	Always
GND	P2-31	PI	Main Ground connection	Always
GND	P1-27	PI	Main Ground connection	Always
GND	P2-26	PI	Main Ground connection	Always
GND	P2-19	PI	Main Ground connection	Always
GND	P2-14	PI	Main Ground connection	Always
GND	P2-7	PI	Main Ground connection	Always
GND	P2-2	PI	Main Ground connection	Always
VCC_RTC	P1-96	PI	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave unconnected if RTC functionality is not required.	Always
VSYS	P1-22	PI	Main Power connection	Always
VSYS	P1-16	PI	Main Power connection	Always
VSYS	P1-9	PI	Main Power connection	Always
VSYS	P1-8	PI	Main Power connection	Always
VSYS	P1-7	PI	Main Power connection	Always
VSYS	P1-6	PI	Main Power connection	Always
VSYS	P1-5	PI	Main Power connection	Always
VSYS	P1-4	PI	Main Power connection	Always
VSYS	P1-3	PI	Main Power connection	Always
VSYS	P1-2	PI	Main Power connection	Always
VSYS	P1-1	PI	Main Power connection	Always

5.2 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX7. Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the reset interface signals

Table 60 Reset Interface Signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	P1-89	I	i.MX7 SoC cold reset input. A logic low input resets all modules and logic in the SoC	Always

5.3 Boot Sequence

UCM-iMX7 boot sequence defines which interface/media is used by UCM-iMX7 to load and execute the initial software (such as U-boot). UCM-iMX7 can load initial software from the following interfaces/media:

- The on-board primary boot device (SPI Flash with pre-flashed boot-loader).
- An external SD/MMC card using the MMC/SD/SDIO 0 interface

UCM-iMX7 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by UCM-iMX7:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows UCM-iMX7 to boot from an external SD card, effectively bypassing the onboard SPI Flash.

The table below summarizes boot sequences and devices supported with CL-SOM-iMX6

Table 61 UCM-iMX7 Boot sequences

sequence	ALT_BOOT	First	Second	Third	Fourth
Standard	Low or floating	Onboard SPI Flash		SD card on "MMC/SD/SDIO1" (only if card is detected, 1-bit mode)	Host PC on "Native USB port 1" in serial mode
Alternate	High	SD card on "MMC/SD/SDIO1" (4-bit mode)	Onboard SPI Flash		

NOTE: If during an alternate boot sequence, UCM-iMX7 cannot load the initial software from the external SD card, UCM-iMX7 will fall back and try to load the initial software from the onboard SPI flash.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system. The table below summarizes the alternative boot selection interface signals

Table 62 Alternative Boot selection Interface Signals

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P1-90	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always

5.4 System and Miscellaneous Signals

5.4.1 External regulator control and power management

UCM-iMX7 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX7 SoC. The logic that controls both signals draws its power from the VCC_RTC power rail, meaning that this power supply must always be present in order to use the external regulator control features.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that UCM-iMX7 is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the Power Control interface signals

Table 63 Power Control Interface Signals

Signal Name	Pin #	Type	Description	Availability
ONOFF	P1-97	I	i.MX7 SoC ONOFF input. In normal mode, may be connected to ON/OFF button (De-bouncing provided at this input). This signal is pulled up to RTC supply voltage generated by PF3000 PMIC onboard UCM-iMX7. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes "forced" OFF.	Always
PMIC_ON_REQ	P1-93	O	Active high power-up request output from i.MX7 SoC. This signal is referenced to RTC supply voltage generated by PF3000 PMIC onboard UCM-iMX7	Always
PMIC_STBY_REQ	P2-39	O	When the processor enters SUSPEND mode, it will assert this signal. This signal is referenced to RTC supply voltage generated by PF3000 PMIC onboard UCM-iMX7	Always

5.4.2 Flash Write-protection

The EEPROM_WP signal can be used to prevent accidental corruption of the data stored on the onboard SPI Flash as well as the onboard ID EEPROM. The UCM-iMX7 on-board EEPROM is used to store board specific production information while the onboard SPI flash is used to store the boot-loader as described in chapter 3.2.2.

NOTE: The EEPROM_WP must be used in conjunction with SW to enable SPI Flash write protection. Using the EEPROM_WP signal alone will not enable SPI Flash write protection.

The table below summarizes the Flash Write protection interface signals

Table 64 Flash Write protection Interface Signals

Signal Name	Pin #	Type	Description	Availability
EEPROM_WP	P2-99	PU33	Active low input enabling onboard EEPROM write protection and allowing SPI Flash write-protection.	Always

5.5 Signal Multiplexing Characteristics

Up to 116 of the UCM-iMX7 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX7 SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 9 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX7 pins are derived from the i.MX7 SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 65 Multifunctional Signals

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Availability
P1-10	ENET1.RGMII_RD1	PWM2.OUT	I2C3.SDA	UART1.RTS_B		GPIO7.IO[1]	KPP.COL[3]		not "E"
P1-11	LCDIF.DATA[8]		CORESIGHT.TRACE[8]	CSI1.DATA[9]	WEIM.DATA[8]	GPIO3.IO[13]	SRC.BT_CFG[8]		Always
P1-12	ENET1.RGMII_TX_CTL		SAI1.RX_SYNC	GPT2.COMPARE1		GPIO7.IO[10]			not "E"
P1-13	LCDIF.DATA[9]		CORESIGHT.TRACE[9]	CSI1.DATA[8]	WEIM.DATA[9]	GPIO3.IO[14]	SRC.BT_CFG[9]		Always
P1-14	ENET1.RGMII_TXC	ENET1.TX_ER	SAI1.RX_BCLK	GPT2.COMPARE2		GPIO7.IO[11]			not "E"
P1-15	SAI2.TX_SYNC	ECSPI3.MISO	UART4.RX	UART1.CTS_B	FLEXTIMER2.CH[4]	GPIO6.IO[19]			not "WB"
P1-17	SAI2.TX_DATA[0]	ECSPI3.SS0	UART4.RTS_B	UART2.RTS_B	FLEXTIMER2.CH[7]	GPIO6.IO[22]	KPP.ROW[7]		not "WB"
P1-18	ENET1.RGMII_TD3	CAN2.TX	ECSPI2.SS0	I2C4.SDA		GPIO7.IO[9]			not "E"
P1-19	ENET1.RGMII_RD0	PWM1.OUT	I2C3.SCL	UART1.CTS_B		GPIO7.IO[0]	KPP.ROW[3]		not "E"
P1-20	ENET1.RGMII_TD1	PWM4.OUT	ECSPI2.RDY			GPIO7.IO[7]	KPP.COL[0]		not "E"
P1-21	SAI2.RX_DATA[0]	ECSPI3.SCLK	UART4.CTS_B	UART2.CTS_B	FLEXTIMER2.CH[6]	GPIO6.IO[21]	KPP.COL[7]		not "WB"
P1-23	SAI2.TX_BCLK	ECSPI3.MOSI	UART4.TX	UART1.RTS_B	FLEXTIMER2.CH[5]	GPIO6.IO[20]			not "WB"
P1-24	ENET1.RGMII_RD3	CAN1.TX	ECSPI2.MOSI	UART1.TX		GPIO7.IO[3]	KPP.COL[2]		not "E"
P1-25	USDHC2.DATA0	SAI2.RX_DATA[0]	UART4.RX	GPT4.CAPTURE2	SIM2.PORT1_CLK	GPIO5.IO[14]			not "WB"
P1-26	ENET1.RGMII_RD2	CAN1.RX	ECSPI2.SCLK	UART1.RX		GPIO7.IO[2]	KPP.ROW[2]		not "E"
P1-28	LCDIF.ENABLE	ECSPI4.MOSI	ENET1.1588_EVENT3_IN	CSI1.DATA[17]	UART2.TX	GPIO3.IO[1]			Always
P1-29	USDHC2.CLK	SAI2.RX_SYNC	MQS.RIGHT	GPT4.CLK		GPIO5.IO[12]			not "WB"
P1-30	ENET1.RGMII_RX_CTL		ECSPI2.SS1			GPIO7.IO[4]	KPP.ROW[1]		not "E"
P1-31	USDHC2.DATA1	SAI2.TX_BCLK	UART4.TX	GPT4.COMPARE1	SIM2.PORT1_RST_B	GPIO5.IO[15]			not "WB"
P1-32	ENET1.RGMII_RXC	ENET1.RX_ER	ECSPI2.SS2			GPIO7.IO[5]	KPP.COL[1]		not "E"
P1-33	USDHC2.DATA2	SAI2.TX_SYNC	UART4.CTS_B	GPT4.COMPARE2	SIM2.PORT1_SVEN	GPIO5.IO[16]			not "WB"
P1-35	USDHC2.DATA3	SAI2.TX_DATA[0]	UART4.RTS_B	GPT4.COMPARE3	SIM2.PORT1_PD	GPIO5.IO[17]			not "WB"
P1-37	USDHC2.CMD	SAI2.RX_BCLK	MQS.LEFT	GPT4.CAPTURE1	SIM2.PORT1_TRXD	GPIO5.IO[13]			not "WB"
P1-38	ENET1.RGMII_TD0	PWM3.OUT	ECSPI2.SS3			GPIO7.IO[6]	KPP.ROW[0]		not "E"
P1-40	LCDIF.DATA[23]	FLEXTIMER2.CH[7]	ENET2.1588_EVENT3_OUT	CSI1.DATA[10]	WEIM.ADDR[26]	GPIO3.IO[28]	I2C4.SDA		"C1000D"
P1-40	LCDIF.DATA[23]	FLEXTIMER2.CH[7]		CSI1.DATA[10]	WEIM.ADDR[26]	GPIO3.IO[28]	I2C4.SDA		not "C1000D"
P1-42	LCDIF.DATA[10]		CORESIGHT.TRACE[10]	CSI1.DATA[7]	WEIM.DATA[10]	GPIO3.IO[15]	SRC.BT_CFG[10]		Always
P1-44	LCDIF.DATA[22]	FLEXTIMER2.CH[6]	ENET2.1588_EVENT2_OUT	CSI1.DATA[11]	WEIM.ADDR[25]	GPIO3.IO[27]	I2C4.SCL		"C1000D"
P1-44	LCDIF.DATA[22]	FLEXTIMER2.CH[6]		CSI1.DATA[11]	WEIM.ADDR[25]	GPIO3.IO[27]	I2C4.SCL		not "C1000D"
P1-45	GPIO1.IO[8]		WDOG1.WDOG_B	UART3.RX	I2C3.SCL		KPP.COL[5]	PWM1.OUT	Always
P1-48	LCDIF.HSYNC	ECSPI4.SCLK	ENET2.1588_EVENT2_IN	CSI1.DATA[18]	UART2.RTS_B	GPIO3.IO[2]			"C1000D"
P1-48	LCDIF.HSYNC	ECSPI4.SCLK		CSI1.DATA[18]	UART2.RTS_B	GPIO3.IO[2]			not "C1000D"
P1-50	LCDIF.DATA[16]	FLEXTIMER1.CH[4]	CORESIGHT.TRACE_CLK	CSI1.DATA[1]	WEIM.CRE	GPIO3.IO[21]	SRC.BT_CFG[16]		Always
P1-52	LCDIF.DATA[18]	FLEXTIMER1.CH[6]	CORESIGHT.EVENTO	CSI1.DATA[15]	WEIM.CS2_B	GPIO3.IO[23]	SRC.BT_CFG[18]		Always
P1-54	LCDIF.DATA[19]	FLEXTIMER1.CH[7]		CSI1.DATA[14]	WEIM.CS3_B	GPIO3.IO[24]	SRC.BT_CFG[19]		Always
P1-56	LCDIF.DATA[11]		CORESIGHT.TRACE[11]	CSI1.DATA[6]	WEIM.DATA[11]	GPIO3.IO[16]	SRC.BT_CFG[11]		Always
P1-57	ENET1.RGMII_TD2	CAN2.RX	ECSPI2.MISO	I2C4.SCL		GPIO7.IO[8]			not "E"

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Availability
P1-60	LCDIF.DATA[15]		CORESIGHT.TRACE[15]	CSI1.DATA[2]	WEIM.DATA[15]	GPIO3.IO[20]	SRC.BT_CFG[15]		Always
P1-62	LCDIF.DATA[20]	FLEXTIMER2.CH[4]	ENET1.1588_EVENT2_OUT	CSI1.DATA[13]	WEIM.ADDR[23]	GPIO3.IO[25]	I2C3.SCL		Always
P1-64	LCDIF.DATA[13]		CORESIGHT.TRACE[13]	CSI1.DATA[4]	WEIM.DATA[13]	GPIO3.IO[18]	SRC.BT_CFG[13]		Always
P1-66	LCDIF.DATA[14]		CORESIGHT.TRACE[14]	CSI1.DATA[3]	WEIM.DATA[14]	GPIO3.IO[19]	SRC.BT_CFG[14]		Always
P1-68	LCDIF.DATA[12]		CORESIGHT.TRACE[12]	CSI1.DATA[5]	WEIM.DATA[12]	GPIO3.IO[17]	SRC.BT_CFG[12]		Always
P1-69	GPIO1.IO[9]	USDHC1.LCTL	CCM.ENET3_REF_CLK_ROOT	UART3.TX	I2C3.SDA	CCM.PMIC_READY	KPP.ROW[5]	PWM2.OUT	Always
P1-72	I2C1.SDA	UART4.RTS_B	CAN1.TX	ECSPI3.MOSI	CCM.ENET1_REF_CLK_ROOT	GPIO4.IO[9]			Always
P1-74	USDHC2.WP	ENET1.MDC	ENET2.MDC	ECSPI3.SS3	USB.OTG1_ID	GPIO5.IO[10]	SDMA.EXT_EVENT[1]		"C1000D" and not "E"
P1-74	USDHC2.WP	ENET1.MDC		ECSPI3.SS3	USB.OTG1_ID	GPIO5.IO[10]	SDMA.EXT_EVENT[1]		not "C1000D" and not "E"
P1-76	I2C1.SCL	UART4.CTS_B	CAN1.RX	ECSPI3.MISO		GPIO4.IO[8]			Always
P1-77		FLEXTIMER2.PHA			WEIM.AD[9]	GPIO2.IO[30]	LCDIF.HSYNC	LCDIF.DATA[11]	not "C1000D"
P1-77		FLEXTIMER2.PHA	ENET2.CRS		WEIM.AD[9]	GPIO2.IO[30]	LCDIF.HSYNC	LCDIF.DATA[11]	"C1000D"
P1-78		UART4.TX	WDOG3.WDOG_RST_B_DEB	ECSPI3.SS0	CCM.ENET3_REF_CLK_ROOT	GPIO4.IO[11]			Always
P1-80		UART4.RX	WDOG3.WDOG_B	ECSPI3.SCLK	CCM.ENET2_REF_CLK_ROOT	GPIO4.IO[10]			Always
P1-82	USDHC1.CD_B		UART6.RX	ECSPI4.MISO	FLEXTIMER1.CH[0]	GPIO5.IO[0]	CCM.CLKO1		Always
P1-86	ENET1.TX_CLK	CCM.ENET1_REF_CLK_ROOT	SAI1.RX_DATA[0]	GPT2.COMPARE3		GPIO7.IO[12]	CCM.EXT_CLK1		not "A"
P1-88	ENET1.CRS	WDOG2.WDOG_RST_B_DEB	SAI1.TX_SYNC	GPT2.CAPTURE1		GPIO7.IO[14]	CCM.EXT_CLK3		not "A"
P1-89	SRC.POR_B								Always
P1-91	UART3.CTS_B	USB.OTG2_PWR	SAI3.TX_SYNC		ENET1.1588_EVENT1_OUT	GPIO4.IO[7]			"C1000D" and not "WB"
P1-91	UART3.CTS_B		SAI3.TX_SYNC		ENET1.1588_EVENT1_OUT	GPIO4.IO[7]			not "C1000D" and not "WB"
P1-92	ENET1.COL	WDOG.GLOBAL	SAI1.TX_DATA[0]	GPT2.CAPTURE2		GPIO7.IO[15]	CCM.EXT_CLK4		not "A"
P1-93	SNVS_LP_WRAPPER.PMIC_ON_REQ								Always
P1-94	ENET1.RX_CLK	WDOG2.WDOG_B	SAI1.TX_BCLK	GPT2.CLK		GPIO7.IO[13]	CCM.EXT_CLK2		not "A"
P1-95	UART3.RTS_B	USB.OTG2_OC	SAI3.TX_DATA[0]		ENET1.1588_EVENT1_IN	GPIO4.IO[6]			"C1000D" and not "WB"
P1-95	UART3.RTS_B		SAI3.TX_DATA[0]		ENET1.1588_EVENT1_IN	GPIO4.IO[6]			not "C1000D" and not "WB"
P1-97	SRC.RESET_B								Always
P1-98	SAI1.RX_SYNC		SAI2.RX_SYNC	I2C4.SCL	SIM1.PORT1_PD	GPIO6.IO[16]	MQS.RIGHT		not "A"
P1-100	SAI1.RX_BCLK		SAI2.RX_BCLK	I2C4.SDA	FLEXTIMER2.PHA	GPIO6.IO[17]	MQS.LEFT		not "A"
P2-1	GPIO1.IO[10]	USDHC2.LCTL	ENET1.MDIO	UART3.RTS_B	I2C4.SCL	FLEXTIMER1.PHA	KPP.COL[6]	PWM3.OUT	Always
P2-3	GPIO1.IO[11]		ENET1.MDC	UART3.CTS_B	I2C4.SDA	FLEXTIMER1.PHB	KPP.ROW[6]	PWM4.OUT	Always
P2-4	USDHC1.CLK	SAI3.RX_SYNC	UART6.CTS_B	ECSPI4.SS0	FLEXTIMER1.CH[3]	GPIO5.IO[3]			Always
P2-6	GPIO1.IO[5]	USB.OTG1_PWR	FLEXTIMER1.CH[5]	UART5.RTS_B	I2C1.SDA				Always
P2-8	USDHC1.DATA3	SAI3.TX_DATA[0]	UART7.RTS_B	ECSPI3.SS1	FLEXTIMER1.PHA	GPIO5.IO[8]	CCM.EXT_CLK4		Always
P2-10	USDHC1.DATA2	SAI3.TX_SYNC	UART7.CTS_B	ECSPI4.RDY	FLEXTIMER2.CH[3]	GPIO5.IO[7]	CCM.EXT_CLK3		Always
P2-12	USDHC1.CMD	SAI3.RX_BCLK		ECSPI4.SS1	FLEXTIMER2.CH[0]	GPIO5.IO[4]			Always
P2-16	USDHC1.DATA0	SAI3.RX_DATA[0]	UART7.RX	ECSPI4.SS2	FLEXTIMER2.CH[1]	GPIO5.IO[5]	CCM.EXT_CLK1		Always
P2-18	USDHC1.RESET_B	SAI3.MCLK	UART6.RTS_B	ECSPI4.SCLK	FLEXTIMER1.CH[2]	GPIO5.IO[2]			Always
P2-20				CCM.ENET2_REF_CLK_ROOT	WEIM.ADDR[22]	GPIO2.IO[28]	LCDIF.CS	LCDIF.DATA[7]	not "C1000D"
P2-20			ENET2.TX_CLK	CCM.ENET2_REF_CLK_ROOT	WEIM.ADDR[22]	GPIO2.IO[28]	LCDIF.CS	LCDIF.DATA[7]	"C1000D"
P2-22		FLEXTIMER2.PHB			WEIM.EB_B[1]	GPIO2.IO[31]	LCDIF.VSYNC	LCDIF.DATA[12]	not "C1000D"
P2-22		FLEXTIMER2.PHB	ENET2.COL		WEIM.EB_B[1]	GPIO2.IO[31]	LCDIF.VSYNC	LCDIF.DATA[12]	"C1000D"
P2-24	USDHC1.DATA1	SAI3.TX_BCLK	UART7.TX	ECSPI4.SS3	FLEXTIMER2.CH[2]	GPIO5.IO[6]	CCM.EXT_CLK2		Always
P2-27	I2C4.SCL	UART5.RX	WDOG4.WDOG_B	CSI1.PIXCLK	USB.OTG1_ID	GPIO4.IO[14]			Always
P2-29	I2C4.SDA	UART5.TX	WDOG4.WDOG_RST_B_DEB	CSI1.MCLK	USB.OTG2_ID	GPIO4.IO[15]			"C1000D"
P2-29	I2C4.SDA	UART5.TX	WDOG4.WDOG_RST_B_DEB	CSI1.MCLK		GPIO4.IO[15]			not "C1000D"
P2-33	LCDIF.CLK	ECSPI4.MISO	ENET1.1588_EVENT2_IN	CSI1.DATA[16]	UART2.RX	GPIO3.IO[0]			Always
P2-35					WEIM.AD[8]	GPIO2.IO[29]	LCDIF.ENABLE	LCDIF.DATA[6]	not "C1000D"
P2-35			ENET2.RX_CLK		WEIM.AD[8]	GPIO2.IO[29]	LCDIF.ENABLE	LCDIF.DATA[6]	"C1000D"
P2-37	LCDIF.DATA[21]	FLEXTIMER2.CH[5]	ENET1.1588_EVENT3_OUT	CSI1.DATA[12]	WEIM.ADDR[24]	GPIO3.IO[26]	I2C3.SDA		Always
P2-39	CCM.PMIC_VSTBY_REQ								Always
P2-41	LCDIF.VSYNC	ECSPI4.SS0		CSI1.DATA[19]	UART2.CTS_B	GPIO3.IO[3]			not "C1000D"
P2-41	LCDIF.VSYNC	ECSPI4.SS0	ENET2.1588_EVENT3_IN	CSI1.DATA[19]	UART2.CTS_B	GPIO3.IO[3]			"C1000D"
P2-45	LCDIF.DATA[7]		CORESIGHT.TRACE[7]	CSI1.MCLK	WEIM.DATA[7]	GPIO3.IO[12]	SRC.BT_CFG[7]		Always
P2-47	LCDIF.DATA[17]	FLEXTIMER1.CH[5]	CORESIGHT.TRACE_CTL	CSI1.DATA[0]	WEIM.ACLK_FREERUN	GPIO3.IO[22]	SRC.BT_CFG[17]		Always
P2-49	USDHC1.WP		UART6.TX	ECSPI4.MOSI	FLEXTIMER1.CH[1]	GPIO5.IO[1]	CCM.CLKO2		Always
P2-51		SIM2.PORT1_RST_B	QSPI.B_SS1_B	UART7.CTS_B	WEIM.CS1_B	GPIO2.IO[15]	LCDIF.DATA[15]	LCDIF.WR_RWN	Always
P2-53		SIM2.PORT1_CLK	QSPI.B_SS0_B	UART7.RTS_B	WEIM.EB_B[0]	GPIO2.IO[14]	LCDIF.DATA[14]	LCDIF.DATA[22]	Always
P2-57		SIM2.PORT1_TRXD	QSPI.B_SCLK	UART7.TX	WEIM.WAIT	GPIO2.IO[13]	LCDIF.DATA[13]	LCDIF.CS	Always
P2-59		SIM1.PORT1_PD	QSPI.B_DQS	UART7.RX	WEIM.LBA_B	GPIO2.IO[12]	LCDIF.DATA[12]	LCDIF.DATA[21]	Always
P2-61		SIM1.PORT1_SVEN	QSPI.B_DATA[3]	UART6.CTS_B	WEIM.BCLK	GPIO2.IO[11]	LCDIF.DATA[11]	LCDIF.DATA[1]	Always
P2-63		SIM1.PORT1_RST_B	QSPI.B_DATA[2]	UART6.RTS_B	WEIM.CS0_B	GPIO2.IO[10]	LCDIF.DATA[10]	LCDIF.DATA[9]	Always
P2-64	LCDIF.DATA[5]		CORESIGHT.TRACE[5]	CSI1.HSYNC	WEIM.DATA[5]	GPIO3.IO[10]	SRC.BT_CFG[5]		Always
P2-65		SIM1.PORT1_CLK	QSPI.B_DATA[1]	UART6.TX	WEIM.RW	GPIO2.IO[9]	LCDIF.DATA[9]	LCDIF.DATA[0]	Always
P2-66	LCDIF.DATA[4]	GPT1.CAPTURE2	CORESIGHT.TRACE[4]	CSI1.VSYNC	WEIM.DATA[4]	GPIO3.IO[9]	SRC.BT_CFG[4]		Always
P2-68	GPIO1.IO[1]	PWM1.OUT	CCM.ENET3_REF_CLK_ROOT	SAI1.MCLK					not "A"
P2-69		SIM1.PORT1_TRXD	QSPI.B_DATA[0]	UART6.RX	WEIM.OE	GPIO2.IO[8]	LCDIF.DATA[8]	LCDIF.BUSY	Always
P2-70	ECSPI2.SS0	UART7.CTS_B	USDHC1.DATA7	CSI1.DATA[9]	LCDIF.RESET	GPIO4.IO[23]			Always
P2-71		SIM2.PORT2_RST_B	QSPI.A_SS1_B	KPP.COL[0]	WEIM.AD[7]	GPIO2.IO[7]	LCDIF.DATA[7]		Always
P2-72	ECSPI2.MISO	UART7.RTS_B	USDHC1.DATA6	CSI1.DATA[8]	LCDIF.DATA[15]	GPIO4.IO[22]			Always

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Availability
P2-73		SIM2.PORT2_CLK	QSPI.A_SS0_B	KPP.ROW[0]	WEIM.AD[6]	GPIO2.IO[6]	LCDIF.DATA[6]		Always
P2-75		SIM2.PORT2_TRXD	QSPI.A_SCLK	KPP.COL[1]	WEIM.AD[5]	GPIO2.IO[5]	LCDIF.DATA[5]		Always
P2-76	USDHC2.CD_B	ENET1.MDIO		ECSPI3.SS2	FLEXTIMER1.PHB	GPIO5.IO[9]	SDMA.EXT_EVENT[0]		not "C1000D" and not "E"
P2-76	USDHC2.CD_B	ENET1.MDIO	ENET2.MDIO	ECSPI3.SS2	FLEXTIMER1.PHB	GPIO5.IO[9]	SDMA.EXT_EVENT[0]		"C1000D" and not "E"
P2-77		SIM1.PORT2_PD	QSPI.A_DQS	KPP.ROW[1]	WEIM.AD[4]	GPIO2.IO[4]	LCDIF.DATA[4]		Always
P2-78	LCDIF.DATA[6]		CORESIGHT.TRACE[6]	CSI1.PIXCLK	WEIM.DATA[6]	GPIO3.IO[11]	SRC.BT_CFG[6]		Always
P2-80	LCDIF.RESET	GPT1.COMPARE1	CORESIGHT.EVENTI	CSI1.FIELD	WEIM.DTACK_B	GPIO3.IO[4]			Always
P2-81	LCDIF.DATA[3]	GPT1.CAPTURE1	CORESIGHT.TRACE[3]	CSI1.DATA[23]	WEIM.DATA[3]	GPIO3.IO[8]	SRC.BT_CFG[3]		Always
P2-82	UART1.TX	I2C1.SDA	SAI3.MCLK			GPIO4.IO[1]	ENET1.MDC		not "C1000D"
P2-82	UART1.TX	I2C1.SDA	SAI3.MCLK		ENET2.1588_EVENT0_OUT	GPIO4.IO[1]	ENET1.MDC		"C1000D"
P2-83	LCDIF.DATA[2]	GPT1.CLK	CORESIGHT.TRACE[2]	CSI1.DATA[22]	WEIM.DATA[2]	GPIO3.IO[7]	SRC.BT_CFG[2]		Always
P2-84	UART1.RX	I2C1.SCL	CCM.PMIC_READY			GPIO4.IO[0]	ENET1.MDIO		not "C1000D"
P2-84	UART1.RX	I2C1.SCL	CCM.PMIC_READY		ENET2.1588_EVENT0_IN	GPIO4.IO[0]	ENET1.MDIO		"C1000D"
P2-85	LCDIF.DATA[1]	GPT1.COMPARE3	CORESIGHT.TRACE[1]	CSI1.DATA[21]	WEIM.DATA[1]	GPIO3.IO[6]	SRC.BT_CFG[1]		Always
P2-87	LCDIF.DATA[0]	GPT1.COMPARE2	CORESIGHT.TRACE[0]	CSI1.DATA[20]	WEIM.DATA[0]	GPIO3.IO[5]	SRC.BT_CFG[0]		Always
P2-88	ECSPI2.MOSI	UART7.TX	USDHC1.DATA5	CSI1.DATA[7]	LCDIF.DATA[14]	GPIO4.IO[21]			Always
P2-89		SIM1.PORT2_CLK	QSPI.A_DATA[1]	KPP.COL[3]	WEIM.AD[1]	GPIO2.IO[1]	LCDIF.DATA[1]	LCDIF.ENABLE	Always
P2-90	ECSPI2.SCLK	UART7.RX	USDHC1.DATA4	CSI1.DATA[6]	LCDIF.DATA[13]	GPIO4.IO[20]			Always
P2-92	GPIO1.IO[3]	PWM3.OUT	CCM.ENET2_REF_CLK_ROOT	SAI3.MCLK		CCM.CLKO2			not "C1000D"
P2-92	GPIO1.IO[3]	PWM3.OUT	CCM.ENET2_REF_CLK_ROOT	SAI3.MCLK		CCM.CLKO2		USB.OTG2_ID	"C1000D"
P2-93		SIM1.PORT2_TRXD	QSPI.A_DATA[0]	KPP.ROW[3]	WEIM.AD[0]	GPIO2.IO[0]	LCDIF.DATA[0]	LCDIF.CLK	Always
P2-94	I2C3.SCL	UART5.CTS_B	CAN2.RX	CSI1.VSYNC	SDMA.EXT_EVENT[0]	GPIO4.IO[12]			Always
P2-95		SIM1.PORT2_RST_B	QSPI.A_DATA[2]	KPP.ROW[2]	WEIM.AD[2]	GPIO2.IO[2]	LCDIF.DATA[2]	LCDIF.VSYNC	Always
P2-96	I2C3.SDA	UART5.RTS_B	CAN2.TX	CSI1.HSYNC	SDMA.EXT_EVENT[1]	GPIO4.IO[13]			Always
P2-97		SIM1.PORT2_SVEN	QSPI.A_DATA[3]	KPP.COL[2]	WEIM.AD[3]	GPIO2.IO[3]	LCDIF.DATA[3]	LCDIF.HSYNC	Always
P2-100	GPIO1.IO[2]	PWM2.OUT	CCM.ENET1_REF_CLK_ROOT	SAI2.MCLK		CCM.CLKO1		USB.OTG1_ID	Always

5.6 RTC

The UCM-iMX7 RTC is implemented with the Ambiq Micro AM1805 RTC. The RTC provides time and calendar information. Additionally, a backup battery can keep the RTC running if the main supply is not present. The backup battery should be connected to the VCC_RTC power input.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

5.7 LED

The UCM-iMX7 features a single general purpose green LED controlled by GPIO6_14 signal of the i.MX7. The LED is ON when GPIO6_14 is logic High.

6 CARRIER BOARD INTERFACE

The UCM-iMX7 CoM/SoM carrier board interface uses the UCM edge connector. The SoM pinout is detailed in the table below

6.1 Connector Pinout

Table 66 Connector P1

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-1	VSYS	5.1	P1-2	VSYS	5.1
P1-3	VSYS	5.1	P1-4	VSYS	5.1
P1-5	VSYS	5.1	P1-6	VSYS	5.1
P1-7	VSYS	5.1	P1-8	VSYS	5.1
P1-9	VSYS	5.1	P1-10	ETH1_LED_ACT ENET1.RGMII_RD1 UART1.RTS_B I2C3.SDA PWM2.OUT KPP.COL[3] GPIO7.IO[1]	4.5.1 4.5.2 4.13 4.14 4.20 4.24 4.26
P1-11	LCDIF.DATA[8] CSI1.DATA[9] GPIO3.IO[13] CORESIGHT.TRACE[8]	4.1 4.3 4.26 4.29.2	P1-12	ETH1_MDI0N ENET1.RGMII_TX_CTL SAI1.RX_SYNC GPT2.COMPARE1 GPIO7.IO[10]	4.5.1 4.5.2 4.8 4.21 4.26
P1-13	LCDIF.DATA[9] CSI1.DATA[8] GPIO3.IO[14] CORESIGHT.TRACE[9]	4.1 4.3 4.26 4.29.2	P1-14	ETH1_MDI0P ENET1.RGMII_TXC ENET1.TX_ER SAI1.RX_BCLK GPT2.COMPARE2 GPIO7.IO[11]	4.5.1 4.5.2 4.5.2 4.8 4.21 4.26
P1-15	SAI2.TX_SYNC UART1.CTS_B UART4.RX ECSPI3.MISO FLEXTIMER2.CH[4] GPIO6.IO[19]	4.8 4.13 4.13 4.15 4.23 4.26	P1-16	VSYS	5.1
P1-17	SAI2.TX_DATA[0] UART2.RTS_B UART4.RTS_B ECSPI3.SS0 FLEXTIMER2.CH[7] KPP.ROW[7] GPIO6.IO[22]	4.8 4.13 4.13 4.15 4.23 4.24 4.26	P1-18	ETH1_MDI1P ENET1.RGMII_TD3 I2C4.SDA ECSPI2.SS0 CAN2.TX GPIO7.IO[9]	4.5.1 4.5.2 4.14 4.15 4.17 4.26
P1-19	ETH1_LED3 ENET1.RGMII_RD0 UART1.CTS_B I2C3.SCL PWM1.OUT KPP.ROW[3] GPIO7.IO[0]	4.5.1 4.5.2 4.13 4.14 4.20 4.24 4.26	P1-20	ETH1_MDI1N ENET1.RGMII_TD1 ECSPI2.RDY PWM4.OUT KPP.COL[0] GPIO7.IO[7]	4.5.1 4.5.2 4.15 4.20 4.24 4.26
P1-21	SAI2.RX_DATA[0] UART2.CTS_B UART4.CTS_B ECSPI3.SCLK FLEXTIMER2.CH[6] KPP.COL[7] GPIO6.IO[21]	4.8 4.13 4.13 4.15 4.23 4.24 4.26	P1-22	VSYS	5.1
P1-23	SAI2.TX_BCLK UART1.RTS_B UART4.TX ECSPI3.MOSI FLEXTIMER2.CH[5] GPIO6.IO[20]	4.8 4.13 4.13 4.15 4.23 4.26	P1-24	ETH1_MDI2P ENET1.RGMII_RD3 UART1.TX ECSPI2.MOSI CAN1.TX KPP.COL[2] GPIO7.IO[3]	4.5.1 4.5.2 4.13 4.15 4.17 4.24 4.26

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-25	SAI2.RX_DATA[0] USDHC2.DATA0 UART4.RX GPT4.CAPTURE2 SIM2.PORT1_CLK GPIO5.IO[14]	4.8 4.12 4.13 4.21 4.25 4.26	P1-26	ETH1_MDI2N ENET1.RGMII_RD2 UART1.RX ECSPI2.SCLK CAN1.RX KPP.ROW[2] GPIO7.IO[2]	4.5.1 4.5.2 4.13 4.15 4.17 4.24 4.26
P1-27	GND	5.1	P1-28	LCDIF.ENABLE CSI1.DATA[17] ENET1.1588_EVENT3_IN UART2.TX ECSPI4.MOSI GPIO3.IO[1]	4.1 4.3 4.5.2 4.13 4.15 4.26
P1-29	SAI2.RX_SYNC MQS.RIGHT USDHC2.CLK GPT4.CLK GPIO5.IO[12]	4.8 4.9 4.12 4.21 4.26	P1-30	ETH1_MDI3P ENET1.RGMII_RX_CTL ECSPI2.SS1 KPP.ROW[1] GPIO7.IO[4]	4.5.1 4.5.2 4.15 4.24 4.26
P1-31	SAI2.TX_BCLK USDHC2.DATA1 UART4.TX GPT4.COMPARE1 SIM2.PORT1_RST_B GPIO5.IO[15]	4.8 4.12 4.13 4.21 4.25 4.26	P1-32	ETH1_MDI3N ENET1.RGMII_RXC ENET1.RX_ER ECSPI2.SS2 KPP.COL[1] GPIO7.IO[5]	4.5.1 4.5.2 4.5.2 4.15 4.24 4.26
P1-33	SAI2.TX_SYNC USDHC2.DATA2 UART4.CTS_B GPT4.COMPARE2 SIM2.PORT1_SVEN GPIO5.IO[16]	4.8 4.12 4.13 4.21 4.25 4.26	P1-34	GND	5.1
P1-35	SAI2.TX_DATA[0] USDHC2.DATA3 UART4.RTS_B GPT4.COMPARE3 SIM2.PORT1_PD GPIO5.IO[17]	4.8 4.12 4.13 4.21 4.25 4.26	P1-36	RESERVED	
P1-37	SAI2.RX_BCLK MQS.LEFT USDHC2.CMD GPT4.CAPTURE1 SIM2.PORT1_TRXD GPIO5.IO[13]	4.8 4.9 4.12 4.21 4.25 4.26	P1-38	ETH1_LED1_SPD ENET1.RGMII_TD0 ECSPI2.SS3 PWM3.OUT KPP.ROW[0] GPIO7.IO[6]	4.5.1 4.5.2 4.15 4.20 4.24 4.26
P1-39	GND	5.1	P1-40	LCDIF.DATA[23] CSI1.DATA[10] I2C4.SDA FLEXTIMER2.CH[7] GPIO3.IO[28]	4.1 4.3 4.14 4.23 4.26
P1-41	MIPI_CSI_D0_P	4.4	P1-42	LCDIF.DATA[10] CSI1.DATA[7] GPIO3.IO[15] CORESIGHT.TRACE[10]	4.1 4.3 4.26 4.29.2
P1-43	MIPI_CSI_D0_N	4.4	P1-44	LCDIF.DATA[22] CSI1.DATA[11] I2C4.SCL FLEXTIMER2.CH[6] GPIO3.IO[27]	4.1 4.3 4.14 4.23 4.26
P1-45	UART3.RX I2C3.SCL PWM1.OUT WDOG1.WDOG_B KPP.COL[5] GPIO1.IO[8]	4.13 4.14 4.20 4.22 4.24 4.26	P1-46	GND	5.1
P1-47	MIPI_CSI_D1_P	4.4	P1-48	LCDIF.HSYNC CSI1.DATA[18] UART2.RTS_B ECSPI4.SCLK GPIO3.IO[2]	4.1 4.3 4.13 4.15 4.26
P1-49	MIPI_CSI_D1_N	4.4	P1-50	LCDIF.DATA[16] CSI1.DATA[1] FLEXTIMER1.CH[4] GPIO3.IO[21] CORESIGHT.TRACE_CLK	4.1 4.3 4.23 4.26 4.29.2

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-51	GND	5.1	P1-52	LCDIF.DATA[18] CSI1.DATA[15] FLEXTIMER1.CH[6] GPIO3.IO[23] CORESIGHT.EVENTO	4.1 4.3 4.23 4.26 4.29.2
P1-53	MIPI_CSI_CLK_P	4.4	P1-54	LCDIF.DATA[19] CSI1.DATA[14] FLEXTIMER1.CH[7] GPIO3.IO[24]	4.1 4.3 4.23 4.26
P1-55	MIPI_CSI_CLK_N	4.4	P1-56	LCDIF.DATA[11] CSI1.DATA[6] GPIO3.IO[16] CORESIGHT.TRACE[11]	4.1 4.3 4.26 4.29.2
P1-57	ENET1.RGMII_TD2 I2C4.SCL ECSPI2.MISO CAN2.RX GPIO7.IO[8]	4.5.2 4.14 4.15 4.17 4.26	P1-58	GND	5.1
P1-59	MIPI_DSI_D0_P	4.2	P1-60	LCDIF.DATA[15] CSI1.DATA[2] GPIO3.IO[20] CORESIGHT.TRACE[15]	4.1 4.3 4.26 4.29.2
P1-61	MIPI_DSI_D0_N	4.2	P1-62	LCDIF.DATA[20] CSI1.DATA[13] ENET1.1588_EVENT2_OUT I2C3.SCL FLEXTIMER2.CH[4] GPIO3.IO[25]	4.1 4.3 4.5.2 4.14 4.23 4.26
P1-63	GND	5.1	P1-64	LCDIF.DATA[13] CSI1.DATA[4] GPIO3.IO[18] CORESIGHT.TRACE[13]	4.1 4.3 4.26 4.29.2
P1-65	MIPI_DSI_D1_P	4.2	P1-66	LCDIF.DATA[14] CSI1.DATA[3] GPIO3.IO[19] CORESIGHT.TRACE[14]	4.1 4.3 4.26 4.29.2
P1-67	MIPI_DSI_D1_N	4.2	P1-68	LCDIF.DATA[12] CSI1.DATA[5] GPIO3.IO[17] CORESIGHT.TRACE[12]	4.1 4.3 4.26 4.29.2
P1-69	USDHC1.LCTL UART3.TX I2C3.SDA PWM2.OUT KPP.ROW[5] GPIO1.IO[9] CCM.ENET3_REF_CLK_ROOT CCM.PMIC_READY	4.12 4.13 4.14 4.20 4.24 4.26 4.28 4.28	P1-70	GND	5.1
P1-71	MIPI_DSI_CLK_P	4.2	P1-72	UART4.RTS_B I2C1.SDA ECSPI3.MOSI CAN1.TX GPIO4.IO[9] CCM.ENET1_REF_CLK_ROOT	4.13 4.14 4.15 4.17 4.26 4.28
P1-73	MIPI_DSI_CLK_N	4.2	P1-74	ENET1.MDC USB.OTG1_ID USDHC2.WP ECSPI3.SS3 GPIO5.IO[10] SDMA.EXT_EVENT[1]	4.5.2 4.10.1 4.12 4.15 4.26 4.27
P1-75	GND	5.1	P1-76	UART4.CTS_B I2C1.SCL ECSPI3.MISO CAN1.RX GPIO4.IO[8]	4.13 4.14 4.15 4.17 4.26
P1-77	LCDIF.DATA[11] LCDIF.HSYNC FLEXTIMER2.PHA GPIO2.IO[30]	4.1 4.1 4.23 4.26	P1-78	UART4.TX ECSPI3.SS0 WDOG3.WDOG_RST_B_DEB GPIO4.IO[11] CCM.ENET3_REF_CLK_ROOT	4.13 4.15 4.22 4.26 4.28

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P1-79	ADC1_IN0 RTOUCH_X+	4.18 4.19	P1-80	UART4.RX ECSPI3.SCLK WDOG3.WDOG_B GPIO4.IO[10] CCM.ENET2_REF_CLK_ROOT	4.13 4.15 4.22 4.26 4.28
P1-81	ADC1_IN1 RTOUCH_X-	4.18 4.19	P1-82	USDHC1.CD_B UART6.RX ECSPI4.MISO FLEXTIMER1.CH[0] GPIO5.IO[0] CCM.CLKO1	4.12 4.13 4.15 4.23 4.26 4.28
P1-83	ADC1_IN2 RTOUCH_Y+	4.18 4.19	P1-84	GND	5.1
P1-85	ADC1_IN3 RTOUCH_Y-	4.18 4.19	P1-86	ENET1.TX_CLK MICIN SAI1.RX_DATA[0] GPT2.COMPARE3 GPIO7.IO[12] CCM.ENET1_REF_CLK_ROOT CCM.EXT_CLK1	4.5.2 4.7 4.8 4.21 4.26 4.28 4.28
P1-87	GND	5.1	P1-88	ENET1.CRS MICBIAS SAI1.TX_SYNC GPT2.CAPTURE1 WDOG2.WDOG_RST_B_DEB GPIO7.IO[14] CCM.EXT_CLK3	4.5.2 4.7 4.8 4.21 4.22 4.26 4.28
P1-89	COLD_RESET_IN	5.2	P1-90	ALT_BOOT	5.3
P1-91	ENET1.1588_EVENT1_OUT SAI3.TX_SYNC USB.OTG2_PWR UART3.CTS_B GPIO4.IO[7]	4.5.2 4.8 4.10.1 4.13 4.26	P1-92	ENET1.COL RLINEIN SAI1.TX_DATA[0] GPT2.CAPTURE2 WDOG.GLOBAL GPIO7.IO[15] CCM.EXT_CLK4	4.5.2 4.7 4.8 4.21 4.22 4.26 4.28
P1-93	PMIC_ON_REQ	5.4.1	P1-94	ENET1.RX_CLK LLINEIN SAI1.TX_BCLK GPT2.CLK WDOG2.WDOG_B GPIO7.IO[13] CCM.EXT_CLK2	4.5.2 4.7 4.8 4.21 4.22 4.26 4.28
P1-95	ENET1.1588_EVENT1_IN SAI3.TX_DATA[0] USB.OTG2_OC UART3.RTS_B GPIO4.IO[6]	4.5.2 4.8 4.10.1 4.13 4.26	P1-96	VCC_RTC	5.1
P1-97	ONOFF	5.4.1	P1-98	RHPOUT SAI1.RX_SYNC SAI2.RX_SYNC MQS.RIGHT I2C4.SCL SIM1.PORT1_PD GPIO6.IO[16]	4.7 4.8 4.8 4.9 4.14 4.25 4.26
P1-99	GND	5.1	P1-100	LHPOUT SAI1.RX_BCLK SAI2.RX_BCLK MQS.LEFT I2C4.SDA FLEXTIMER2.PHA GPIO6.IO[17]	4.7 4.8 4.8 4.9 4.14 4.23 4.26

Table 67 Connector P2

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-1	ENET1.MDIO USDHC2.LCTL UART3.RTS_B I2C4.SCL PWM3.OUT FLEXTIMER1.PHA KPP.COL[6] GPIO1.IO[10]	4.5.2 4.12 4.13 4.14 4.20 4.23 4.24 4.26	P2-2	GND	5.1
P2-3	ENET1.MDC UART3.CTS_B I2C4.SDA PWM4.OUT FLEXTIMER1.PHB KPP.ROW[6] GPIO1.IO[11]	4.5.2 4.13 4.14 4.20 4.23 4.24 4.26	P2-4	SAI3.RX_SYNC USDHC1.CLK UART6.CTS_B ECSPI4.SS0 FLEXTIMER1.CH[3] GPIO5.IO[3]	4.8 4.12 4.13 4.15 4.23 4.26
P2-5	USB_OTG1_ID	4.10.1	P2-6	USB.OTG1_PWR UART5.RTS_B I2C1.SDA FLEXTIMER1.CH[5] GPIO1.IO[5]	4.10.1 4.13 4.14 4.23 4.26
P2-7	GND	5.1	P2-8	SAI3.TX_DATA[0] USDHC1.DATA3 UART7.RTS_B ECSPI3.SS1 FLEXTIMER1.PHA GPIO5.IO[8] CCM.EXT_CLK4	4.8 4.12 4.13 4.15 4.23 4.26 4.28
P2-9	USB_H2_DN	4.10.2	P2-10	SAI3.TX_SYNC USDHC1.DATA2 UART7.CTS_B ECSPI4.RDY FLEXTIMER2.CH[3] GPIO5.IO[7] CCM.EXT_CLK3	4.8 4.12 4.13 4.15 4.23 4.26 4.28
P2-11	USB_H2_DP	4.10.2	P2-12	SAI3.RX_BCLK USDHC1.CMD ECSPI4.SS1 FLEXTIMER2.CH[0] GPIO5.IO[4]	4.8 4.12 4.15 4.23 4.26
P2-13	VBUS_NOVERCURRENT	4.10.2	P2-14	GND	5.1
P2-15	USB_H3_DN	4.10.2	P2-16	SAI3.RX_DATA[0] USDHC1.DATA0 UART7.RX ECSPI4.SS2 FLEXTIMER2.CH[1] GPIO5.IO[5] CCM.EXT_CLK1	4.8 4.12 4.13 4.15 4.23 4.26 4.28
P2-17	USB_H3_DP	4.10.2	P2-18	SAI3.MCLK USDHC1.RESET_B UART6.RTS_B ECSPI4.SCLK FLEXTIMER1.CH[2] GPIO5.IO[2]	4.8 4.12 4.13 4.15 4.23 4.26
P2-19	GND	5.1	P2-20	LCDIF.CS LCDIF.DATA[7] GPIO2.IO[28] CCM.ENET2_REF_CLK_ROOT	4.1 4.1 4.26 4.28
P2-21	USB_H1_DN	4.10.2	P2-22	LCDIF.DATA[12] LCDIF.VSYNC FLEXTIMER2.PHB GPIO2.IO[31]	4.1 4.1 4.23 4.26
P2-23	USB_H1_DP	4.10.2	P2-24	SAI3.TX_BCLK USDHC1.DATA1 UART7.TX ECSPI4.SS3 FLEXTIMER2.CH[2] GPIO5.IO[6] CCM.EXT_CLK2	4.8 4.12 4.13 4.15 4.23 4.26 4.28
P2-25	VBUS_EN_REQ	4.10.2	P2-26	GND	5.1

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-27	CSI1.PIXCLK USB.OTG1_ID UART5.RX I2C4.SCL WDOG4.WDOG_B GPIO4.IO[14]	4.3 4.10.1 4.13 4.14 4.22 4.26	P2-28	USB_OTG2_DP	4.10.1
P2-29	CSI1.MCLK USB.OTG2_ID UART5.TX I2C4.SDA WDOG4.WDOG_RST_B_DEB GPIO4.IO[15]	4.3 4.10.1 4.13 4.14 4.22 4.26	P2-30	USB_OTG2_DN	4.10.1
P2-31	GND	5.1	P2-32	USB_OTG2_VBUS	4.10.1
P2-33	LCDIF.CLK CSI1.DATA[16] ENET1.1588_EVENT2_IN UART2.RX ECSPI4.MISO GPIO3.IO[0]	4.1 4.3 4.5.2 4.13 4.15 4.26	P2-34	USB_OTG1_DN	4.10.1
P2-35	LCDIF.DATA[6] LCDIF.ENABLE GPIO2.IO[29]	4.1 4.1 4.26	P2-36	USB_OTG1_DP	4.10.1
P2-37	LCDIF.DATA[21] CSI1.DATA[12] ENET1.1588_EVENT3_OUT I2C3.SDA FLEXTIMER2.CH[5] GPIO3.IO[26]	4.1 4.3 4.5.2 4.14 4.23 4.26	P2-38	GND	5.1
P2-39	PMIC_STBY_REQ	5.4.1	P2-40	PCIE_REFCLKIN_P	4.11
P2-41	LCDIF.VSYNC CSI1.DATA[19] UART2.CTS_B ECSPI4.SS0 GPIO3.IO[3]	4.1 4.3 4.13 4.15 4.26	P2-42	PCIE_REFCLKIN_N	4.11
P2-43	GND	5.1	P2-44	USB_OTG1_VBUS	4.10.1
P2-45	LCDIF.DATA[7] CSI1.MCLK GPIO3.IO[12] CORESIGHT.TRACE[7]	4.1 4.3 4.26 4.29.2	P2-46	PCIE_REFCLKOUT_P	4.11
P2-47	LCDIF.DATA[17] CSI1.DATA[0] FLEXTIMER1.CH[5] GPIO3.IO[22] CORESIGHT.TRACE_CTL	4.1 4.3 4.23 4.26 4.29.2	P2-48	PCIE_REFCLKOUT_N	4.11
P2-49	USDHC1.WP UART6.TX ECSPI4.MOSI FLEXTIMER1.CH[1] GPIO5.IO[1] CCM.CLKO2	4.12 4.13 4.15 4.23 4.26 4.28	P2-50	GND	5.1
P2-51	LCDIF.DATA[15] LCDIF.WR_RWN UART7.CTS_B QSPI.B_SS1_B SIM2.PORT1_RST_B GPIO2.IO[15]	4.1 4.1 4.13 4.16 4.25 4.26	P2-52	PCIE_RX_N	4.11
P2-53	LCDIF.DATA[14] LCDIF.DATA[22] UART7.RTS_B QSPI.B_SS0_B SIM2.PORT1_CLK GPIO2.IO[14]	4.1 4.1 4.13 4.16 4.25 4.26	P2-54	PCIE_RX_P	4.11
P2-55	GND	5.1	P2-56	USB_OTG1_CHD_B	4.10.1
P2-57	LCDIF.CS LCDIF.DATA[13] UART7.TX QSPI.B_SCLK SIM2.PORT1_TRXD GPIO2.IO[13]	4.1 4.1 4.13 4.16 4.25 4.26	P2-58	PCIE_TX_N	4.11

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-59	LCDIF.DATA[12] LCDIF.DATA[21] UART7.RX QSPI.B_DQS SIM1.PORT1_PD GPIO2.IO[12]	4.1 4.1 4.13 4.16 4.25 4.26	P2-60	PCIE_TX_P	4.11
P2-61	LCDIF.DATA[1] LCDIF.DATA[11] UART6.CTS_B QSPI.B_DATA[3] SIM1.PORT1_SVEN GPIO2.IO[11]	4.1 4.1 4.13 4.16 4.25 4.26	P2-62	GND	5.1
P2-63	LCDIF.DATA[10] LCDIF.DATA[9] UART6.RTS_B QSPI.B_DATA[2] SIM1.PORT1_RST_B GPIO2.IO[10]	4.1 4.1 4.13 4.16 4.25 4.26	P2-64	LCDIF.DATA[5] CSI1.HSYNC GPIO3.IO[10] CORESIGHT.TRACE[5]	4.1 4.3 4.26 4.29.2
P2-65	LCDIF.DATA[0] LCDIF.DATA[9] UART6.TX QSPI.B_DATA[1] SIM1.PORT1_CLK GPIO2.IO[9]	4.1 4.1 4.13 4.16 4.25 4.26	P2-66	LCDIF.DATA[4] CSI1.VSYNC GPT1.CAPTURE2 GPIO3.IO[9] CORESIGHT.TRACE[4]	4.1 4.3 4.21 4.26 4.29.2
P2-67	GND	5.1	P2-68	SAI1.MCLK PWM1.OUT GPIO1.IO[1] CCM.ENET3_REF_CLK_ROOT	4.8 4.20 4.26 4.28
P2-69	LCDIF.BUSY LCDIF.DATA[8] UART6.RX QSPI.B_DATA[0] SIM1.PORT1_TRXD GPIO2.IO[8]	4.1 4.1 4.13 4.16 4.25 4.26	P2-70	LCDIF.RESET CSI1.DATA[9] USDHC1.DATA7 UART7.CTS_B ECSPI2.SS0 GPIO4.IO[23]	4.1 4.3 4.12 4.13 4.15 4.26
P2-71	LCDIF.DATA[7] QSPI.A_SS1_B KPP.COL[0] SIM2.PORT2_RST_B GPIO2.IO[7]	4.1 4.16 4.24 4.25 4.26	P2-72	LCDIF.DATA[15] CSI1.DATA[8] USDHC1.DATA6 UART7.RTS_B ECSPI2.MISO GPIO4.IO[22]	4.1 4.3 4.12 4.13 4.15 4.26
P2-73	LCDIF.DATA[6] QSPI.A_SS0_B KPP.ROW[0] SIM2.PORT2_CLK GPIO2.IO[6]	4.1 4.16 4.24 4.25 4.26	P2-74	GND	5.1
P2-75	LCDIF.DATA[5] QSPI.A_SCLK KPP.COL[1] SIM2.PORT2_TRXD GPIO2.IO[5]	4.1 4.16 4.24 4.25 4.26	P2-76	ENET1.MDIO USDHC2.CD_B ECSPI3.SS2 FLEXTIMER1.PHB GPIO5.IO[9] SDMA.EXT_EVENT[0]	4.5.2 4.12 4.15 4.23 4.26 4.27
P2-77	LCDIF.DATA[4] QSPI.A_DQS KPP.ROW[1] SIM1.PORT2_PD GPIO2.IO[4]	4.1 4.16 4.24 4.25 4.26	P2-78	LCDIF.DATA[6] CSI1.PIXCLK GPIO3.IO[11] CORESIGHT.TRACE[6]	4.1 4.3 4.26 4.29.2
P2-79	GND	5.1	P2-80	LCDIF.RESET CSI1.FIELD GPT1.COMPARE1 GPIO3.IO[4] CORESIGHT.EVENTI	4.1 4.3 4.21 4.26 4.29.2
P2-81	LCDIF.DATA[3] CSI1.DATA[23] GPT1.CAPTURE1 GPIO3.IO[8] CORESIGHT.TRACE[3]	4.1 4.3 4.21 4.26 4.29.2	P2-82	ENET1.MDC SAI3.MCLK UART1.TX I2C1.SDA GPIO4.IO[1]	4.5.2 4.8 4.13 4.14 4.26
P2-83	LCDIF.DATA[2] CSI1.DATA[22] GPT1.CLK GPIO3.IO[7] CORESIGHT.TRACE[2]	4.1 4.3 4.21 4.26 4.29.2	P2-84	ENET1.MDIO UART1.RX I2C1.SCL GPIO4.IO[0] CCM.PMIC_READY	4.5.2 4.13 4.14 4.26 4.28

Pin #	Signal Name	Ref.	Pin #	Signal Name	Ref.
P2-85	LCDIF.DATA[1] CSI1.DATA[21] GPT1.COMPARE3 GPIO3.IO[6] CORESIGHT.TRACE[1]	4.1 4.3 4.21 4.26 4.29.2	P2-86	GND	5.1
P2-87	LCDIF.DATA[0] CSI1.DATA[20] GPT1.COMPARE2 GPIO3.IO[5] CORESIGHT.TRACE[0]	4.1 4.3 4.21 4.26 4.29.2	P2-88	LCDIF.DATA[14] CSI1.DATA[7] USDHC1.DATA5 UART7.TX ECSPI2.MOSI GPIO4.IO[21]	4.1 4.3 4.12 4.13 4.15 4.26
P2-89	LCDIF.DATA[1] LCDIF.ENABLE QSPI.A_DATA[1] KPP.COL[3] SIM1.PORT2_CLK GPIO2.IO[1]	4.1 4.1 4.16 4.24 4.25 4.26	P2-90	LCDIF.DATA[13] CSI1.DATA[6] USDHC1.DATA4 UART7.RX ECSPI2.SCLK GPIO4.IO[20]	4.1 4.3 4.12 4.13 4.15 4.26
P2-91	GND	5.1	P2-92	SAI3.MCLK USB.OTG2_ID PWM3.OUT GPIO1.IO[3] CCM.CLKO2 CCM.ENET2_REF_CLK_ROOT	4.8 4.10.1 4.20 4.26 4.28 4.28
P2-93	LCDIF.CLK LCDIF.DATA[0] QSPI.A_DATA[0] KPP.ROW[3] SIM1.PORT2_TRXD GPIO2.IO[0]	4.1 4.1 4.16 4.24 4.25 4.26	P2-94	CSI1.VSYNC UART5.CTS_B I2C3.SCL CAN2.RX GPIO4.IO[12] SDMA.EXT_EVENT[0]	4.3 4.13 4.14 4.17 4.26 4.27
P2-95	LCDIF.DATA[2] LCDIF.VSYNC QSPI.A_DATA[2] KPP.ROW[2] SIM1.PORT2_RST_B GPIO2.IO[2]	4.1 4.1 4.16 4.24 4.25 4.26	P2-96	CSI1.HSYNC UART5.RTS_B I2C3.SDA CAN2.TX GPIO4.IO[13] SDMA.EXT_EVENT[1]	4.3 4.13 4.14 4.17 4.26 4.27
P2-97	LCDIF.DATA[3] LCDIF.HSYNC QSPI.A_DATA[3] KPP.COL[2] SIM1.PORT2_SVEN GPIO2.IO[3]	4.1 4.1 4.16 4.24 4.25 4.26	P2-98	GND	5.1
P2-99	EEPROM_WP	5.4.2	P2-100	SAI2.MCLK USB.OTG1_ID PWM2.OUT GPIO1.IO[2] CCM.CLKO1 CCM.ENET1_REF_CLK_ROOT	4.8 4.10.1 4.20 4.26 4.28 4.28

6.2 Mating Connectors

Table 68 Connector type

UCM-iMX7 connector			Carrier board (mating) connector P/N		
Ref.	Mfg.	P/N	Mfg.	P/N	Notes
P1,P2	Hirose	DF40C-100DP-0.4V(51)	Hirose	DF40HC(3.0)-100DS-0.4V(51)	3±0.15mm board to board height
			Hirose	DF40C-100DS-0.4V(51)	1.5±0.15mm board to board height

6.3 Mechanical Drawings

Figure 3 UCM-iMX7 Top

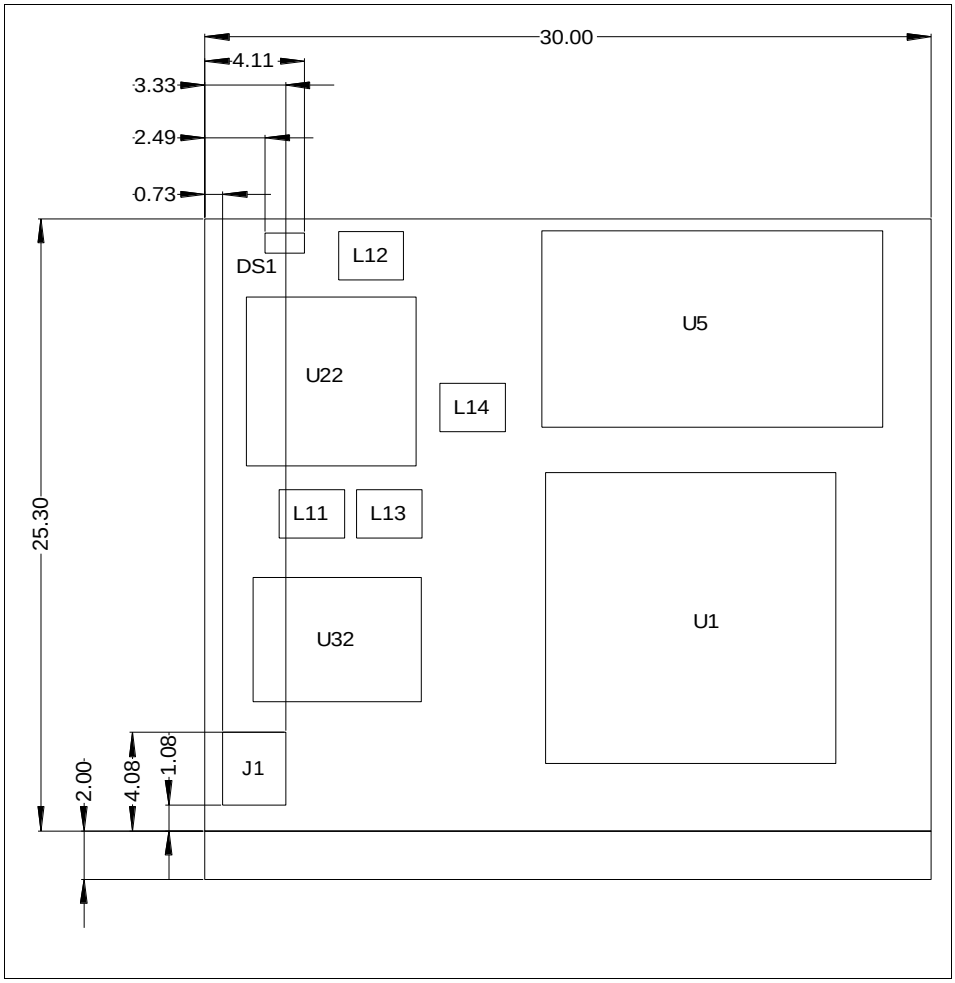
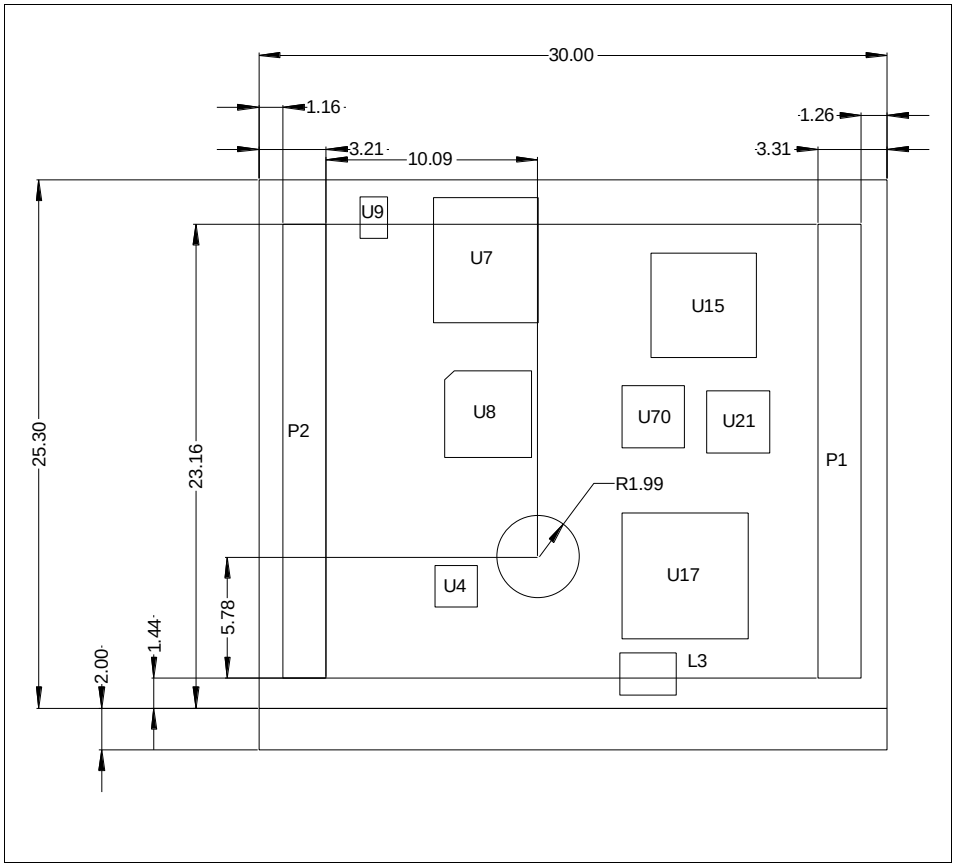


Figure 4 UCM-iMX7 bottom



1. All dimensions are in millimeters.

2. Height of all components is < 2.0mm.

3. Baseboard connectors provide two options for board-to-board clearance. Refer to chapter 6.2 for details.

Mechanical drawings are available in DXF format at
http://www.compulab.com/products/computer-on-modules/ucm-imx7/#devres

6.4 Standoffs/Spacers

UCM-iMX7 features an M2 screw soldered to the bottom side of the module (round pad in figure4 above). Carrier board designer must place an M2 mechanical hole (refer to SB-UCM design for reference), enabling access to UCM-iMX7 screw from bottom side of carrier board. It is recommended to lock the carrier board to UCM-iMX7 using an M2 nut in conjunction with the module screw. Depending on choice of carrier board connectors, one or more M2 washers might be needed between the module and carrier board PCB.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 69 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)		-0.3		4.8	V
Backup battery supply voltage (VCC_RTC)		-0.3		3.6	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 70 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	Normal operation	3.4		4.5	V
Backup battery supply voltage (VCC_RTC)		1.8	3.0	3.3	V

7.3 DC Electrical Characteristics

Table 71 DC Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{OH}	3.3V operation, i.MX7 drive strength set to Ioh= -0.1mA, Ioh= -1mA.	3.05			V
V_{OL}				0.15	V
V_{IH}	3.3V operation	2.38		3.3	V
V_{IL}		0		0.96	V
V_{OH}	1.8V operation, i.MX7 drive strength set to Ioh= -0.1mA, Ioh= -1mA.	1.55			V
V_{OL}				0.15	V
V_{IH}	1.8V operation	1.33		1.8	V
V_{IL}		0		0.51	V

7.4 ESD Performance

Table 72 ESD Performance

Interface	ESD Performance
i.MX7 pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)
USB Hub pins (UH option)	5kV Human Body Model (HBM)
LVDS (L option)	2kV Human Body Model (HBM)

7.5 Operating Temperature Ranges

The UCM-iMX7 is available with three options of operating temperature range.

Table 73 UCM-iMX7 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for UCM-iMX7 operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX7.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the UCM-iMX7 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the UCM-iMX7.
- Refer to the SB-UCM carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect

- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX7, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCM carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of "Qualified Magnetics" contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 74 Qualified Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-UCM reference design schematics