CL-SOM-iMX8

Reference Guide

Compulab

Compulab Ltd.
P.O. Box 687 Yokneam Illit
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.com
Fax: +972 (4) 8325251

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Table 1 Revision Notes

Date	Description
Jan 2018	First release
Feb 2019	Updated to reflect changes in revision 1v1: • ESPI1 is permanently routed to SODIMM connector Updated tables 47, 33, 48 • USB port 2 is multiplexed either to SODIMM connector or to on-board Bluetooth Added section 4.12.1 • On board wireless module changed from Murata LBEH5UL1CX to Intel 8265. USB port 2 is used for on-board Bluetooth functionality Updated section 4.7

Please check for a newer revision of this manual at the CompuLab website http://www.compulab.com/. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX8 Computer-on-Module.

1.2 CL-SOM-iMX8 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-iMX8 part number: http://www.compulab.com/products/computer-on-modules/cl-som-imx8-nxp-i-mx-8-system-on-module-computer/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX8 Developer Resources	http://www.compulab.com/products/computer-on-modules/cl-som-imx8-nxp-i-mx-8-system-on-module-computer/#devres
iMX8M Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-family-armcortex-a53-cortex-m4-audio-voice-video:i.MX8M?tab=Documentation_Tab
iMX8M Datasheet	

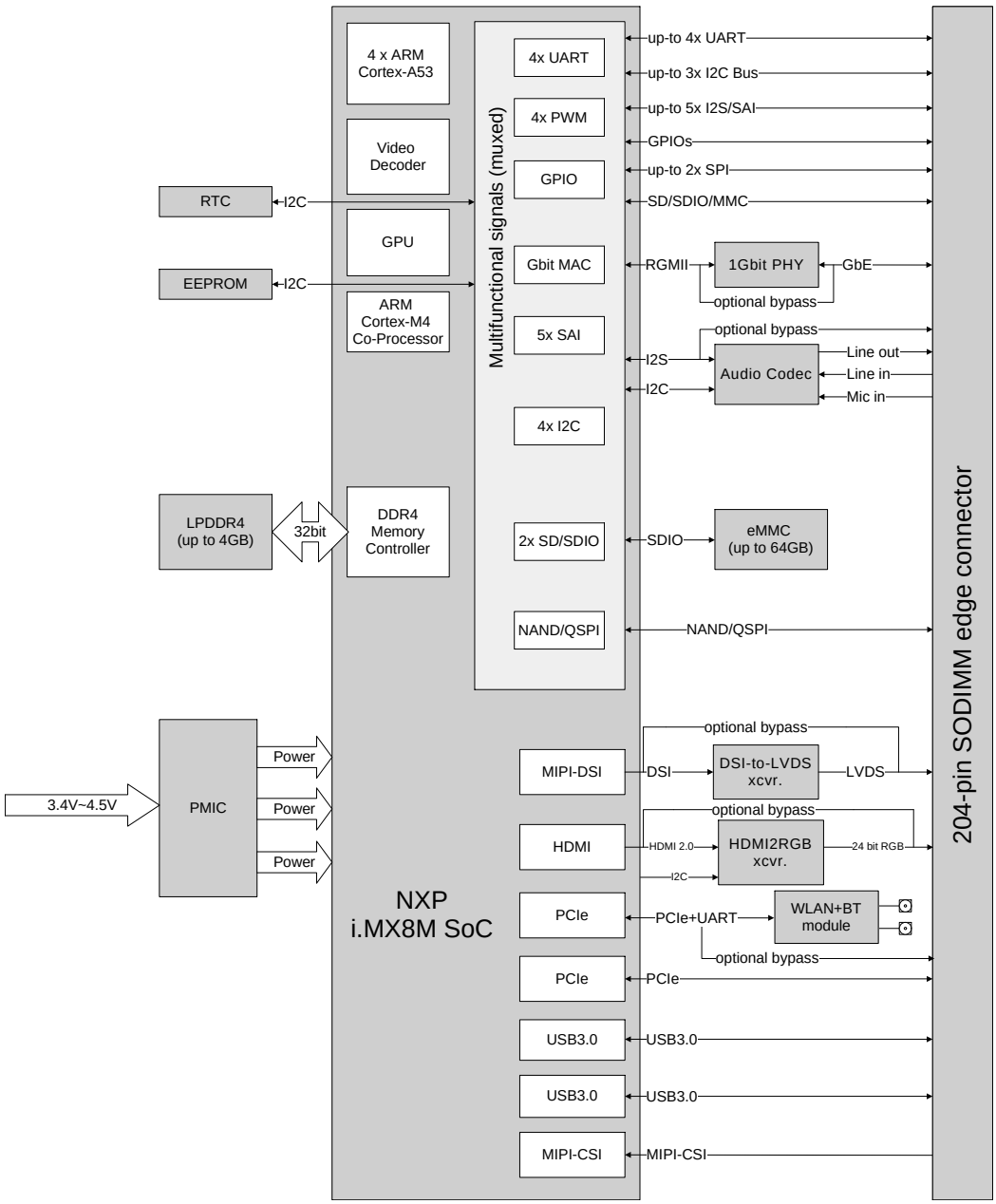
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M ARM Cortex-A53 MPCore platform @ 1.5GHz
- Real-time ARM Cortex-M4 co-processor
- Up to 4GB of LPDDR4
- Up to 64GB on-board eMMC storage
- HDMI 2.0a, LVDS, MIPI-DSI, up to 4096 x 2160
- Gbit Ethernet, WiFi 802.11a/b/g/n/ac, BT 4.1
- 2x PCIe, 2x USB3.0, 4x UART, 60x GPIO
- Miniature size: 42 x 68 x 5 mm
- SB-iMX8 carrier board turns the CL-SOM-iMX8 System-on-Module into SBC-iMX8, a single board computer

2.2 Block Diagram

Figure 1 CL-SOM-iMX8 Block Diagram



2.3 CL-SOM-iMX8 Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Quad, quad-core ARM Cortex-A53, 1.5GHz	C1500Q
	NXP i.MX8M Dual, dual-core ARM Cortex-A53, 1.5GHz	C1500D
Memory and Storage		
RAM	1GB to 4GB, LPDDR4-3200 with 32-bit bus width.	D
Storage	eMMC flash, 4GB - 32GB	N
Display and Camera		
Display	HDMI 2.0 port up to DCI 4K (4096 x 2160) @60Hz	+
	MIPI DSI 4 lanes up to FHD (1920 x 1080) @60Hz	~~LL~~
	LVDS, up-to 1920 x 1080 @60Hz	LL
Camera	MIPI CSI 4 lanes	+
Network		
Ethernet	1x Gigabit Ethernet port (MAC+PHY)	E
	1x RGMII	~~E~~
WiFi	Certified 802.11ac WiFi interface Intel 8265 chipset	WB
Bluetooth	Bluetooth 4.2 BLE * mutually exclusive with 2nd USB port	
Audio		
Analog Audio	WM8731 Audio codec with analog stereo output, stereo input, and electret microphone support	A
Digital Audio	4x I2S compliant digital audio interface	+
	1x I2S compliant digital audio interface	~~A~~
	Sony Philips Digital Interconnect Format (SPDIF)	+
I/O		
USB	2x USB3.0 dual-role ports	+
	* 2nd USB port is functionally mutually exclusive with Bluetooth	+
Serial Ports (UARTs)	1x UART debug port - TX, RX Only, levels (UART3)	+
	Up to 2x UART ports, up to 4 Mbps	+
	1x UART port - TX, RX, CTS, RTS	~~WB~~
MMC/SD/SDIO	Up to 1x MMC/SD/SDIO interface	+
SPI	Up to 2x SPI	+
	1x SPI	~~WB~~
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 90x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

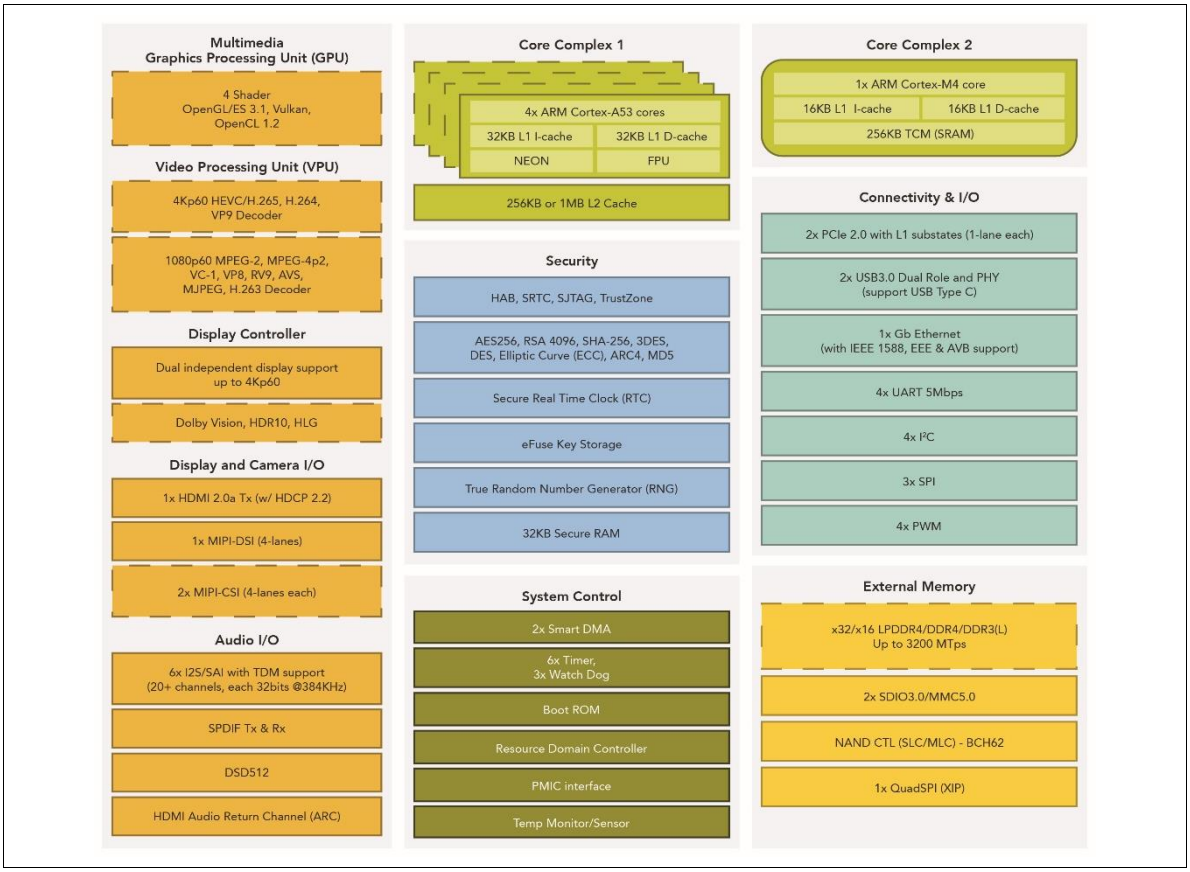
Electrical Specifications	
Supply Voltage	3.35V to 4.55V / Li-Ion battery
Digital I/O voltage	3.3V
Active power consumption	0.5 - 6 W, depending on configuration and system load
RTC battery current consumption	666nA@3V
Mechanical Specifications	
Dimensions	42 x 68 x 5 mm
Weight	14 gram
Connectors	204-pin SO-DIMM edge connector
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 iMX8M SoC

The i.MX 8M family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M4 core processor is for low-power processing.

Figure 2 i.MX8M Block Diagram



3.2 Memory

3.2.1 DRAM

CL-SOM-iMX8 is equipped with up to 4GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide and operates at 1600 MHz clock frequency (LPDDR4-3200).

3.2.2 Bootloader and General Purpose Storage

The CL-SOM-iMX8 uses on-board non-volatile memory (eMMC) storage as its bootloader host. The remaining eMMC space is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

CL-SOM-iMX8 implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-iMX8 SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the CL-SOM-iMX8 carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the CL-SOM-iMX8 digital interfaces operate at 3.3V voltage levels unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-iMX8 Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-SOM-IMX8. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD"** - Always pulled down onboard CL-SOM-IMX8, followed by pull value.
- **"PU"** - Always pulled up onboard CL-SOM-IMX8, followed by pull value.
- **"LVDS"** - Low-voltage differential signaling.

4.1 HDMI

CL-SOM-iMX8 HDMI 2.0 interface (optional) is derived from the i.MX8M HD Display Transmitter Controller IP. For more detailed information, please refer to the i.MX8M TRM chapter 13: HD Display Transmitter Controller (HDMI TX).

The controller supports the following protocols:

- HDMI 1.4 Specification
- HDMI 2.0a Specification
- High-bandwidth Digital Content Protection system, Mapping HDCP to HDMI, Revision 2.2
- High-bandwidth Digital Content Protection system, Mapping HDCP to HDMI, Revision 1.4
- CEA-861-F
- IEC60958

The table below summarizes the HDMI interface signals

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_AUXN	27	AIO	HEAC -	Only w/o ‘LP’ and 'LLP' option.
HDMI_AUXP	29	AIO	HEAC +	Only w/o ‘LP’ and 'LLP' option.
HDMI_CEC	34	O	Consumer Electronics Control	Only w/o ‘LP’ and 'LLP' option.
HDMI_CLKN	32	AO	TMDS Clock-	Only w/o ‘LP’ and 'LLP' option.
HDMI_CLKP	30	AO	TMDS Clock+	Only w/o ‘LP’ and 'LLP' option.
HDMI_DDC_SCL	25	O	VESA Data Display Channel clock	Only w/o ‘LP’ and 'LLP' option.
HDMI_DDC_SDA	31	IO	VESA Data Display Channel data signal	Only w/o ‘LP’ and 'LLP' option.
HDMI_HPD	40	AO	Hot Plug Detect	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXN0	38	AO	TMDS Data0-	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXN1	44	AO	TMDS Data1-	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXN2	50	AO	TMDS Data2-	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXP0	36	AO	TMDS Data0+	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXP1	42	AO	TMDS Data1+	Only w/o ‘LP’ and 'LLP' option.
HDMI_TXP2	48	AO	TMDS Data2+	Only w/o ‘LP’ and 'LLP' option.

4.2 MIPI-DSI Interface

The MIPI-DSI interface (optional) available with CL-SOM-iMX8 is based on the four-lane MIPI display interface available with the iMX8M SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 Data Lanes
- Supports MIPI Standard for D-PHY
- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI_CKN	57*	AO	Negative part of MIPI-CSI clock diff-pair	Only w/o "LL", "LLD" and "LLP"
DSI_CKP	57*	AO	Positive part of MIPI-CSI clock diff-pair	Only w/o "LL", "LLD" and "LLP"
DSI_DN0	41	AO	Negative part of MIPI-DSI data diff-pair 0	Only w/o "LL", "LLD" and "LLP"
DSI_DN1	47	AO	Negative part of MIPI-DSI data diff-pair 2	Only w/o "LL", "LLD" and "LLP"
DSI_DN2	35	AO	Negative part of MIPI-DSI data diff-pair 2	Only w/o "LL", "LLD" and "LLP"
DSI_DN3	53	AO	Negative part of MIPI-DSI data diff-pair 2	Only w/o "LL", "LLD" and "LLP"
DSI_DP0	39	AO	Positive part of MIPI-DSI data diff-pair 0	Only w/o "LL", "LLD" and "LLP"
DSI_DP1	45	AO	Positive part of MIPI-DSI data diff-pair 1	Only w/o "LL", "LLD" and "LLP"
DSI_DP2	33	AO	Positive part of MIPI-DSI data diff-pair 2	Only w/o "LL", "LLD" and "LLP"
DSI_DP3	51	AO	Positive part of MIPI-DSI data diff-pair 3	Only w/o "LL", "LLD" and "LLP"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.3 LVDS Display interface

The LVDS display interface (optional) is implemented onboard CL-SOM-iMX8 by converting the iMX8M MIPI-DSI interface into LVDS interface using the Texas Instruments SN65DSI83 DSI to LVDS transceiver. Texas Instruments SN65DSI83 supports following main features:

- LVDS Output Clock Range of 25 MHz to 154MHz
- ESD Rating ±2 kV (HBM)
- Suitable for up to 60 fps WUXGA 1920 x 1080 at 18 bpp and 24 bpp Color with Reduced Blanking
- Capable of supporting the full resolution of the iMX8M MIPI-DSI interface with reduced blanking

The tables below summarize the LVDS interface signals

Table 7 LVDS 0 display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CLK_N	35	AO	Negative part of differential clock	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_CLK_P	33	AO	Positive part of differential clock	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX0_N	41	AO	Negative part of differential data 0	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX0_P	39	AO	Positive part of differential data 0	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX1_N	47	AO	Negative part of differential data 1	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX1_P	45	AO	Positive part of differential data 1	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX2_N	53	AO	Negative part of differential data 2	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX2_P	51	AO	Positive part of differential data 2	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX3_N	59	AO	Negative part of differential data 3	Only with 'LL', 'LL2' or 'LLP' option
LVDS0_TX3_P	57	AO	Positive part of differential data 3	Only with 'LL', 'LL2' or 'LLP' option

Table 8 LVDS 1 Display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS1_CLK_N	79	AO	Negative part of differential clock	Only with 'LL2' option
LVDS1_CLK_P	77	AO	Positive part of differential clock	Only with 'LL2' option
LVDS1_TX0_N	23	AO	Negative part of differential clock	Only with 'LL2' option
LVDS1_TX0_P	21	AO	Positive part of differential data 0	Only with 'LL2' option
LVDS1_TX1_N	95	AO	Negative part of differential data 1	Only with 'LL2' option
LVDS1_TX1_P	93	AO	Positive part of differential data 1	Only with 'LL2' option
LVDS1_TX2_N	99	AO	Negative part of differential data 2	Only with 'LL2' option
LVDS1_TX2_P	97	AO	Positive part of differential data 2	Only with 'LL2' option
LVDS1_TX3_N	163	AO	Negative part of differential data 3	Only with 'LL2' option
LVDS1_TX3_P	161	AO	Positive part of differential data 3	Only with 'LL2' option

4.4 Camera Serial Interface

CL-SOM-iMX8 MIPI-CSI interface is derived from the four-lane MIPI CSI1 host controller (MIPI_CSI1) integrated into the iMX8M SoC. The CSI1 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-1 specification, providing an interface between CL-SOM-iMX8 and a MIPI CSI-1 compliant camera sensor. The following main features are supported:

- Up-to four data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Compliant to MIPI CSI2 Standard Specification V1.01r06.
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits.
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 9 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI_P1_CKN	109	AO	Always available	Always available
CSI_P1_CKP	107	AO	Always available	Always available
CSI_P1_DN0	85	AI	Always available	Always available
CSI_P1_DN1	91	AI	Always available	Always available
CSI_P1_DN2	103	AI	Always available	Always available
CSI_P1_DN3	113	AI	Always available	Always available
CSI_P1_DP0	83	AI	Always available	Always available
CSI_P1_DP1	89	AI	Always available	Always available
CSI_P1_DP2	101	AI	Always available	Always available
CSI_P1_DP3	115	AI	Always available	Always available

4.5 Ethernet

CL-SOM-iMX8 incorporates a single full-featured 10/100/1000 Ethernet interface (optional), implemented with the iMX8M MAC-NET core in conjunction with a 10/100/1000-Mbit/s MAC coupled with an onboard Atheros AR8033 RGMII GbE PHY.

4.5.1 GbE

CL-SOM-iMX8 with onboard AR8033 PHY supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The table below summarizes the GbE interface signals

Table 10 GbE Interface Signals

Signal Name	Pin #	Type	Description	Availability
AVDD33_ETH	2	P	Center tap supply for Ethernet magnetics.	Only with 'E' option
ETH1_LED_ACT	4	IO;PD8K2	Active High, activity LED driver. 2.5V signal, PHY STRAP	Only with 'E' option
ETH1_LED1_SPD	16	O;PD8K2	Active High, 1Gbps link LED driver. 2.5V signal	Only with 'E' option
ETH1_LED3	22	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	Only with 'E' option
ETH1_MDI0N	6	AIO	Negative part of 100ohm diff-pair 0	Only with 'E' option
ETH1_MDI0P	8	AIO	Positive part of 100ohm diff-pair 0	Only with 'E' option
ETH1_MDI1N	12	AIO	Negative part of 100ohm diff-pair 1	Only with 'E' option
ETH1_MDI1P	14	AIO	Positive part of 100ohm diff-pair 1	Only with 'E' option
ETH1_MDI2N	18	AIO	Negative part of 100ohm diff-pair 2	Only with 'E' option
ETH1_MDI2P	20	AIO	Positive part of 100ohm diff-pair 2	Only with 'E' option
ETH1_MDI3N	24	AIO	Negative part of 100ohm diff-pair 3	Only with 'E' option
ETH1_MDI3P	26	AIO	signal	Only with 'E' option

4.5.2 RGMII

For CL-SOM-iMX8 module w/o “E” option, the iMX8M Ethernet MAC RGMII and MDIO lines are routed directly to carrier board interface. Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the Ethernet RGMII interface signals

Table 11 Ethernet RGMII Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET1.RGMII_TX_CTL	6*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode).	Only w/o ‘E’ option.

Signal Name	Pin #	Type	Description	Availability
ENET1.RGMII_TXC	8*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Only w/o 'E' option.
ENET1.TX_ER	8*	O	When asserted for one or more clock cycles while TXEN is also asserted, PHY sends one or more illegal symbols (MII/RMII mode)	Only w/o 'E' option.
ENET1_MDC	52*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Only w/o 'E' option.
ENET1_MDC	129	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Only w/o 'E' option.
ENET1_MDIO	135	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Only w/o 'E' option.
ENET1_RGMII_RD0	22*	I	Ethernet input data from the PHY	Only w/o 'E' option.
ENET1_RGMII_RD1	4*	I	Ethernet input data from the PHY	Only w/o 'E' option.
ENET1_RGMII_RD2	18*	I	Ethernet input data from the PHY	Only w/o 'E' option.
ENET1_RGMII_RD3	20*	I	Ethernet input data from the PHY	Only w/o 'E' option.
ENET1_RGMII_RX_CTL	26*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode).	Only w/o 'E' option.
ENET1_RGMII_RXC	24*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Only w/o 'E' option.
ENET1_RGMII_TD0	16*	O	Serial output Ethernet data to PHY	Only w/o 'E' option.
ENET1_RGMII_TD1	12*	O	Serial output Ethernet data to PHY	Only w/o 'E' option.
ENET1_RGMII_TD2	62*	O	Serial output Ethernet data to PHY	Only w/o 'E' option.
ENET1_RGMII_TD3	14*	O	Serial output Ethernet data to PHY	Only w/o 'E' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 Wireless Interface

CL-SOM-iMX8 optional 802.11ac WLAN 2x2 MIMO and Bluetooth 4.2/EDR functions are implemented with the Intel 8265 chipset. i.MX8M SoC is interfaced with the WLAN subsystem over i.MX8M PICe 2 interface, while USB port 2 can be optionally multiplexed for the Bluetooth function.

Bluetooth is operational only when GPIO1_IO04 (which controls USB port 2 multiplexing) is driven high.

CL-SOM-iMX8 is equipped with two MHF4 high-frequency connectors allowing easy integration with external antennas:

- Primary WLAN/BT antenna connector ANT3. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality.
- Secondary WLAN antenna connector ANT1. Can be used with any type of 2.4GHz/5.0GHz antenna for dual-band WLAN functionality.

Table 12 ANT1 & ANT32 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	W.FL2-R-MT(60)	Hirose W.FL2-LP-062HF

NOTE: CL-SOM-iMX8 WiFi 802.11ac and Bluetooth functionality are available only with the 'WB' ordering option.

NOTE: When Bluetooth is used, USB port 2 signals are not available on the CL-SOM-iMX8 carrier-board interface connector.

4.6.1 Board revision 1.0

CL-SOM-iMX8 optional 802.11a/b/g/n/ac WLAN 2x2 MIMO and Bluetooth 4.1/EDR functions are implemented with the Cypress CYW4356 chipset. i.MX8M SoC is interfaced with the WLAN Cypress subsystem over i.MX8M PICe 2 interface, while UART4 and SAI3 are dedicated to Bluetooth functionality.

CL-SOM-iMX8 is equipped with two U.FL high-frequency connectors allowing easy integration with external antennas:

- Primary WLAN/BT antenna connector J1. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality.
- Secondary WLAN antenna connector J2. Can be used with any type of 2.4GHz/5.0GHz antenna for Dual-Band WLAN functionality.

Table 13 J1 & J2 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

NOTE: CL-SOM-iMX8 WiFi 802.11 a/b/g/n and Bluetooth functionality is available only with the 'WB' ordering option.

4.7 PCI-Express

The iMX8M SoC is equipped with two single lane PCI Express port (PCIe) v2.1 ports. CL-SOM-iMX8 enables access to the iMX8M PCI-Express port 1 (PCIe 1) through the carrier board interface. This interface requires an external PCIe clock to be supplied in order to utilize interface. The second PCIe port (PCIe) is dedicated to the WLAN solution, and is available on the SODIMM connector only when "WB" option is not populated. PCI port 2 has a build in PCIe reference clock, and doesn't require an external one. The PCI Express port supports the following main features:

- Single lane compliant with PCI Express base specification v2.1 (6.0Gbps).
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface.
- Supports spread spectrum clocking in transmitter and receiver.

Please refer to the iMX8M Reference manual for additional details. The tables below summarize the PCI interface signals

Table 14 PCIE 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE1_CLKREQ_B	5*	I	PCIe clock request signal	Always available
PCIE1_CLKREQ_B	73*	I	PCIe clock request signal	Always available
PCIE1_REF_CLKN	121	AI	100 MHz negative-side reference clock differential input for PCIe	Always available
PCIE1_REF_CLKP	119	AI	100 MHz positive-side reference clock differential input for PCIe	Always available
PCIE1_RXN_N	133	AI	PCI Express receive data negative	Always available

Signal Name	Pin #	Type	Description	Availability
PCIE1_RXN_P	131	AI	PCI Express receive data positive	Always available
PCIE1_TXN_N	127	AO	PCI Express transmit data negative	Always available
PCIE1_TXN_P	125	AO	PCI Express transmit data positive	Always available

Table 15 PCIE 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE2_CLKREQ_B	3	I	PCIe clock request signal	Only w/o 'WB' option.
PCIE2_CLKREQ_B	75	I	PCIe clock request signal	Only w/o 'WB' option.
PCIE2_REF_CLKN	179	AO	100 MHz negative-side reference clock differential output for PCIe. Must be pulled low through 49.9Ω resistor on carrier board.	Only w/o 'WB' option.
PCIE2_REF_CLKP	181	AO	100 MHz positive-side reference clock differential output for PCIe. Must be pulled low through 49.9Ω resistor on carrier board.	Only w/o 'WB' option.
PCIE2_RXN_N	167	AI	PCI Express receive data negative	Only w/o 'WB' option.
PCIE2_RXN_P	169	AI	PCI Express receive data positive	Only w/o 'WB' option.
PCIE2_TXN_N	173	AO	PCI Express transmit data negative	Only w/o 'WB' option.
PCIE2_TXN_P	175	AO	PCI Express transmit data positive	Only w/o 'WB' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Analog Audio

CL-SOM-iMX8 analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with the iMX8M SAI2 port. The WM8731L codec supports the following main features:

- Highly Efficient Headphone driver
- Audio performance (‘A’ weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

NOTE: CL-SOM-iMX8 Analog audio interface is available only with the ‘A’ ordering option.

Table 16 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB

Parameter	Test conditions		Min	Typ	Max	Unit
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
Programmable gain	1 kHz output		-73	0	6	dB
Programmable-gain step size	1 kHz			1		dB
Mute attenuation	1 kHz output, 0dB			80		dB
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0dB gain, Fsample = 48 kHz.		85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.			90		
Dynamic range	A-weighted, −60-dB full-scale input		85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain			-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω		-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10	15		kΩ
	0 dB input gain		20	30		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0-dB gain			85		dB
Dynamic range,	A-weighted, −60-dB full-scale input			85		dB
Total harmonic distortion,	0dB input, 0dB gain			-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.			34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,			14		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance				10		kΩ
Input capacitance				10		pF
Microphone Bias						
Bias voltage			2.375	2.475	2.575	V
Bias-current source					3	mA
Output noise voltage	1kHz to 20kHz			25		nV/√Hz

Please refer to the Wolfson Microelectronics WM8731L datasheet for additional details. The table below summarizes the analog audio interface signals

Table 17 Analog Audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
LHPOUT	203	AO	Left channel headphone output	Only with "A" option
LLINEIN	199	AI	Left channel line input	Only with "A" option
MICBIAS	191	AP	Electret microphone bias supply	Only with "A" option
MICIN	193	AI	Microphone input	Only with "A" option
RHPOUT	201	AO	Right channel headphone output	Only with "A" option
RLINEIN	197	AI	Right channel line input	Only with "A" option

4.9 Sony/Philips Digital Interface (SPDIF)

CL-SOM-iMX8 provides one SPDIF transmitter with one output and one SPDIF receiver with one input.

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the SPDIF interface signals

Table 18 SPDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF1_EXT_CLK	200*	I	External clock signal	Always available
SPDIF1_IN	198*	I	SPDIF input data line signal	Always available
SPDIF1_OUT	196*	O	SPDIF output data line signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.10 Digital Audio (SAI)

CL-SOM-iMX8 enables access to 4 of the iMX8M integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

NOTE: CL-SOM-iMX8 SAI2 interface is available only without the 'A' ordering option.

Please refer to the iMX8M Reference manual for additional details. The tables below summarize the SAI interface signals

Table 19 SAI 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1_MCLK	108*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_RX_BCLK	192	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI1_RX_DATA[0]	134*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI1_RX_DATA[1]	136*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI1_RX_DATA[2]	138*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI1_RX_DATA[4]	137*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RX_DATA[5]	139*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RX_DATA[6]	145*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RX_DATA[7]	152*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RX_SYNC	106*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_RX_SYNC	139*^	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Signal Name	Pin #	Type	Description	Availability
SAI1_TX_BCLK	108*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_BCLK	112*	OI	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_BCLK	142*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[0]	116*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[0]	144*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[1]	118*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[1]	146*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[2]	120*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[2]	148*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[3]	122*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[3]	126*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[4]	128*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_DATA[4]	152*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TX_DATA[4]	194*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TX_DATA[5]	143*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TX_DATA[6]	162*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TX_DATA[7]	130*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI1_TX_SYNC	110*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_SYNC	126*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_SYNC	128*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI1_TX_SYNC	152*^	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI1_RX_DATA[3]	140*^	O	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options

Table 20 SAI 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2_MCLK	191*	IO	Audio master clock. An input when generated externally and an output when generated internally.	only w/o "A" option
SAI2_RX_DATA[0]	203*	I	Receive data, sampled synchronously by the bit clock	only w/o "A" option
SAI2_TX_BCLK	197*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	only w/o "A" option
SAI2_TX_DATA[0]	201*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	only w/o "A" option
SAI2_TX_SYNC	199*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	only w/o "A" option

Table 21 SAI 5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI5_MCLK	191*	IO	Audio master clock. An input when generated externally and an output when generated internally.	only w/o "A" option
SAI5_MCLK	108*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_MCLK	142*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_RX_BCLK	146*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_RX_BCLK	192*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RX_DATA[0]	134*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[0]	148*	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[1]	136*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[2]	128*	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[2]	138*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[3]	140*^	I	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options
SAI5_RX_SYNC	106*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_RX_SYNC	144*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_TX_BCLK	112*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_TX_BCLK	128*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_TX_DATA[0]	116*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI5_TX_DATA[0]	203*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	only w/o "A" option

Signal Name	Pin #	Type	Description	Availability
SAI5_TX_DATA[1]	118*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI5_TX_DATA[1]	199*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	only w/o "A" option
SAI5_TX_DATA[2]	120*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI5_TX_DATA[2]	197*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	only w/o "A" option
SAI5_TX_DATA[3]	122*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o "LP" and "LLP" options
SAI5_TX_DATA[3]	201*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	only w/o "A" option
SAI5_TX_SYNC	110*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_TX_SYNC	126*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o "LP" and "LLP" options
SAI5_RX_DATA[1]	126*	O	Receive data, sampled synchronously by the bit clock	Only w/o "LP" and "LLP" options

Table 22 SAI 6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI6_MCLK	130*^	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o "LP" and "LLP" options
SAI6_MCLK	152*^	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI6_RX_BCLK	137*^	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI6_RX_DATA[0]	139*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI6_RX_DATA[0]	143*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI6_RX_SYNC	145*^	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI6_RX_SYNC	162*^	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI6_TX_BCLK	137*^	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI6_TX_BCLK	194*^	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI6_TX_DATA[0]	139*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI6_TX_DATA[0]	143*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI6_TX_SYNC	145*^	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI6_TX_SYNC	162*^	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI6_RX_BCLK	194*^	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

4.11 USB3.0 ports

The iMX8M SoC is equipped two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains USB 3.0 core, which can operate in both 3.0 and 2.0 mode. One port supports dual-role functionality, while the second port is configured permanently for host mode. USB ports support the following main features:

- SuperSpeed, Hi Speed and Full Speed support
- USB3 U1/U2/U3 Support
- 32 endpoints per slot
- Separate Power Domains for Host and Peripheral Device logic
- Full Power Management capabilities (U1, U2 and U3) with LFPS support for SuperSpeed

Please refer to the iMX8M Reference manual for additional details.

4.11.1 USB3.0 port 2 multiplexing

USB port 2 signals are multiplexed on-board CL-SOM-iMX8 to support two mutually exclusive operation modes:

- USB port 2 signals are routed to the SODIMM connector to be used with external USB devices
- USB port 2 signals are routed to the on-board WiFi/Bluetooth module to be used for Bluetooth functionality

USB port 2 multiplexing is controlled by GPIO1_IO04.

The tables below summarize the USB3.0 interface signals

Table 23 USB3.0 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB1_DN	178	AIO	USB2.0 negative data	Always available
USB1_DP	176	AIO	USB2.0 positive data	Always available
USB1_ID	174	I	USB1 OTG ID signal	Always available
USB1_RX_N	184	AI	USB3.0 receive negative lane	Always available
USB1_RX_P	182	AI	USB3.0 receive positive lane	Always available
USB1_TX_N	190	AO	USB3.0 transmit negative lane	Always available
USB1_TX_P	188	AO	USB3.0 transmit positive lane	Always available
USB1_VBUS_DET	180	I	USB1 VBUS detect	Always available

Table 24 USB3.0 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB2_DN	170	AIO	USB2.0 negative data	Available when GPIO1_IO04 is low
USB2_DP	172	AIO	USB2.0 positive data	Available when GPIO1_IO04 is low
USB2_RX_N	160	AI	USB3.0 receive negative lane	Available when GPIO1_IO04 is low
USB2_RX_P	158	AI	USB3.0 receive positive lane	Available when GPIO1_IO04 is low
USB2_TX_N	166	AO	USB3.0 transmit negative lane	Available when GPIO1_IO04 is low
USB2_TX_P	164	AO	USB3.0 transmit positive lane	Available when GPIO1_IO04 is low
USB2_VBUS_DET	156	I	USB2 VBUS detect	Always available

4.12 MMC / SD /SDIO

One MMC/SD/SDIO port is available through the CL-SOM-iMX8 carrier board interface. The port is derived from the iMX8M on-chip MMC/SD/SDIO controller (uSDHC). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS400 (8-bit transfer mode is only available on uSDHC port 1).
- Dedicated “card detection” and “write protection” signals and (hardware reset not supported).

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals

Table 25 MMC/SD/SDIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC2_CD_B	61*	I	Card detection pin	Always available
USDHC2_CLK	80*	O	Clock for MMC/SD/SDIO card	Always available
USDHC2_CMD	82*	IO	CMD line connect to card	Always available
USDHC2_DATA0	84*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
USDHC2_DATA1	86*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always available
USDHC2_DATA2	88*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
USDHC2_DATA3	90*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
USDHC2_RESET_B	154*	O	Card hardware reset signal, active LOW	Always available
USDHC2_WP	67*	I	Card write protect detection	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 UART

CL-SOM-iMX8 enables access to all 4 of the iMX8M universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The iMX8M UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: The UART2 interface is used onboard CL-SOM-iMX8 for Bluetooth functionality. Using the UART2 interface signals available through the carrier board interface precludes onboard Bluetooth operation.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the UART interface signals

Table 26 UART 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	117*	O	UART-1 clear to send	Always available
UART1_RTS_B	111*	I	UART-1 request to send	Always available
UART1_RX	69*	I	UART-1 serial data receive	Always available
UART1_TX	65*	O	UART-1 serial data transmit	Always available

Table 27 UART 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS_B	5*	O	UART-2 clear to send	Always available
UART2_RTS_B	3*	I	UART-2 request to send	Always available
UART2_RX	63*	I	UART-2 serial data receive	Always available
UART2_TX	58*	O	UART-2 serial data transmit	Always available

Table 28 UART 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3_RX	117*	I	UART-3 serial data receive	Always available
UART3_TX	111*	O	UART-3 serial data transmit	Always available

Table 29 UART 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4_RX	5	I	UART-4 serial data receive	Only w/o "WB" option
UART4_TX	3	O	UART-4 serial data transmit	Only w/o "WB" option

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 I2C

CL-SOM-iMX8 is equipped with three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the I2C interface signals

Table 30 I2C 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_SCL	129*	O	Always available	Always available
I2C1_SDA	135*	IO	Always available	Always available

Table 31 I2C 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	43*	O	I2C serial clock line	Always available
I2C3_SDA	49*	IO	I2C serial data line	Always available

Table 32 I2C 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	73*	O	I2C serial clock line	Always available
I2C4_SDA	75*	IO	Always available	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 ECSPI

Up-to two SPI interfaces are accessible through the CL-SOM-iMX8 carrier board interface. The SPI interfaces are derived from iMX8M integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the ECSPI interface signals

Table 33 ECSPI 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI1_MISO	15*	I	SPI-1 Master data in; slave data out	Always available, starting from board revision 1.1
ECSPI1_MOSI	11*	O	SPI-1 Master data out; slave data in	Always available, starting from board revision 1.1
ECSPI1_SCLK	13*	O	SPI-1 Master clock out; slave clock in	Always available, starting from board revision 1.1
ECSPI1_SS0	17*	O	SPI-1 Chip select 0	Always available, starting from board revision 1.1

Table 34 ECSPI 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3_MISO	63*	I	SPI-3 Master data in; slave data out	Always available
ECSPI3_MOSI	65*	O	SPI-3 Master data out; slave data in	Always available
ECSPI3_SCLK	69*	O	SPI-3 Master clock out; slave clock in	Always available
ECSPI3_SS0	58*	O	SPI-3 Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 JTAG

Documentation of JTAG functionality will be added in a later revision of this document.

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the JTAG interface signals

Table 35 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_MOD	54	I	JTAG MODE	Always available
JTAG_NTRST	56	I	Test Reset	Always available
JTAG_TCK	66	I	Test Clock	Always available
JTAG_TDI	70	I	Test Data In	Always available
JTAG_TDO	72	O	Test Data Out	Always available
JTAG_TMS	68	I	Test Mode Select	Always available

4.17 QSPI

Documentation of QSPI functionality will be added in a later revision of this document.

The tables below summarize the QSPI interface signals

Table 36 QSPI A Interface Signals

Signal Name	Pin #	Type	Description	Availability
QSPI_A_DATA[0]	74*	IO	Data IO 0	Only w/o "LP" and "LLP" options
QSPI_A_DATA[1]	76*	IO	Data IO 1	Only w/o "LP" and "LLP" options
QSPI_A_DATA[2]	92*	IO	Data IO 2	Only w/o "LP" and "LLP" options
QSPI_A_DATA[3]	94*	IO	Data IO 3	Only w/o "LP" and "LLP" options
QSPI_A_DQS	102*	O	Data strobe signal to serial flash device A	Only w/o "LP" and "LLP" options
QSPI_A_SCLK	104*	O	Serial clock	Only w/o "LP" and "LLP" options
QSPI_A_SS0_B	98*	O	Chip select 0	Only w/o "LP" and "LLP" options

Signal Name	Pin #	Type	Description	Availability
QSPI_A_SS1_B	100*	O	Chip select 1	Only w/o "LP" and "LLP" options

Table 37 QSPI B Interface Signals

Signal Name	Pin #	Type	Description	Availability
QSPI_B_DATA[0]	155*	IO	Data IO 0	Always available
QSPI_B_DATA[1]	153*	IO	Data IO 1	Always available
QSPI_B_DATA[2]	151*	IO	Data IO 2	Always available
QSPI_B_DATA[3]	149*	IO	Data IO 3	Always available
QSPI_B_DQS	157*	O	Data strobe signal to serial flash device B	Always available
QSPI_B_SCLK	147*	O	Serial clock	Always available
QSPI_B_SS0_B	7*	O	Chip select 0	Always available
QSPI_B_SS1_B	9*	O	Chip select 1	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.18 NAND

Documentation of NAND functionality will be added in a later revision of this document.

The table below summarizes the NAND interface signals

Table 38 NAND Interface Signals

Signal Name	Pin #	Type	Description	Availability
RAWNAND_ALE	104	O	NAND address latch enable	Always available
RAWNAND_CE0_B	98	O	NAND chip enable 0	Always available
RAWNAND_CE1_B	100	O	NAND chip enable 1	Always available
RAWNAND_CE2_B	7*	O	NAND chip enable 2	Always available
RAWNAND_CE3_B	9*	O	NAND chip enable 3	Always available
RAWNAND_CLE	147*	O	NAND command latch enable	Always available
RAWNAND_DATA00	74	IO	NAND data IO 0	Always available
RAWNAND_DATA01	76	IO	NAND data IO 1	Always available
RAWNAND_DATA02	92	IO	NAND data IO 2	Always available
RAWNAND_DATA03	94	IO	NAND data IO 3	Always available
RAWNAND_DATA04	155*	IO	NAND data IO 4	Always available
RAWNAND_DATA05	153*	IO	NAND data IO 5	Always available
RAWNAND_DATA06	151*	IO	NAND data IO 6	Always available
RAWNAND_DATA07	149*	IO	NAND data IO 7	Always available
RAWNAND_DQS	102	I	NAND DQS strobe	Always available
RAWNAND_RE_B	157*	O	NAND read enable	Always available
RAWNAND_READY_B	124	I	NAND ready ready/busy	Always available
RAWNAND_WE_B	60*	O	NAND write enable	Always available
RAWNAND_WP_B	81*	O	NAND write protect	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.19 PWM

Up to four independent PWM output signals are available at the CL-SOM-iMX8 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the PWM interface signals

Table 39 PWM Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	75*	O	PWM functional output	Always available
PWM1_OUT	200*	O	PWM functional output	Always available
PWM2_OUT	73*	O	PWM functional output	Always available
PWM2_OUT	198*	O	PWM functional output	Always available
PWM3_OUT	49*	O	PWM functional output	Always available
PWM3_OUT	196*	O	PWM functional output	Always available
PWM4_OUT	43*	O	PWM functional output	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.20 GPIO

Up-to 90 of the iMX8M general purpose input/output (GPIO) signals are available through the carrier board interface of CL-SOM-iMX8. When configured as an output, it is possible to write to an iMX8M register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an iMX8M register. In addition, GPIOs peripheral can produce interrupts. The GPIO signals can be configured for the following applications:

NOTE: Not all GPIO signals supported by the iMX8M SoC are available through the CL-SOM-iMX8 carrier board interface.

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the GPIO interface signals

Table 40 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1_IO[16]	52*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[18]	14*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[19]	62*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[20]	12*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[21]	16*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[22]	6*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[23]	8*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[24]	26*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[25]	24*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[26]	22*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[27]	4*	IO	GPIO	Only w/o ‘E’ option.
GPIO1_IO[28]	18*	IO	GPIO	Only w/o ‘E’ option.

Signal Name	Pin #	Type	Description	Availability
GPIO1_IO[29]	20*	IO	GPIO	Only w/o 'E' option.
GPIO2_IO[12]	61*	IO	GPIO	Always available
GPIO2_IO[13]	80*	IO	GPIO	Always available
GPIO2_IO[14]	82*	IO	GPIO	Always available
GPIO2_IO[15]	84*	IO	GPIO	Always available
GPIO2_IO[16]	86*	IO	GPIO	Always available
GPIO2_IO[17]	88*	IO	GPIO	Always available
GPIO2_IO[18]	90*	IO	GPIO	Always available
GPIO2_IO[19]	154*	IO	GPIO	Always available
GPIO2_IO[20]	67*	IO	GPIO	Always available
GPIO3_IO[0]	104*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[1]	98*	O	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[10]	155*	IO	GPIO	Always available
GPIO3_IO[11]	153*	IO	GPIO	Always available
GPIO3_IO[12]	151*	IO	GPIO	Always available
GPIO3_IO[13]	149*	IO	GPIO	Always available
GPIO3_IO[14]	102*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[15]	128*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[15]	157*	IO	GPIO	Always available
GPIO3_IO[16]	124	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[17]	60*	IO	GPIO	Always available
GPIO3_IO[18]	81*	IO	GPIO	Always available
GPIO3_IO[19]	144*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[2]	100*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[20]	146*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[21]	148*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[22]	126*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[25]	142*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[3]	7*	IO	GPIO	Always available
GPIO3_IO[4]	9*	IO	GPIO	Always available
GPIO3_IO[5]	147*	IO	GPIO	Always available
GPIO3_IO[6]	74*	O	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[7]	76*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[8]	92*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO3_IO[9]	94*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[0]	106*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[1]	192*	IO	GPIO	Always available
GPIO4_IO[1]	194*^	IO	GPIO	Always available
GPIO4_IO[10]	110*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[11]	112*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[12]	116*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[13]	118*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[14]	120*^	AO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[15]	122*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[17]	143*^	IO	GPIO	Always available
GPIO4_IO[18]	162*^	IO	GPIO	Always available
GPIO4_IO[19]	130*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[2]	134*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[20]	108*	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[23]	203*	IO	GPIO	only w/o "A" option
GPIO4_IO[24]	199*	IO	GPIO	only w/o "A" option
GPIO4_IO[25]	197*	IO	GPIO	only w/o "A" option
GPIO4_IO[26]	201*	IO	GPIO	only w/o "A" option
GPIO4_IO[3]	136*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[4]	138*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[5]	140*^	IO	GPIO	Only w/o "LP" and "LLP" options
GPIO4_IO[6]	137*^	IO	GPIO	Always available
GPIO4_IO[7]	139*^	IO	GPIO	Always available
GPIO4_IO[8]	145*^	IO	GPIO	Always available
GPIO4_IO[9]	152*^	IO	GPIO	Always available
GPIO5_IO[14]	129*	IO	GPIO	Always available
GPIO5_IO[15]	135*	IO	GPIO	Always available
GPIO5_IO[18]	43*	IO	GPIO	Always available
GPIO5_IO[19]	49*	IO	GPIO	Always available
GPIO5_IO[20]	73*	IO	GPIO	Always available
GPIO5_IO[21]	75*	IO	GPIO	Always available
GPIO5_IO[22]	69*	IO	GPIO	Always available
GPIO5_IO[23]	65*	IO	GPIO	Always available
GPIO5_IO[24]	63*	IO	GPIO	Always available
GPIO5_IO[25]	58*	IO	GPIO	Always available

Signal Name	Pin #	Type	Description	Availability
GPIO5_IO[26]	117*	IO	GPIO	Always available
GPIO5_IO[27]	111*	IO	GPIO	Always available
GPIO5_IO[28]	5*	IO	GPIO	Always available
GPIO5_IO[29]	3*	IO	GPIO	Always available
GPIO5_IO[3]	196*	IO	GPIO	Always available
GPIO5_IO[4]	198*	IO	GPIO	Always available
GPIO5_IO[5]	200*	IO	GPIO	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

5 SYSTEM LOGIC

5.1 Power Supply

The CL-SOM-iMX8 supports two power supply options:

- Regulated DC supply
- Lithium-ion polymer battery

CL-SOM-iMX8 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board

Table 41 Power signals

Signal Name	Pin#	Type	Description
VSYS	10,28,46,64,78,96,114 132,150,168,186	P	Main power supply. Connect to a regulated DC supply or Li-iON battery
V3_COIN	183	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Use 4.7uF capacitor instead of a coin-cell battery if RTC back-up is not required.
ENET1_PHY_VDDA	2	P	TBD
USB_OTG1_VBUS	180	P	Supply for USB PHY. Connect to USB1 VBUS
USB_OTG2_VBUS	196	P	Supply for USB PHY. Connect to 5V if USB2 used.
GND	19,37,55,71,87,105 123,141,159,177,195	P	Common ground.

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

CL-SOM-iMX8 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the iMX8M SoC. The logic that controls both signals is supplied by the iMX8M SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that CL-SOM-iMX8 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the external regulator control signals

Table 42 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	181	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	202	O	Active high power-up request output from iMX8M SoC.	Always available
ONOFF	165	I/PU 100K	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch). ON and OFF requests can be triggered upon voltage sensed through this signal.	Always available

5.2.2 Flash Write-protection

The EEPROM_WP signal can be used to prevent accidental corruption of the data stored in the onboard ID EEPROM. The CL-SOM-iMX8 on-board EEPROM is used to store board specific production information.

NOTE: The EEPROM_WP must be used in conjunction with SW to enable write protection. Using the EEPROM_WP signal alone will not enable write protection.

Table 43 Flash Write protection signals

Signal Name	Pin #	Type	Description	Availability
EEPROM_WP	189	PU	Active low input to enable onboard EEPROM write protection.	Always available

5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX8. Please refer to the iMX8M Reference manual for additional details.

Table 44 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset A valid pulse is low for at least 31mS, with 5.0nS rise/fall times (max).	Always available

5.4 Boot Sequence

CL-SOM-iMX8 boot sequence defines which interface/media is used by CL-SOM-iMX8 to load and execute the initial software (such as U-boot). CL-SOM-iMX8 can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD/MMC card using the MMC/SD/SDIO 2 interface

CL-SOM-iMX8 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CL-SOM-iMX8:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows CL-SOM-iMX8 to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 45 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 46 CL-SOM-iMX8 Boot sequences

sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (Primary boot storage)
Alternate	High	SD card on MMC/SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 90 of the CL-SOM-iMX8 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX8 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 5 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX8 pins are derived from the iMX8M SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 47 Multifunctional Signals

Pin #	i.MX8 signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
3	UART4_TX	UART2_RTS_B	PCIE2_CLKREQ_B			GPIO5_IO[29]	Always available
4	ENET1_RGMII_RD1					GPIO1_IO[27]	Only w/o "E" option
5	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO[28]	Always available
6	ENET1_RGMII_TX_CTL					GPIO1_IO[22]	Only w/o "E" option
7	RAWNAND_CE2_B	QSPI_B_SS0_B				GPIO3_IO[3]	Always available
8	ENET1_RGMII_TXC	ENET1_TX_ER				GPIO1_IO[23]	Only w/o "E" option
9	RAWNAND_CE3_B	QSPI_B_SS1_B				GPIO3_IO[4]	Always available
11	ECSPI1_MOSI	UART3_TX				GPIO5_IO[7]	Always available (rev1.1)
12	ENET1_RGMII_TD1					GPIO1_IO[20]	Only w/o "E" option
13	ECSPI1_SCLK	UART3_RX				GPIO5_IO[6]	Always available (rev1.1)
14	ENET1_RGMII_TD3					GPIO1_IO[18]	Only w/o "E" option
15	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]	Always available (rev1.1)
16	ENET1_RGMII_TD0					GPIO1_IO[21]	Only w/o "E" option
17	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO[9]	Always available (rev1.1)
18	ENET1_RGMII_RD2					GPIO1_IO[28]	Only w/o "E" option
20	ENET1_RGMII_RD3					GPIO1_IO[29]	Only w/o "E" option
22	ENET1_RGMII_RD0					GPIO1_IO[26]	Only w/o "E" option
24	ENET1_RGMII_RXC	ENET1_RX_ER				GPIO1_IO[25]	Only w/o "E" option
26	ENET1_RGMII_RX_CTL					GPIO1_IO[24]	Only w/o "E" option
43	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]	Always available
49	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]	Always available
52	ENET1_MDC					GPIO1_IO[16]	Only w/o "E" option
58	UART2_TX	ECSPI3_SS0				GPIO5_IO[25]	Always available
60	RAWNAND_WE_B					GPIO3_IO[17]	Always available
61	USDHC2_CD_B					GPIO2_IO[12]	Always available
62	ENET1_RGMII_TD2					GPIO1_IO[19]	Only w/o "E" option
63	UART2_RX	ECSPI3_MISO				GPIO5_IO[24]	Always available
65	UART1_TX	ECSPI3_MOSI				GPIO5_IO[23]	Always available
67	USDHC2_WP					GPIO2_IO[20]	Always available
69	UART1_RX	ECSPI3_SCLK				GPIO5_IO[22]	Always available
73	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO[20]	Always available

Pin #	i.MX8 signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
74	RAWNAND_DATA00	QSPI_A_DATA[0]				GPIO3_IO[6]	Only w/o “LP” and “LLP” options
75	I2C4_SDA	PWM1_OUT	PCIE2_CLKREQ_B			GPIO5_IO[21]	ALWAYS AVAILABLE
76	RAWNAND_DATA01	QSPI_A_DATA[1]				GPIO3_IO[7]	Only w/o “LP” and “LLP” options
80	USDHC2_CLK					GPIO2_IO[13]	Always available
81	RAWNAND_WP_B					GPIO3_IO[18]	NAND
82	USDHC2_CMD					GPIO2_IO[14]	Always available
84	USDHC2_DATA0					GPIO2_IO[15]	Always available
86	USDHC2_DATA1					GPIO2_IO[16]	Always available
88	USDHC2_DATA2					GPIO2_IO[17]	Always available
90	USDHC2_DATA3					GPIO2_IO[18]	Always available
92	RAWNAND_DATA02	QSPI_A_DATA[2]				GPIO3_IO[8]	Only w/o “LP” and “LLP” options
94	RAWNAND_DATA03	QSPI_A_DATA[3]				GPIO3_IO[9]	Only w/o “LP” and “LLP” options
98	RAWNAND_CE0_B	QSPI_A_SS0_B				GPIO3_IO[1]	Only w/o “LP” and “LLP” options
100	RAWNAND_CE1_B	QSPI_A_SS1_B				GPIO3_IO[2]	Only w/o “LP” and “LLP” options
102	RAWNAND_DQS	QSPI_A_DQS				GPIO3_IO[14]	Only w/o “LP” and “LLP” options
104	RAWNAND_ALE	QSPI_A_SCLK				GPIO3_IO[0]	Only w/o “LP” and “LLP” options
106	SAI1_RX_SYNC	SAI5_RX_SYNC				GPIO4_IO[0]	Only w/o “LP” and “LLP” options
108	SAI1_MCLK	SAI5_MCLK	SAI1_TX_BCLK			GPIO4_IO[20]	Only w/o “LP” and “LLP” options
110	SAI1_TX_SYNC	SAI5_TX_SYNC				GPIO4_IO[10]	Only w/o “LP” and “LLP” options
111	UART3_TX	UART1_RTS_B				GPIO5_IO[27]	DBG CONSOLE
112	SAI1_TX_BCLK	SAI5_TX_BCLK				GPIO4_IO[11]	Only w/o “LP” and “LLP” options
116	SAI1_TX_DATA[0]	SAI5_TX_DATA[0]				GPIO4_IO[12]	Only w/o “LP” and “LLP” options
117	UART3_RX	UART1_CTS_B				GPIO5_IO[26]	DBG CONSOLE
118	SAI1_TX_DATA[1]	SAI5_TX_DATA[1]				GPIO4_IO[13]	Only w/o “LP” and “LLP” options
120	SAI1_TX_DATA[2]	SAI5_TX_DATA[2]				GPIO4_IO[14]	Only w/o “LP” and “LLP” options
122	SAI1_TX_DATA[3]	SAI5_TX_DATA[3]				GPIO4_IO[15]	Only w/o “LP” and “LLP” options
124	RAWNAND_READY_B					GPIO3_IO[16]	Only w/o “LP” and “LLP” options
126	SAI5_RX_DATA[1]	SAI1_TX_DATA[3]	SAI1_TX_SYNC	SAI5_TX_SYNC		GPIO3_IO[22]	Only w/o “LP” and “LLP” options
128	SAI5_RX_DATA[2]	SAI1_TX_DATA[4]	SAI1_TX_SYNC	SAI5_TX_BCLK		GPIO3_IO[23]	Only w/o “LP” and “LLP” options
129	I2C1_SCL	ENET1_MDC				GPIO5_IO[14]	ALWAYS AVAILABLE
130	SAI1_TX_DATA[7]	SAI6_MCLK				GPIO4_IO[19]	Only w/o “LP” and “LLP” options
134	SAI1_RX_DATA[0]	SAI5_RX_DATA[0]				GPIO4_IO[2]	Only w/o “LP” and “LLP” options
135	I2C1_SDA	ENET1_MDIO				GPIO5_IO[15]	ALWAYS AVAILABLE
136	SAI1_RX_DATA[1]	SAI5_RX_DATA[1]				GPIO4_IO[3]	Only w/o “LP” and “LLP” options
137	SAI1_RX_DATA[4]	SAI6_TX_BCLK	SAI6_RX_BCLK			GPIO4_IO[6]	bootstrap
138	SAI1_RX_DATA[2]	SAI5_RX_DATA[2]				GPIO4_IO[4]	Only w/o “LP” and “LLP” options
139	SAI1_RX_DATA[5]	SAI6_TX_DATA[0]	SAI6_RX_DATA[0]	SAI1_RX_SYNC		GPIO4_IO[7]	bootstrap
140	SAI1_RX_DATA[3]	SAI5_RX_DATA[3]				GPIO4_IO[5]	Only w/o “LP” and “LLP” options
142	SAI5_MCLK	SAI1_TX_BCLK				GPIO3_IO[25]	Only w/o “LP” and “LLP” options
143	SAI1_TX_DATA[5]	SAI6_RX_DATA[0]	SAI6_TX_DATA[0]			GPIO4_IO[17]	bootstrap
144	SAI5_RX_SYNC	SAI1_TX_DATA[0]				GPIO3_IO[19]	Only w/o “LP” and “LLP” options
145	SAI1_RX_DATA[6]	SAI6_TX_SYNC	SAI6_RX_SYNC			GPIO4_IO[8]	bootstrap
146	SAI5_RX_BCLK	SAI1_TX_DATA[1]				GPIO3_IO[20]	Only w/o “LP” and “LLP” options
147	RAWNAND_CLE	QSPI_B_SCLK				GPIO3_IO[5]	QSPI
148	SAI5_RX_DATA[0]	SAI1_TX_DATA[2]				GPIO3_IO[21]	Only w/o “LP” and “LLP” options
149	RAWNAND_DATA07	QSPI_B_DATA[3]				GPIO3_IO[13]	QSPI
151	RAWNAND_DATA06	QSPI_B_DATA[2]				GPIO3_IO[12]	QSPI
152	SAI1_RX_DATA[7]	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA[4]		GPIO4_IO[9]	bootstrap (LCD)

Pin #	i.MX8 signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
153	RAWNAND_DATA05	QSPI_B_DATA[1]				GPIO3_IO[11]	QSPI
154	USDHC2_RESET_B					GPIO2_IO[19]	SDCARD
155	RAWNAND_DATA04	QSPI_B_DATA[0]				GPIO3_IO[10]	QSPI
157	RAWNAND_RE_B	QSPI_B_DQS				GPIO3_IO[15]	QSPI
162	SAI1_TX_DATA[6]	SAI6_RX_SYNC	SAI6_TX_SYNC			GPIO4_IO[18]	bootstrap
191	SAI2_MCLK	SAI5_MCLK				GPIO4_IO[27]	
192	SAI1_RX_BCLK	SAI5_RX_BCLK				GPIO4_IO[1]	
194	SAI1_TX_DATA[4]	SAI6_RX_BCLK	SAI6_TX_BCLK			GPIO4_IO[16]	bootstrap
196	SPDIF1_OUT	PWM3_OUT				GPIO5_IO[3]	
197	SAI2_TX_BCLK	SAI5_TX_DATA[2]				GPIO4_IO[25]	CODEC
198	SPDIF1_IN	PWM2_OUT				GPIO5_IO[4]	
199	SAI2_TX_SYNC	SAI5_TX_DATA[1]				GPIO4_IO[24]	CODEC
200	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO[5]	
201	SAI2_TX_DATA[0]	SAI5_TX_DATA[3]				GPIO4_IO[26]	CODEC
203	SAI2_RX_DATA[0]	SAI5_TX_DATA[0]				GPIO4_IO[23]	CODEC

5.6 RTC

CL-SOM-iMX8 features an on-board ultra-low-power EM3027 real time clock (RTC). The RTC connected to the i.MX8M SoC using I2C3 interface at address 56h.

At main power supply absence, in order to maintain activities of the RTC, i.e. clock advancement and data storage, use of a backup power supply is essential. External backup battery should be used in order to maintain clock and time information when main supply is not present. A rechargeable battery can be charged from the VSYS voltage using an internal trickle charger of the RTC.

For more information about CL-SOM-iMX8 RTC please refer to the EM3027 datasheet.

5.7 LED

CL-SOM-iMX8 features a single general purpose green LED controlled by GPIO1_124 signal of the iMX8M. The LED is ON when GPIO1_12 is logic High.

5.8 Boot Strap Signals

The following CL-SOM-iMX8 signals must not be pulled or driven by carrier board during SoM power-up or reset.

Table 48 Boot Strap Signals

Pin#
P1-130, P1-162, P1-143, P1-194, P1-122, P1-120, P1-118, P1-116, P1-152, P1-145, P1-139, P1-137, P1-140, P1-138, P1-136, P1-134

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX8 CoM/SoM carrier board interface uses the SODIMM-204 edge connector. The SoM pinout is detailed in the table below.

6.1 Connector Pinout

Table 49 Connector P1

Pin #	CL-SOM-iMX8 Signal Name	Ref.		Pin #	CL-SOM-iMX8 Signal Name	Ref.
1	GND	5.1		2	AVDD33_ETH	4.5.1
3	PCIE2_CLKREQ_B UART2_RTS_B UART4_TX GPIO5_IO[29]	4.7 4.13 4.13 4.21		4	ETH1_LED_ACT ENET1_RGMII_RD1 GPIO1_IO[27]	4.5.1 4.5.2 4.20
5	PCIE1_CLKREQ_B UART2_CTS_B UART4_RX GPIO5_IO[28]	4.7 4.13 4.13 4.20		6	ETH1_MDI0N ENET1.RGMII_TX_CTL GPIO1_IO[22]	4.5.1 4.5.2 4.21
7	QSPI_B_SS0_B RAWNAND_CE2_B GPIO3_IO[3]	4.17 4.18 4.21		8	ETH1_MDI0P ENET1.RGMII_TXC ENET1.TX_ER GPIO1_IO[23]	4.5.1 4.5.2 4.5.2 4.20
9	QSPI_B_SS1_B RAWNAND_CE3_B GPIO3_IO[4]	4.17 4.18 4.21		10	VSYS	5.1
11	UART3_TX ECSPI1_MOSI GPIO5_IO[7]	4.13 4.15 4.20		12	ETH1_MDI1N ENET1_RGMII_TD1 GPIO1_IO[20]	4.5.1 4.5.2 4.21
13	UART3_RX ECSPI1_SCLK GPIO5_IO[6]	4.13 4.15 4.21		14	ETH1_MDI1P ENET1_RGMII_TD3 GPIO1_IO[18]	4.5.1 4.5.2 4.21
15	UART3_CTS_B ECSPI1_MISO GPIO5_IO[8]	4.13 4.15 4.21		16	ETH1_LED1_SPD ENET1_RGMII_TD0 GPIO1_IO[21]	4.5.1 4.5.2 4.21
17	UART3_RTS_B ECSPI1_SS0 GPIO5_IO[9]	4.13 4.15 4.20		18	ETH1_MDI2N ENET1_RGMII_RD2 GPIO1_IO[28]	4.5.1 4.5.2
19	GND	5.1		20	ETH1_MDI2P ENET1_RGMII_RD3 GPIO1_IO[29]	4.5.1 4.5.2 4.20
21	LVDS1_TX0_P	4.3		22	ETH1_LED3 ENET1_RGMII_RD0 GPIO1_IO[26]	4.5.1 4.5.2 4.21
23	LVDS1_TX0_N	4.3		24	ETH1_MDI3N ENET1_RGMII_RXC GPIO1_IO[25]	4.5.1 4.5.2 4.21
25	HDMI_DDC_SCL	4.1		26	ETH1_MDI3P ENET1_RGMII_RX_CTL GPIO1_IO[24]	4.5.1 4.5.2
27	HDMI_AUXN	4.1		28	VSYS	5.1
29	HDMI_AUXP	4.1		30	HDMI_CLKP	4.1
31	HDMI_DDC_SDA	4.1		32	HDMI_CLKN	4.1
33	DSI_DP2 LVDS0_CLK_P	4.2 4.3		34	HDMI_CEC	4.1
35	DSI_DN2 LVDS0_CLK_N	4.2 4.3		36	HDMI_TXP0	4.1
37	GND	5.1		38	HDMI_TXN0	4.1
39	DSI_DP0 LVDS0_TX0_P	4.2 4.3		40	HDMI_HPD	4.1
41	DSI_DN0 LVDS0_TX0_N	4.2 4.3		42	HDMI_TXP1	4.1
43	I2C3_SCL PWM4_OUT GPIO5_IO[18]	4.14 4.19 4.21		44	HDMI_TXN1	4.1
45	DSI_DP1 LVDS0_TX1_P	4.2 4.3		46	VSYS	5.1
47	DSI_DN1 LVDS0_TX1_N	4.2 4.3		48	HDMI_TXP2	4.1

49	I2C3_SDA PWM3_OUT GPIO5_IO[19]	4.14 4.19 4.21		50	HDMI_TXN2	4.1
51	DSI_DP3 LVDS0_TX2_P	4.2 4.3		52	ENET1_MDC GPIO1.IO[16]	4.5.2 4.20
53	DSI_DN3 LVDS0_TX2_N	4.2 4.3		54	JTAG_MOD	4.16
55	GND	5.1		56	JTAG_NTRST	4.16
57	DSI_CKN DSI_CKP LVDS0_TX3_P	4.2 4.2 4.3		58	UART2_TX ECSPI3_SS0 GPIO5_IO[25]	4.13 4.15 4.20
59	LVDS0_TX3_N	4.3		60	RAWNAND_WE_B GPIO3_IO[17]	4.18 4.21
61	USDHC2_CD_B GPIO2_IO[12]	4.12 4.21		62	ENET1_RGMII_TD2 GPIO1_IO[19]	4.5.2 4.20
63	UART2_RX ECSPI3_MISO GPIO5_IO[24]	4.13 4.15 4.21		64	VSYS	5.1
65	UART1_TX ECSPI3_MOSI GPIO5_IO[23]	4.13 4.15 4.21		66	JTAG_TCK	4.16
67	USDHC2_WP GPIO2_IO[20]	4.12 4.21		68	JTAG_TMS	4.16
69	UART1_RX ECSPI3_SCLK GPIO5_IO[22]	4.13 4.15 4.21		70	JTAG_TDI	4.16
71	GND	5.1		72	JTAG_TDO	4.16
73	PCIE1_CLKREQ_B I2C4_SCL PWM2_OUT GPIO5_IO[20]	4.7 4.14 4.19 4.21		74	QSPI_A_DATA[0] RAWNAND_DATA00 GPIO3_IO[6]	4.17 4.18 4.20
75	PCIE2_CLKREQ_B I2C4_SDA PWM1_OUT GPIO5_IO[21]	4.7 4.14 4.19 4.21		76	QSPI_A_DATA[1] RAWNAND_DATA01 GPIO3_IO[7]	4.17 4.18 4.21
77	LVDS1_CLK_P	4.3		78	VSYS	5.1
79	LVDS1_CLK_N	4.3		80	USDHC2_CLK GPIO2_IO[13]	4.12 4.21
81	RAWNAND_WP_B GPIO3_IO[18]	4.18 4.21		82	USDHC2_CMD GPIO2_IO[14]	4.12 4.21
83	CSI_P1_DP0	4.4		84	USDHC2_DATA0 GPIO2_IO[15]	4.12 4.21
85	CSI_P1_DN0	4.4		86	USDHC2_DATA1 GPIO2_IO[16]	4.12 4.21
87	GND	5.1		88	USDHC2_DATA2 GPIO2_IO[17]	4.12 4.21
89	CSI_P1_DP1	4.4		90	USDHC2_DATA3 GPIO2_IO[18]	4.12 4.21
91	CSI_P1_DN1	4.4		92	QSPI_A_DATA[2] RAWNAND_DATA02 GPIO3_IO[8]	4.17 4.18 4.21
93	LVDS1_TX1_P	4.3		94	QSPI_A_DATA[3] RAWNAND_DATA03 GPIO3_IO[9]	4.17 4.18 4.21
95	LVDS1_TX1_N	4.3		96	VSYS	5.1
97	LVDS1_TX2_P	4.3		98	QSPI_A_SS0_B RAWNAND_CE0_B GPIO3_IO[1]	4.17 4.18 4.20
99	LVDS1_TX2_N	4.3		100	QSPI_A_SS1_B RAWNAND_CE1_B GPIO3_IO[2]	4.17 4.18 4.21
101	CSI_P1_DP2	4.4		102	QSPI_A_DQS RAWNAND_DQS GPIO3_IO[14]	4.17 4.18 4.21
103	CSI_P1_DN2	4.4		104	QSPI_A_SCLK RAWNAND_ALE GPIO3_IO[0]	4.17 4.18 4.21
105	GND	5.1		106	SAI1_RX_SYNC SAI5_RX_SYNC GPIO4_IO[0]	4.10 4.10 4.21
107	CSI_P1_CKP	4.4		108	SAI1_MCLK SAI1_TX_BCLK SAI5_MCLK GPIO4_IO[20]	4.10 4.10 4.10 4.21

109	CSI_P1_CKN	4.4		110	SAI1_TX_SYNC SAI5_TX_SYNC GPIO4_IO[10]	4.10 4.10 4.21
111	UART1_RTS_B UART3_TX GPIO5_IO[27]	4.13 4.13 4.21		112	SAI1_TX_BCLK SAI5_TX_BCLK GPIO4_IO[11]	4.10 4.10 4.21
113	CSI_P1_DN3	4.4		114	VSYS	5.1
115	CSI_P1_DP3	4.4		116	SAI1_TX_DATA[0] SAI5_TX_DATA[0] GPIO4_IO[12]	4.10 4.10
117	UART1_CTS_B UART3_RX GPIO5_IO[26]	4.13 4.13 4.21		118	SAI1_TX_DATA[1] SAI5_TX_DATA[1] GPIO4_IO[13]	4.10 4.10 4.21
119	PCIE1_REF_CLKP	4.7		120	SAI1_TX_DATA[2] SAI5_TX_DATA[2] GPIO4_IO[14]	4.10 4.10 4.21
121	PCIE1_REF_CLKN	4.7		122	SAI1_TX_DATA[3] SAI5_TX_DATA[3] GPIO4_IO[15]	4.10 4.10 4.21
123	GND	5.1		124	RAWNAND_READY_B GPIO3_IO[16]	4.18 4.21
125	PCIE1_TXN_P	4.7		126	SAI1_TX_DATA[3] SAI1_TX_SYNC SAI5_RX_DATA[1] SAI5_TX_SYNC GPIO3_IO[22]	4.10 4.10 4.10 4.10 4.21
127	PCIE1_TXN_N	4.7		128	SAI1_TX_DATA[4] SAI1_TX_SYNC SAI5_RX_DATA[2] SAI5_TX_BCLK GPIO3_IO[15]	4.10 4.10 4.10 4.10 4.21
129	ENET1_MDC I2C1_SCL GPIO5_IO[14]	4.5.2 4.14 4.21		130	SAI1_TX_DATA[7] SAI6_MCLK SAI6_MCLK GPIO4_IO[19]	4.10 4.10 4.10 4.20
131	PCIE1_RXN_P	4.7		132	VSYS	5.1
133	PCIE1_RXN_N	4.7		134	SAI1_RX_DATA[0] SAI5_RX_DATA[0] GPIO4_IO[2]	4.10 4.10 4.21
135	ENET1_MDIO I2C1_SDA GPIO5_IO[15]	4.5.2 4.14 4.21		136	SAI1_RX_DATA[1] SAI5_RX_DATA[1] GPIO4_IO[3]	4.10 4.10 4.21
137	SAI1_RX_DATA[4] SAI6_RX_BCLK SAI6_TX_BCLK GPIO4_IO[6]	4.10 4.10 4.10 4.21		138	SAI1_RX_DATA[2] SAI5_RX_DATA[2] GPIO4_IO[4]	4.10 4.10 4.21
139	SAI1_RX_DATA[5] SAI1_RX_SYNC SAI6_RX_DATA[0] SAI6_TX_DATA[0] GPIO4_IO[7]	4.10 4.10 4.10 4.10 4.21		140	SAI1_RX_DATA[3] SAI5_RX_DATA[3] GPIO4_IO[5]	4.10 4.10 4.20
141	GND	5.1		142	SAI1_TX_BCLK SAI5_MCLK GPIO3_IO[25]	4.10 4.10 4.21
143	SAI1_TX_DATA[5] SAI6_RX_DATA[0] SAI6_TX_DATA[0] GPIO4_IO[17]	4.10 4.10 4.10 4.21		144	SAI1_TX_DATA[0] SAI5_RX_SYNC GPIO3_IO[19]	4.10 4.10 4.21
145	SAI1_RX_DATA[6] SAI6_RX_SYNC SAI6_TX_SYNC GPIO4_IO[8]	4.10 4.10 4.10 4.21		146	SAI1_TX_DATA[1] SAI5_RX_BCLK GPIO3_IO[20]	4.10 4.10 4.21
147	QSPI_B_SCLK RAWNAND_CLE GPIO3_IO[5]	4.17 4.18 4.21		148	SAI1_TX_DATA[2] SAI5_RX_DATA[0] GPIO3_IO[21]	4.10 4.10 4.21
149	QSPI_B_DATA[3] RAWNAND_DATA07 GPIO3_IO[13]	4.17 4.18 4.20		150	VSYS	5.1
151	QSPI_B_DATA[2] RAWNAND_DATA06 GPIO3_IO[12]	4.17 4.18 4.20 4.21		152	SAI1_RX_DATA[7] SAI1_TX_DATA[4] SAI1_TX_SYNC SAI6_MCLK GPIO4_IO[9]	4.10 4.10 4.10 4.10 4.21

153	QSPI_B_DATA[1] RAWNAND_DATA05 GPIO3_IO[11]	4.17 4.18 4.20		154	USDHC2_RESET_B GPIO2_IO[19]	4.12 4.21
155	QSPI_B_DATA[0] RAWNAND_DATA04 GPIO3_IO[10]	4.17 4.18 4.20		156	USB2_VBUS_DET	4.11
157	QSPI_B_DQS RAWNAND_RE_B GPIO3_IO[15]	4.17 4.18 4.20		158	USB2_RX_P	4.11
159	GND	5.1		160	USB2_RX_N	4.11
161	LVDS1_TX3_P	4.3		162	SAI1_TX_DATA[6] SAI6_RX_SYNC SAI6_TX_SYNC GPIO4_IO[18]	4.10 4.10 4.10 4.20
163	LVDS1_TX3_N	4.3		164	USB2_TX_P	4.11
165	ONOFF	5.2.1		166	USB2_TX_N	4.11
167	PCIE2_RXN_N	4.7		168	VSYS	5.1
169	PCIE2_RXN_P	4.7		170	USB2_DN	4.11
171	COLD_RESET_IN	5.3		172	USB2_DP	4.11
173	PCIE2_TXN_N	4.7		174	USB1_ID	4.11
175	PCIE2_TXN_P	4.7		176	USB1_DP	4.11
177	GND	5.1		178	USB1_DN	4.11
179	PCIE2_REF_CLKN	4.7		180	USB1_VBUS_DET	4.11
181	PCIE2_REF_CLKP PMIC_STBY_REQ	4.7 5.2.1		182	USB1_RX_P	4.11
183	VCC_RTC	5.1		184	USB1_RX_N	4.11
185	ALT_BOOT	5.4		186	VSYS	5.1
187	NC			188	USB1_TX_P	4.11
189	EEPROM_WP	5.2.2		190	USB1_TX_N	4.11
191	MICBIAS	4.8		192	SAI1_RX_BCLK SAI5_RX_BCLK GPIO4_IO[1]	4.10 4.10 4.21
193	MICIN	4.8		194	SAI1_TX_DATA[4] SAI6_RX_BCLK SAI6_TX_BCLK GPIO4_IO[1]	4.10 4.10 4.10 4.21
195	AUD_GND	5.1		196	SPDIF1_OUT PWM3_OUT GPIO5_IO[3]	4.9 4.19 4.20
197	RLINEIN SAI2_TX_BCLK SAI5_TX_DATA[2] GPIO4_IO[25]	4.8 4.10 4.10 4.20		198	SPDIF1_IN PWM2_OUT GPIO5_IO[4]	4.9 4.19 4.20
199	LLINEIN SAI2_TX_SYNC SAI5_TX_DATA[1] GPIO4_IO[24]	4.8 4.10 4.10 4.20		200	SPDIF1_EXT_CLK PWM1_OUT GPIO5_IO[5]	4.9 4.19 4.21
201	RHPOUT SAI2_TX_DATA[0] SAI5_TX_DATA[3] GPIO4_IO[26]	4.8 4.10 4.10 4.20		202	PMIC_ON_REQ	5.2.1
203	LHPOUT SAI2_RX_DATA[0] SAI5_TX_DATA[0] GPIO4_IO[23]	4.8 4.10 4.10 4.20		204	VSYS	5.1

6.2 Mating Connectors

Table 50 Connector type

CL-SOM-iMX8 connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 3 CL-SOM-iMX8 top

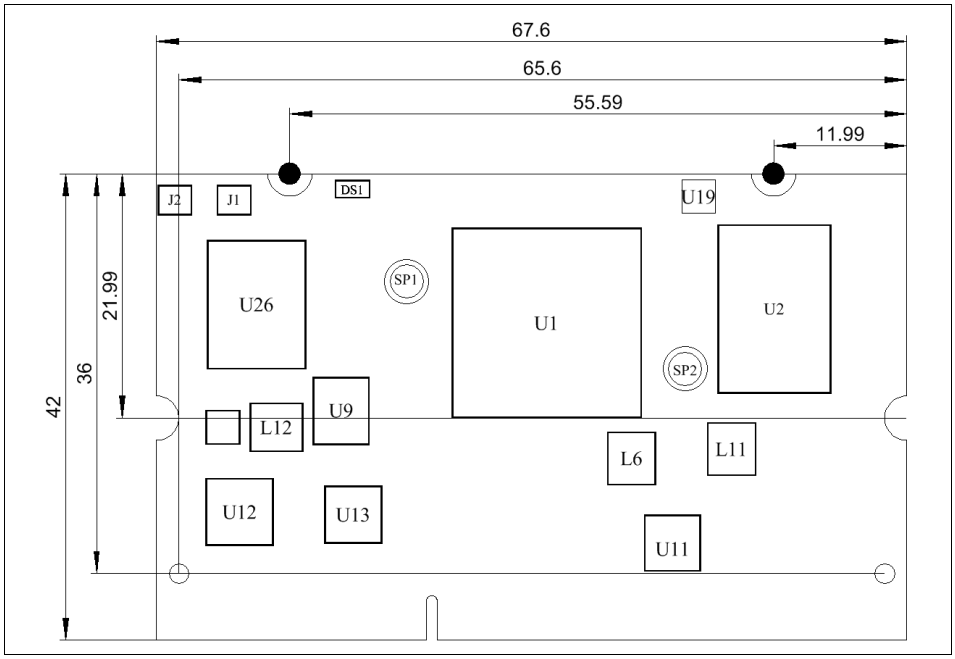
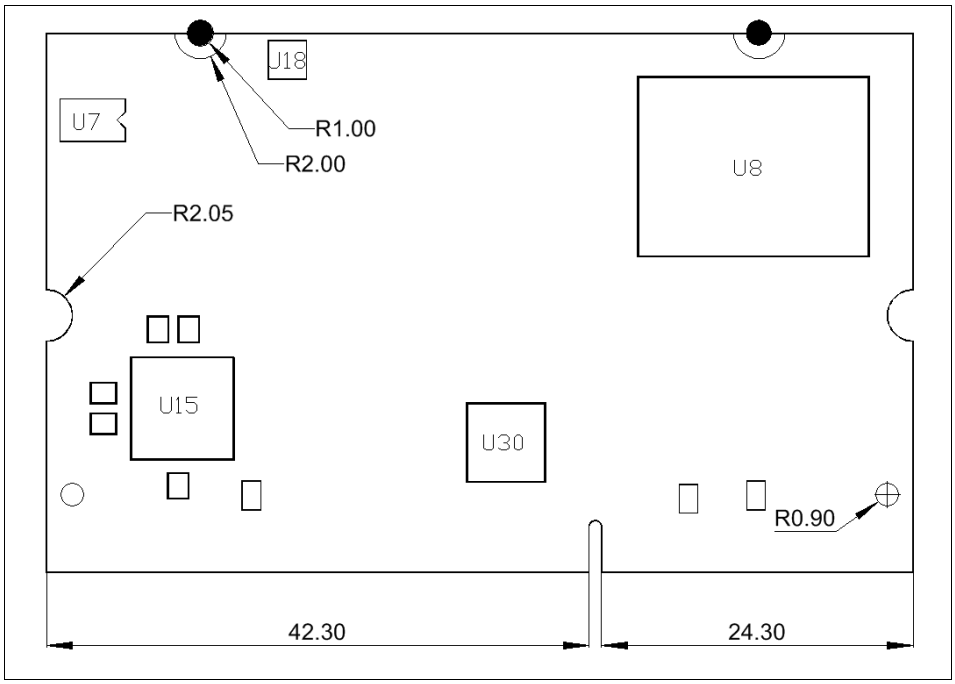


Figure 4 CL-SOM-iMX8 bottom



1. All dimensions are in millimeters.
2. The height of all components is < 2mm.
3. Baseboard connectors provide 2.8 ± 0.25mm board-to-board clearance.
4. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at TBD

6.4 Standoffs/Spacers

CL-SOM-iMX8 has two semi-circular mounting holes to physically secure the SoM to the carrier board. Secure CL-SOM-iMX8 to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 3.0±0.1 mm length

6.5 Heat Spreader and Cooling Solutions

CompuLab provides CL-SOM-iMX8 with an optional heat-spreader assembly. The CL-SOM-iMX8 heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the CL-SOM-iMX8 temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 51 Absolute Maximum ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (VSYS)	-0.3		4.8	V
USB OTG VBUS (USB_OTGX_VBUS)	0		5.25	V
Voltage on any non-power supply pin	-0.5		3.6	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 52 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (VSYS)	3.35	4.2	4.5	V
Backup battery supply voltage (V3_COIN)	1.4	3.0	5.5	V
VBUS_5V_OTG	2.7	5	5.25	V

7.3 DC Electrical Characteristics

Table 53 DC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
V_{OH}	3.05			V
V_{OL}			0.15	V
V_{IH}	2.38		3.3	V
V_{IL}	0		0.96	V

7.4 ESD Performance

Table 54 ESD Performance

Interface	ESD Performance
iMX8M pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)
USB Hub pins (UH option)	5kV Human Body Model (HBM)
LVDS (L option)	2kV Human Body Model (HBM)

7.5 Operating Temperature Ranges

CL-SOM-iMX8 is available with three options of operating temperature range.

Table 55 CL-SOM-iMX8 Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CL-SOM-iMX8 operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-iMX8.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB3.0: DP/DM and SS_TX/SS_RX have impedance requirement of 90 ohms.
  - All single-ended signals: have impedance requirement of 50 ohms.
  - PCIe TX/RX data pairs: have impedance requirement of 85 ohms.
  - Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI): have impedance requirement of 100 ohms.
- Be careful when placing components under the CL-SOM-iMX8 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CL-SOM-iMX8.
- Refer to the SB-iMX8 carrier board reference design schematics.
- It is recommended to send custom carrier board schematics to the Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.

- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX8, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-iMX8 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of “Qualified Magnetics” contains magnetics recommended by Micrel. Designers should test and qualify all magnetics before using them in an application.

Table 56 Qualified Magnetics

Vendor	P/N	Auto MDI-X
UDE	RB1-125BAK1A	Integrated RJ45
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-iMX8 reference design schematics