SB-iMX8

BOARD REVISION: 1.1

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03	ETHERNET
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09	POWER
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11	PCIe X1 SLOT
12	Mechanics

I2C ADDRESSES

DEVICE	ADDRESS
EEPROM	0x54..57
GPIO EXT	0x20

PCB1

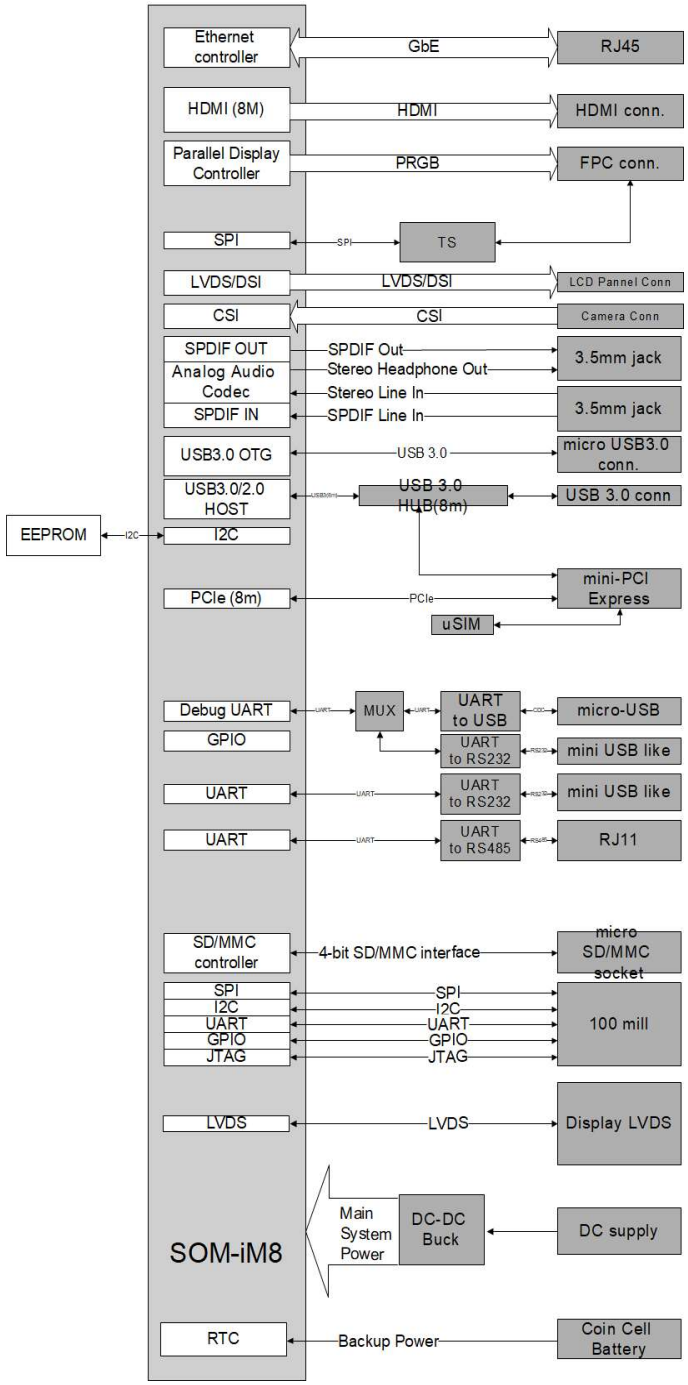
PCB, SB-iMX8 Rev 1.1
188C03101

ZZ1

PARSER_VERSION_1.0

FID1 FID2 FID3 FID4 FID5 FID6

SB-iMX8 REV 1.1



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C	01. BLOCK DIAGRAM	1.1
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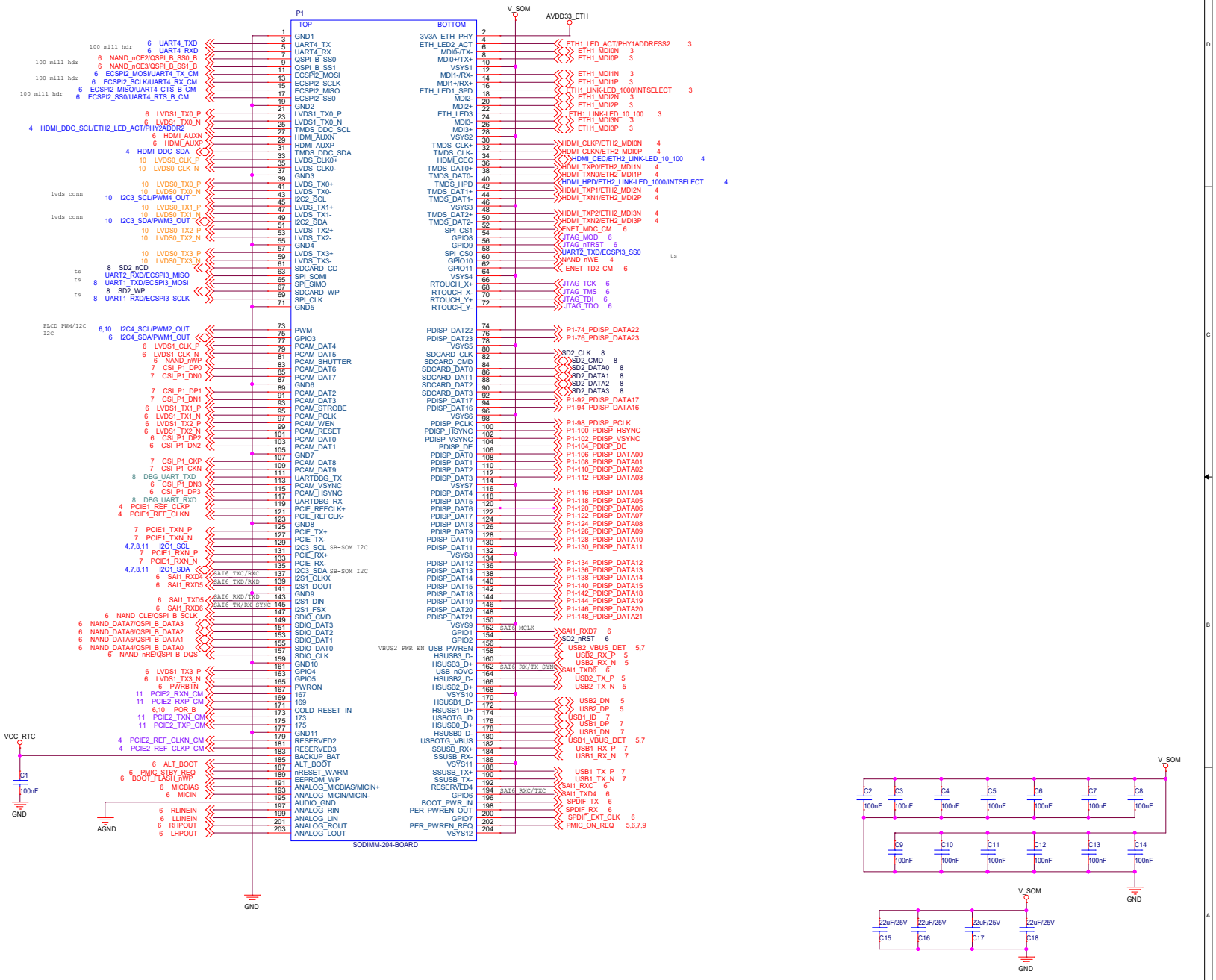
CARIER SODIMM INTERFACE



Size	Title	Rev
C	02. SODIMM	1.1
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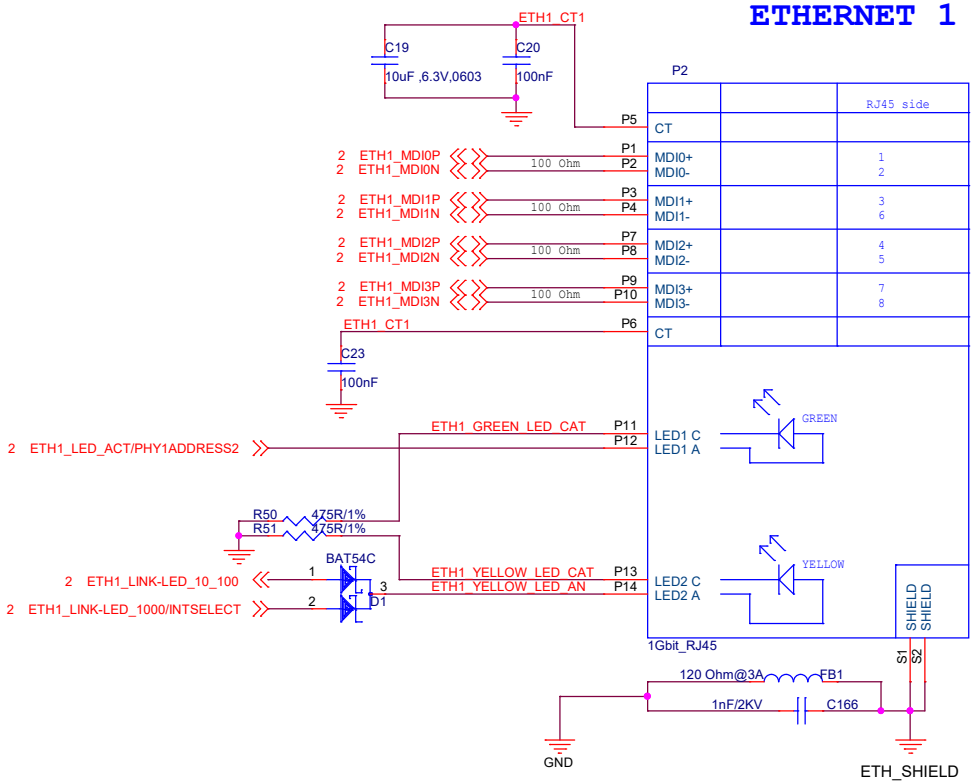
ETHERNET 1



Layout notes
1: 100ohm differential impedance control.
2: Match each differential signals pair ± 5 mils.
3: Not more than two vias on each differential trace
4: GND stitching VIA near every signal VIA
5: The spacing between differential pair signals and other signals should be at least three times the trace width.

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B	03. ETHERNET 1, LCD CONN	1.1
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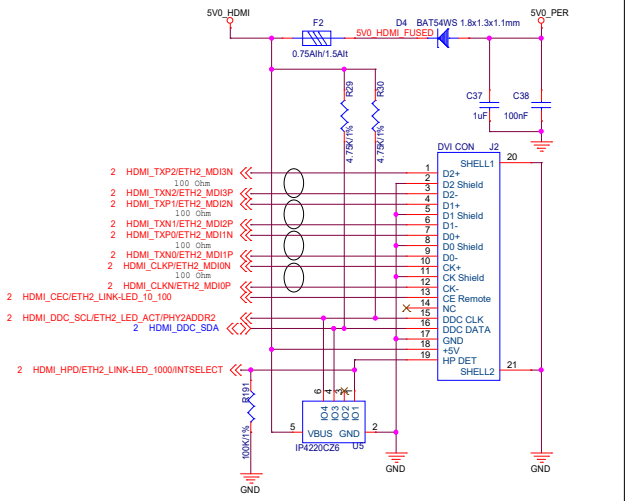
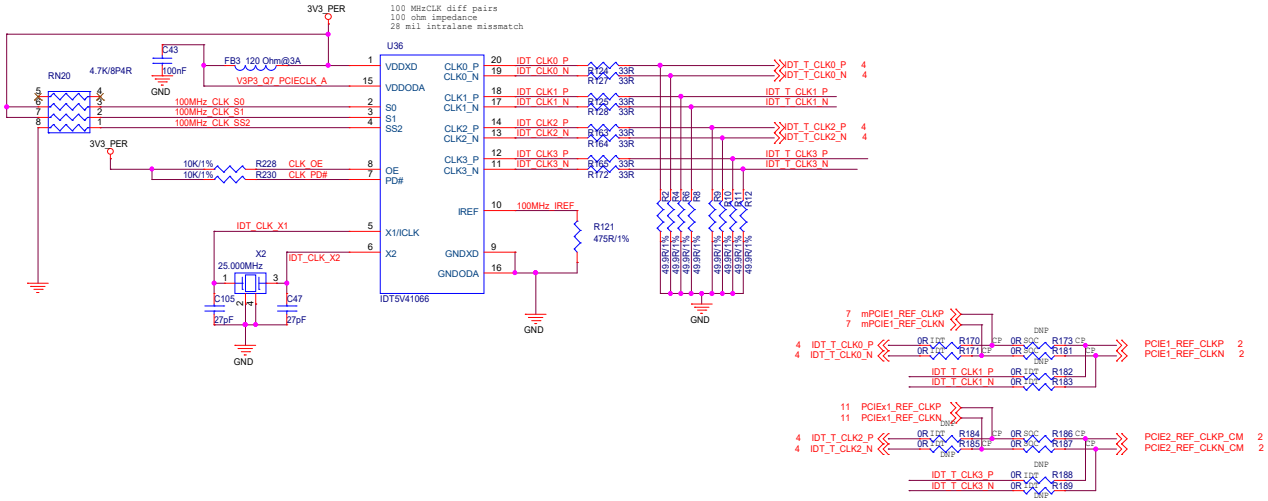
HDMI (8M)



PCIe CLK

100MHz clk

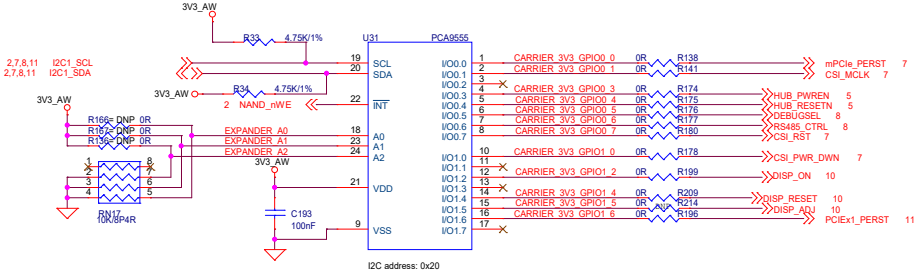
Make trace to VDD AsShortAsPossible, decoupling caps and FB can be placed on back and placed ACAP to VDD



PCIe1 is connected to mini PCIe.
The clock generator generates Mini PCIe's ref clock and iMX8's PCIe1 ref clock (in SOM-iMX8)

PCIe2 is connected to WLAN (if assembled) in SOM-iMX8 or to PCIe X1 Slot.
In SOM-iMX8 REV 1.1: iMX8's clock output provides PCIe2 REF CLK to iMX8 and in addition to that provides ref clock to WLAN (if assembled) or to PCIe X1 Slot.
In SOM-iMX8 REV 1.0: The clock generator also generates PCIe X1 Slot's ref clock and iMX8's PCIe2 ref clock (in SOM-iMX8)

GPIO EXPANDER



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C	04. HDMI, GPIO EXT, PCIe CLK	1.1
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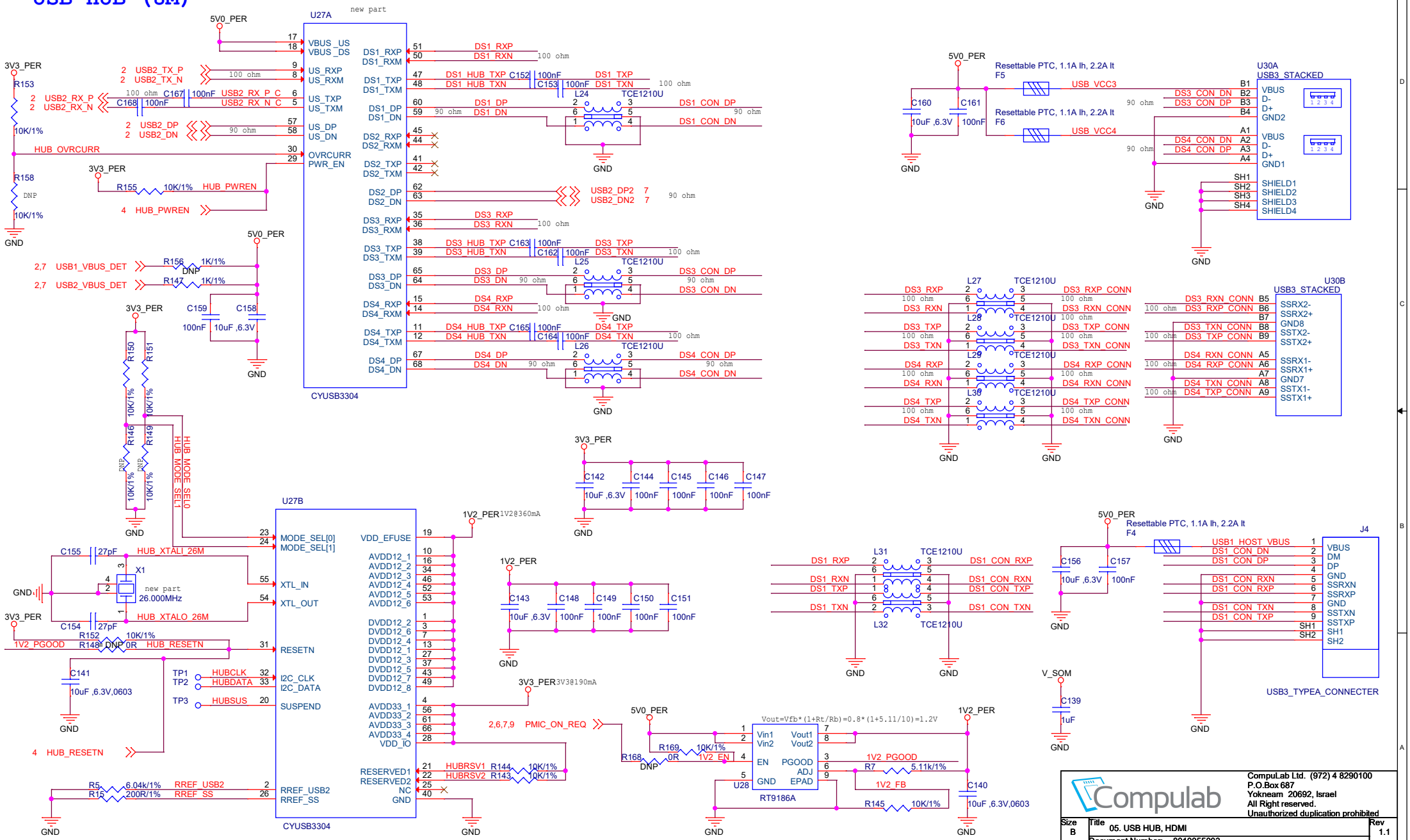
USB HUB (8M)


U27A
new part
CYUSB3304
U27B
CYUSB3304
U30A
USB3_STACKED
U30B
USB3_STACKED
J4
USB3_TYPEA_CONNECTER
TCE1210U
RT9186A
Resettable PTC, 1.1A Ih, 2.2A It
F4
F5
F6
new part
26.000MHz
Vout=Vfb*(1+Rt/Rb)=0.8*(1+5.11/10)=1.2V
3V3@190mA
1V2@360mA
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Size B
Title 05. USB HUB, HDMI
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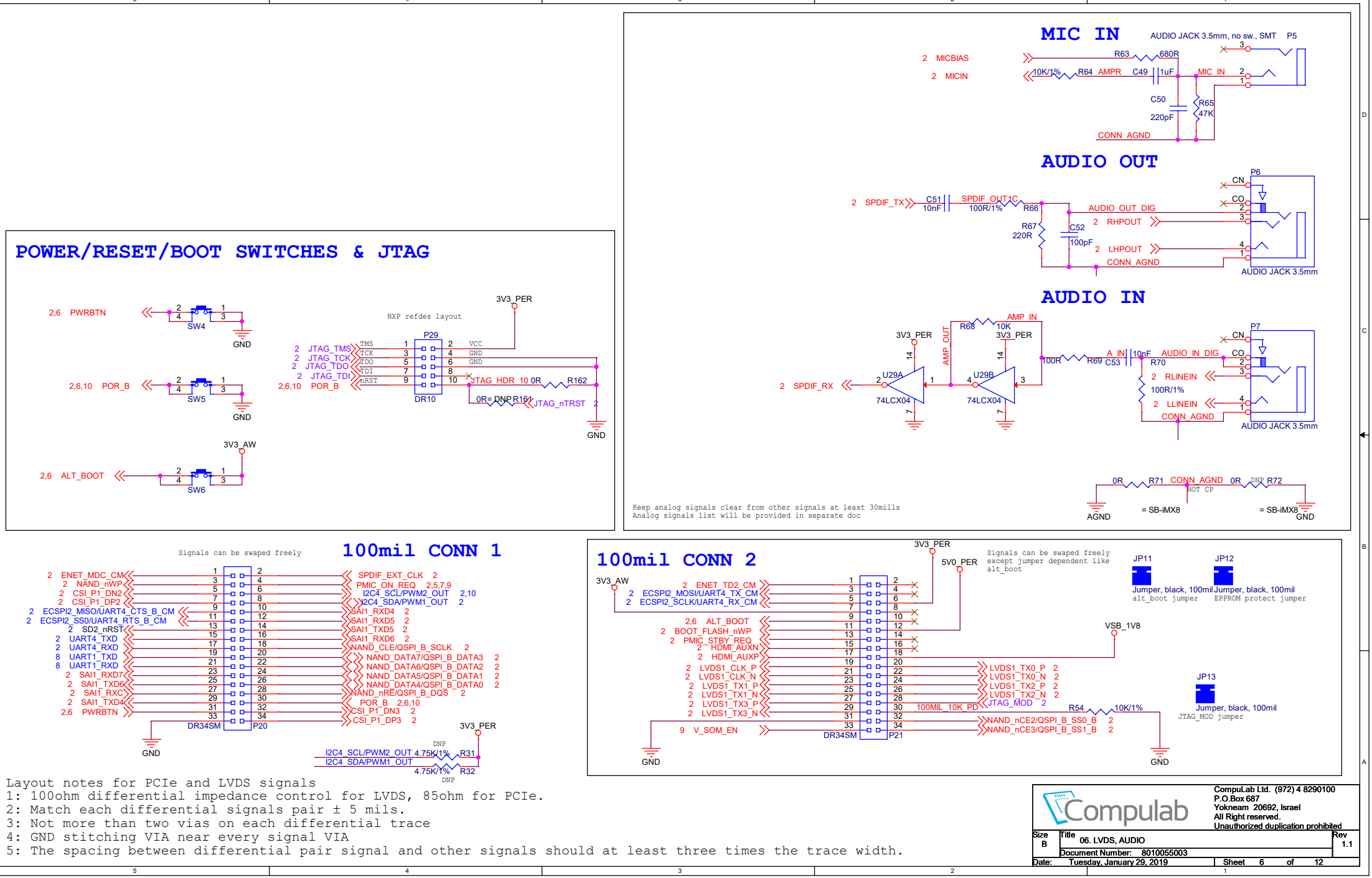
POWER/RESET/BOOT SWITCHES & JTAG
2,6 PWRBTN
SW4
GND
2,6,10 POR_B
SW5
GND
3V3_AW
2,6 ALT_BOOT
SW6
NXP refdes layout
3V3_PER
P29
2 JTAG_TMS
2 JTAG_TCK
2 JTAG_TDO
2 JTAG_TDI
2,6,10 POR_B
TMS
TCK
TDO
TDI
nRST
VCC
GND
JTAG_HDR_10 0R
R162
0R= DNP R161
JTAG_nTRST 2
DR10
MIC IN
AUDIO JACK 3.5mm, no sw., SMT P5
2 MICBIAS
2 MICIN
R63 680R
10K/1% R64 AMPR
C49 1uF
MIC_IN
C50 220pF
R65 47K
CONN_AGND
AUDIO OUT
P6
2 SPDIF_TX
C51 10nF
SPDIF_OUT1C
100R/1%
R66
AUDIO_OUT_DIG
2 RHPOUT
R67 220R
C52 100pF
2 LHPOUT
CONN_AGND
AUDIO JACK 3.5mm
AUDIO IN
AMP_IN
R68 10K
3V3_PER
AMP_OUT
2 SPDIF_RX
U29A
74LCX04
U29B
74LCX04
100R
R69 C53
A_IN
10nF
AUDIO_IN_DIG
P7
R70
2 RLINEIN
100R/1%
2 LLINEIN
CONN_AGND
AUDIO JACK 3.5mm
0R R71 CONN_AGND 0R DNP R72
NOT CP
AGND
= SB-iMX8
= SB-iMX8
GND
Keep analog signals clear from other signals at least 30mills
Analog signals list will be provided in separate doc
100mil CONN 1
Signals can be swaped freely
2 ENET_MDC_CM
2 NAND_nWP
2 CSI_P1_DN2
2 CSI_P1_DP2
2 ECSPI2_MISO/UART4_CTS_B_CM
2 ECSPI2_SS0/UART4_RTS_B_CM
2 SD2_nRST
2 UART4_TXD
2 UART4_RXD
8 UART1_TXD
8 UART1_RXD
2 SAI1_RXD7
2 SAI1_TXD6
2 SAI1_RXC
2 SAI1_TXD4
2,6 PWRBTN
SPDIF_EXT_CLK 2
PMIC_ON_REQ 2,5,7,9
I2C4_SCL/PWM2_OUT 2,10
I2C4_SDA/PWM1_OUT 2
SAI1_RXD4 2
SAI1_RXD5 2
SAI1_TXD5 2
SAI1_RXD6 2
NAND_CLE/QSPI_B_SCLK 2
NAND_DATA7/QSPI_B_DATA3 2
NAND_DATA6/QSPI_B_DATA2 2
NAND_DATA5/QSPI_B_DATA1 2
NAND_DATA4/QSPI_B_DATA0 2
NAND_nRE/QSPI_B_DQS 2
POR_B 2,6,10
CSI_P1_DN3 2
CSI_P1_DP3 2
DR34SM
P20
GND
3V3_PER
DNP
I2C4_SCL/PWM2_OUT 4.75K/1% R31
I2C4_SDA/PWM1_OUT
4.75K/1% R32
DNP
100mil CONN 2
3V3_PER
5V0_PER
3V3_AW
Signals can be swaped freely except jumper dependent like alt_boot
JP11
Jumper, black, 100mil
alt_boot jumper
JP12
Jumper, black, 100mil
EPPROM protect jumper
2 ENET_TD2_CM
2 ECSPI2_MOSI/UART4_TX_CM
2 ECSPI2_SCLK/UART4_RX_CM
2,6 ALT_BOOT
2 BOOT_FLASH_nWP
2 PMIC_STBY_REQ
2 HDMI_AUXN
2 HDMI_AUXP
2 LVDS1_CLK_P
2 LVDS1_CLK_N
2 LVDS1_TX1_P
2 LVDS1_TX1_N
2 LVDS1_TX3_P
2 LVDS1_TX3_N
9 V_SOM_EN
VSB_1V8
LVDS1_TX0_P 2
LVDS1_TX0_N 2
LVDS1_TX2_P 2
LVDS1_TX2_N 2
JTAG_MOD 2
100MIL_10K_PD
R54 10K/1%
NAND_nCE2/QSPI_B_SS0_B 2
NAND_nCE3/QSPI_B_SS1_B 2
JP13
Jumper, black, 100mil
JTAG_MOD jumper
DR34SM
P21
GND
GND
Layout notes for PCIe and LVDS signals
1: 100ohm differential impedance control for LVDS, 85ohm for PCIe.
2: Match each differential signals pair ± 5 mils.
3: Not more than two vias on each differential trace
4: GND stitching VIA near every signal VIA
5: The spacing between differential pair signal and other signals should at least three times the trace width.
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Title 06. LVDS, AUDIO
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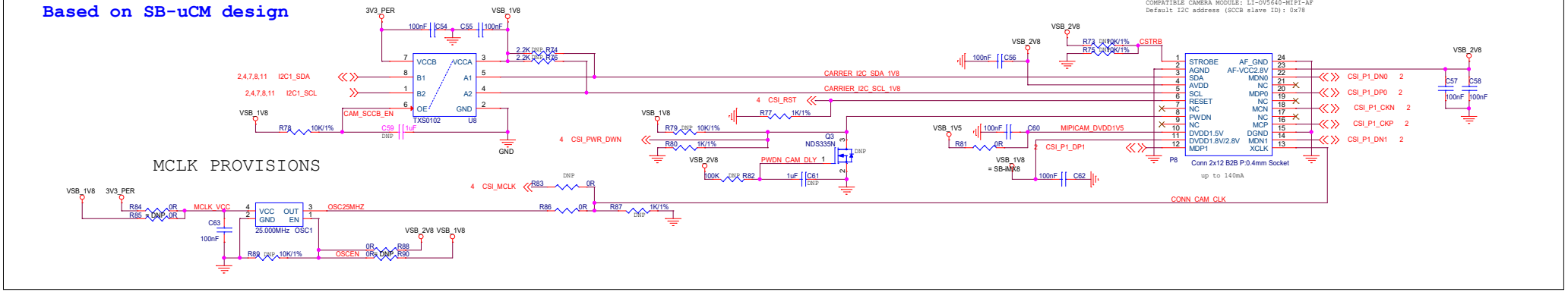
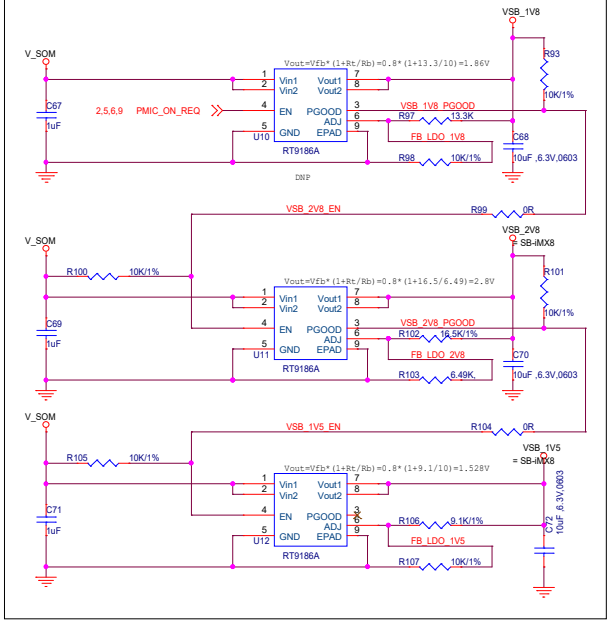
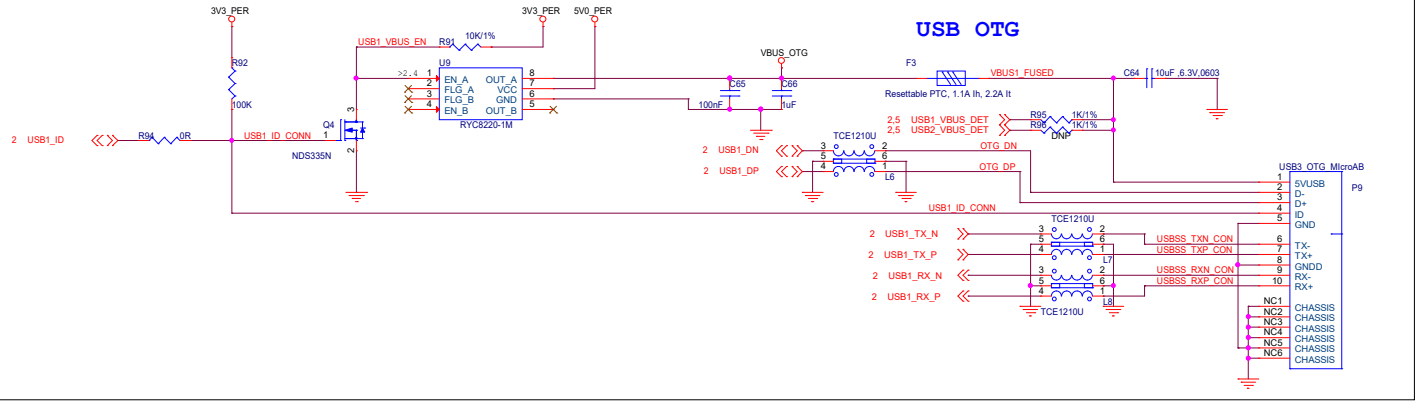
MIPI-CSI MODULE
Based on SB-uCM design



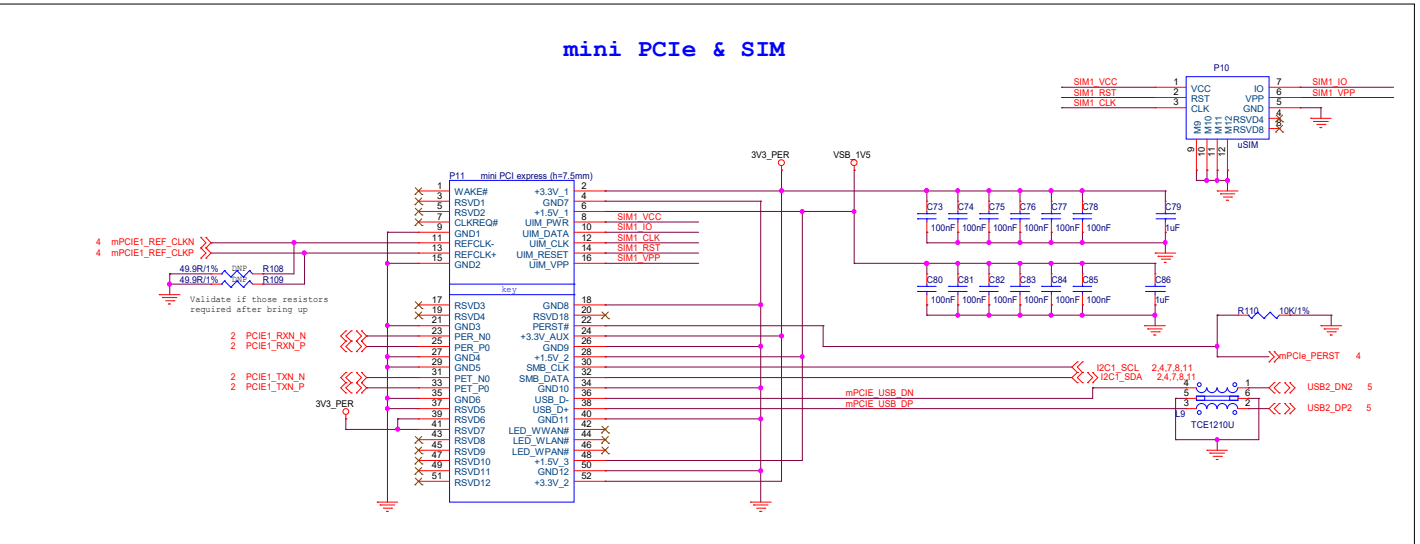
VSB_1V5, VSB_1V8 & VCC_2V8 CSI sources



USB OTG



mini PCIe & SIM



Layout notes
1: 100ohm differential impedance control for CSI, 85 for PCIe, 90 for USB.
2: Match each differential signals pair ± 5 mils and 40 mils for usb
3: Not more than two vias on each differential trace
4: GND stitching VIA near every signal VIA
5: The spacing between differential pair signal and other signals should at least three times the trace width.

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C	07. CSI, USB OTG, PCIe	1.1
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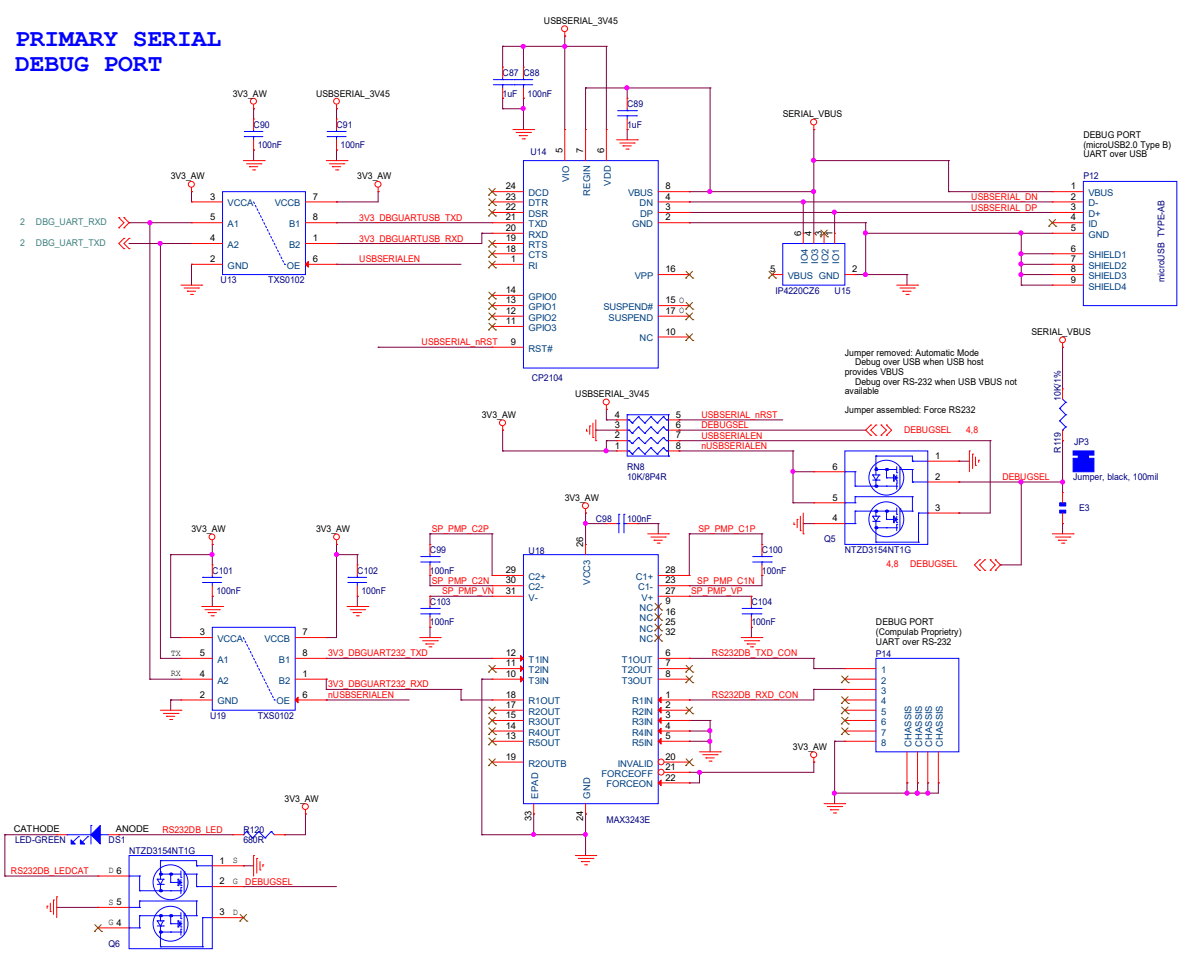

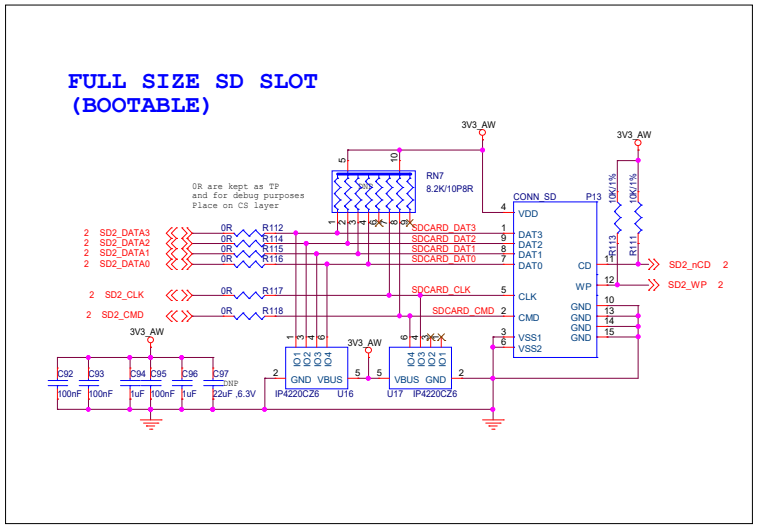

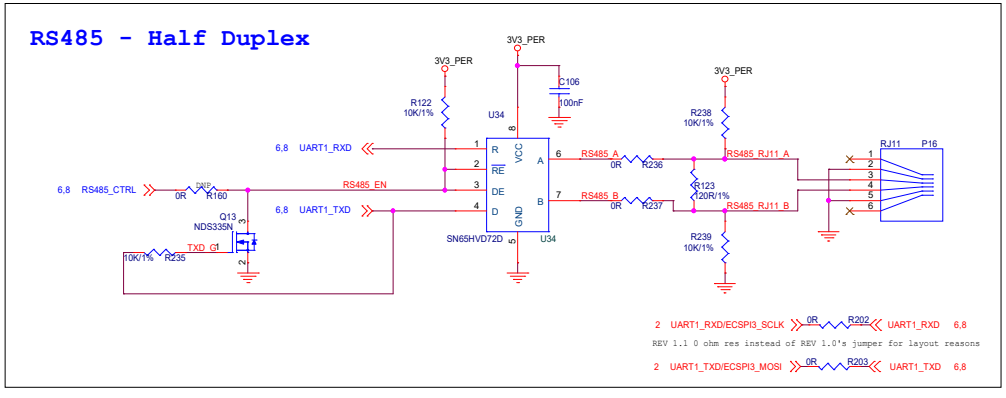

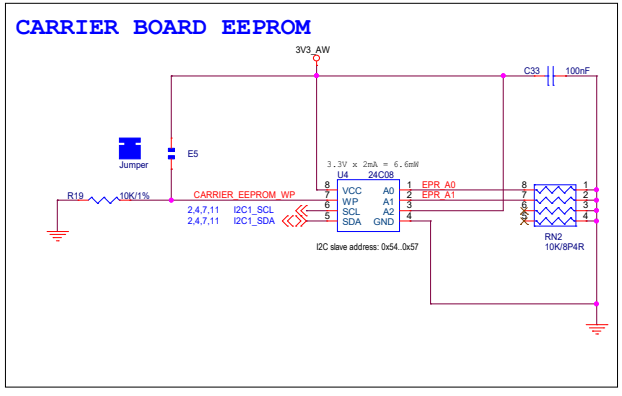

Layout notes
1: 120ohm differential impedance control for *485* signals.
2: Match each differential signals pair ± 5 mils.
3: Not more than two vias on each differential trace
4: GND stitching VIA near every signal VIA
5: The spacing between differential pair signal and other signals should at least three times the trace width.

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Size	Title	Rev
C	08. UART, RS232, RS485, EEPROM	1.1
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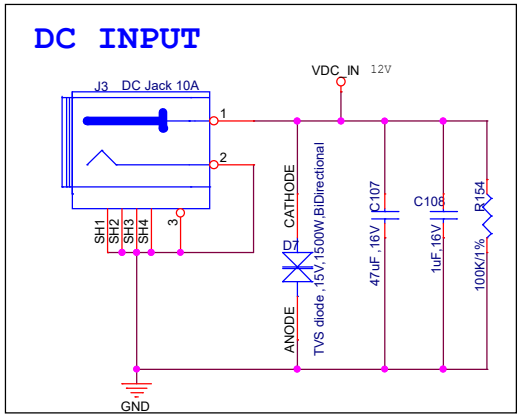

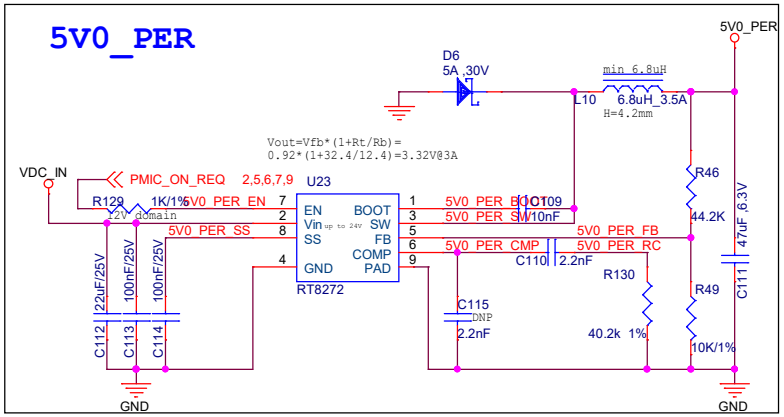

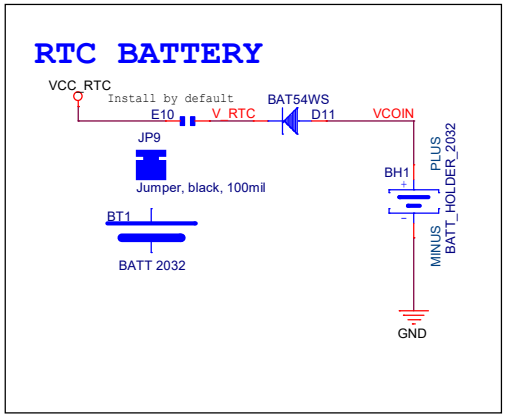

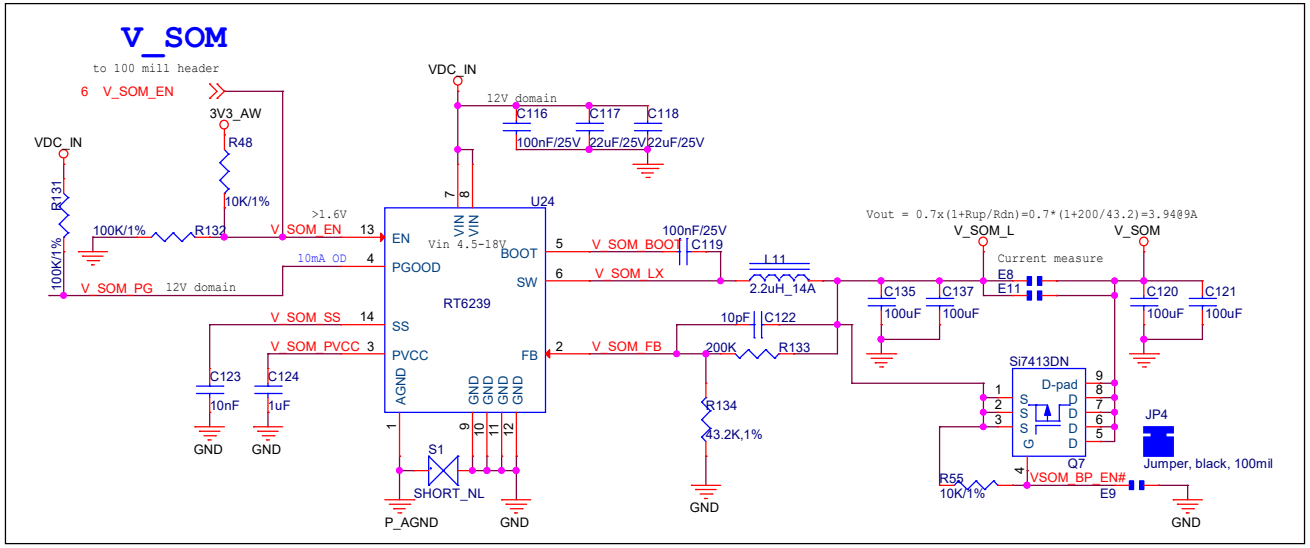

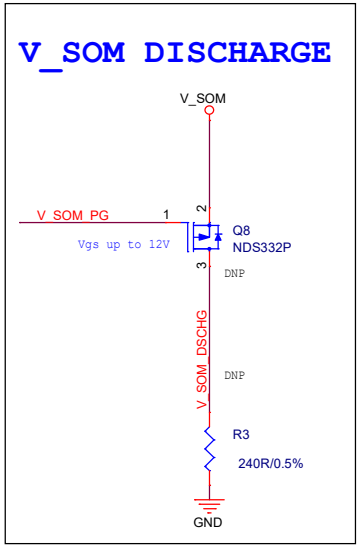

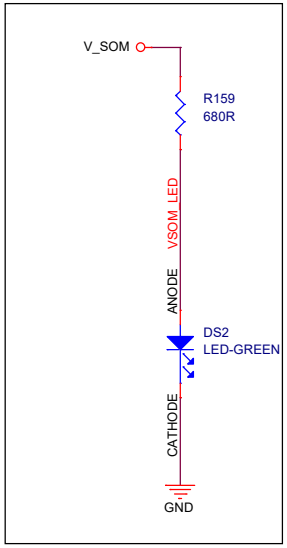

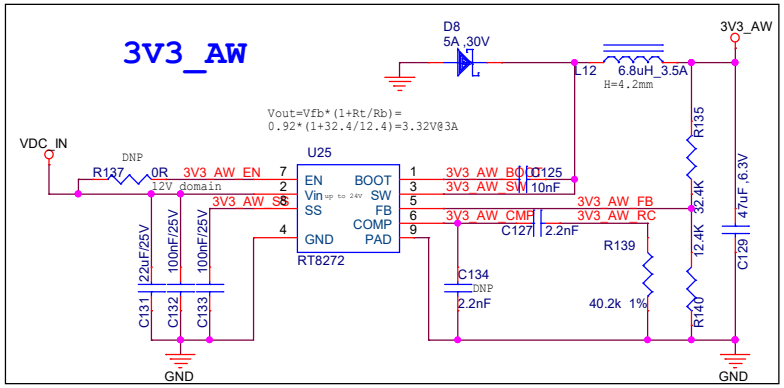

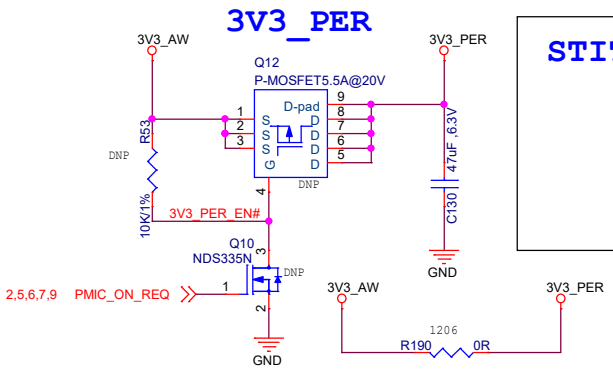

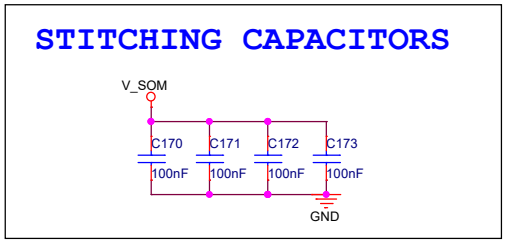

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B	09. Power	1.1
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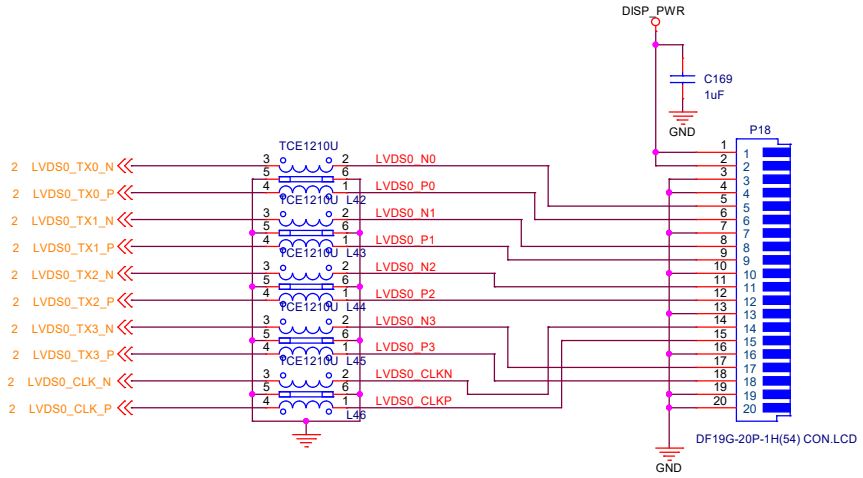
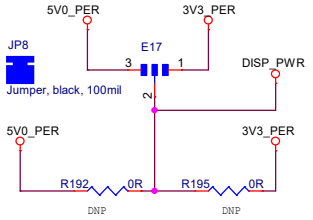
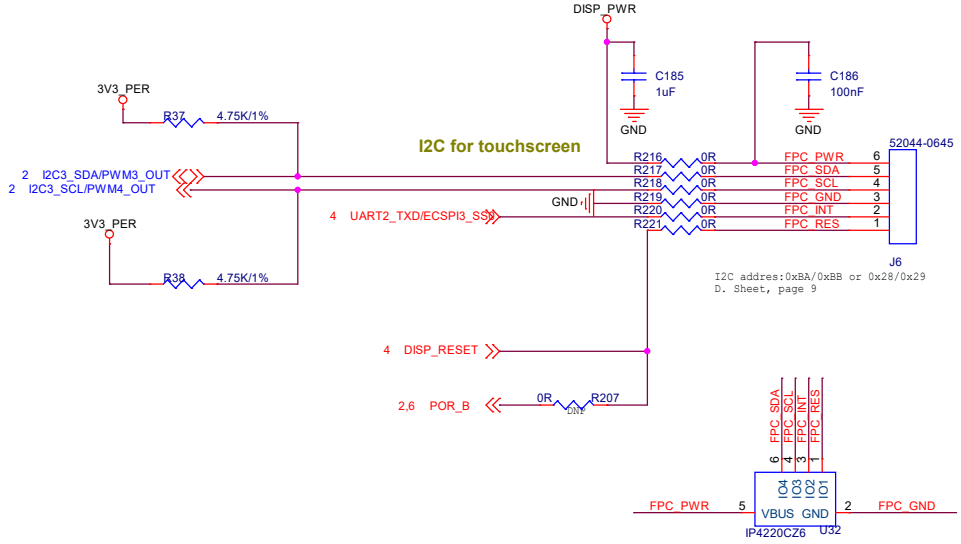
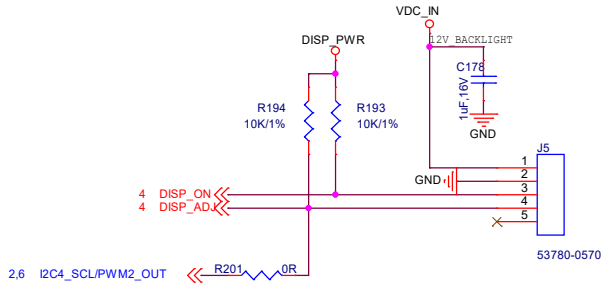
LVDS LCD









Size	Title	Rev
A3	10. LVDS LCD	1.1
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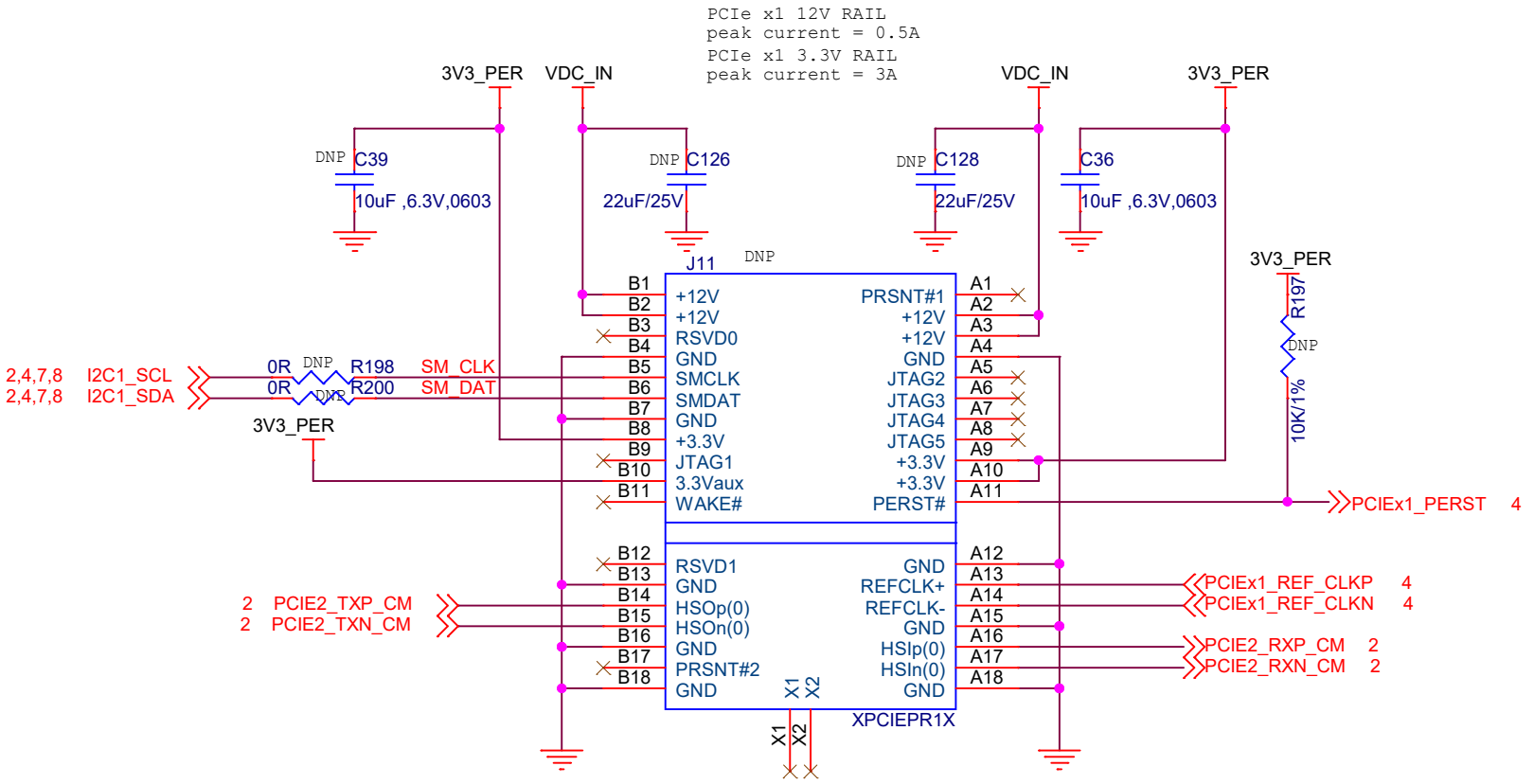
PCIe X1 SLOT



Title	11. PCIe x1	
Size A	Document Number 8010055003	Rev 1.1
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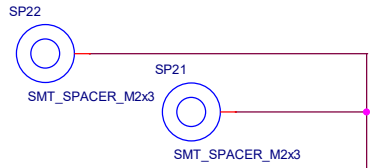
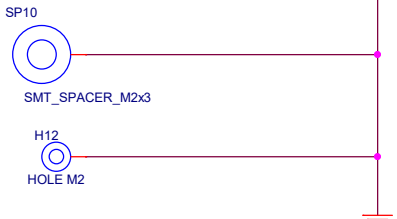
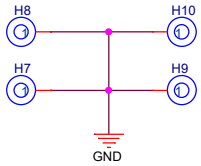
SODIMM SPACERS

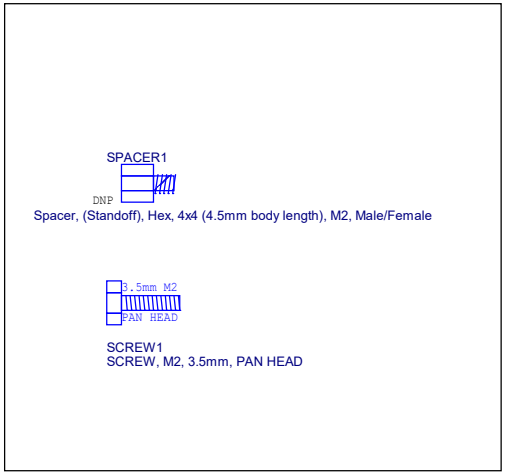


mPCIe SPACER



SB-iMX8 SPACERS





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Size	Title	Rev
B	12. Mechanics	1.1
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