CL-SOM-iMX7

Reference Guide

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Table 1 Revision Notes

Date	Description
Dec 2015	First release
Mar 2018	Fixed PCIE_REFCLKOUT pinout in section 4.13, table 22 Fixed PCIE_REFCLKOUT pinout in section 6.1, table 68 Fixed PCIE_REFCLKOUT pinout in attached spreadsheet Added RGMII signals description in section 4.6.2

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.com/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX7 Computer-on-Module.

1.2 CL-SOM-iMX7 Part Number Legend

Please refer to the CompuLab website 'Pricing and Ordering' section to decode the CL-SOM-iMX7 part number: http://www.compulab.co.il/products/computer-on-modules/cl-som-imx7-freescale-i-mx-7-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX7 Developer Resources	http://www.compulab.com/
i.MX7 Reference Manual	http://www.freescale.com/
i.MX7 Datasheet	http://www.freescale.com/

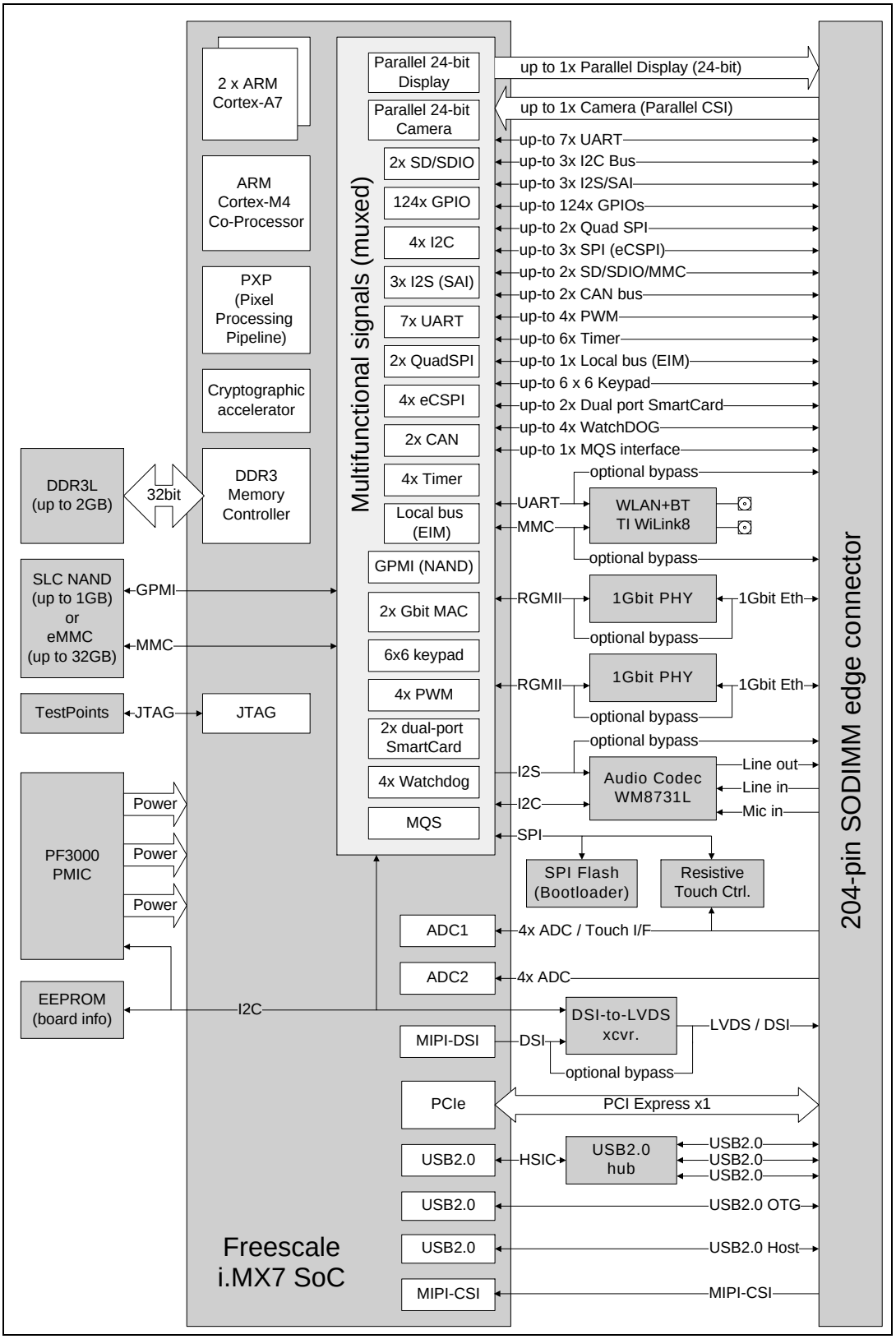
2 OVERVIEW

2.1 Highlights

- Freescale i.MX7 Dual / Single core Cortex-A7 SoC, up to 1GHz
- Up to 2GB DDR3L-1066 with 32-bit data bus.
- Up to 32GB on-board eMMC storage.
- Dual-band 802.11a/b/g/n WiFi and Bluetooth 4.1 BLE
- PCIe, 2x GbE, 5x USB2, 7x UART, 2x CAN, 124x GPIO
- LVDS, MIPI-DSI, Parallel RGB, up to 1920 x 1080
- ARM Cortex-M4, 200Mhz Co-Processor dedicated for real-time tasks

2.2 Block Diagram

Figure 1 CL-SOM-iMX7 Block Diagram



2.3 CL-SOM-iMX7 Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	Freescale i.MX 7Solo ARM Cortex-A7, 800MHz NEON SIMD and VFPv4	C800
	Freescale i.MX 7Dual ARM Cortex-A7, 1GHz NEON SIMD and VFPv4	C1000D
Real-Time Coprocessor	ARM Cortex-M4, 200Mhz	+
Memory and Storage		
RAM	256MB – 2GB, DDR3L-1066	D
Storage	SLC NAND flash, 128MB - 1GB	N
	eMMC flash, 4GB - 32GB	
Display and Camera		
Display	Parallel 24-bit display interface, up to 1920 x 1080 @60Hz	+
	LVDS, up to 1400 x 1050 @60Hz	L
	MIPI-DSI, 2 data lanes, up to 1400 x 1050 @60Hz	~~L~~
Touchscreen	On-board 4-wire resistive touch-screen controller	I
	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	Parallel camera interface, up to 24-bit	+
	MIPI-CSI, 2 data lanes	+
Network		
Gigabit Ethernet	1x 10/100/1000Mbps Ethernet port (MAC+PHY)	E1
	2x 10/100/1000Mbps Ethernet ports (MAC+PHY)	E2 and C1000D
WiFi	802.11b/g/n WiFi interface, Texas Instruments WiLink 8 WL1801 chipset	W
	Dual-band 2x2 802.11a/b/g/n WiFi interface, Texas Iinstruments WiLink 8 WL1837chipset	WAB
Bluetooth	Bluetooth 4.1 BLE	WAB
Audio		
Analog Audio	Audio codec with analog stereo output, stereo input and electret microphone support	A
Digital Audio	I2S compliant digital audio interface	+
	MQS audio interface	+
I/O		
PCI Express	PCIe x1 Gen. 2.1	C1000D
Local Bus	External local bus interface, up to 32-bit	+
USB	1x USB2.0 OTG port	+
	Additional 1x USB2.0 host ports	C1000D
	Additional 3x USB2.0 host ports	UH
Serial Ports (UARTs)	Up to 7x UART ports, up to 4 Mbps	+
CAN bus	Up to 2x CAN bus, 3.3V levels	+
MMC/SD/SDIO	Up to 2x MMC/SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 124x GPIO (multifunctional signals shared with other functions)	+
Timers	Up to 6x Timer outputs	+
ADC	4x general-purpose ADC channels	+
	Additional 4x general-purpose ADC channels	~~I~~
System Logic		
RTC	Real time clock, powered by external battery	+

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	3.5V to 4.5V / Li-Ion battery
Digital I/O voltage	3.3V
Active power consumption	0.5 - 3 W, depending on configuration and system load
Mechanical Specifications	
Dimensions	42 x 68 x 5 mm
Weight	14 gram
Connectors	204-pin SO-DIMM edge connector
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

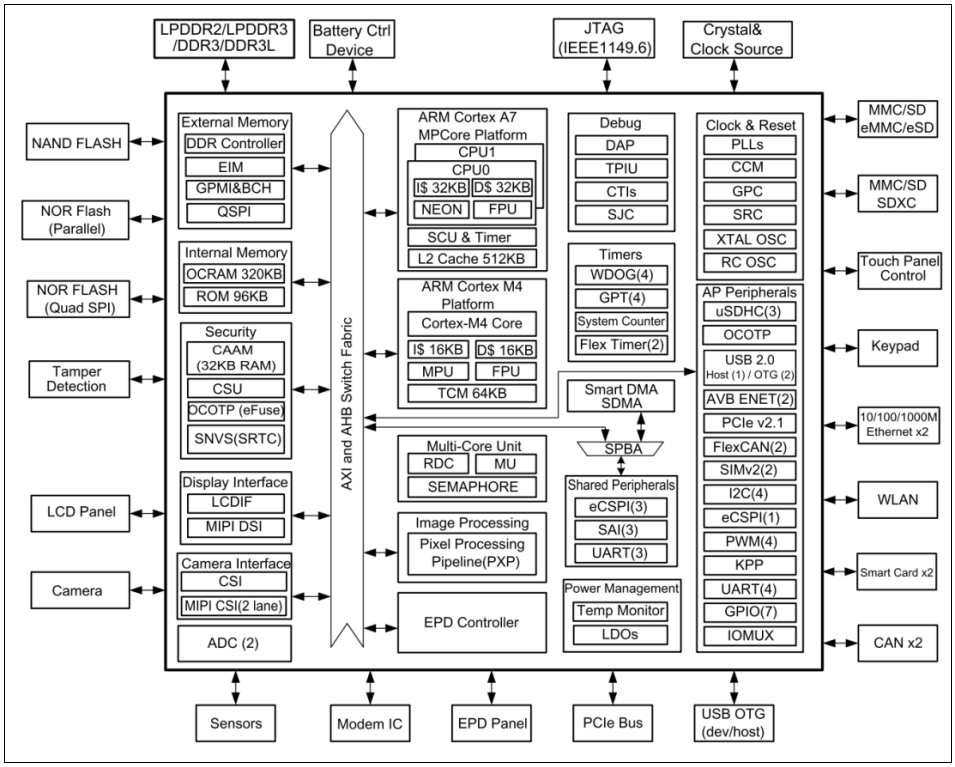
3 CORE SYSTEM COMPONENTS

3.1 i.MX7 SoC

The i.MX7 family of processors combines an implementation of two ARM® Cortex®-A7 cores intended for high level O/S, with an ARM® Cortex®-M4 core dedicated for real-time tasks. The i.MX7 has the following main features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology), each core includes:
  - Up to 1GHz operation frequency
  - 32 KByte L1 Instruction Cache, 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - NEON MPE coprocessor
- One ARM Cortex-M4 Core dedicated for real-time tasks, with the following features:
  - 200MHz operation frequency
  - MPU, FPU
  - 16 KByte instruction cache, 16 KByte data cache
  - 64 KByte TCM (tightly-coupled memory)
- Cryptographic acceleration and assurance module, containing cryptographic and hash engines supporting DPA (differential power analysis) protection, 32 KB secure RAM, and true and pseudo random number generator (NIST certified)
- PXP—PiXel processing pipeline for imagine resize, rotation, overlay and CSC. Offloading key pixel processing operations are required to support the display applications

Figure 2 i.MX 7Dual Block Diagram



3.2 Memory

3.2.1 DRAM

CL-SOM-iMX7 is equipped with up to 2GB of onboard DDR3L memory. The DDR3L data bus is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

NOTE: CL-SOM-iMX7 boards with 256MB of DRAM (D256 option) feature a 16-bit wide DDR3 data bus.

3.2.2 Bootloader Storage

The CL-SOM-iMX7 is assembled with 2MBytes of SPI NOR flash. The SPI NOR flash is the primary non-volatile memory device of CL-SOM-iMX7, used for the boot-loader and configuration blocks storage.

3.2.3 General Purpose Storage

CL-SOM-iMX7 is available with optional secondary on-board storage designed to store the operating system and user data. One of the following on-board non-volatile memory devices can be used as the secondary on-board storage.

- On-board eMMC flash (up to 32GBytes).
- On-board raw SLC NAND Flash (up to 1GBytes).

The secondary storage device is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

CL-SOM-iMX7 implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of CL-SOM-iMX7. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Many of the CL-SOM-iMX7 carrier board interface pins are multifunctional. Up-to 9 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5 of this document.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the CL-SOM-iMX7 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-iMX7 Configuration options, certain carrier board interface pins are physically disconnected (floating) from the carrier board interface connector on-board CL-SOM-iMX7. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Signal Input
- **"AO"** – Analog Signal Output
- **"AIO"** – Analog Signal Input/Output
- **"APO"** – Analog Power Output
- **"API"** – Analog Power Input
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"IOD"** – Open Drain Signal (not pulled up on-board CL-SOM-iMX7 unless otherwise noted).
- **"PI"** – Power Input
- **"PO"** – Power Output
- "**SPU" –** Software controlled pull up to 3.3V
- "**SPD" –** Software controlled pull down to GND

- "**PU18**" – Always pulled up to 1.8V on-board CL-SOM-iMX7, (typ. 5KΩ-15KΩ).
- "**PU33**" – Always pulled up to 3.3V on-board CL-SOM-iMX7, (typ. 5KΩ-15KΩ).
- "**PUSUPPLY**" – Always pulled up to 3.3V - 4.5V on-board CL-SOM-iMX7, (typ. 5KΩ-15KΩ).
- "**PD**" **-** Always pulled down on-board CL-SOM-iMX7, (typ. 5KΩ-15KΩ).

4.1 Parallel Display interface

CL-SOM-iMX7 Parallel display interface is derived from the i.MX7 integrated Enhanced LCD interface (eLCDIF) designed to drive a wide range of display devices varying in size and capabilities. eLCDIF supports the following main features:

- Support for parallel LCD displays (up to 24-bit) with resolutions up to 1920x1080 at 60Hz.
- Support for both synchronous and asynchronous "smart" displays.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode, including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the Parallel display interface signals

Table 5 Parallel display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LCDIF.BUSY	40*	I	Busy Signal	not "E2"
LCDIF.BUSY	124*	I	Busy Signal	Always
LCDIF.CLK	5*	O	Clock Signal	Always
LCDIF.CLK	42*	O	Clock Signal	not "E2"
LCDIF.CLK	98*	O	Clock Signal	Always
LCDIF.CS	136*	O	Chip Select	Always
LCDIF.CS	194*	O	Chip Select	Always
LCDIF.DATA[0]	98*	IO	Data Signal	Always
LCDIF.DATA[0]	106*^	IO; PD	Data Signal	Always
LCDIF.DATA[0]	126*	IO	Data Signal	Always
LCDIF.DATA[1]	104*	IO	Data Signal	Always
LCDIF.DATA[1]	108*^	IO; PD	Data Signal	Always
LCDIF.DATA[1]	130*	IO	Data Signal	Always
LCDIF.DATA[10]	34*	IO	Data Signal	not "E2"
LCDIF.DATA[10]	54*^	IO; PD	Data Signal	Always
LCDIF.DATA[10]	128*	IO	Data Signal	Always
LCDIF.DATA[11]	56*^	IO; PD	Data Signal	Always
LCDIF.DATA[11]	75*	IO	Data Signal	Always
LCDIF.DATA[11]	130*	IO	Data Signal	Always
LCDIF.DATA[12]	79*^	IO; PD/PU33	Data Signal. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[12]	134*	IO	Data Signal	Always
LCDIF.DATA[12]	152*	IO	Data Signal	Always
LCDIF.DATA[13]	77*^	IO; PU33/PD	Data Signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[13]	83*	IO	Data Signal	Always
LCDIF.DATA[13]	136*	IO	Data Signal	Always
LCDIF.DATA[14]	85*	IO	Data Signal	Always
LCDIF.DATA[14]	91*^	IO; PU33/PD	Data Signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
LCDIF.DATA[14]	138*	IO	Data Signal	Always
LCDIF.DATA[15]	89*^	IO; PD	Data Signal	Always
LCDIF.DATA[15]	107*	IO	Data Signal	Always
LCDIF.DATA[15]	140*	IO	Data Signal	Always
LCDIF.DATA[16]	38*	IO	Data Signal	not "E2"
LCDIF.DATA[16]	50*	IO	Data Signal	not "E2"
LCDIF.DATA[16]	94*^	IO; PD	Data Signal	Always
LCDIF.DATA[17]	40*	IO	Data Signal	not "E2"
LCDIF.DATA[17]	48*	IO	Data Signal	not "E2"
LCDIF.DATA[17]	92*^	IO; PU33	Data Signal	Always
LCDIF.DATA[18]	34*	IO	Data Signal	not "E2"
LCDIF.DATA[18]	36*	IO	Data Signal	not "E2"
LCDIF.DATA[18]	142*^	IO; PD	Data Signal	Always
LCDIF.DATA[19]	25*	IO	Data Signal	not "E2"
LCDIF.DATA[19]	44*	IO	Data Signal	not "E2"

Signal Name	Pin #	Type	Description	Availability
LCDIF.DATA[19]	144*^	IO; PD	Data Signal	Always
LCDIF.DATA[2]	30*	IO	Data Signal	not "E2"
LCDIF.DATA[2]	102*	IO	Data Signal	Always
LCDIF.DATA[2]	110*^	IO; PD	Data Signal	Always
LCDIF.DATA[20]	31*	IO	Data Signal	not "E2"
LCDIF.DATA[20]	42*	IO	Data Signal	not "E2"
LCDIF.DATA[20]	146*	IO	Data Signal	Always
LCDIF.DATA[21]	32*	IO	Data Signal	not "E2"
LCDIF.DATA[21]	134*	IO	Data Signal	Always
LCDIF.DATA[21]	148*	IO	Data Signal	Always
LCDIF.DATA[22]	30*	IO	Data Signal	not "E2"
LCDIF.DATA[22]	74*	IO	Data Signal	Always
LCDIF.DATA[22]	138*	IO	Data Signal	Always
LCDIF.DATA[23]	38*	IO	Data Signal	not "E2"
LCDIF.DATA[23]	48*	IO	Data Signal	not "E2"
LCDIF.DATA[23]	76*	IO	Data Signal	Always
LCDIF.DATA[3]	32*	IO	Data Signal	not "E2"
LCDIF.DATA[3]	100*	IO	Data Signal	Always
LCDIF.DATA[3]	112*^	IO; PD	Data Signal	Always
LCDIF.DATA[4]	31*	IO	Data Signal	not "E2"
LCDIF.DATA[4]	113*^	IO; PD	Data Signal	Always
LCDIF.DATA[4]	116*	IO	Data Signal	Always
LCDIF.DATA[5]	44*	IO	Data Signal	not "E2"
LCDIF.DATA[5]	115*^	IO; PD	Data Signal	Always
LCDIF.DATA[5]	118*	IO	Data Signal	Always
LCDIF.DATA[6]	60*	IO	Data Signal	Always
LCDIF.DATA[6]	95*^	IO; PD	Data Signal	Always
LCDIF.DATA[6]	120*	IO	Data Signal	Always
LCDIF.DATA[7]	122*	IO	Data Signal	Always
LCDIF.DATA[7]	154*^	IO; PD	Data Signal	Always
LCDIF.DATA[7]	194*	IO	Data Signal	Always
LCDIF.DATA[8]	50*	IO	Data Signal	not "E2"
LCDIF.DATA[8]	124*	IO	Data Signal	Always
LCDIF.DATA[8]	161*^	IO; PD	Data Signal	Always
LCDIF.DATA[9]	126*	IO	Data Signal	Always
LCDIF.DATA[9]	128*	IO	Data Signal	Always
LCDIF.DATA[9]	163*^	IO; PD	Data Signal	Always
LCDIF.ENABLE	3*	IO	Enable Signal	Always
LCDIF.ENABLE	60*	IO	Enable Signal	Always
LCDIF.ENABLE	104*	IO	Enable Signal	Always
LCDIF.HSYNC	7*	I	HSYNC enable	Always
LCDIF.HSYNC	75*	I	HSYNC enable	Always
LCDIF.HSYNC	100*	I	HSYNC enable	Always
LCDIF.RD_E	25*	IO	RD_E Signal	not "E2"
LCDIF.RESET	99*	IO	LCD reset Signal	Always
LCDIF.RESET	109*	IO	LCD reset Signal	Always
LCDIF.VSYNC	9*	I	VSYNC Signal	Always
LCDIF.VSYNC	102*	I	VSYNC Signal	Always
LCDIF.VSYNC	152*	I	VSYNC Signal	Always
LCDIF.WR_RWN	36*	IO	WR Signal	not "E2"
LCDIF.WR_RWN	140*	IO	WR Signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.2 MIPI-DSI Interface

The MIPI-DSI interface available with CL-SOM-iMX7 is based on the two-lane MIPI display interface available with the i.MX7 SoC. The following main features are supported:

- Up-to two data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.

- Complies to MIPI DSI Standard Specification V1.01r11.
- Maximum resolution ranges up to SXGA+(1400 x 1050 @ 60 Hz, 24 bpp).
- Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24bpp

NOTE: CL-SOM-iMX7 MIPI-DSI interface is available only without the 'L' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_DSI_CLK_N	47	AO	Negative part of MIPI-DSI clock diff-pair	not "L"
MIPI_DSI_CLK_P	45	AO	Positive part of MIPI-DSI clock diff-pair	not "L"
MIPI_DSI_D0_N	35	AO	Negative part of MIPI-DSI data diff-pair 0	not "L"
MIPI_DSI_D0_P	33	AO	Positive part of MIPI-DSI data diff-pair 0	not "L"
MIPI_DSI_D1_N	41	AO	Negative part of MIPI-DSI data diff-pair 1	not "L"
MIPI_DSI_D1_P	39	AO	Positive part of MIPI-DSI data diff-pair 1	not "L"

4.3 LVDS Display interface

The LVDS display interface is implemented onboard CL-SOM-iMX7 by converting the i.MX7 MIPI-DSI interface into LVDS interface using the Texas Instruments SN65DSI83 DSI to LVDS transceiver. Texas Instruments SN65DSI83 supports following main features:

- LVDS Output Clock Range of 25 MHz to 154MHz.
- ESD Rating ±2 kV (HBM).
- Suitable for 60 fps 1366 x 768 / 1280 x 800 at 18 bpp and 24 bpp.
- Capable of supporting the full resolution of the i.MX7 MIPI-DSI interface with reduced blanking.

NOTE: CL-SOM-iMX7 LVDS display interface is available only with the 'L' ordering option.

Please refer to the Texas Instruments SN65DSI83 datasheet for additional details. The table below summarizes the LVDS display interface signals

Table 7 LVDS display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS_CLKN	35	AO	Negative part of differential clock	"L"
LVDS_CLKP	33	AO	Positive part of differential clock	"L"
LVDS_TX0N	41	AO	Negative part of differential data 0	"L"
LVDS_TX0P	39	AO	Positive part of differential data 0	"L"
LVDS_TX1N	47	AO	Negative part of differential data 1	"L"
LVDS_TX1P	45	AO	Positive part of differential data 1	"L"
LVDS_TX2N	53	AO	Negative part of differential data 2	"L"
LVDS_TX2P	51	AO	Positive part of differential data 2	"L"
LVDS_TX3N	59	AO	Negative part of differential data 3	"L"
LVDS_TX3P	57	AO	Positive part of differential data 3	"L"

4.4 Parallel Camera Interface

The CL-SOM-iMX7 parallel camera interface is derived from the i.MX7 integrated CSI IP. The CSI block enables direct connection between CL-SOM-iMX7 and external CMOS image sensors. The capabilities of CSI include:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Embedded DMA controllers to transfer data from receive FIFO or statistic FIFO through AHB bus.
- Up to 133 MHz operation frequency.
- Configurable master clock frequency output to sensor.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the Parallel camera interface signals

Table 8 Parallel camera Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI1.DATA[0]	92*^	I; PU33	CMOS Sensor data	Always
CSI1.DATA[1]	94*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[10]	76*	I	CMOS Sensor data	Always
CSI1.DATA[11]	74*	I	CMOS Sensor data	Always
CSI1.DATA[12]	148*	I	CMOS Sensor data	Always
CSI1.DATA[13]	146*	I	CMOS Sensor data	Always
CSI1.DATA[14]	144*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[15]	142*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[16]	5*	I	CMOS Sensor data	Always
CSI1.DATA[17]	3*	I	CMOS Sensor data	Always
CSI1.DATA[18]	7*	I	CMOS Sensor data	Always
CSI1.DATA[19]	9*	I	CMOS Sensor data	Always
CSI1.DATA[2]	89*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[20]	106*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[21]	108*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[22]	110*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[23]	112*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[3]	91*^	I; PU33/PD	CMOS Sensor data. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[4]	77*^	I; PU33/PD	CMOS Sensor data. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[5]	79*^	I; PD/PU33	CMOS Sensor data. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
CSI1.DATA[6]	56*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[6]	83*	I	CMOS Sensor data	Always
CSI1.DATA[7]	54*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[7]	85*	I	CMOS Sensor data	Always
CSI1.DATA[8]	107*	I	CMOS Sensor data	Always
CSI1.DATA[8]	163*^	I; PD	CMOS Sensor data	Always
CSI1.DATA[9]	109*	I	CMOS Sensor data	Always
CSI1.DATA[9]	161*^	I; PD	CMOS Sensor data	Always
CSI1.FIELD	99*	I	CSI Field Signal	Always
CSI1.HSYNC	15*	I	Horizontal Sync (Blank Signal)	Always
CSI1.HSYNC	115*^	I; PD	Horizontal Sync (Blank Signal)	Always
CSI1.MCLK	11*	O	CMOS Sensor Master Clock	Always
CSI1.MCLK	154*^	O; PD	CMOS Sensor Master Clock	Always
CSI1.PIXCLK	13*	I	Pixel Clock	Always
CSI1.PIXCLK	95*^	I; PD	Pixel Clock	Always
CSI1.VSYNC	17*	I	Vertical Sync (Start Of Frame)	Always
CSI1.VSYNC	113*^	I; PD	Vertical Sync (Start Of Frame)	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.5 MIPI-CSI Camera Interface

The MIPI-CSI interface available with CL-SOM-iMX7 is derived from the two-lane MIPI CSI2 host controller (MIPI_CSI2) integrated into the i.MX7 SoC. The CSI2 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between CL-SOM-iMX7 and a MIPI CSI-2 compliant camera sensor. The following main features are supported:

- Up-to two data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Compliant to MIPI CSI2 Standard Specification V1.01r06.
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits.
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 9 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_CSI_CLK_N	184	AI	Negative part of MIPI-CSI clock diff-pair 1	Always
MIPI_CSI_CLK_P	182	AI	Positive part of MIPI-CSI clock diff-pair	Always
MIPI_CSI_D0_N	23	AI	Negative part of MIPI-CSI data diff-pair 0	Always
MIPI_CSI_D0_P	21	AI	Positive part of MIPI-CSI data diff-pair 0	Always
MIPI_CSI_D1_N	29	AI	Negative part of MIPI-CSI data diff-pair 1	Always
MIPI_CSI_D1_P	27	AI	Positive part of MIPI-CSI data diff-pair 1	Always

4.6 Ethernet

4.6.1 Gbit Ethernet Interfaces

CL-SOM-iMX7 incorporates two full-featured 10/100/1000 ethernet ports implemented with the two MACs built into the i.MX7 SoC, coupled with two AR8033 RGMII Ethernet PHYs from Atheros. Both ethernet interfaces support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

NOTE: CL-SOM-iMX7 primary Ethernet port is available only with the 'E2' or 'E1' ordering options.

NOTE: CL-SOM-iMX7 secondary Ethernet port is available only with both "C1000D" and 'E2' ordering options.

Please refer to the i.MX7 and the Atheros AR8033 respective reference manuals for additional details. The tables below summarize the ethernet interface signals.

Table 10 Ethernet1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH1_LED_ACT	4*^	IO; PD	Active High, activity LED driver. 2.5V signal	"E1" or "E2"
ETH1_LED1_SPD	16*^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal	"E1" or "E2"
ETH1_LED3	22	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	"E1" or "E2"
ETH1_MDI0N	6	AIO	Negative part of 100ohm diff-pair 0	"E1" or "E2"
ETH1_MDI0P	8	AIO	Positive part of 100ohm diff-pair 0	"E1" or "E2"
ETH1_MDI1N	12	AIO	Negative part of 100ohm diff-pair 1	"E1" or "E2"
ETH1_MDI1P	14	AIO	Positive part of 100ohm diff-pair 1	"E1" or "E2"
ETH1_MDI2N	18	AIO	Negative part of 100ohm diff-pair 2	"E1" or "E2"
ETH1_MDI2P	20	AIO	Positive part of 100ohm diff-pair 2	"E1" or "E2"
ETH1_MDI3N	24	AIO	Negative part of 100ohm diff-pair 3	"E1" or "E2"
ETH1_MDI3P	26	AIO	Positive part of 100ohm diff-pair 3	"E1" or "E2"

Table 11 Ethernet2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH2_LED_LINK10_100	34	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	"C1000D" and "E2"
ETH2_LINK-LED_1000	40*^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal	"C1000D" and "E2"
ETH2_LINK-LED_ACT	25*^	IO; PD	Active High, activity LED driver. 2.5V signal	"C1000D" and "E2"
ETH2_MDI0N	30	AIO	Negative part of 100ohm diff-pair 0	"C1000D" and "E2"
ETH2_MDI0P	32	AIO	Positive part of 100ohm diff-pair 0	"C1000D" and "E2"
ETH2_MDI1N	36	AIO	Negative part of 100ohm diff-pair 1	"C1000D" and "E2"
ETH2_MDI1P	38	AIO	Positive part of 100ohm diff-pair 1	"C1000D" and "E2"
ETH2_MDI2N	42	AIO	Negative part of 100ohm diff-pair 2	"C1000D" and "E2"
ETH2_MDI2P	44	AIO	Positive part of 100ohm diff-pair 2	"C1000D" and "E2"
ETH2_MDI3N	48	AIO	Negative part of 100ohm diff-pair 3	"C1000D" and "E2"
ETH2_MDI3P	50	AIO	Positive part of 100ohm diff-pair 3	"C1000D" and "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.6.2 RGMII Interfaces

CL-SOM-iMX7 modules assembled without “E1” or “E2” configuration options expose the i.MX7 SoC RGMII signals on the interface connector.

NOTE: CL-SOM-iMX7 primary RGMII interface is available only without ‘E2’ and ‘E1’ ordering options.

NOTE: CL-SOM-iMX7 secondary RGMII interface is available only with “C1000D” ordering option and without ‘E2’ ordering option.

The tables below summarize the RGMII interface signals.

Table 12 RGMII1 Interface Signals

Signal Name	Pin #	Availability
ENET1_RD1	4*^	not "E1" and not "E2"
ENET1_TD0	16*^	not "E1" and not "E2"
ENET1_RD0	22	not "E1" and not "E2"
ENET1_TX_CTL	6	not "E1" and not "E2"
ENET1_TXC	8	not "E1" and not "E2"
ENET1_TD1	12	not "E1" and not "E2"
ENET1_TD3	14	not "E1" and not "E2"
ENET1_RD2	18	not "E1" and not "E2"
ENET1_RD3	20	not "E1" and not "E2"
ENET1_RXC	24	not "E1" and not "E2"
ENET1_RX_CTL	26	not "E1" and not "E2"
ENET1_TD2	62	not "E1" and not "E2"

Table 13 RGMII2 Interface Signals

Signal Name	Pin #	Availability
ENET2_RD3	34	"C1000D" and not "E2"
ENET2_TXC	40*^	"C1000D" and not "E2"
ENET2_TX_CTL	25*^	"C1000D" and not "E2"
ENET2_TD1	30	"C1000D" and not "E2"
ENET2_RXC	31	"C1000D" and not "E2"
ENET2_TD0	32	"C1000D" and not "E2"
ENET2_TD3	36	"C1000D" and not "E2"
ENET2_TD2	38	"C1000D" and not "E2"
ENET2_RD0	42	"C1000D" and not "E2"
ENET2_RX_CTL	44	"C1000D" and not "E2"
ENET2_RD2	48	"C1000D" and not "E2"
ENET2_RD1	50	"C1000D" and not "E2"

4.7 Wireless Interfaces

CL-SOM-iMX7 optional wireless communication capabilities are implemented with one of the following two assembly options:

- 2.4GHz WiFi only capability, Implemented with the "W" ordering option of CL-SOM-iMX7. Please refer to WLAN Only section for additional details.
- Dual-Band WiFi and Bluetooth capabilities, Implemented with the "WAB" ordering option of CL-SOM-iMX7. Please refer to Dual Band WLAN & Bluetooth section for additional details.

CL-SOM-iMX7 is equipped with up-to two U.FL high frequency connectors allowing easy integration with external antennas:

- Primary WLAN/BT antenna connector J1. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality. J1 is available with either "W" or "WAB" ordering options of CL-SOM-iMX7.
- Secondary WLAN antenna connector J2. Can be used with any type of 2.4GHz/5.0GHz antenna for Dual-Band WLAN functionality. J2 is only available with the "WAB" ordering option of CL-SOM-iMX7.

Table 14 J1 & J2 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

4.7.1 WLAN Only

CL-SOM-iMX7 simple WLAN Only capabilities are based on the optional Texas Instruments WL1801MOD WLAN module soldered onboard.

WL1801MOD is a WiLink™ 8 based Single-Band combo module enabling Wi-Fi® functionality with CL-SOM-iMX7. WL1801MOD supports the following features:

- FCC, IC, ETSI/CE, and TELEC modular certification.
- Support of IEEE Std 802.11a, 802.11b, 802.11g and 802.11n.
- 20- and 40-MHz SISO and 20-MHz 2 x 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP).
- 2.4-GHz MRC Support for Extended Range.
- Wi-Fi Direct Concurrent Operation (Multichannel, Multirole).

When populated, WL1801MOD is interfaced with the i.MX7 through the following interfaces:

- i.MX7 MMC/SD/SDIO2 interface is used for WLAN data.

Please refer to the i.MX7 and the Texas Instruments WL1801MOD respective reference manuals for additional details.

NOTE: CL-SOM-iMX7 WiFi 802.11 b/g/n (without Bluetooth) functionality is available only with the 'W' ordering option.

4.7.2 Dual Band WLAN & Bluetooth

CL-SOM-iMX7 can be optionally shipped with the Texas Instruments WL1837MOD WLAN/Bluetooh module soldered onboard.

WL1837MOD is a WiLink™ 8 based Dual-Band industrial module enabling Wi-Fi®, Bluetooth®, and Bluetooth Low Energy (BLE) functionality with CL-SOM-iMX7. WL1837MOD supports the following features:

- FCC, IC, ETSI/CE, and TELEC modular certification.
- Support of IEEE Std 802.11a, 802.11b, 802.11g and 802.11n.
- 20- and 40-MHz SISO and 20-MHz 2 x 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP).
- 2.4-GHz MRC Support for Extended Range and 5-GHz Diversity Capable.
- Wi-Fi Direct Concurrent Operation (Multichannel, Multirole).
- Bluetooth 4.1 Compliance and CSA2 Support.
- Dedicated Audio Processor Support of SBC Encoding + A2DP.
- Dual-Mode Bluetooth and BLE.

When populated, WL1837MOD is interfaced with the i.MX7 through the following interfaces:

- i.MX7 MMC/SD/SDIO2 interface is used for WLAN data.
- i.MX7 UART3 and SAI2 interfaces are employed fur Bluetooth and A2DP data.

Please refer to the i.MX7 and the Texas Instruments WL1837MOD respective reference manuals for additional details.

NOTE: CL-SOM-iMX7 WiFi 802.11 a/b/g/n and Bluetooth functionality is available only with the 'WAB' ordering option.

4.8 Analog Audio

The CL-SOM-iMX7 analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with the i.MX7 SAI1 port. The WM8731L codec supports the following main features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

NOTE: CL-SOM-iMX7 Analog audio interface is available only with the 'A' ordering option.

Table 15 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
Programmable gain	1 kHz output		-73	0	6	dB
Programmable-gain step size	1 kHz			1		dB
Mute attenuation	1 kHz output, 0dB			80		dB

Parameter	Test conditions	Min	Typ	Max	Unit
Line Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio	A-weighted, 0dB gain, Fsample = 48 kHz.	85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.		90		
Dynamic range	A-weighted, −60-dB full-scale input	85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain		-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVp-p		45		
ADC Channel Separation	1 kHz input tone		90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω	-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic		1.5		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance	12 dB input gain	10	15		kΩ
	0 dB input gain	20	30		
Input capacitance			10		pF
Microphone Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio	A-weighted, 0-dB gain		85		dB
Dynamic range,	A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion,	0dB input, 0dB gain		-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVp-p		45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,		14		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance			10		kΩ
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

Please refer to the Wolfson Microelectronics WM8731L datasheet for additional details. The table below summarizes the analog audio interface signals

Table 16 analog audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
LHPOUT	203	AO	Left channel headphone output	"A"
LLINEIN	199	LI	Left channel line input	"A"
MICBIAS	191	APO	Electret microphone bias supply	"A"
MICIN	193	AI	Microphone input	"A"
RHPOUT	201	AO	Right channel headphone output	"A"
RLINEIN	197	AI	Right channel line input	"A"

4.9 Digital Audio (SAI)

CL-SOM-iMX7 enables access to all 3 of the i.MX7 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for first word and remaining words in frame.

- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

NOTE: CL-SOM-iMX7 SAI1 interface is available only without the 'A' ordering option.

NOTE: CL-SOM-iMX7 SAI2 interface is available only without the 'WAB' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SAI interface signals

Table 17 SAI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1.MCLK	93*	IO	Audio master clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.RX_BCLK	8*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "E1" and not "E2"
SAI1.RX_BCLK	203*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.RX_DATA[0]	193*	I	Receive data, sampled synchronously by the bit clock	not "A"
SAI1.RX_SYNC	6*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "E1" and not "E2"
SAI1.RX_SYNC	201*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"
SAI1.TX_BCLK	199*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI1.TX_DATA[0]	197*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "A"
SAI1.TX_SYNC	191*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"

Table 18 SAI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2.MCLK	73*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI2.RX_BCLK	147*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "W" and not "WAB"
SAI2.RX_BCLK	203*	IO	Receive bit clock. An input when generated externally and an output when generated internally.	not "A"
SAI2.RX_DATA[0]	143*	I	Receive data, sampled synchronously by the bit clock	not "WAB"
SAI2.RX_DATA[0]	155*	I	Receive data, sampled synchronously by the bit clock	not "W" and not "WAB"
SAI2.RX_SYNC	157*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "W" and not "WAB"
SAI2.RX_SYNC	201*	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "A"
SAI2.TX_BCLK	137*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "WAB"
SAI2.TX_BCLK	153*	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	not "W" and not "WAB"
SAI2.TX_DATA[0]	139*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "WAB"
SAI2.TX_DATA[0]	149*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "W" and not "WAB"
SAI2.TX_SYNC	145*	IO	Transmit frame sync. An input sampled by bit	not "WAB"

Signal Name	Pin #	Type	Description	Availability
			clock when generated externally. A bit clock synchronous output when generated internally.	
SAI2.TX_SYNC	151*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "W" and not "WAB"

Table 19 SAI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI3.MCLK	81*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.MCLK	111*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.MCLK	179*~	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always
SAI3.RX_BCLK	82*~	IO	Receive bit clock. An input when generated externally and an output when generated internally.	Always
SAI3.RX_DATA[0]	84*~	I	Receive data, sampled synchronously by the bit clock	Always
SAI3.RX_SYNC	80*~	IO	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always
SAI3.TX_BCLK	86*~	IO	Transmit bit clock. An input when generated externally and an output when generated internally.	Always
SAI3.TX_DATA[0]	90*~	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always
SAI3.TX_DATA[0]	198*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	not "WAB"
SAI3.TX_SYNC	88*~	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always
SAI3.TX_SYNC	187*	IO	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	not "WAB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.10 Medium Quality Sound module (MQS)

The i.MX7 integrated medium-quality sound module (MQS) is used to generate 2-channel, medium-quality, PWM-like audio, via two standard digital GPIO pins, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. The MQS block accepts valid signals from SAI1 and provides up-to 20dB output SNR for signals below 10kHz. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided. Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the MQS interface signals

Table 20 MQS Interface Signals

Signal Name	Pin #	Type	Description	Availability
MQS.LEFT	147*	O	Left signal output	not "W" and not "WAB"
MQS.LEFT	203*	O	Left signal output	not "A"
MQS.RIGHT	157*	O	Right signal output	not "W" and not "WAB"
MQS.RIGHT	201*	O	Right signal output	not "A"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.11 Native USB2.0 ports

The i.MX7 SoC is equipped with two high-speed OTG controller modules and integrated high-speed analog USB PHYs. CL-SOM-iMX7 enables full access to both ports trough the carrier board interface connector. The USB ports support the following main features:

- High speed, full speed and low speed operation in host mode.
- High speed and full speed operation in peripheral mode.
- Up to 8 bidirectional endpoints.
- CL-SOM-iMX7 USB port 0 (i.MX7 port 1) supports for OTG signaling, session request protocol (SRP), host negotiation protocol (HNP), and attach detection protocol (ADP). ADP support includes dedicated timer hardware and register interface.
- CL-SOM-iMX7 USB port 1 (i.MX7 port 2) is configured to operate in host only mode onboard CL-SOM-iMX7.
- Supports charger detection with USB_OTG1_CHD_B pin (i.MX7 port 1 only) and register interface (both i.MX7 ports)

NOTE: CL-SOM-iMX7 USB port 1 (i.MX7 port 2) is available only with the 'C1000D' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the native USB interface signals

Table 21 Native USB port 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB.OTG1_ID	13*	I	OTG1 ID Signal (MUXED)	Always
USB.OTG1_ID	52*	I	OTG1 ID Signal (MUXED)	not "E1" and not "E2"
USB.OTG1_ID	73*	I	OTG1 ID Signal (MUXED)	Always
USB.OTG1_PWR	200*	O	external USB_OTG1_VBUS power supply control signal	not "L"
USB_OTG1_CHD_B	192	IO	OTG1 Charge detect signal	Always
USB_OTG1_DN	178	AIO	Negative part of i.MX7 OTG port1 diff pair	Always
USB_OTG1_DP	176	AIO	Positive part of i.MX7 OTG port1 diff pair	Always
USB_OTG1_ID	174	AI	OTG1 ID Signal (non-muxed)	Always
USB_OTG1_VBUS	180	PI	VBUS input for USB_OTG1	Always

Table 22 Native USB port 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB.OTG2_ID	11*	I	OTG2 ID Signal (MUXED)	"C1000D"
USB.OTG2_ID	81*	I	OTG2 ID Signal (MUXED)	"C1000D"
USB.OTG2_OC	198*	I	Input for USB_OTG2_VBUS overcurrent detection signal (MUXED).	"C1000D" and not "WAB"
USB.OTG2_PWR	187*	O	external USB_OTG2_VBUS power supply control signal (MUXED).	"C1000D" and not "WAB"
USB_OTG2_DN	170	AIO	Negative part of i.MX7 OTG port2 diff pair	"C1000D"
USB_OTG2_DP	172	AIO	Positive part of i.MX7 OTG port2 diff pair	"C1000D"
USB_OTG2_VBUS	196	PI	VBUS input for USB_OTG2	"C1000D"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.12 Onboard USB2.0 Hub

CL-SOM-iMX7 is equipped with an optional onboard USB2.0 hub supporting three downstream USB2.0 host ports. The 3 additional ports are implemented through a combination of the i.MX7

on-chip HSIC high-speed host-only port with the Microchip USB3503 USB hub. The USB hub supports the following main features:

- Three USB 2.0 High Speed (480Mbps) compatible downstream ports
- Supports either Single-TT or Multi-TT configurations for Full-Speed (12Mbps) and Low-Speed (1.5Mbps) connections

NOTE: CL-SOM-iMX7 onboard USB hub is available only with the 'UH' ordering option.

Please refer to the Microchip USB3503 datasheet for additional information. The table below summarizes the USB Hub interface signals

Table 23 USB Hub Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_H1_DN	164	AIO	Negative part of USB hub port1 diff pair.	"UH"
USB_H1_DP	166	AIO	Positive part of USB hub port1 diff pair.	"UH"
USB_H2_DN	158	AIO	Negative part of USB hub port2 diff pair.	"UH"
USB_H2_DP	160	AIO	Positive part of USB hub port2 diff pair.	"UH"
USB_H3_DN	190	AIO	Negative part of USB hub port3 diff pair.	"UH"
USB_H3_DP	188	AIO	Positive part of USB hub port3 diff pair.	"UH"
VBUS_EN_REQ	156	O	external VBUS power supply control signal for onboard USB2.0 Hub ports	"UH"
VBUS_NOVERCURRENT	162	I	Input for USB2.0 Hub ports VBUS overcurrent detection signal.	"UH"

4.13 PCI-Express

The i.MX7Dual SoC is equipped with a single lane PCI Express port (PCIe) v2.1 port. CL-SOM-iMX7 enables access to the i.MX7Dual PCI-Express port through the carrier board interface. The PCI Express port supports the following main features:

- Single lane compliant with PCI Express base specification v2.1 (6.0Gbps).
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface.
- Supports spread spectrum clocking in transmitter and receiver.

NOTE: CL-SOM-iMX7 PCI-Express interface is available only with the 'C1000D' ordering option.

Please refer to the i.MX7 Dual Reference manual for additional details. The table below summarizes the PCI-Express interface signals

Table 24 PCI-Express Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_REFCLKIN_N	101	AI	100 MHz negative-side reference clock differential input for PCIe (optional). Must not be left floating if used.	"C1000D"
PCIE_REFCLKIN_P	103	AI	100 MHz positive-side reference clock differential input for PCIe (optional). Must not be left floating if used.	"C1000D"
PCIE_REFCLKOUT_P	119	AO	100 MHz positive-side reference clock differential output for PCIe (optional). Must be pulled low through 49.9Ω resistor on carrier board if used.	"C1000D"
PCIE_REFCLKOUT_N	121	AO	100 MHz negative-side reference clock differential output for PCIe (optional). Must be pulled low through 49.9Ω resistor on carrier board if used.	"C1000D"
PCIE_RX_N	133	AI	Negative-side received differential input from the PHY	"C1000D"

Signal Name	Pin #	Type	Description	Availability
PCIE_RX_P	131	AI	Positive-side received differential input from the PHY	"C1000D"
PCIE_TX_N	127	AO	Negative-side transmitted differential output from the PHY	"C1000D"
PCIE_TX_P	125	AO	Positive-side transmitted differential output from the PHY	"C1000D"

4.14 Local Bus (EIM)

CL-SOM-iMX7 enables full access to the External Interface Module (EIM) available with the i.MX7 SoC. The EIM block provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface. EIM supports the following main features:

- Up to 4 chip select signals for external devices supporting flexible address decoding. Each chip select memory space determined separately.
- Selectable write protection for each chip select.
- Support for multiplexed address / data bus operation x16 port size.
- Programmable data port sizes for each chip select (x8, x16).
- Programmable wait-state generators for each chip select, for write and read accesses separately.
- Asynchronous accesses with programmable setup and hold times for control signals
- Support for asynchronous page mode accesses (x16 port size).
- Independent synchronous memory burst read mode support for NOR-Flash and PSRAM memories (x16 port size).
- Independent synchronous Memory Burst Write Mode support for PSRAM and NOR-Flash like memories (CellularRAM™ from Micron, Infineon, and Cypress, OneNAND™ and utRAM™ from Samsung, and COSMORAM™ from Toshiba)
- Support of NAND-Flash devices with NOR-Flash like interface - MDOC™ (M-Systems), OneNAND™ (Samsung)
- Support for Big Endian and Little Endian operation modes per access

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the EIM interface signals

Table 25 EIM Interface Signals

Signal Name	Pin #	Type	Description	Availability
WEIM.ACLK_FREERUN	92*^	I; PU33	AXI clock signal	Always
WEIM.AD[0]	98*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[1]	104*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[10]	42*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[11]	50*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[12]	48*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[13]	34*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[14]	44*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[15]	31*	IO	LSB multiplexed Address/Data Bus signal	not "E2"
WEIM.AD[2]	102*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[3]	100*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[4]	116*	IO	LSB multiplexed Address/Data Bus	Always

Signal Name	Pin #	Type	Description	Availability
			signal	
WEIM.AD[5]	118*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[6]	120*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[7]	122*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[8]	60*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.AD[9]	75*	IO	LSB multiplexed Address/Data Bus signal	Always
WEIM.ADDR[16]	32*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[17]	30*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[18]	38*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[19]	36*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[20]	25*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[21]	40*	O	MSB Address Bus signal	not "E2"
WEIM.ADDR[22]	194*	O	MSB Address Bus signal	Always
WEIM.ADDR[23]	146*	O	MSB Address Bus signal	Always
WEIM.ADDR[24]	148*	O	MSB Address Bus signal	Always
WEIM.ADDR[25]	74*	O	MSB Address Bus signal	Always
WEIM.ADDR[26]	76*	O	MSB Address Bus signal	Always
WEIM.BCLK	130*	O	Burst Clock (BCLK). This signal is used to clock external burst capable devices allowing delivery of burst data to/from the EIM	Always
WEIM.CRE	94*^	O; PD	Used as CRE/PS for CellularRam memory	Always
WEIM.CS0_B	128*	O	chip select	Always
WEIM.CS1_B	140*	O	chip select	Always
WEIM.CS2_B	142*^	O; PD	chip select	Always
WEIM.CS3_B	144*^	O; PD	chip select	Always
WEIM.DATA[0]	106*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[1]	108*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[10]	54*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[11]	56*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[12]	79*^	IO; PD/PU33	MSB Data Bus signal. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
WEIM.DATA[13]	77*^	IO; PU33/PD	MSB Data Bus signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
WEIM.DATA[14]	91*^	IO; PU33/PD	MSB Data Bus signal. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
WEIM.DATA[15]	89*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[2]	110*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[3]	112*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[4]	113*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[5]	115*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[6]	95*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[7]	154*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[8]	161*^	IO; PD	MSB Data Bus signal	Always
WEIM.DATA[9]	163*^	IO; PD	MSB Data Bus signal	Always
WEIM.DTACK_B	99*	I	Data Acknowledge, asynchronous access	Always
WEIM.EB_B[0]	138*	O	Byte Enable 0	Always
WEIM.EB_B[1]	152*	O	Byte Enable 1	Always
WEIM.LBA_B	134*	O	Address Valid	Always
WEIM.OE	124*	O	Output Enable	Always
WEIM.RW	126*	O	Memory Write Enable	Always
WEIM.WAIT	136*	I	Ready/Busy/Wait signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.15 MMC / SD /SDIO

Up to two MMC/SD/SDIO ports are available through the CL-SOM-iMX7 carrier board interface. Both ports are derived from the i.MX7 on-chip MMC/SD/SDIO controller IPs (uSDHC). The uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS400 (8-bit transfer mode is only available on uSDHC port 1).
- Dedicated “card detection” and “write protection” signals and (hardware reset not supported).
- Both 1.8V and 3.3V signaling support (uSDHC port 1 with 1-bit and 4-bit operation modes only).

NOTE: CL-SOM-iMX7 MMC/SD/SDIO port 2 is available only without the ‘W’ and ‘WAB’ ordering options.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the MMC/SD/SDIO interface signals

Table 26 MMC/SD/SDIO1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC1.CD_B	61*~	I	Card detection pin	Always
USDHC1.CLK	80*~	O	Clock for MMC/SD/SDIO card	Always
USDHC1.CMD	82*~	IO	CMD line connect to card	Always
USDHC1.DATA0	84*~	IO	DATA0 line in all modes. Also used to detect busy state	Always
USDHC1.DATA1	86*~	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always
USDHC1.DATA2	88*~	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always
USDHC1.DATA3	90*~	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always
USDHC1.DATA4	83*	IO	DATA4 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA5	85*	IO	DATA5 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA6	107*	IO	DATA6 line in 8-bit mode, not used in other modes	Always
USDHC1.DATA7	109*	IO	DATA7 line in 8-bit mode, not used in other modes	Always
USDHC1.LCTL	49*	O	LED control used to drive an external LED	Always
USDHC1.RESET_B	179*~	O	Card hardware reset signal, active LOW	Always
USDHC1.WP	67*~	I	Card write protect detection	Always

Table 27 MMC/SD/SDIO2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC2.CD_B	97*	I	Card detection pin	not "E1" and not "E2"
USDHC2.CLK	157*	O	Clock for MMC/SD/SDIO card	not "W" and not "WAB"

Signal Name	Pin #	Type	Description	Availability
USDHC2.CMD	147*	IO	CMD line connect to card	not "W" and not "WAB"
USDHC2.DATA0	155*	IO	DATA0 line in all modes Also used to detect busy state	not "W" and not "WAB"
USDHC2.DATA1	153*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	not "W" and not "WAB"
USDHC2.DATA2	151*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	not "W" and not "WAB"
USDHC2.DATA3	149*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	not "W" and not "WAB"
USDHC2.LCTL	129*	O	LED control used to drive an external LED	Always
USDHC2.WP	52*	I	Card write protect detection	not "E1" and not "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.16 UART

CL-SOM-iMX7 enables access to all 7 of the i.MX7 universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX7 UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: The UART3 interface is used onboard CL-SOM-iMX7 for bluetooth functionality. Using the UART3 interface signals available through the carrier board interface precludes onboard bluetooth operation.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the UART interface signals

Table 28 UART1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1.CTS_B	22*	O	Clear to send	not "E1" and not "E2"
UART1.CTS_B	145*	O	Clear to send	not "WAB"
UART1.RTS_B	4*	I	Request to send	not "E1" and not "E2"
UART1.RTS_B	137*	I	Request to send	not "WAB"
UART1.RX	18*	I	Serial / infrared data receive	not "E1" and not "E2"
UART1.RX	117*	I	Serial / infrared data receive	Always

Signal Name	Pin #	Type	Description	Availability
UART1.TX	20*	O	Serial / infrared data transmit	not "E1" and not "E2"
UART1.TX	111*	O	Serial / infrared data transmit	Always

Table 29 UART2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2.CTS_B	9*	O	Clear to send	Always
UART2.CTS_B	143*	O	Clear to send	not "WAB"
UART2.RTS_B	7*	I	Request to send	Always
UART2.RTS_B	139*	I	Request to send	not "WAB"
UART2.RX	5*	I	Serial / infrared data receive	Always
UART2.TX	3*	O	Serial / infrared data transmit	Always

Table 30 UART3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3.CTS_B	135*	O	Clear to send	Always
UART3.CTS_B	187*	O	Clear to send	not "WAB"
UART3.RTS_B	129*	I	Request to send	Always
UART3.RTS_B	198*	I	Request to send	not "WAB"
UART3.RX	43*	I	Serial / infrared data receive	Always
UART3.TX	49*	O	Serial / infrared data transmit	Always

Table 31 UART4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4.CTS_B	63*	O	Clear to send	Always
UART4.CTS_B	143*	O	Clear to send	not "WAB"
UART4.CTS_B	151*	O	Clear to send	not "W" and not "WAB"
UART4.RTS_B	65*	I	Request to send	Always
UART4.RTS_B	139*	I	Request to send	not "WAB"
UART4.RTS_B	149*	I	Request to send	not "W" and not "WAB"
UART4.RX	69*	I	Serial / infrared data receive	Always
UART4.RX	145*	I	Serial / infrared data receive	not "WAB"
UART4.RX	155*	I	Serial / infrared data receive	not "W" and not "WAB"
UART4.TX	58*	O	Serial / infrared data transmit	Always
UART4.TX	137*	O	Serial / infrared data transmit	not "WAB"
UART4.TX	153*	O	Serial / infrared data transmit	not "W" and not "WAB"

Table 32 UART5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART5.CTS_B	17*	O	Clear to send	Always
UART5.RTS_B	15*	I	Request to send	Always
UART5.RTS_B	200*	I	Request to send	not "L"
UART5.RX	13*	I	Serial / infrared data receive	Always
UART5.TX	11*	O	Serial / infrared data transmit	Always

Table 33 UART6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART6.CTS_B	80*~	O	Clear to send	Always
UART6.CTS_B	130*	O	Clear to send	Always
UART6.RTS_B	128*	I	Request to send	Always
UART6.RTS_B	179*~	I	Request to send	Always
UART6.RX	61*~	I	Serial / infrared data receive	Always
UART6.RX	124*	I	Serial / infrared data receive	Always
UART6.TX	67*~	O	Serial / infrared data transmit	Always
UART6.TX	126*	O	Serial / infrared data transmit	Always

Table 34 UART7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART7.CTS_B	88*~	O	Clear to send	Always
UART7.CTS_B	109*	O	Clear to send	Always
UART7.CTS_B	140*	O	Clear to send	Always
UART7.RTS_B	90*~	I	Request to send	Always
UART7.RTS_B	107*	I	Request to send	Always

Signal Name	Pin #	Type	Description	Availability
UART7.RTS_B	138*	I	Request to send	Always
UART7.RX	84*~	I	Serial / infrared data receive	Always
UART7.RX	83*	I	Serial / infrared data receive	Always
UART7.RX	134*	I	Serial / infrared data receive	Always
UART7.TX	85*	O	Serial / infrared data transmit	Always
UART7.TX	86*~	O	Serial / infrared data transmit	Always
UART7.TX	136*	O	Serial / infrared data transmit	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.17 I2C

CL-SOM-iMX7 is equipped with three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the I2C interface signals

Table 35 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1.SCL	63*	IOD	Serial Clock	Always
I2C1.SCL	117*	IOD	Serial Clock	Always
I2C1.SDA	65*	IOD	Serial Data	Always
I2C1.SDA	111*	IOD	Serial Data	Always
I2C1.SDA	200*	IOD	Serial Data	not "L"

Table 36 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3.SCL	17*	IOD	Serial Clock	Always
I2C3.SCL	22*	IOD	Serial Clock	not "E1" and not "E2"
I2C3.SCL	43*	IOD	Serial Clock	Always
I2C3.SCL	146*	IOD	Serial Clock	Always
I2C3.SDA	4*	IOD	Serial Data	not "E1" and not "E2"
I2C3.SDA	15*	IOD	Serial Data	Always
I2C3.SDA	49*	IOD	Serial Data	Always
I2C3.SDA	148*	IOD	Serial Data	Always

Table 37 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4.SCL	13*	IOD	Serial Clock	Always
I2C4.SCL	62*	IOD	Serial Clock	not "E1" and not "E2"
I2C4.SCL	74*	IOD	Serial Clock	Always
I2C4.SCL	129*	IOD	Serial Clock	Always
I2C4.SCL	201*	IOD	Serial Clock	not "A"
I2C4.SDA	11*	IOD	Serial Data	Always
I2C4.SDA	14*	IOD	Serial Data	not "E1" and not "E2"
I2C4.SDA	203*	IOD	Serial Data	not "A"
I2C4.SDA	76*	IOD	Serial Data	Always
I2C4.SDA	135*	IOD	Serial Data	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.18 SPI

Up-to three SPI interfaces are accessible through the CL-SOM-iMX7 carrier board interface. The SPI interfaces are derived from i.MX7 integrated synchronous serial interface (eCSPI). Each instance of eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SPI interface signals

Table 38 SPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2.MISO	62*	IO	Master data in; slave data out	not "E1" and not "E2"
ECSPI2.MISO	107*	IO	Master data in; slave data out	Always
ECSPI2.MOSI	20*	IO	Master data out; slave data in	not "E1" and not "E2"
ECSPI2.MOSI	85*	IO	Master data out; slave data in	Always
ECSPI2.RDY	12*	I	SPI data ready signal	not "E1" and not "E2"
ECSPI2.SCLK	18*	IO	SPI clock signal	not "E1" and not "E2"
ECSPI2.SCLK	83*	IO	SPI clock signal	Always
ECSPI2.SS0	14*	IO	Chip select signal	not "E1" and not "E2"
ECSPI2.SS0	109*	IO	Chip select signal	Always
ECSPI2.SS1	26*	IO	Chip select signal	not "E1" and not "E2"
ECSPI2.SS2	24*	IO	indicates the PHY detects an error in	not "E1" and not "E2"
ECSPI2.SS3	16*	IO	Chip select signal	not "E1" and not "E2"

Table 39 SPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3.MISO	63*	IO	Master data in; slave data out	Always
ECSPI3.MISO	145*	IO	Master data in; slave data out	not "WAB"
ECSPI3.MOSI	65*	IO	Master data out; slave data in	Always
ECSPI3.MOSI	137*	IO	Master data out; slave data in	not "WAB"
ECSPI3.SCLK	69*	IO	SPI clock signal	Always
ECSPI3.SCLK	143*	IO	SPI clock signal	not "WAB"
ECSPI3.SS0	58*	IO	Chip select signal	Always
ECSPI3.SS0	139*	IO	Chip select signal	not "WAB"
ECSPI3.SS1	90*~	IO	Chip select signal	Always
ECSPI3.SS2	97*	IO	Chip select signal	not "E1" and not "E2"
ECSPI3.SS3	52*	IO	Chip select signal	not "E1" and not "E2"

Table 40 SPI4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI4.MISO	5*	IO	Master data in; slave data out	Always
ECSPI4.MISO	61*~	IO	Master data in; slave data out	Always
ECSPI4.MOSI	3*	IO	Master data out; slave data in	Always
ECSPI4.MOSI	67*~	IO	Master data out; slave data in	Always
ECSPI4.RDY	88*~	I	SPI data ready signal	Always
ECSPI4.SCLK	7*	IO	SPI clock signal	Always

Signal Name	Pin #	Type	Description	Availability
ECSPI4.SCLK	179*~	IO	SPI clock signal	Always
ECSPI4.SS0	9*	IO	Chip select signal	Always
ECSPI4.SS0	80*~	IO	Chip select signal	Always
ECSPI4.SS1	82*~	IO	Chip select signal	Always
ECSPI4.SS2	84*~	IO	Chip select signal	Always
ECSPI4.SS3	86*~	IO	Chip select signal	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.19 Quad SPI

CL-SOM-iMX7 is equipped with two instances of the Quad SPI interface. The interface is implemented with the i.MX7 integrated QSPI controller. The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- DMA support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the QSPI interface signals

Table 41 QSPI Interface Signals

Signal Name	Pin #	Type	Description	Availability
QSPI.A_DATA[0]	98*	IO	I/O data signal 1 port 0 for serial flash device A	Always
QSPI.A_DATA[1]	104*	IO	I/O data signal 1 port 1 for serial flash device A	Always
QSPI.A_DATA[2]	102*	IO	I/O data signal 1 port 2 for serial flash device A	Always
QSPI.A_DATA[3]	100*	IO	I/O data signal 1 port 3 for serial flash device A	Always
QSPI.A_DQS	116*	I	Data strobe signal 1 to serial flash device A	Always
QSPI.A_SCLK	118*	O	Serial clock output 1 to serial flash device A	Always
QSPI.A_SS0_B	120*	O	Chip select 1 port 0 for serial flash device A	Always
QSPI.A_SS1_B	122*	O	Chip select 1 port 1 for serial flash device A	Always
QSPI.B_DATA[0]	124*	IO	I/O data signal 1 port 0 for serial flash device B	Always
QSPI.B_DATA[1]	126*	IO	I/O data signal 1 port 1 for serial flash device B	Always
QSPI.B_DATA[2]	128*	IO	I/O data signal 1 port 2 for serial flash device B	Always
QSPI.B_DATA[3]	130*	IO	I/O data signal 1 port 3 for serial flash device B	Always
QSPI.B_DQS	134*	I	Data strobe signal 1 to serial flash device B	Always
QSPI.B_SCLK	136*	O	Serial clock output 1 to serial flash device B	Always
QSPI.B_SS0_B	138*	O	Chip select 1 port 0 for serial flash device B	Always
QSPI.B_SS1_B	140*	O	Chip select 1 port 1 for serial flash device B	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.20 CAN Bus

CL-SOM-iMX7 is equipped with two instances of the CAN bus controller. Each interface is implemented with the i.MX7 integrated FlexCAN module. The following features are supported by the DCAN module:

- Supports CAN protocol version 2.0B.
- Programmable bit rate up to 1 Mbps.
- Flexible Mailboxes of eight bytes data length
- 100% backwards compatibility with previous FLEXCAN version

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the CAN bus interface signals

Table 42 CAN bus 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN1.RX	18*	I	FLEXCAN receive pin	not "E1" and not "E2"
CAN1.RX	63*	I	FLEXCAN receive pin	Always
CAN1.TX	20*	O	FLEXCAN transmit pin	not "E1" and not "E2"
CAN1.TX	65*	O	FLEXCAN transmit pin	Always

Table 43 CAN bus 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN2.RX	17*	I	FLEXCAN receive pin	Always
CAN2.RX	62*	I	FLEXCAN receive pin	not "E1" and not "E2"
CAN2.TX	14*	O	FLEXCAN transmit pin	not "E1" and not "E2"
CAN2.TX	15*	O	FLEXCAN transmit pin	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.21 ADC

CL-SOM-iMX7 is equipped with two instances of the general purpose ADC controller. Each instance is implemented with the i.MX7 integrated 12-bit general purpose analog to digital converter module (ADC). The i.MX7 ADC module supports the following main features:

- 12-bit word size.
- Support single and continuous conversion.
- Support compare mode and channel auto disable if data match the requirement.
- Support average conversion and flexible 4, 8, 16, 32 number of conversion data.
- Configurable sample time and conversion speed / power. Sample rates up to 1MHz.
- Conversion complete, hardware average complete, compare, DMA, time out flag and interrupt.
- Automatic compare with interrupt for less than, greater than, and equal to, within range, or out-of-range, programmable value.

NOTE: CL-SOM-iMX7 ADC port 2 is available only without the 'I' ordering option.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the ADC interface signals

Table 44 ADC1 Interface Signals

Signal Name	Pin #	Type	Description	Availability

Signal Name	Pin #	Type	Description	Availability
ADC1_IN0	167	AI	Analog channel 2 input 0	Always
ADC1_IN1	169	AI	Analog channel 2 input 1	Always
ADC1_IN2	173	AI	Analog channel 2 input 2	Always
ADC1_IN3	175	AI	Analog channel 2 input 3	Always

Table 45 ADC2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ADC2_IN0	66	AI	Analog channel 1 input 0	not "I"
ADC2_IN1	68	AI	Analog channel 1 input 1	not "I"
ADC2_IN2	70	AI	Analog channel 1 input 2	not "I"
ADC2_IN3	72	AI	Analog channel 1 input 3	not "I"

4.22 Resistive Touch Interface

CL-SOM-iMX7 features an optional on-board Texas Instruments TSC2046 resistive touch-screen controller. The controller is communicating with the i.MX7 SoC over the SPI1 interface. The interface supports 4-wire touch panels and is available through the CL-SOM-iMX7 carrier board interface.

NOTE: CL-SOM-iMX7 Resistive touch interface is available only with the 'I' ordering option.

Please refer to Texas Instruments TSC2046 datasheet for additional details. The table below summarizes the resistive touch interface signals

Table 46 Resistive Touch Interface Signals

Signal Name	Pin #	Type	Description	Availability
RTOUCH_X-	68	AIO	Touch screen X- (left)	"I"
RTOUCH_X+	66	AIO	Touch screen X+ (right)	"I"
RTOUCH_Y-	72	AIO	Touch screen Y- (bottom)	"I"
RTOUCH_Y+	70	AIO	Touch screen Y+ (top)	"I"

4.23 PWM

Four PWM output signals are available at the CL-SOM-iMX7 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the PWM interface signals

Table 47 PWM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1.OUT	22*	O	PWM1 functional output	not "E1" and not "E2"
PWM1.OUT	43*	O	PWM1 functional output	Always
PWM1.OUT	93*	O	PWM1 functional output	not "A"

Table 48 PWM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM2.OUT	4*	O	PWM2 functional output	not "E1" and not "E2"

Signal Name	Pin #	Type	Description	Availability
PWM2.OUT	49*	O	PWM2 functional output	Always
PWM2.OUT	73*	O	PWM2 functional output	Always

Table 49 PWM3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM3.OUT	16*	O	PWM3 functional output	not "E1" and not "E2"
PWM3.OUT	81*	O	PWM3 functional output	Always
PWM3.OUT	129*	O	PWM3 functional output	Always

Table 50 PWM4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM4.OUT	12*	O	PWM4 functional output	not "E1" and not "E2"
PWM4.OUT	135*	O	PWM4 functional output	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.24 General Purpose Timer

CL-SOM-iMX7 features 3 instances of a general purpose timer module (GPT). The GPT is capable of generating an event on CL-SOM-iMX7 carrier board interface and/or a system interrupt when the timer reaches a programmed value. Additional GPT functionality includes capturing the counter value in a register (this can be triggered by an event on the CL-SOM-iMX7 carrier board interface). The following main features are supported with each GPT module:

- One 32-bit up-counter with clock source selection, including external clock.
- 12-bit prescaler for division of input clock frequency.
- Two “Capture Event” trigger inputs (2 channels) with a programmable trigger edge.
- Three “Compare Event Occurred” outputs (3 channels) with programmable “active” state. A "forced compare" feature is also available.
- Interrupt generation at capture, compare, and rollover events.
- Restart or free-run modes for counter operations.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the GPT interface signals

Table 51 GPT1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT1.CAPTURE1	112*^	I; PD	Input pin for a capture event	Always
GPT1.CAPTURE2	113*^	I; PD	Input pin for a capture event	Always
GPT1.CLK	110*^	I; PD	Input pin for an option external clock to use with timer	Always
GPT1.COMPARE1	99*	O	Output pin that indicates a "compare event" occurrence	Always
GPT1.COMPARE2	106*^	O; PD	Output pin that indicates a "compare event" occurrence	Always
GPT1.COMPARE3	108*^	O; PD	Output pin that indicates a "compare event" occurrence	Always

Table 52 GPT2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT2.CAPTURE1	191*	I	Input pin for a capture event	not "A"
GPT2.CAPTURE2	197*	I	Input pin for a capture event	not "A"
GPT2.CLK	199*	I	Input pin for an option external clock to use with timer	not "A"
GPT2.COMPARE1	6*	O	Output pin that indicates a "compare event"	not "E1" and not

Signal Name	Pin #	Type	Description	Availability
			occurrence	"E2"
GPT2.COMPARE2	8*	O	Output pin that indicates a "compare event" occurrence	not "E1" and not "E2"
GPT2.COMPARE3	193*	O	Output pin that indicates a "compare event" occurrence	not "A"

Table 53 GPT4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPT4.CAPTURE1	147*	I	Input pin for a capture event	not "W" and not "WAB"
GPT4.CAPTURE2	155*	I	Input pin for a capture event	not "W" and not "WAB"
GPT4.CLK	157*	I	Input pin for an option external clock to use with timer	not "W" and not "WAB"
GPT4.COMPARE1	153*	O	Output pin that indicates a "compare event" occurrence	not "W" and not "WAB"
GPT4.COMPARE2	151*	O	Output pin that indicates a "compare event" occurrence	not "W" and not "WAB"
GPT4.COMPARE3	149*	O	Output pin that indicates a "compare event" occurrence	not "W" and not "WAB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

4.25 Watch dog Timers

CL-SOM-iMX7 is equipped with four “Watchdog timers” (WDOG) derived from the i.MX7 SoC. The WDOG can be used to protect system from failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a timeout, the WDOG will assert the internal system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. WDOG supports the following main features:

- A configurable timeout counter with periods from 0.5 seconds up to 128 seconds.
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the WDOG interface signals

Table 54 WDOG Interface Signals

Signal Name	Pin #	Type	Description	Availability
WDOG.GLOBAL	197*	IO	Global WDOG signal	not "A"
WDOG1.WDOG_B	43*	IO	This signal will power down the system	Always
WDOG2.WDOG_B	199*	IO	This signal will power down the system	not "A"
WDOG2.WDOG_RST_B_DEB	191*	O	This signal is a reset source for the system	not "A"
WDOG3.WDOG_B	69*	IO	This signal will power down the system	Always
WDOG3.WDOG_RST_B_DEB	58*	O	This signal is a reset source for the system	Always
WDOG4.WDOG_B	13*	IO	This signal will power down the system	Always
WDOG4.WDOG_RST_B_DEB	11*	O	This signal is a reset source for the system	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.26 FlexTimer Module

External signals for two instances of the i.MX7 integrated flexible time module (FTM) are accessible through the CL-SOM-iMX7 carrier board interface. The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The following features are supported:

- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128.
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode.
- In output compare mode the output signal can be set, cleared, or toggled on match.
- All channels can be configured for center-aligned PWM mode.
- Quadrature decoder with input filters, relative position counting, and interrupts on position count or capture of position count on external event.
- Backwards compatible with TPM.
- Software control of PWM outputs.

Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the flextimer interface signals

Table 55 FLEXTIMER1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXTIMER1.CH[0]	48*	IO	Flextimer channel 0	not "E2"
FLEXTIMER1.CH[0]	61*~	IO	Flextimer channel 0	Always
FLEXTIMER1.CH[1]	34*	IO	Flextimer channel 1	not "E2"
FLEXTIMER1.CH[1]	67*~	IO	Flextimer channel 1	Always
FLEXTIMER1.CH[2]	44*	IO	Flextimer channel 2	not "E2"
FLEXTIMER1.CH[2]	179*~	IO	Flextimer channel 2	Always
FLEXTIMER1.CH[3]	31*	IO	Flextimer channel 3	not "E2"
FLEXTIMER1.CH[3]	80*~	IO	Flextimer channel 3	Always
FLEXTIMER1.CH[4]	94*^	IO; PD	Flextimer channel 4	Always
FLEXTIMER1.CH[5]	92*^	IO; PU33	Flextimer channel 5	Always
FLEXTIMER1.CH[5]	200*	IO	Flextimer channel 5	not "L"
FLEXTIMER1.CH[6]	142*^	IO; PD	Flextimer channel 6	Always
FLEXTIMER1.CH[7]	144*^	IO; PD	Flextimer channel 7	Always
FLEXTIMER1.PHA	90*~	I	Quadrature decoder phase A input	Always
FLEXTIMER1.PHA	129*	I	Quadrature decoder phase A input	Always
FLEXTIMER1.PHB	97*	I	Quadrature decoder phase B input	not "E1" and not "E2"
FLEXTIMER1.PHB	135*	I	Quadrature decoder phase B input	Always

Table 56 FLEXTIMER2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
FLEXTIMER2.CH[0]	38*	IO	Flextimer channel 0	not "E2"
FLEXTIMER2.CH[0]	82*~	IO	Flextimer channel 0	Always
FLEXTIMER2.CH[1]	36*	IO	Flextimer channel 1	not "E2"
FLEXTIMER2.CH[1]	84*~	IO	Flextimer channel 1	Always
FLEXTIMER2.CH[2]	25*	IO	Flextimer channel 2	not "E2"
FLEXTIMER2.CH[2]	86*~	IO	Flextimer channel 2	Always
FLEXTIMER2.CH[3]	40*	IO	Flextimer channel 3	not "E2"
FLEXTIMER2.CH[3]	88*~	IO	Flextimer channel 3	Always
FLEXTIMER2.CH[4]	145*	IO	Flextimer channel 4	not "WAB"
FLEXTIMER2.CH[4]	146*	IO	Flextimer channel 4	Always
FLEXTIMER2.CH[5]	137*	IO	Flextimer channel 5	not "WAB"
FLEXTIMER2.CH[5]	148*	IO	Flextimer channel 5	Always
FLEXTIMER2.CH[6]	74*	IO	Flextimer channel 6	Always
FLEXTIMER2.CH[6]	143*	IO	Flextimer channel 6	not "WAB"
FLEXTIMER2.CH[7]	76*	IO	Flextimer channel 7	Always

Signal Name	Pin #	Type	Description	Availability
FLEXTIMER2.CH[7]	139*	IO	Flextimer channel 7	not "WAB"
FLEXTIMER2.PHA	203*	I	Quadrature decoder phase A input	not "A"
FLEXTIMER2.PHA	75*	I	Quadrature decoder phase A input	Always
FLEXTIMER2.PHB	152*	I	Quadrature decoder phase B input	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

4.27 Keypad interface

CL-SOM-iMX7 carrier board interface allows access the i.MX7 integrated keypad port (KPP). The KPP is a 16-bit peripheral designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad. The KPP includes these distinctive features:

- Supports up to an 8 x 8 external key pad matrix.
- Open drain design.
- Glitch suppression circuit design.
- Multiple-key detection.
- Long key-press detection.
- Standby key-press detection.
- Synchronizer chain clear.
- Supports a 2-point and 3-point contact key matrix.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the KPP interface signals

Table 57 KPP Interface Signals

Signal Name	Pin #	Type	Description	Availability
KPP.COL[0]	12*	IO	Column input or output	not "E1" and not "E2"
KPP.COL[0]	122*	IO	Column input or output	Always
KPP.COL[1]	24*	IO	Column input or output	not "E1" and not "E2"
KPP.COL[1]	118*	IO	Column input or output	Always
KPP.COL[2]	20*	IO	Column input or output	not "E1" and not "E2"
KPP.COL[2]	100*	IO	Column input or output	Always
KPP.COL[3]	4*	IO	Column input or output	not "E1" and not "E2"
KPP.COL[3]	104*	IO	Column input or output	Always
KPP.COL[4]	50*	IO	Column input or output	not "E2"
KPP.COL[5]	43*	IO	Column input or output	Always
KPP.COL[5]	48*	IO	Column input or output	not "E2"
KPP.COL[6]	32*	IO	Column input or output	not "E2"
KPP.COL[6]	129*	IO	Column input or output	Always
KPP.COL[7]	38*	IO	Column input or output	not "E2"
KPP.COL[7]	143*	IO	Column input or output	not "WAB"
KPP.ROW[0]	16*	IO	Row input or output	not "E1" and not "E2"
KPP.ROW[0]	120*	IO	Row input or output	Always
KPP.ROW[1]	26*	IO	Row input or output	not "E1" and not "E2"
KPP.ROW[1]	116*	IO	Row input or output	Always
KPP.ROW[2]	18*	IO	Row input or output	not "E1" and not "E2"
KPP.ROW[2]	102*	IO	Row input or output	Always
KPP.ROW[3]	22*	IO	Row input or output	not "E1" and not "E2"

Signal Name	Pin #	Type	Description	Availability
KPP.ROW[3]	98*	IO	Row input or output	Always
KPP.ROW[4]	42*	IO	Row input or output	not "E2"
KPP.ROW[5]	34*	IO	Row input or output	not "E2"
KPP.ROW[5]	49*	IO	Row input or output	Always
KPP.ROW[6]	30*	IO	Row input or output	not "E2"
KPP.ROW[6]	135*	IO	Row input or output	Always
KPP.ROW[7]	36*	IO	Row input or output	not "E2"
KPP.ROW[7]	139*	IO	Row input or output	not "WAB"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.28 SmartCard interface

The i.MX7 features two instances of the smart card identification module (SIM). The module is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards and compatible with ISO/IEC 7816-3. The CL-SOM-iMX7 carrier board interface allows access to signals of both interfaces. Please refer to the i.MX7 Reference manual for additional details. The tables below summarize the SIM interface signals

Table 58 SIM1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SIM1.PORT1_CLK	126*	O	Clock for the smartcard	Always
SIM1.PORT1_PD	134*	I	Card insertion detect	Always
SIM1.PORT1_PD	201*	I	Card insertion detect	not "A"
SIM1.PORT1_RST_B	128*	O	Reset signal	Always
SIM1.PORT1_SVEN	130*	O	Vcc enable	Always
SIM1.PORT1_TRXD	124*	IO	Transmit/receive data	Always
SIM1.PORT2_CLK	104*	O	Clock for the smartcard	Always
SIM1.PORT2_PD	116*	I	Card insertion detect	Always
SIM1.PORT2_RST_B	102*	O	Reset signal	Always
SIM1.PORT2_SVEN	100*	O	Vcc enable	Always
SIM1.PORT2_TRXD	98*	IO	Transmit/receive data	Always

Table 59 SIM2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SIM2.PORT1_CLK	138*	O	Clock for the smartcard	Always
SIM2.PORT1_CLK	155*	O	Clock for the smartcard	not "W" and not "WAB"
SIM2.PORT1_PD	30*	I	Card insertion detect	not "E2"
SIM2.PORT1_PD	149*	I	Card insertion detect	not "W" and not "WAB"
SIM2.PORT1_RST_B	140*	O	Reset signal	Always
SIM2.PORT1_RST_B	153*	O	Reset signal	not "W" and not "WAB"
SIM2.PORT1_SVEN	32*	O	Vcc enable	not "E2"
SIM2.PORT1_SVEN	151*	O	Vcc enable	not "W" and not "WAB"
SIM2.PORT1_TRXD	136*	IO	Transmit/receive data	Always
SIM2.PORT1_TRXD	147*	IO	Transmit/receive data	not "W" and not "WAB"
SIM2.PORT2_CLK	120*	O	Clock for the smartcard	Always
SIM2.PORT2_PD	50*	I	Card insertion detect	not "E2"
SIM2.PORT2_RST_B	122*	O	Reset signal	Always
SIM2.PORT2_SVEN	42*	O	Vcc enable	not "E2"
SIM2.PORT2_TRXD	118*	IO	Transmit/receive data	Always

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.29 GPIO

Up-to 124 of the i.MX7 general purpose input/output (GPIO) signals are available through the carrier board interface of CL-SOM-iMX7. When configured as an output, it is possible to write to an i.MX7 register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX7 register. In addition GPIOs peripheral can produce interrupts. The GPIO signals can be configured for the following applications:

NOTE: Not all GPIO signals supported by the i.MX7 SoC are available through the CL-SOM-iMX7 carrier board interface.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the GPIO interface signals

Table 60 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1.IO[1]	93*	IO	General purpose input/output	not "A"
GPIO1.IO[10]	129*	IO	General purpose input/output	Always
GPIO1.IO[11]	135*	IO	General purpose input/output	Always
GPIO1.IO[2]	73*	IO	General purpose input/output	Always
GPIO1.IO[3]	81*	IO	General purpose input/output	Always
GPIO1.IO[5]	200*	IO	General purpose input/output	not "L"
GPIO1.IO[8]	43*	IO	General purpose input/output	Always
GPIO1.IO[9]	49*	IO	General purpose input/output	Always
GPIO2.IO[0]	98*	IO	General purpose input/output	Always
GPIO2.IO[1]	104*	IO	General purpose input/output	Always
GPIO2.IO[10]	128*	IO	General purpose input/output	Always
GPIO2.IO[11]	130*	IO	General purpose input/output	Always
GPIO2.IO[12]	134*	IO	General purpose input/output	Always
GPIO2.IO[13]	136*	IO	General purpose input/output	Always
GPIO2.IO[14]	138*	IO	General purpose input/output	Always
GPIO2.IO[15]	140*	IO	General purpose input/output	Always
GPIO2.IO[16]	42*	IO	General purpose input/output	not "E2"
GPIO2.IO[17]	50*	IO	General purpose input/output	not "E2"
GPIO2.IO[18]	48*	IO	General purpose input/output	not "E2"
GPIO2.IO[19]	34*	IO	General purpose input/output	not "E2"
GPIO2.IO[2]	102*	IO	General purpose input/output	Always
GPIO2.IO[20]	44*	IO	General purpose input/output	not "E2"
GPIO2.IO[21]	31*	IO	General purpose input/output	not "E2"
GPIO2.IO[22]	32*	IO	General purpose input/output	not "E2"
GPIO2.IO[23]	30*	IO	General purpose input/output	not "E2"
GPIO2.IO[24]	38*	IO	General purpose input/output	not "E2"
GPIO2.IO[25]	36*	IO	General purpose input/output	not "E2"
GPIO2.IO[26]	25*	IO	General purpose input/output	not "E2"
GPIO2.IO[27]	40*	IO	General purpose input/output	not "E2"
GPIO2.IO[28]	194*	IO	General purpose input/output	Always
GPIO2.IO[29]	60*	IO	General purpose input/output	Always
GPIO2.IO[3]	100*	IO	General purpose input/output	Always
GPIO2.IO[30]	75*	IO	General purpose input/output	Always
GPIO2.IO[31]	152*	IO	General purpose input/output	Always
GPIO2.IO[4]	116*	IO	General purpose input/output	Always
GPIO2.IO[5]	118*	IO	General purpose input/output	Always
GPIO2.IO[6]	120*	IO	General purpose input/output	Always
GPIO2.IO[7]	122*	IO	General purpose input/output	Always
GPIO2.IO[8]	124*	IO	General purpose input/output	Always
GPIO2.IO[9]	126*	IO	General purpose input/output	Always
GPIO3.IO[0]	5*	IO	General purpose input/output	Always
GPIO3.IO[1]	3*	IO	General purpose input/output	Always
GPIO3.IO[10]	115*^	IO; PD	General purpose input/output	Always
GPIO3.IO[11]	95*^	IO; PD	General purpose input/output	Always
GPIO3.IO[12]	154*^	IO; PD	General purpose input/output	Always
GPIO3.IO[13]	161*^	IO; PD	General purpose input/output	Always
GPIO3.IO[14]	163*^	IO; PD	General purpose input/output	Always
GPIO3.IO[15]	54*^	IO; PD	General purpose input/output	Always
GPIO3.IO[16]	56*^	IO; PD	General purpose input/output	Always

Signal Name	Pin #	Type	Description	Availability
GPIO3.IO[17]	79*^	IO; PD/PU33	General purpose input/output. Pulled low on SoM during normal operation. Pulled high on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[18]	77*^	IO; PU33/PD	General purpose input/output. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[19]	91*^	IO; PU33/PD	General purpose input/output. Pulled high on SoM during normal operation. Pulled low on SoM when alternate boot sequence is selected.	Always
GPIO3.IO[2]	7*	IO	General purpose input/output	Always
GPIO3.IO[20]	89*^	IO; PD	General purpose input/output	Always
GPIO3.IO[21]	94*^	IO; PD	General purpose input/output	Always
GPIO3.IO[22]	92*^	IO; PU33	General purpose input/output	Always
GPIO3.IO[23]	142*^	IO; PD	General purpose input/output	Always
GPIO3.IO[24]	144*^	IO; PD	General purpose input/output	Always
GPIO3.IO[25]	146*	IO	General purpose input/output	Always
GPIO3.IO[26]	148*	IO	General purpose input/output	Always
GPIO3.IO[27]	74*	IO	General purpose input/output	Always
GPIO3.IO[28]	76*	IO	General purpose input/output	Always
GPIO3.IO[3]	9*	IO	General purpose input/output	Always
GPIO3.IO[4]	99*	IO	General purpose input/output	Always
GPIO3.IO[5]	106*^	IO; PD	General purpose input/output	Always
GPIO3.IO[6]	108*^	IO; PD	General purpose input/output	Always
GPIO3.IO[7]	110*^	IO; PD	General purpose input/output	Always
GPIO3.IO[8]	112*^	IO; PD	General purpose input/output	Always
GPIO3.IO[9]	113*^	IO; PD	General purpose input/output	Always
GPIO4.IO[0]	117*	IO	General purpose input/output	Always
GPIO4.IO[1]	111*	IO	General purpose input/output	Always
GPIO4.IO[10]	69*	IO	General purpose input/output	Always
GPIO4.IO[11]	58*	IO	General purpose input/output	Always
GPIO4.IO[12]	17*	IO	General purpose input/output	Always
GPIO4.IO[13]	15*	IO	General purpose input/output	Always
GPIO4.IO[14]	13*	IO	General purpose input/output	Always
GPIO4.IO[15]	11*	IO	General purpose input/output	Always
GPIO4.IO[20]	83*	IO	General purpose input/output	Always
GPIO4.IO[21]	85*	IO	General purpose input/output	Always
GPIO4.IO[22]	107*	IO	General purpose input/output	Always
GPIO4.IO[23]	109*	IO	General purpose input/output	Always
GPIO4.IO[6]	198*	IO	General purpose input/output	not "WAB"
GPIO4.IO[7]	187*	IO	General purpose input/output	not "WAB"
GPIO4.IO[8]	63*	IO	General purpose input/output	Always
GPIO4.IO[9]	65*	IO	General purpose input/output	Always
GPIO5.IO[0]	61*~	IO	General purpose input/output	Always
GPIO5.IO[1]	67*~	IO	General purpose input/output	Always
GPIO5.IO[10]	52*	IO	General purpose input/output	not "E1" and not "E2"
GPIO5.IO[12]	157*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[13]	147*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[14]	155*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[15]	153*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[16]	151*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[17]	149*	IO	General purpose input/output	not "W" and not "WAB"
GPIO5.IO[2]	179*~	IO	General purpose input/output	Always
GPIO5.IO[3]	80*~	IO	General purpose input/output	Always
GPIO5.IO[4]	82*~	IO	General purpose input/output	Always
GPIO5.IO[5]	84*~	IO	General purpose input/output	Always
GPIO5.IO[6]	86*~	IO	General purpose input/output	Always
GPIO5.IO[7]	88*~	IO	General purpose input/output	Always
GPIO5.IO[8]	90*~	IO	General purpose input/output	Always
GPIO5.IO[9]	97*	IO	General purpose input/output	not "E1" and not "E2"
GPIO6.IO[16]	201*	IO	General purpose input/output	not "A"
GPIO6.IO[17]	203*	IO	General purpose input/output	not "A"
GPIO6.IO[19]	145*	IO	General purpose input/output	not "WAB"

Signal Name	Pin #	Type	Description	Availability
GPIO6.IO[20]	137*	IO	General purpose input/output	not "WAB"
GPIO6.IO[21]	143*	IO	General purpose input/output	not "WAB"
GPIO6.IO[22]	139*	IO	General purpose input/output	not "WAB"
GPIO7.IO[0]	22*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[1]	4*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[10]	6*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[11]	8*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[12]	193*	IO	General purpose input/output	not "A"
GPIO7.IO[13]	199*	IO	General purpose input/output	not "A"
GPIO7.IO[14]	191*	IO	General purpose input/output	not "A"
GPIO7.IO[15]	197*	IO	General purpose input/output	not "A"
GPIO7.IO[2]	18*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[3]	20*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[4]	26*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[5]	24*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[6]	16*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[7]	12*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[8]	62*	IO	General purpose input/output	not "E1" and not "E2"
GPIO7.IO[9]	14*	IO	General purpose input/output	not "E1" and not "E2"

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up / reset.

NOTE: I/O voltage of pins denoted with "~" can dynamically change between 3.3V and 1.8V when MMC/SD/SDIO1 interface is utilized

5 SYSTEM LOGIC

CL-SOM-iMX7 allows access to several system logic related signals through the carrier board interface. Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Supply

The CL-SOM-iMX7 supports two power supply options:

- Regulated DC supply (3.7V Typical).
- Lithium-ion polymer battery
- CL-SOM-iMX7 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board

Table 61 Power signals

Signal Name	Type	Description
VSYS	P	Main power supply. (3.3V - 4.5VTyp.).
VCC_RTC	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave floating if unused.
GND	P	Common ground.

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

CL-SOM-iMX7 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX7 SoC. The logic that controls both signals draws its power from the VCC_RTC power rail, meaning that this power supply must always be present in order to use the external regulator control features.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that CL-SOM-iMX7 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the external regulator control signals

Table 62 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	181	O	When the processor enters SUSPEND mode, it will assert this signal. This signal is referenced to RTC supply voltage generated by PF3000 PMIC onboard CL-SOM-iMX7	Always available
PMIC_ON_REQ	202	O	Active high power-up request output from i.MX7 SoC. This signal is referenced to RTC supply voltage generated by PF3000 PMIC onboard CL-SOM-iMX7	Always available
ONOFF	165	I; PU	ON/OFF button input (De-bouncing provided at this input). Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF	Always available

NOTE: The external regulator control signals logic is powered on-board CL-SOM-iMX7 from the VCC_RTC power supply. VCC_RTC must remain valid at all times for proper operation of these signals.

5.2.2 External DMA Requests

CL-SOM-iMX7 provides two optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the i.MX7 internal SDMA controller. A logical channel can be configured to respond to an external synchronization request.

Please refer to the i.MX7 Reference manual for additional details. The table below summarizes the SDMA interface signals

Table 63 System signals

Signal Name	Pin #	Type	Description	Availability
SDMA.EXT_EVT[0]	17*	I	External DMA request 0	Always
SDMA.EXT_EVT[1]	15*	I	External DMA request 1	Always
SDMA.EXT_EVT[1]	52*	I	External DMA request 1	not "E1" and not "E2"

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.5 of this document.

5.2.3 General Purpose clocks

The i.MX7 clock controller module (CCM) signals are fully accessible through the CL-SOM-iMX7 carrier board interface.

The CCM allows the i.MX7 SoC to utilize carrier board generated clocks as well as providing on-SoC generated clocks to the carrier board. For additional details, please refer to the “Smart Direct Memory Access Controller” of the “i.MX6 Reference Manual”.

Table 64 General Purpose clock signals

Signal Name	Pin #	Type	Description	Availability
CCM.CLKO1	61*	O	SoC Clock 1 output for off-som devices	Always
CCM.CLKO1	73*	O	SoC Clock 1 output for off-som devices	Always
CCM.CLKO2	81*	O	SoC Clock 2 output for off-som devices	Always
CCM.CLKO2	67*	O	SoC Clock 2 output for off-som devices	Always
CCM.ENET1_REF_CLK_ROOT	65*	O	ENET Reference Clock 1	Always
CCM.ENET1_REF_CLK_ROOT	73*	O	ENET Reference Clock 1	Always
CCM.ENET1_REF_CLK_ROOT	193*	O	ENET Reference Clock 1	not "A"
CCM.ENET2_REF_CLK_ROOT	69*	O	ENET Reference Clock 2	Always
CCM.ENET2_REF_CLK_ROOT	81*	O	ENET Reference Clock 2	Always
CCM.ENET2_REF_CLK_ROOT	194*	O	ENET Reference Clock 2	Always
CCM.ENET3_REF_CLK_ROOT	49*	O	ENET Reference Clock 3	Always
CCM.ENET3_REF_CLK_ROOT	58*	O	ENET Reference Clock 3	Always
CCM.ENET3_REF_CLK_ROOT	93*	O	ENET Reference Clock 3	not "A"
CCM.EXT_CLK1	84*	I	External Clock 1	Always
CCM.EXT_CLK1	193*	I	External Clock 1	not "A"
CCM.EXT_CLK2	86*	I	External Clock 2	Always
CCM.EXT_CLK2	199*	I	External Clock 2	not "A"
CCM.EXT_CLK3	88*	I	External Clock 3	Always
CCM.EXT_CLK3	191*	I	External Clock 3	not "A"
CCM.EXT_CLK4	90*	I	External Clock 4	Always
CCM.EXT_CLK4	197*	I	External Clock 4	not "A"

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.5 of this document.

5.2.4 Flash Write-protection

The EEPROM_WP signal can be used to prevent accidental corruption of the data stored on the onboard SPI Flash as well as the onboard ID EEPROM. The CL-SOM-iMX7 on-board EEPROM is used to store board specific production information while the onboard SPI flash is used to store the boot-loader as described in chapter 3.2.2.

NOTE: The EEPROM_WP must be used in conjunction with SW to enable SPI Flash write protection. Using the EEPROM_WP signal alone will not enable SPI Flash write protection.

Table 65 Flash Write protection signals

Signal Name	Pin #	Type	Description	Availability
EEPROM_WP	189	PU33	Active low input to enable onboard EEPROM write protection and allow SPI Flash write-protection.	Always available

5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX7. Please refer to the i.MX7 Reference manual for additional details.

Table 66 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset A valid pulse is low for at least 31mS, with 5.0nS rise/fall times (max).	Always available

5.4 Boot Sequence

CL-SOM-iMX7 boot sequence defines which interface/media is used by CL-SOM-iMX7 to load and execute the initial software (such as U-boot). CL-SOM-iMX7 can load initial software from the following interfaces/media:

- The on-board primary boot device (SPI Flash with pre-flashed boot-loader).
- An external SD/MMC card using the MMC/SD/SDIO 0 interface

CL-SOM-iMX7 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CL-SOM-iMX7:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows CL-SOM-iMX7 to boot from an external SD card, effectively bypassing the onboard SPI Flash.

NOTE: If during an alternate boot sequence, the CL-SOM-iMX7 cannot load the initial software from the external SD card, CL-SOM-iMX7 will fall back and try to load the initial software from the onboard SPI flash.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 67 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 68 CL-SOM-iMX7 Boot sequences

sequence	ALT_BOOT	First	Second	Third	Fourth
Standard	Low or floating	Onboard SPI Flash		SD card on "MMC/SD/SDIO1" (only if card is detected, 1-bit mode)	Host PC on "Native USB port 1" in serial mode
Alternate	High	SD card on "MMC/SD/SDIO1" (4-bit mode)	Onboard SPI Flash		

5.5 Signal Multiplexing Characteristics

Up to 124 of the CL-SOM-iMX7 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX7 SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 9 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX7 pins are derived from the i.MX7 SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

NOTE: The excel spreadsheet CL-SOM-iMX7 PINMUX is included in this document as an attachment.

Table 69 Multifunctional Signals

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Availability
3	LCDIF.ENABLE	ECSPI4.MOSI	ENET1.1588_EVENT3_IN	CSI1.DATA[17]	UART2.TX	GPIO3.IO[1]				Always
4	ENET1.RGMII_RD1	PWM2.OUT	I2C3.SDA	UART1.RTS_B		GPIO7.IO[1]	KPP.COL[3]			not "E1" and not "E2"
5	LCDIF.CLK	ECSPI4.MISO	ENET1.1588_EVENT2_IN	CSI1.DATA[16]	UART2.RX	GPIO3.IO[0]				Always
6	ENET1.RGMII_TX_CTL		SAI1.RX_SYNC	GPT2.COMPARE1		GPIO7.IO[10]				not "E1" and not "E2"
7	LCDIF.HSYNC	ECSPI4.SCLK		CSI1.DATA[18]	UART2.RTS_B	GPIO3.IO[2]				not "C1000D"
7	LCDIF.HSYNC	ECSPI4.SCLK	ENET2.1588_EVENT2_IN	CSI1.DATA[18]	UART2.RTS_B	GPIO3.IO[2]				"C1000D"
8	ENET1.RGMII_TXC	ENET1.TX_ER	SAI1.RX_BCLK	GPT2.COMPARE2		GPIO7.IO[11]				not "E1" and not "E2"
9	LCDIF.VSYNC	ECSPI4.SS0		CSI1.DATA[19]	UART2.CTS_B	GPIO3.IO[3]				not "C1000D"
9	LCDIF.VSYNC	ECSPI4.SS0	ENET2.1588_EVENT3_IN	CSI1.DATA[19]	UART2.CTS_B	GPIO3.IO[3]				"C1000D"
11	I2C4.SDA	UART5.TX	WDOG4.WDOG_RST_B_DEB	CSI1.MCLK		GPIO4.IO[15]				not "C1000D"
11	I2C4.SDA	UART5.TX	WDOG4.WDOG_RST_B_DEB	CSI1.MCLK	USB.OTG2_ID	GPIO4.IO[15]				"C1000D"
12	ENET1.RGMII_TD1	PWM4.OUT	ECSPI2.RDY			GPIO7.IO[7]	KPP.COL[0]			not "E1" and not "E2"
13	I2C4.SCL	UART5.RX	WDOG4.WDOG_B	CSI1.PIXCLK	USB.OTG1_ID	GPIO4.IO[14]				Always
14	ENET1.RGMII_TD3	CAN2.TX	ECSPI2.SS0	I2C4.SDA		GPIO7.IO[9]				not "E1" and not "E2"
15	I2C3.SDA	UART5.RTS_B	CAN2.TX	CSI1.HSYNC	SDMA.EXT_EVENT[1]	GPIO4.IO[13]				Always
16	ENET1.RGMII_TD0	PWM3.OUT	ECSPI2.SS3			GPIO7.IO[6]	KPP.ROW[0]			not "E1" and not "E2"
17	I2C3.SCL	UART5.CTS_B	CAN2.RX	CSI1.VSYNC	SDMA.EXT_EVENT[0]	GPIO4.IO[12]				Always
18	ENET1.RGMII_RD2	CAN1.RX	ECSPI2.SCLK	UART1.RX		GPIO7.IO[2]	KPP.ROW[2]			not "E1" and not "E2"
20	ENET1.RGMII_RD3	CAN1.TX	ECSPI2.MOSI	UART1.TX		GPIO7.IO[3]	KPP.COL[2]			not "E1" and not "E2"
22	ENET1.RGMII_RD0	PWM1.OUT	I2C3.SCL	UART1.CTS_B		GPIO7.IO[0]	KPP.ROW[3]			not "E1" and not "E2"
24	ENET1.RGMII_RXC	ENET1.RX_ER	ECSPI2.SS2			GPIO7.IO[5]	KPP.COL[1]			not "E1" and not "E2"
25		FLEXTIMER2.CH[2]			WEIM.ADDR[20]	GPIO2.IO[26]	LCDIF.RD_E	LCDIF.DATA[19]		not "C1000D" and not "E2"
25		FLEXTIMER2.CH[2]	ENET2.RGMII_TX_CTL		WEIM.ADDR[20]	GPIO2.IO[26]	LCDIF.RD_E	LCDIF.DATA[19]		"C1000D" and not "E2"
26	ENET1.RGMII_RX_CTL		ECSPI2.SS1			GPIO7.IO[4]	KPP.ROW[1]			not "E1" and not "E2"
30		SIM2.PORT1_PD		KPP.ROW[6]	WEIM.ADDR[17]	GPIO2.IO[23]	LCDIF.DATA[22]	LCDIF.DATA[2]		not "C1000D" and not "E2"
30		SIM2.PORT1_PD	ENET2.RGMII_TD1	KPP.ROW[6]	WEIM.ADDR[17]	GPIO2.IO[23]	LCDIF.DATA[22]	LCDIF.DATA[2]		"C1000D" and not "E2"
31		FLEXTIMER1.CH[3]			WEIM.AD[15]	GPIO2.IO[21]	LCDIF.DATA[20]	LCDIF.DATA[4]		not "C1000D" and not "E2"
31		FLEXTIMER1.CH[3]	ENET2.RGMII_RXC		WEIM.AD[15]	GPIO2.IO[21]	LCDIF.DATA[20]	LCDIF.DATA[4]		"C1000D" and not "E2"
32		SIM2.PORT1_SVEN		KPP.COL[6]	WEIM.ADDR[16]	GPIO2.IO[22]	LCDIF.DATA[21]	LCDIF.DATA[3]		not "C1000D" and not "E2"
32		SIM2.PORT1_SVEN	ENET2.RGMII_TD0	KPP.COL[6]	WEIM.ADDR[16]	GPIO2.IO[22]	LCDIF.DATA[21]	LCDIF.DATA[3]		"C1000D" and not "E2"
34		FLEXTIMER1.CH[1]		KPP.ROW[5]	WEIM.AD[13]	GPIO2.IO[19]	LCDIF.DATA[18]	LCDIF.DATA[10]		not "C1000D" and not "E2"
34		FLEXTIMER1.CH[1]	ENET2.RGMII_RD3	KPP.ROW[5]	WEIM.AD[13]	GPIO2.IO[19]	LCDIF.DATA[18]	LCDIF.DATA[10]		"C1000D" and not "E2"
36		FLEXTIMER2.CH[1]		KPP.ROW[7]	WEIM.ADDR[19]	GPIO2.IO[25]	LCDIF.WR_RWN	LCDIF.DATA[18]		not "C1000D" and not "E2"
36		FLEXTIMER2.CH[1]	ENET2.RGMII_TD3	KPP.ROW[7]	WEIM.ADDR[19]	GPIO2.IO[25]	LCDIF.WR_RWN	LCDIF.DATA[18]		"C1000D" and not "E2"

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Availability
38		FLEXTIMER2.CH[0]		KPP.COL[7]	WEIM.ADDR[18]	GPIO2.IO[24]	LCDIF.DATA[23]	LCDIF.DATA[16]		not "C1000D" and not "E2"
38		FLEXTIMER2.CH[0]	ENET2.RGMII_TD2	KPP.COL[7]	WEIM.ADDR[18]	GPIO2.IO[24]	LCDIF.DATA[23]	LCDIF.DATA[16]		"C1000D" and not "E2"
40		FLEXTIMER2.CH[3]			WEIM.ADDR[21]	GPIO2.IO[27]	LCDIF.BUSY	LCDIF.DATA[17]		not "C1000D" and not "E2"
40		FLEXTIMER2.CH[3]	ENET2.RGMII_TXC	ENET2.TX_ER	WEIM.ADDR[21]	GPIO2.IO[27]	LCDIF.BUSY	LCDIF.DATA[17]		"C1000D" and not "E2"
42		SIM2.PORT2_SVEN		KPP.ROW[4]	WEIM.AD[10]	GPIO2.IO[16]	LCDIF.CLK	LCDIF.DATA[20]		not "C1000D" and not "E2"
42		SIM2.PORT2_SVEN	ENET2.RGMII_RD0	KPP.ROW[4]	WEIM.AD[10]	GPIO2.IO[16]	LCDIF.CLK	LCDIF.DATA[20]		"C1000D" and not "E2"
43	GPIO1.IO[8]		WDOG1.WDOG_B	UART3.RX	I2C3.SCL		KPP.COL[5]	PWM1.OUT		Always
44		FLEXTIMER1.CH[2]			WEIM.AD[14]	GPIO2.IO[20]	LCDIF.DATA[19]	LCDIF.DATA[5]		not "C1000D" and not "E2"
44		FLEXTIMER1.CH[2]	ENET2.RGMII_RX_CTL	ENET2.RX_EN	WEIM.AD[14]	GPIO2.IO[20]	LCDIF.DATA[19]	LCDIF.DATA[5]		"C1000D" and not "E2"
48		FLEXTIMER1.CH[0]		KPP.COL[5]	WEIM.AD[12]	GPIO2.IO[18]	LCDIF.DATA[17]	LCDIF.DATA[23]		not "C1000D" and not "E2"
48		FLEXTIMER1.CH[0]	ENET2.RGMII_RD2	KPP.COL[5]	WEIM.AD[12]	GPIO2.IO[18]	LCDIF.DATA[17]	LCDIF.DATA[23]		"C1000D" and not "E2"
49	GPIO1.IO[9]	USDHC1.LCTL	CCM.ENET3_REF_CLK_ROOT	UART3.TX	I2C3.SDA	GPC.PMIC_RDY	KPP.ROW[5]	PWM2.OUT		Always
50		SIM2.PORT2_PD		KPP.COL[4]	WEIM.AD[11]	GPIO2.IO[17]	LCDIF.DATA[16]	LCDIF.DATA[8]		not "C1000D" and not "E2"
50		SIM2.PORT2_PD	ENET2.RGMII_RD1	KPP.COL[4]	WEIM.AD[11]	GPIO2.IO[17]	LCDIF.DATA[16]	LCDIF.DATA[8]		"C1000D" and not "E2"
52	USDHC2.WP	ENET1.MDC		ECSPI3.SS3	USB.OTG1_ID	GPIO5.IO[10]	SDMA.EXT_EVENT[1]			not "C1000D" and not "E1" and not "E2"
52	USDHC2.WP	ENET1.MDC	ENET2.MDC	ECSPI3.SS3	USB.OTG1_ID	GPIO5.IO[10]	SDMA.EXT_EVENT[1]			"C1000D" and not "E1" and not "E2"
54	LCDIF.DATA[10]		CORESIGHT.TRACE[10]	CSI1.DATA[7]	WEIM.DATA[10]	GPIO3.IO[15]	SRC.BT_CFG[10]			Always
56	LCDIF.DATA[11]		CORESIGHT.TRACE[11]	CSI1.DATA[6]	WEIM.DATA[11]	GPIO3.IO[16]	SRC.BT_CFG[11]			Always
58		UART4.TX	WDOG3.WDOG_RST_B_DEB	ECSPI3.SS0	CCM.ENET3_REF_CLK_ROOT	GPIO4.IO[11]	usdhc3.WP			Always
60					WEIM.AD[8]	GPIO2.IO[29]	LCDIF.ENABLE	LCDIF.DATA[6]		not "C1000D"
60			ENET2.RX_CLK		WEIM.AD[8]	GPIO2.IO[29]	LCDIF.ENABLE	LCDIF.DATA[6]		"C1000D"
61	USDHC1.CD_B		UART6.RX	ECSPI4.MISO	FLEXTIMER1.CH[0]	GPIO5.IO[0]	CCM.CLKO1			Always
62	ENET1.RGMII_TD2	CAN2.RX	ECSPI2.MISO	I2C4.SCL		GPIO7.IO[8]				not "E1" and not "E2"
63	I2C1.SCL	UART4.CTS_B	CAN1.RX	ECSPI3.MISO	ANATOP.24M_OUT	GPIO4.IO[8]				Always
65	I2C1.SDA	UART4.RTS_B	CAN1.TX	ECSPI3.MOSI	CCM.ENET1_REF_CLK_ROOT	GPIO4.IO[9]				Always
67	USDHC1.WP		UART6.TX	ECSPI4.MOSI	FLEXTIMER1.CH[1]	GPIO5.IO[1]	CCM.CLKO2			Always
69		UART4.RX	WDOG3.WDOG_B	ECSPI3.SCLK	CCM.ENET2_REF_CLK_ROOT	GPIO4.IO[10]	USDHC3.CD_B			Always
73	GPIO1.IO[2]	PWM2.OUT	CCM.ENET1_REF_CLK_ROOT	SAI2.MCLK	ANATOP.32K_OUT	CCM.CLKO1		USB.OTG1_ID		Always
74	LCDIF.DATA[22]	FLEXTIMER2.CH[6]		CSI1.DATA[11]	WEIM.ADDR[25]	GPIO3.IO[27]	I2C4.SCL			not "C1000D"
74	LCDIF.DATA[22]	FLEXTIMER2.CH[6]	ENET2.1588_EVENT2_OUT	CSI1.DATA[11]	WEIM.ADDR[25]	GPIO3.IO[27]	I2C4.SCL			"C1000D"
75		FLEXTIMER2.PHA			WEIM.AD[9]	GPIO2.IO[30]	LCDIF.HSYNC	LCDIF.DATA[11]		not "C1000D"
75		FLEXTIMER2.PHA	ENET2.CRS		WEIM.AD[9]	GPIO2.IO[30]	LCDIF.HSYNC	LCDIF.DATA[11]		"C1000D"
76	LCDIF.DATA[23]	FLEXTIMER2.CH[7]		CSI1.DATA[10]	WEIM.ADDR[26]	GPIO3.IO[28]	I2C4.SDA			not "C1000D"
76	LCDIF.DATA[23]	FLEXTIMER2.CH[7]	ENET2.1588_EVENT3_OUT	CSI1.DATA[10]	WEIM.ADDR[26]	GPIO3.IO[28]	I2C4.SDA			"C1000D"
77	LCDIF.DATA[13]		CORESIGHT.TRACE[13]	CSI1.DATA[4]	WEIM.DATA[13]	GPIO3.IO[18]	SRC.BT_CFG[13]			Always
79	LCDIF.DATA[12]		CORESIGHT.TRACE[12]	CSI1.DATA[5]	WEIM.DATA[12]	GPIO3.IO[17]	SRC.BT_CFG[12]			Always
80	USDHC1.CLK	SAI3.RX_SYNC	UART6.CTS_B	ECSPI4.SS0	FLEXTIMER1.CH[3]	GPIO5.IO[3]				Always
81	GPIO1.IO[3]	PWM3.OUT	CCM.ENET2_REF_CLK_ROOT	SAI3.MCLK	OSC32K.32K_OUT	CCM.CLKO2				not "C1000D"
81	GPIO1.IO[3]	PWM3.OUT	CCM.ENET2_REF_CLK_ROOT	SAI3.MCLK	OSC32K.32K_OUT	CCM.CLKO2		USB.OTG2_ID		"C1000D"
82	USDHC1.CMD	SAI3.RX_BCLK		ECSPI4.SS1	FLEXTIMER2.CH[0]	GPIO5.IO[4]				Always
83	ECSPI2.SCLK	UART7.RX	USDHC1.DATA4	CSI1.DATA[6]	LCDIF.DATA[13]	GPIO4.IO[20]				Always
84	USDHC1.DATA0	SAI3.RX_DATA[0]	UART7.RX	ECSPI4.SS2	FLEXTIMER2.CH[1]	GPIO5.IO[5]	CCM.EXT_CLK1			Always
85	ECSPI2.MOSI	UART7.TX	USDHC1.DATA5	CSI1.DATA[7]	LCDIF.DATA[14]	GPIO4.IO[21]				Always
86	USDHC1.DATA1	SAI3.TX_BCLK	UART7.TX	ECSPI4.SS3	FLEXTIMER2.CH[2]	GPIO5.IO[6]	CCM.EXT_CLK2			Always
88	USDHC1.DATA2	SAI3.TX_SYNC	UART7.CTS_B	ECSPI4.RDY	FLEXTIMER2.CH[3]	GPIO5.IO[7]	CCM.EXT_CLK3			Always
89	LCDIF.DATA[15]		CORESIGHT.TRACE[15]	CSI1.DATA[2]	WEIM.DATA[15]	GPIO3.IO[20]	SRC.BT_CFG[15]			Always
90	USDHC1.DATA3	SAI3.TX_DATA[0]	UART7.RTS_B	ECSPI3.SS1	FLEXTIMER1.PHA	GPIO5.IO[8]	CCM.EXT_CLK4			Always
91	LCDIF.DATA[14]		CORESIGHT.TRACE[14]	CSI1.DATA[3]	WEIM.DATA[14]	GPIO3.IO[19]	SRC.BT_CFG[14]			Always
92	LCDIF.DATA[17]	FLEXTIMER1.CH[5]	CORESIGHT.TRACE_CTL	CSI1.DATA[0]	WEIM.ACLK_FREERUN	GPIO3.IO[22]	SRC.BT_CFG[17]			Always
93	GPIO1.IO[1]	PWM1.OUT	CCM.ENET3_REF_CLK_ROOT	SAI1.MCLK	ANATOP.24M_OUT					not "A"
94	LCDIF.DATA[16]	FLEXTIMER1.CH[4]	CORESIGHT.TRACE_CLK	CSI1.DATA[1]	WEIM.CRE	GPIO3.IO[21]	SRC.BT_CFG[16]			Always
95	LCDIF.DATA[6]		CORESIGHT.TRACE[6]	CSI1.PIXCLK	WEIM.DATA[6]	GPIO3.IO[11]	SRC.BT_CFG[6]			Always
97	USDHC2.CD_B	ENET1.MDIO		ECSPI3.SS2	FLEXTIMER1.PHB	GPIO5.IO[9]	SDMA.EXT_EVENT[0]			not "C1000D" and not "E1" and not "E2"
97	USDHC2.CD_B	ENET1.MDIO	ENET2.MDIO	ECSPI3.SS2	FLEXTIMER1.PHB	GPIO5.IO[9]	SDMA.EXT_EVENT[0]			"C1000D" and not "E1" and not "E2"
98		SIM1.PORT2_TRXD	QSPI.A_DATA[0]	KPP.ROW[3]	WEIM.AD[0]	GPIO2.IO[0]	LCDIF.DATA[0]	LCDIF.CLK		Always
99	LCDIF.RESET	GPT1.COMPARE1	CORESIGHT.EVENTI	CSI1.FIELD	WEIM.DTACK_B	GPIO3.IO[4]				Always
100		SIM1.PORT2_SVEN	QSPI.A_DATA[3]	KPP.COL[2]	WEIM.AD[3]	GPIO2.IO[3]	LCDIF.DATA[3]	LCDIF.HSYNC		Always
102		SIM1.PORT2_RST_B	QSPI.A_DATA[2]	KPP.ROW[2]	WEIM.AD[2]	GPIO2.IO[2]	LCDIF.DATA[2]	LCDIF.VSYNC		Always
104		SIM1.PORT2_CLK	QSPI.A_DATA[1]	KPP.COL[3]	WEIM.AD[1]	GPIO2.IO[1]	LCDIF.DATA[1]	LCDIF.ENABLE		Always
106	LCDIF.DATA[0]	GPT1.COMPARE2	CORESIGHT.TRACE[0]	CSI1.DATA[20]	WEIM.DATA[0]	GPIO3.IO[5]	SRC.BT_CFG[0]			Always
107	ECSPI2.MISO	UART7.RTS_B	USDHC1.DATA6	CSI1.DATA[8]	LCDIF.DATA[15]	GPIO4.IO[22]				Always
108	LCDIF.DATA[1]	GPT1.COMPARE3	CORESIGHT.TRACE[1]	CSI1.DATA[21]	WEIM.DATA[1]	GPIO3.IO[6]	SRC.BT_CFG[1]			Always
109	ECSPI2.SS0	UART7.CTS_B	USDHC1.DATA7	CSI1.DATA[9]	LCDIF.RESET	GPIO4.IO[23]				Always
110	LCDIF.DATA[2]	GPT1.CLK	CORESIGHT.TRACE[2]	CSI1.DATA[22]	WEIM.DATA[2]	GPIO3.IO[7]	SRC.BT_CFG[2]			Always
111	UART1.TX	I2C1.SDA	SAI3.MCLK			GPIO4.IO[1]	ENET1.MDC			not "C1000D"
111	UART1.TX	I2C1.SDA	SAI3.MCLK		ENET2.1588_EVENT0_OUT	GPIO4.IO[1]	ENET1.MDC			"C1000D"
112	LCDIF.DATA[3]	GPT1.CAPTURE1	CORESIGHT.TRACE[3]	CSI1.DATA[23]	WEIM.DATA[3]	GPIO3.IO[8]	SRC.BT_CFG[3]			Always
113	LCDIF.DATA[4]	GPT1.CAPTURE2	CORESIGHT.TRACE[4]	CSI1.VSYNC	WEIM.DATA[4]	GPIO3.IO[9]	SRC.BT_CFG[4]			Always
115	LCDIF.DATA[5]		CORESIGHT.TRACE[5]	CSI1.HSYNC	WEIM.DATA[5]	GPIO3.IO[10]	SRC.BT_CFG[5]			Always

Pin #	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	Availability
116		SIM1.PORT2_PD	QSPI.A_DQS	KPP.ROW[1]	WEIM.AD[4]	GPIO2.IO[4]	LCDIF.DATA[4]			Always
117	UART1.RX	I2C1.SCL	GPC.PMIC_RDY			GPIO4.IO[0]	ENET1.MDIO			not "C1000D"
117	UART1.RX	I2C1.SCL	GPC.PMIC_RDY		ENET2.1588_EVENT0_IN	GPIO4.IO[0]	ENET1.MDIO			"C1000D"
118		SIM2.PORT2_TRXD	QSPI.A_SCLK	KPP.COL[1]	WEIM.AD[5]	GPIO2.IO[5]	LCDIF.DATA[5]			Always
120		SIM2.PORT2_CLK	QSPI.A_SS0_B	KPP.ROW[0]	WEIM.AD[6]	GPIO2.IO[6]	LCDIF.DATA[6]			Always
122		SIM2.PORT2_RST_B	QSPI.A_SS1_B	KPP.COL[0]	WEIM.AD[7]	GPIO2.IO[7]	LCDIF.DATA[7]			Always
124		SIM1.PORT1_TRXD	QSPI.B_DATA[0]	UART6.RX	WEIM.OE	GPIO2.IO[8]	LCDIF.DATA[8]	LCDIF.BUSY		Always
126		SIM1.PORT1_CLK	QSPI.B_DATA[1]	UART6.TX	WEIM.RW	GPIO2.IO[9]	LCDIF.DATA[9]	LCDIF.DATA[0]		Always
128		SIM1.PORT1_RST_B	QSPI.B_DATA[2]	UART6.RTS_B	WEIM.CS0_B	GPIO2.IO[10]	LCDIF.DATA[10]	LCDIF.DATA[9]		Always
129	GPIO1.IO[10]	USDHC2.LCTL	ENET1.MDIO	UART3.RTS_B	I2C4.SCL	FLEXTIMER1.PHA	KPP.COL[6]	PWM3.OUT		Always
130		SIM1.PORT1_SVEN	QSPI.B_DATA[3]	UART6.CTS_B	WEIM.BCLK	GPIO2.IO[11]	LCDIF.DATA[11]	LCDIF.DATA[1]		Always
134		SIM1.PORT1_PD	QSPI.B_DQS	UART7.RX	WEIM.LBA_B	GPIO2.IO[12]	LCDIF.DATA[12]	LCDIF.DATA[21]		Always
135	GPIO1.IO[11]	USDHC3.LCTL	ENET1.MDC	UART3.CTS_B	I2C4.SDA	FLEXTIMER1.PHB	KPP.ROW[6]	PWM4.OUT		Always
136		SIM2.PORT1_TRXD	QSPI.B_SCLK	UART7.TX	WEIM.WAIT	GPIO2.IO[13]	LCDIF.DATA[13]	LCDIF.CS		Always
137	SAI2.TX_BCLK	ECSPI3.MOSI	UART4.TX	UART1.RTS_B	FLEXTIMER2.CH[5]	GPIO6.IO[20]				not "WAB"
138		SIM2.PORT1_CLK	QSPI.B_SS0_B	UART7.RTS_B	WEIM.EB_B[0]	GPIO2.IO[14]	LCDIF.DATA[14]	LCDIF.DATA[22]		Always
139	SAI2.TX_DATA[0]	ECSPI3.SS0	UART4.RTS_B	UART2.RTS_B	FLEXTIMER2.CH[7]	GPIO6.IO[22]	KPP.ROW[7]			not "WAB"
140		SIM2.PORT1_RST_B	QSPI.B_SS1_B	UART7.CTS_B	WEIM.CS1_B	GPIO2.IO[15]	LCDIF.DATA[15]	LCDIF.WR_RWN		Always
142	LCDIF.DATA[18]	FLEXTIMER1.CH[6]	CORESIGHT.EVENTO	CSI1.DATA[15]	WEIM.CS2_B	GPIO3.IO[23]	SRC.BT_CFG[18]			Always
143	SAI2.RX_DATA[0]	ECSPI3.SCLK	UART4.CTS_B	UART2.CTS_B	FLEXTIMER2.CH[6]	GPIO6.IO[21]	KPP.COL[7]			not "WAB"
144	LCDIF.DATA[19]	FLEXTIMER1.CH[7]		CSI1.DATA[14]	WEIM.CS3_B	GPIO3.IO[24]	SRC.BT_CFG[19]			Always
145	SAI2.TX_SYNC	ECSPI3.MISO	UART4.RX	UART1.CTS_B	FLEXTIMER2.CH[4]	GPIO6.IO[19]				not "WAB"
146	LCDIF.DATA[20]	FLEXTIMER2.CH[4]	ENET1.1588_EVENT2_OUT	CSI1.DATA[13]	WEIM.ADDR[23]	GPIO3.IO[25]	I2C3.SCL			Always
147	USDHC2.CMD	SAI2.RX_BCLK	MQS.LEFT	GPT4.CAPTURE1	SIM2.PORT1_TRXD	GPIO5.IO[13]				not "W" and not "WAB"
148	LCDIF.DATA[21]	FLEXTIMER2.CH[5]	ENET1.1588_EVENT3_OUT	CSI1.DATA[12]	WEIM.ADDR[24]	GPIO3.IO[26]	I2C3.SDA			Always
149	USDHC2.DATA3	SAI2.TX_DATA[0]	UART4.RTS_B	GPT4.COMPARE3	SIM2.PORT1_PD	GPIO5.IO[17]				not "W" and not "WAB"
151	USDHC2.DATA2	SAI2.TX_SYNC	UART4.CTS_B	GPT4.COMPARE2	SIM2.PORT1_SVEN	GPIO5.IO[16]				not "W" and not "WAB"
152		FLEXTIMER2.PHB			WEIM.EB_B[1]	GPIO2.IO[31]	LCDIF.VSYNC	LCDIF.DATA[12]		not "C1000D"
152		FLEXTIMER2.PHB	ENET2.COL		WEIM.EB_B[1]	GPIO2.IO[31]	LCDIF.VSYNC	LCDIF.DATA[12]		"C1000D"
153	USDHC2.DATA1	SAI2.TX_BCLK	UART4.TX	GPT4.COMPARE1	SIM2.PORT1_RST_B	GPIO5.IO[15]				not "W" and not "WAB"
154	LCDIF.DATA[7]		CORESIGHT.TRACE[7]	CSI1.MCLK	WEIM.DATA[7]	GPIO3.IO[12]	SRC.BT_CFG[7]			Always
155	USDHC2.DATA0	SAI2.RX_DATA[0]	UART4.RX	GPT4.CAPTURE2	SIM2.PORT1_CLK	GPIO5.IO[14]				not "W" and not "WAB"
157	USDHC2.CLK	SAI2.RX_SYNC	MQS.RIGHT	GPT4.CLK		GPIO5.IO[12]				not "W" and not "WAB"
161	LCDIF.DATA[8]		CORESIGHT.TRACE[8]	CSI1.DATA[9]	WEIM.DATA[8]	GPIO3.IO[13]	SRC.BT_CFG[8]			Always
163	LCDIF.DATA[9]		CORESIGHT.TRACE[9]	CSI1.DATA[8]	WEIM.DATA[9]	GPIO3.IO[14]	SRC.BT_CFG[9]			Always
179	USDHC1.RESET_B	SAI3.MCLK	UART6.RTS_B	ECSPI4.SCLK	FLEXTIMER1.CH[2]	GPIO5.IO[2]				Always
187	UART3.CTS_B		SAI3.TX_SYNC		ENET1.1588_EVENT1_OUT	GPIO4.IO[7]				not "C1000D" and not "WAB"
187	UART3.CTS_B	USB.OTG2_PWR	SAI3.TX_SYNC		ENET1.1588_EVENT1_OUT	GPIO4.IO[7]				"C1000D" and not "WAB"
191	ENET1.CRS	WDOG2.WDOG_RST_B_DEB	SAI1.TX_SYNC	GPT2.CAPTURE1		GPIO7.IO[14]	CCM.EXT_CLK3			not "A"
193	ENET1.TX_CLK	CCM.ENET1_REF_CLK_ROOT	SAI1.RX_DATA[0]	GPT2.COMPARE3		GPIO7.IO[12]	CCM.EXT_CLK1			not "A"
194				CCM.ENET2_REF_CLK_ROOT	WEIM.ADDR[22]	GPIO2.IO[28]	LCDIF.CS	LCDIF.DATA[7]		not "C1000D"
194			ENET2.TX_CLK	CCM.ENET2_REF_CLK_ROOT	WEIM.ADDR[22]	GPIO2.IO[28]	LCDIF.CS	LCDIF.DATA[7]		"C1000D"
197	ENET1.COL	WDOG.GLOBAL	SAI1.TX_DATA[0]	GPT2.CAPTURE2		GPIO7.IO[15]	CCM.EXT_CLK4			not "A"
198	UART3.RTS_B		SAI3.TX_DATA[0]		ENET1.1588_EVENT1_IN	GPIO4.IO[6]				not "C1000D" and not "WAB"
198	UART3.RTS_B	USB.OTG2_OC	SAI3.TX_DATA[0]		ENET1.1588_EVENT1_IN	GPIO4.IO[6]				"C1000D" and not "WAB"
199	ENET1.RX_CLK	WDOG2.WDOG_B	SAI1.TX_BCLK	GPT2.CLK		GPIO7.IO[13]	CCM.EXT_CLK2			not "A"
200	GPIO1.IO[5]	USB.OTG1_PWR	FLEXTIMER1.CH[5]	UART5.RTS_B	I2C1.SDA					not "L"
201	SAI1.RX_SYNC		SAI2.RX_SYNC	I2C4.SCL	SIM1.PORT1_PD	GPIO6.IO[16]	MQS.RIGHT			not "A"
203	SAI1.RX_BCLK		SAI2.RX_BCLK	I2C4.SDA	FLEXTIMER2.PHA	GPIO6.IO[17]	MQS.LEFT			not "A"

5.6 RTC

The CL-SOM-iMX7 RTC is implemented with the internal RTC of the i.MX7 SoC. The RTC provides time and calendar information. Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. The backup battery should be connected to the VCC_RTC power input.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

5.7 LED

The CL-SOM-iMX7 features a single general purpose green LED controlled by GPIO6_14 signal of the i.MX7. The LED is ON when GPIO6_14 is logic High.

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX7 CoM/SoM carrier board interface uses the SODIMM-204 edge connector. The SoM pinout is detailed in the table below

6.1 Connector Pinout

Table 70 Connector P1

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
1	GND	5.1	2	N.C. – leave unconnected	
3	LCDIF.ENABLE ECSPI4.MOSI CSI1.DATA[17] UART2.TX GPIO3.IO[1]	4.1 4.18 4.4 4.16 4.29	4	PWM2.OUT I2C3.SDA UART1.RTS_B GPIO7.IO[1] KPP.COL[3] ETH1_LED_ACT	4.23 4.17 4.16 4.29 4.27 4.6
5	LCDIF.CLK ECSPI4.MISO CSI1.DATA[16] UART2.RX GPIO3.IO[0]	4.1 4.18 4.4 4.16 4.29	6	SAI1.RX_SYNC GPT2.COMPARE1 GPIO7.IO[10] ETH1_MDI0N	4.9 4.24 4.29 4.6
7	LCDIF.HSYNC ECSPI4.SCLK CSI1.DATA[18] UART2.RTS_B GPIO3.IO[2]	4.1 4.18 4.4 4.16 4.29	8	SAI1.RX_BCLK GPT2.COMPARE2 GPIO7.IO[11] ETH1_MDI0P	4.9 4.24 4.29 4.6
9	LCDIF.VSYNC ECSPI4.SS0 CSI1.DATA[19] UART2.CTS_B GPIO3.IO[3]	4.1 4.18 4.4 4.16 4.29	10	VSYS	5.1
11	I2C4.SDA UART5.TX WDOG4.WDOG_RST_B_DEB CSI1.MCLK USB.OTG2_ID GPIO4.IO[15]	4.17 4.16 4.25 4.4 4.11 4.29	12	PWM4.OUT ECSPI2.RDY GPIO7.IO[7] KPP.COL[0] ETH1_MDI1N	4.23 4.18 4.29 4.27 4.6
13	I2C4.SCL UART5.RX WDOG4.WDOG_B CSI1.PIXCLK USB.OTG1_ID GPIO4.IO[14]	4.17 4.16 4.25 4.4 4.11 4.29	14	CAN2.TX ECSPI2.SS0 I2C4.SDA GPIO7.IO[9] ETH1_MDI1P	4.20 4.18 4.17 4.29 4.6
15	I2C3.SDA UART5.RTS_B CAN2.TX CSI1.HSYNC SDMA.EXT_EVENT[1] GPIO4.IO[13]	4.17 4.16 4.20 4.4 5.2.2 4.29	16	PWM3.OUT ECSPI2.SS3 GPIO7.IO[6] KPP.ROW[0] ETH1_LED1_SPD	4.23 4.18 4.29 4.27 4.6
17	I2C3.SCL UART5.CTS_B CAN2.RX CSI1.VSYNC SDMA.EXT_EVENT[0] GPIO4.IO[12]	4.17 4.16 4.20 4.4 5.2.2 4.29	18	CAN1.RX ECSPI2.SCLK UART1.RX GPIO7.IO[2] KPP.ROW[2] ETH1_MDI2N	4.20 4.18 4.16 4.29 4.27 4.6
19	GND	5.1	20	CAN1.TX ECSPI2.MOSI UART1.TX GPIO7.IO[3] KPP.COL[2] ETH1_MDI2P	4.20 4.18 4.16 4.29 4.27 4.6
21	MIPI_CSI_D0_P	4.5	22	PWM1.OUT I2C3.SCL UART1.CTS_B GPIO7.IO[0] KPP.ROW[3] ETH1_LED3	4.23 4.17 4.16 4.29 4.27 4.6

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
23	MIPI_CSI_D0_N	4.5	24	ECSPI2.SS2 GPIO7.IO[5] KPP.COL[1] ETH1_MDI3N	4.18 4.29 4.27 4.6
25	FLEXTIMER2.CH[2] WEIM.ADDR[20] GPIO2.IO[26] LCDIF.RD_E LCDIF.DATA[19] ETH2_LINK-LED_ACT	4.26 4.14 4.29 4.1 4.1 4.6	26	ECSPI2.SS1 GPIO7.IO[4] KPP.ROW[1] ETH1_MDI3P	4.18 4.29 4.27 4.6
27	MIPI_CSI_D1_P	4.5	28	VSYS	5.1
29	MIPI_CSI_D1_N	4.5	30	SIM2.PORT1_PD KPP.ROW[6] WEIM.ADDR[17] GPIO2.IO[23] ETH2_MDI0N LCDIF.DATA[2] LCDIF.DATA[22]	4.28 4.27 4.14 4.29 4.6 4.1 4.1
31	FLEXTIMER1.CH[3] WEIM.AD[15] GPIO2.IO[21] LCDIF.DATA[20] LCDIF.DATA[4]	4.26 4.14 4.29 4.1 4.1	32	SIM2.PORT1_SVEN KPP.COL[6] WEIM.ADDR[16] GPIO2.IO[22] ETH2_MDI0P LCDIF.DATA[21] LCDIF.DATA[3]	4.28 4.27 4.14 4.29 4.6 4.1 4.1
33	LVDS_CLKP MIPI_DSI_D0_P	4.3 4.2	34	LCDIF.DATA[10] FLEXTIMER1.CH[1] KPP.ROW[5] WEIM.AD[13] GPIO2.IO[19] ETH2_LED_LINK10_100 LCDIF.DATA[18]	4.1 4.26 4.27 4.14 4.29 4.6 4.1
35	LVDS_CLKN MIPI_DSI_D0_N	4.3 4.2	36	FLEXTIMER2.CH[1] KPP.ROW[7] WEIM.ADDR[19] GPIO2.IO[25] ETH2_MDI1N LCDIF.DATA[18] LCDIF.WR_RWN	4.26 4.27 4.14 4.29 4.6 4.1 4.1
37	GND	5.1	38	FLEXTIMER2.CH[0] KPP.COL[7] WEIM.ADDR[18] GPIO2.IO[24] ETH2_MDI1P LCDIF.DATA[16] LCDIF.DATA[23]	4.26 4.27 4.14 4.29 4.6 4.1 4.1
39	LVDS_TX0P MIPI_DSI_D1_P	4.3 4.2	40	LCDIF.BUSY FLEXTIMER2.CH[3] WEIM.ADDR[21] GPIO2.IO[27] ETH2_LINK-LED_1000 LCDIF.DATA[17]	4.1 4.26 4.14 4.29 4.6 4.1
41	LVDS_TX0N MIPI_DSI_D1_N	4.3 4.2	42	LCDIF.CLK SIM2.PORT2_SVEN KPP.ROW[4] WEIM.AD[10] GPIO2.IO[16] ETH2_MDI2N LCDIF.DATA[20]	4.1 4.28 4.27 4.14 4.29 4.6 4.1
43	GPIO1.IO[8] WDOG1.WDOG_B UART3.RX I2C3.SCL KPP.COL[5] PWM1.OUT	4.29 4.25 4.16 4.17 4.27 4.23	44	FLEXTIMER1.CH[2] WEIM.AD[14] GPIO2.IO[20] ETH2_MDI2P LCDIF.DATA[19] LCDIF.DATA[5]	4.26 4.14 4.29 4.6 4.1 4.1
45	LVDS_TX1P MIPI_DSI_CLK_P	4.3 4.2	46	VSYS	5.1

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
47	LVDS_TX1N MIPI_DSI_CLK_N	4.3 4.2	48	FLEXTIMER1.CH[0] KPP.COL[5] WEIM.AD[12] GPIO2.IO[18] ETH2_MDI3N LCDIF.DATA[17] LCDIF.DATA[23]	4.26 4.27 4.14 4.29 4.6 4.1 4.1
49	GPIO1.IO[9] USDHC1.LCTL CCM.ENET3_REF_CLK_ROOT UART3.TX I2C3.SDA KPP.ROW[5] PWM2.OUT	4.29 4.15 5.2.3 4.16 4.17 4.27 4.23	50	SIM2.PORT2_PD KPP.COL[4] WEIM.AD[11] GPIO2.IO[17] ETH2_MDI3P LCDIF.DATA[16] LCDIF.DATA[8]	4.28 4.27 4.14 4.29 4.6 4.1 4.1
51	LVDS_TX2P	4.3	52	USDHC2.WP ECSPI3.SS3 GPIO5.IO[10] SDMA.EXT_EVENT[1] USB.OTG1_ID	4.15 4.18 4.29 5.2.2 4.11
53	LVDS_TX2N	4.3	54	LCDIF.DATA[10] CSI1.DATA[7] WEIM.DATA[10] GPIO3.IO[15]	4.1 4.4 4.14 4.29
55	GND	5.1	56	LCDIF.DATA[11] CSI1.DATA[6] WEIM.DATA[11] GPIO3.IO[16]	4.1 4.4 4.14 4.29
57	LVDS_TX3P	4.3	58	UART4.TX WDOG3.WDOG_RST_B_DEB ECSPI3.SS0 CCM.ENET3_REF_CLK_ROOT GPIO4.IO[11]	4.16 4.25 4.18 5.2.3 4.29
59	LVDS_TX3N	4.3	60	WEIM.AD[8] GPIO2.IO[29] LCDIF.DATA[6] LCDIF.ENABLE	4.14 4.29 4.1 4.1
61	USDHC1.CD_B UART6.RX ECSPI4.MISO FLEXTIMER1.CH[0] GPIO5.IO[0] CCM.CLKO1	4.15 4.16 4.18 4.26 4.29 5.2.3	62	GPIO7.IO[8] CAN2.RX ECSPI2.MISO I2C4.SCL	4.29 4.20 4.18 4.17
63	I2C1.SCL UART4.CTS_B CAN1.RX ECSPI3.MISO GPIO4.IO[8]	4.17 4.16 4.20 4.18 4.29	64	VSYS	5.1
65	I2C1.SDA UART4.RTS_B CAN1.TX ECSPI3.MOSI CCM.ENET1_REF_CLK_ROOT GPIO4.IO[9]	4.17 4.16 4.20 4.18 5.2.3 4.29	66	ADC2_IN0 RTOUCH_X+	4.21 4.22
67	USDHC1.WP UART6.TX ECSPI4.MOSI FLEXTIMER1.CH[1] GPIO5.IO[1] CCM.CLKO2	4.15 4.16 4.18 4.26 4.29 5.2.3	68	ADC2_IN1 RTOUCH_X-	4.21 4.22
69	UART4.RX WDOG3.WDOG_B ECSPI3.SCLK CCM.ENET2_REF_CLK_ROOT GPIO4.IO[10]	4.16 4.25 4.18 5.2.3 4.29	70	ADC2_IN2 RTOUCH_Y+	4.21 4.22
71	GND	5.1	72	ADC2_IN3 RTOUCH_Y-	4.21 4.22
73	GPIO1.IO[2] PWM2.OUT CCM.ENET1_REF_CLK_ROOT SAI2.MCLK USB.OTG1_ID CCM.CLKO1	4.29 4.23 5.2.3 4.9 4.11 5.2.3	74	LCDIF.DATA[22] FLEXTIMER2.CH[6] WEIM.ADDR[25] CSI1.DATA[11] I2C4.SCL GPIO3.IO[27]	4.1 4.26 4.14 4.4 4.17 4.29

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
75	FLEXTIMER2.PHA WEIM.AD[9] GPIO2.IO[30] LCDIF.HSYNC LCDIF.DATA[11]	4.26 4.14 4.29 4.1 4.1	76	LCDIF.DATA[23] FLEXTIMER2.CH[7] CSI1.DATA[10] WEIM.ADDR[26] GPIO3.IO[28] I2C4.SDA	4.1 4.26 4.4 4.14 4.29 4.17
77	CSI1.DATA[4] GPIO3.IO[18] LCDIF.DATA[13] WEIM.DATA[13]	4.4 4.29 4.1 4.14	78	VSYS	5.1
79	CSI1.DATA[5] GPIO3.IO[17] LCDIF.DATA[12] WEIM.DATA[12]	4.4 4.29 4.1 4.14	80	USDHC1.CLK SAI3.RX_SYNC UART6.CTS_B ECSPI4.SS0 FLEXTIMER1.CH[3] GPIO5.IO[3]	4.15 4.9 4.16 4.18 4.26 4.29
81	GPIO1.IO[3] PWM3.OUT CCM.ENET2_REF_CLK_ROOT SAI3.MCLK USB.OTG2_ID CCM.CLKO2	4.29 4.23 5.2.3 4.9 4.11 5.2.3	82	USDHC1.CMD SAI3.RX_BCLK ECSPI4.SS1 FLEXTIMER2.CH[0] GPIO5.IO[4]	4.15 4.9 4.18 4.26 4.29
83	CSI1.DATA[6] ECSPI2.SCLK GPIO4.IO[20] LCDIF.DATA[13] UART7.RX USDHC1.DATA4	4.4 4.18 4.29 4.1 4.16 4.15	84	USDHC1.DATA0 SAI3.RX_DATA[0] UART7.RX ECSPI4.SS2 FLEXTIMER2.CH[1] GPIO5.IO[5] CCM.EXT_CLK1	4.15 4.9 4.16 4.18 4.26 4.29 5.2.3
85	ECSPI2.MOSI UART7.TX USDHC1.DATA5 CSI1.DATA[7] LCDIF.DATA[14] GPIO4.IO[21]	4.18 4.16 4.15 4.4 4.1 4.29	86	USDHC1.DATA1 SAI3.TX_BCLK UART7.TX CCM.EXT_CLK2 FLEXTIMER2.CH[2] GPIO5.IO[6] ECSPI4.SS3	4.15 4.9 4.16 5.2.3 4.26 4.29 4.18
87	GND	5.1	88	USDHC1.DATA2 SAI3.TX_SYNC UART7.CTS_B ECSPI4.RDY FLEXTIMER2.CH[3] GPIO5.IO[7] CCM.EXT_CLK3	4.15 4.9 4.16 4.18 4.26 4.29 4.18
89	LCDIF.DATA[15] CSI1.DATA[2] WEIM.DATA[15] GPIO3.IO[20]	4.1 4.4 4.14 4.29	90	USDHC1.DATA3 SAI3.TX_DATA[0] UART7.RTS_B ECSPI3.SS1 FLEXTIMER1.PHA GPIO5.IO[8] CCM.EXT_CLK4	4.15 4.9 4.16 4.18 4.26 4.29 4.18
91	LCDIF.DATA[14] CSI1.DATA[3] WEIM.DATA[14] GPIO3.IO[19]	4.1 4.4 4.14 4.29	92	LCDIF.DATA[17] FLEXTIMER1.CH[5] CSI1.DATA[0] WEIM.ACLK_FREERUN GPIO3.IO[22]	4.1 4.26 4.4 4.14 4.29
93	GPIO1.IO[1] PWM1.OUT CCM.ENET3_REF_CLK_ROOT SAI1.MCLK	4.29 4.23 5.2.3 4.9	94	LCDIF.DATA[16] FLEXTIMER1.CH[4] CSI1.DATA[1] WEIM.CRE GPIO3.IO[21]	4.1 4.26 4.4 4.14 4.29
95	LCDIF.DATA[6] CSI1.PIXCLK WEIM.DATA[6] GPIO3.IO[11]	4.1 4.4 4.14 4.29	96	VSYS	5.1
97	USDHC2.CD_B ECSPI3.SS2 FLEXTIMER1.PHB GPIO5.IO[9] SDMA.EXT_EVENT[0]	4.15 4.18 4.26 4.29 5.2.2	98	SIM1.PORT2_TRXD KPP.ROW[3] WEIM.AD[0] GPIO2.IO[0] LCDIF.DATA[0] QSPI.A_DATA[0] LCDIF.CLK	4.28 4.27 4.14 4.29 4.1 4.19 4.1

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
99	LCDIF.RESET GPT1.COMPARE1 CSI1.FIELD WEIM.DTACK_B GPIO3.IO[4]	4.1 4.24 4.4 4.14 4.29	100	SIM1.PORT2_SVEN WEIM.AD[3] KPP.COL[2] QSPI.A_DATA[3] GPIO2.IO[3] LCDIF.DATA[3] LCDIF.HSYNC	4.28 4.14 4.27 4.19 4.29 4.1 4.1
101	PCIE_REFCLKIN_N	4.13	102	KPP.ROW[2] WEIM.AD[2] SIM1.PORT2_RST_B GPIO2.IO[2] LCDIF.DATA[2] LCDIF.VSYNC QSPI.A_DATA[2]	4.27 4.14 4.28 4.29 4.1 4.1 4.19
103	PCIE_REFCLKIN_P	4.13	104	WEIM.AD[1] SIM1.PORT2_CLK KPP.COL[3] GPIO2.IO[1] LCDIF.DATA[1] LCDIF.ENABLE QSPI.A_DATA[1]	4.14 4.28 4.27 4.29 4.1 4.1 4.19
105	GND	5.1	106	LCDIF.DATA[0] GPT1.COMPARE2 CSI1.DATA[20] GPIO3.IO[5] WEIM.DATA[0]	4.1 4.24 4.4 4.29 4.14
107	ECSPI2.MISO UART7.RTS_B USDHC1.DATA6 CSI1.DATA[8] LCDIF.DATA[15] GPIO4.IO[22]	4.18 4.16 4.15 4.4 4.1 4.29	108	LCDIF.DATA[1] GPT1.COMPARE3 WEIM.DATA[1] CSI1.DATA[21] GPIO3.IO[6]	4.1 4.24 4.14 4.4 4.29
109	ECSPI2.SS0 UART7.CTS_B USDHC1.DATA7 CSI1.DATA[9] LCDIF.RESET GPIO4.IO[23]	4.18 4.16 4.15 4.4 4.1 4.29	110	LCDIF.DATA[2] GPT1.CLK CSI1.DATA[22] WEIM.DATA[2] GPIO3.IO[7]	4.1 4.24 4.4 4.14 4.29
111	UART1.TX I2C1.SDA SAI3.MCLK GPIO4.IO[1]	4.16 4.17 4.9 4.29	112	LCDIF.DATA[3] WEIM.DATA[3] GPT1.CAPTURE1 CSI1.DATA[23] GPIO3.IO[8]	4.1 4.14 4.24 4.4 4.29
113	LCDIF.DATA[4] GPT1.CAPTURE2 CSI1.VSYNC WEIM.DATA[4] GPIO3.IO[9]	4.1 4.24 4.4 4.14 4.29	114	VSYS	5.1
115	LCDIF.DATA[5] CSI1.HSYNC WEIM.DATA[5] GPIO3.IO[10]	4.1 4.4 4.14 4.29	116	SIM1.PORT2_PD KPP.ROW[1] GPIO2.IO[4] WEIM.AD[4] LCDIF.DATA[4] QSPI.A_DQS	4.28 4.27 4.29 4.14 4.1 4.19
117	UART1.RX I2C1.SCL GPIO4.IO[0]	4.16 4.17 4.29	118	KPP.COL[1] SIM2.PORT2_TRXD WEIM.AD[5] GPIO2.IO[5] LCDIF.DATA[5] QSPI.A_SCLK	4.27 4.28 4.14 4.29 4.1 4.19
119	PCIE_REFCLKOUT_P	4.13	120	SIM2.PORT2_CLK KPP.ROW[0] WEIM.AD[6] GPIO2.IO[6] LCDIF.DATA[6] QSPI.A_SS0_B	4.28 4.27 4.14 4.29 4.1 4.19
121	PCIE_REFCLKOUT_N	4.13	122	SIM2.PORT2_RST_B KPP.COL[0] WEIM.AD[7] GPIO2.IO[7] LCDIF.DATA[7] QSPI.A_SS1_B	4.28 4.27 4.14 4.29 4.1 4.19

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
123	GND	5.1	124	WEIM.OE SIM1.PORT1_TRXD UART6.RX LCDIF.DATA[8] GPIO2.IO[8] LCDIF.BUSY QSPI.B_DATA[0]	4.14 4.28 4.16 4.1 4.29 4.1 4.19
125	PCIE_TX_P	4.13	126	SIM1.PORT1_CLK UART6.TX WEIM.RW GPIO2.IO[9] LCDIF.DATA[0] LCDIF.DATA[9] QSPI.B_DATA[1]	4.28 4.16 4.14 4.29 4.1 4.1 4.19
127	PCIE_TX_N	4.13	128	WEIM.CS0_B SIM1.PORT1_RST_B UART6.RTS_B LCDIF.DATA[10] LCDIF.DATA[9] QSPI.B_DATA[2] GPIO2.IO[10]	4.14 4.28 4.16 4.1 4.1 4.19 4.29
129	GPIO1.IO[10] USDHC2.LCTL UART3.RTS_B I2C4.SCL FLEXTIMER1.PHA KPP.COL[6] PWM3.OUT	4.29 4.15 4.16 4.17 4.26 4.27 4.23	130	UART6.CTS_B SIM1.PORT1_SVEN WEIM.BCLK GPIO2.IO[11] LCDIF.DATA[11] LCDIF.DATA[1] QSPI.B_DATA[3]	4.16 4.28 4.14 4.29 4.1 4.1 4.19
131	PCIE_RX_P	4.13	132	VSYS	5.1
133	PCIE_RX_N	4.13	134	LCDIF.DATA[21] GPIO2.IO[12] LCDIF.DATA[12] SIM1.PORT1_PD UART7.RX WEIM.LBA_B QSPI.B_DQS	4.1 4.29 4.1 4.28 4.16 4.14 4.19
135	GPIO1.IO[11] UART3.CTS_B I2C4.SDA FLEXTIMER1.PHB KPP.ROW[6] PWM4.OUT	4.29 4.16 4.17 4.26 4.27 4.23	136	GPIO2.IO[13] LCDIF.CS LCDIF.DATA[13] SIM2.PORT1_TRXD QSPI.B_SCLK UART7.TX WEIM.WAIT	4.29 4.1 4.1 4.28 4.19 4.16 4.14
137	SAI2.TX_BCLK ECSPI3.MOSI UART4.TX UART1.RTS_B FLEXTIMER2.CH[5] GPIO6.IO[20]	4.9 4.18 4.16 4.16 4.26 4.29	138	SIM2.PORT1_CLK UART7.RTS_B WEIM.EB_B[0] QSPI.B_SS0_B GPIO2.IO[14] LCDIF.DATA[14] LCDIF.DATA[22]	4.28 4.16 4.14 4.19 4.29 4.1 4.1
139	SAI2.TX_DATA[0] ECSPI3.SS0 UART4.RTS_B UART2.RTS_B FLEXTIMER2.CH[7] GPIO6.IO[22] KPP.ROW[7]	4.9 4.18 4.16 4.16 4.26 4.29 4.27	140	SIM2.PORT1_RST_B UART7.CTS_B WEIM.CS1_B LCDIF.DATA[15] LCDIF.WR_RWN QSPI.B_SS1_B GPIO2.IO[15]	4.28 4.16 4.14 4.1 4.1 4.19 4.29
141	GND	5.1	142	LCDIF.DATA[18] FLEXTIMER1.CH[6] CSI1.DATA[15] WEIM.CS2_B GPIO3.IO[23]	4.1 4.26 4.4 4.14 4.29
143	SAI2.RX_DATA[0] ECSPI3.SCLK UART4.CTS_B UART2.CTS_B FLEXTIMER2.CH[6] GPIO6.IO[21] KPP.COL[7]	4.9 4.18 4.16 4.16 4.26 4.29 4.27	144	LCDIF.DATA[19] FLEXTIMER1.CH[7] CSI1.DATA[14] WEIM.CS3_B GPIO3.IO[24]	4.1 4.26 4.4 4.14 4.29

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
145	SAI2.TX_SYNC ECSPI3.MISO UART4.RX UART1.CTS_B FLEXTIMER2.CH[4] GPIO6.IO[19]	4.9 4.18 4.16 4.16 4.26 4.29	146	LCDIF.DATA[20] FLEXTIMER2.CH[4] CSI1.DATA[13] WEIM.ADDR[23] GPIO3.IO[25] I2C3.SCL	4.1 4.26 4.4 4.14 4.29 4.17
147	USDHC2.CMD SAI2.RX_BCLK MQS.LEFT GPT4.CAPTURE1 SIM2.PORT1_TRXD GPIO5.IO[13]	4.15 4.9 4.10 4.24 4.28 4.29	148	LCDIF.DATA[21] FLEXTIMER2.CH[5] CSI1.DATA[12] WEIM.ADDR[24] GPIO3.IO[26] I2C3.SDA	4.1 4.26 4.4 4.14 4.29 4.17
149	USDHC2.DATA3 SAI2.TX_DATA[0] UART4.RTS_B GPT4.COMPARE3 SIM2.PORT1_PD GPIO5.IO[17]	4.15 4.9 4.16 4.24 4.28 4.29	150	VSYS	5.1
151	USDHC2.DATA2 SAI2.TX_SYNC UART4.CTS_B GPT4.COMPARE2 SIM2.PORT1_SVEN GPIO5.IO[16]	4.15 4.9 4.16 4.24 4.28 4.29	152	FLEXTIMER2.PHB GPIO2.IO[31] LCDIF.DATA[12] LCDIF.VSYNC WEIM.EB_B[1]	4.26 4.29 4.1 4.1 4.14
153	USDHC2.DATA1 SAI2.TX_BCLK UART4.TX GPT4.COMPARE1 SIM2.PORT1_RST_B GPIO5.IO[15]	4.15 4.9 4.16 4.24 4.28 4.29	154	LCDIF.DATA[7] CSI1.MCLK WEIM.DATA[7] GPIO3.IO[12]	4.1 4.4 4.14 4.29
155	USDHC2.DATA0 SAI2.RX_DATA[0] UART4.RX GPT4.CAPTURE2 SIM2.PORT1_CLK GPIO5.IO[14]	4.15 4.9 4.16 4.24 4.28 4.29	156	VBUS_EN_REQ	4.12
157	USDHC2.CLK SAI2.RX_SYNC MQS.RIGHT GPT4.CLK GPIO5.IO[12]	4.15 4.9 4.10 4.24 4.29	158	USB_H2_DN	4.12
159	GND	5.1	160	USB_H2_DP	4.12
161	LCDIF.DATA[8] CSI1.DATA[9] WEIM.DATA[8] GPIO3.IO[13]	4.1 4.4 4.14 4.29	162	VBUS_NOVERCURRENT	4.12
163	LCDIF.DATA[9] CSI1.DATA[8] WEIM.DATA[9] GPIO3.IO[14]	4.1 4.4 4.14 4.29	164	USB_H1_DN	4.12
165	ONOFF	5.2.1	166	USB_H1_DP	4.12
167	ADC1_IN0	4.21	168	VSYS	5.1
169	ADC1_IN1	4.21	170	USB_OTG2_DN	4.11
171	COLD_RESET_IN	5.3	172	USB_OTG2_DP	4.11
173	ADC1_IN2	4.21	174	USB_OTG1_ID	4.11
175	ADC1_IN3	4.21	176	USB_OTG1_DP	4.11
177	GND	5.1	178	USB_OTG1_DN	4.11
179	USDHC1.RESET_B SAI3.MCLK UART6.RTS_B ECSPI4.SCLK FLEXTIMER1.CH[2] GPIO5.IO[2]	4.15 4.9 4.16 4.18 4.26 4.29	180	USB_OTG1_VBUS	4.11
181	PMIC_STBY_REQ	5.2.1	182	MIPI_CSI_CLK_P	4.5
183	VCC_RTC	5.1	184	MIPI_CSI_CLK_N	4.5
185	ALT_BOOT	5.4	186	VSYS	5.1
187	UART3.CTS_B USB.OTG2_PWR SAI3.TX_SYNC GPIO4.IO[7]	4.16 4.11 4.9 4.29	188	USB_H3_DP	4.12
189	EEPROM_WP	5.2.4	190	USB_H3_DN	4.12

Pin #	CL-SOM-iMX7 Signal Name	Ref.	Pin #	CL-SOM-iMX7 Signal Name	Ref.
191	WDOG2.WDOG_RST_B_DEB SAI1.TX_SYNC GPT2.CAPTURE1 GPIO7.IO[14] CCM.EXT_CLK3 MICBIAS	4.25 4.9 4.24 4.29 5.2.3 4.8	192	USB_OTG1_CHD_B	4.11
193	CCM.ENET1_REF_CLK_ROOT SAI1.RX_DATA[0] GPT2.COMPARE3 GPIO7.IO[12] CCM.EXT_CLK1 MICIN	5.2.3 4.9 4.24 4.29 5.2.3 4.8	194	CCM.ENET2_REF_CLK_ROOT WEIM.ADDR[22] GPIO2.IO[28] LCDIF.CS LCDIF.DATA[7]	5.2.3 4.14 4.29 4.1 4.1
195	GND	5.1	196	USB_OTG2_VBUS	4.11
197	WDOG.GLOBAL SAI1.TX_DATA[0] GPT2.CAPTURE2 GPIO7.IO[15] CCM.EXT_CLK4 RLINEIN	4.25 4.9 4.24 4.29 5.2.3 4.8	198	UART3.RTS_B USB.OTG2_OC GPIO4.IO[6] SAI3.TX_DATA[0]	4.16 4.11 4.29 4.9
199	WDOG2.WDOG_B SAI1.TX_BCLK GPT2.CLK GPIO7.IO[13] CCM.EXT_CLK2 LLINEIN	4.25 4.9 4.24 4.29 5.2.3 4.8	200	GPIO1.IO[5] USB.OTG1_PWR FLEXTIMER1.CH[5] I2C1.SDA UART5.RTS_B	4.29 4.11 4.26 4.17 4.16
201	SAI1.RX_SYNC SAI2.RX_SYNC I2C4.SCL SIM1.PORT1_PD GPIO6.IO[16] MQS.RIGHT RHPOUT	4.9 4.9 4.17 4.28 4.29 4.10 4.8	202	PMIC_ON_REQ	5.2.1
203	SAI1.RX_BCLK SAI2.RX_BCLK I2C4.SDA FLEXTIMER2.PHA GPIO6.IO[17] MQS.LEFT LHPOUT	4.9 4.9 4.17 4.26 4.29 4.10 4.8	204	VSYS	5.1

6.2 Mating Connectors

Table 71 Connector type

CL-SOM-iMX7 connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 3 CL-SOM-iMX7 Top

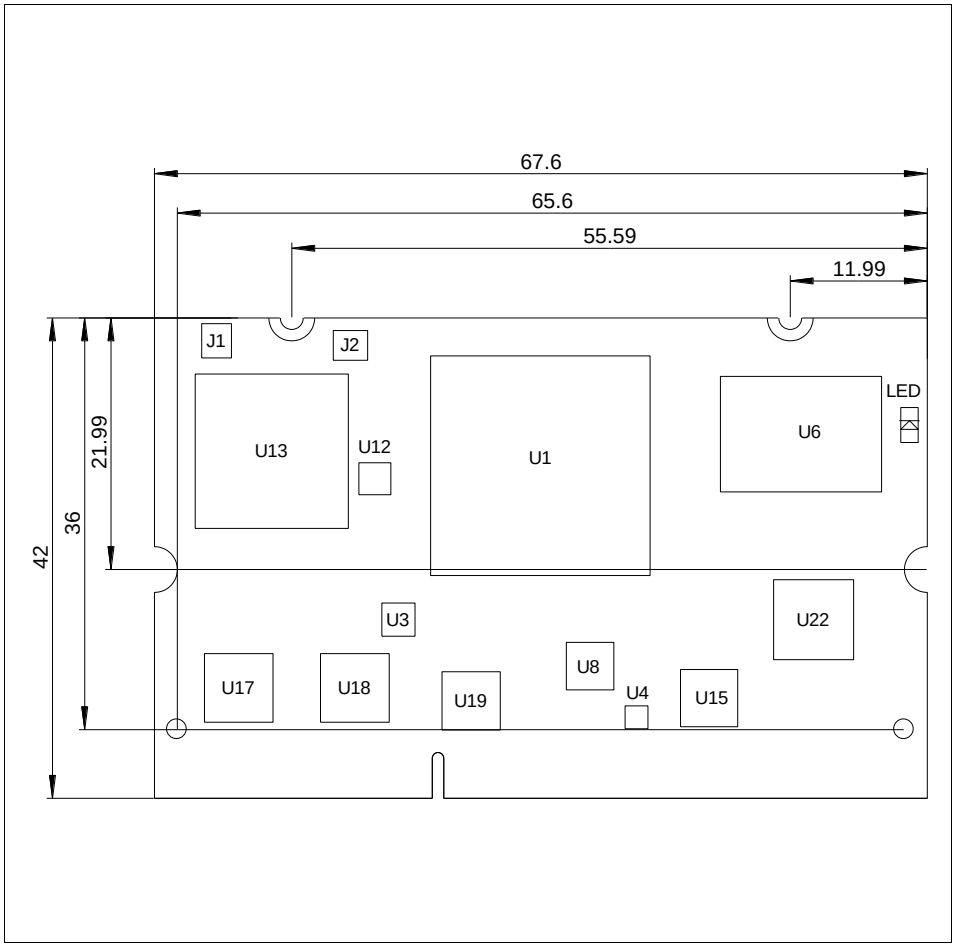
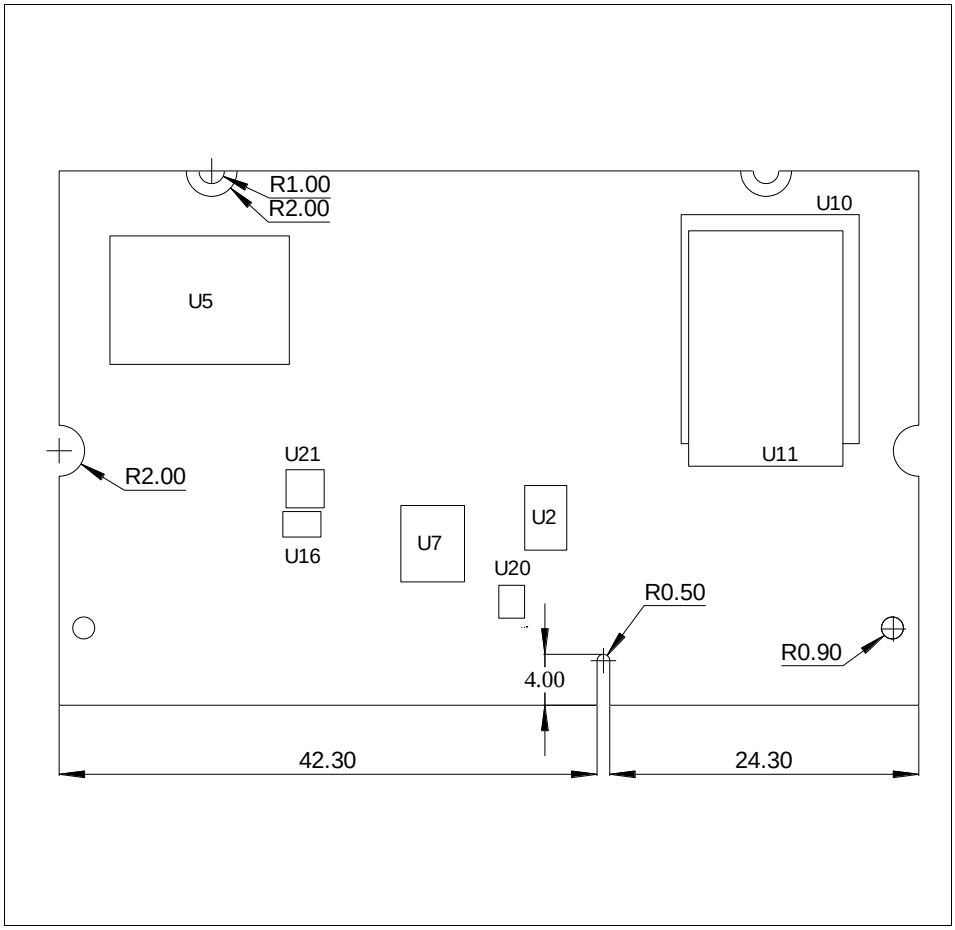


Figure 4 CL-SOM-iMX7 bottom



1. All dimensions are in millimeters.
2. Height of all components is < 3.5mm.
3. Baseboard connectors provide 2.8 ± 0.25mm board-to-board clearance.
4. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at
http://www.compulab.co.il/products/computer-on-modules/cl-som-imx7-freescale-i-mx-7-system-on-module/#devres

6.4 Standoffs/Spacers

CL-SOM-iMX7 has two semicircular mounting holes to physically secure the CoM/SoM to the carrier board. Secure CL-SOM-iMX7 to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 3.0±0.1 mm length

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 72 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)		-0.3		4.8	V
Backup battery supply voltage (VCC_RTC)		-0.3		3.6	V
					V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 73 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	Normal operation	3.4		4.5	V
Backup battery supply voltage (VCC_RTC)		1.8	3.0	3.3	V
					V

7.3 DC Electrical Characteristics

Table 74 DC Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{OH}	3.3V operation, i.MX7 drive strength set to Ioh= -0.1mA, Ioh= -1mA.	3.05			V
V_{OL}				0.15	V
V_{IH}	3.3V operation	2.38		3.3	V
V_{IL}		0		0.96	V
V_{OH}	1.8V operation, i.MX7 drive strength set to Ioh= -0.1mA, Ioh= -1mA.	1.55			V
V_{OL}				0.15	V
V_{IH}	1.8V operation	1.33		1.8	V
V_{IL}		0		0.51	V

7.4 ESD Performance

Table 75 ESD Performance

Interface	ESD Performance
i.MX7 pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)
USB Hub pins (UH option)	5kV Human Body Model (HBM)
LVDS (L option)	2kV Human Body Model (HBM)

7.5 Operating Temperature Ranges

The CL-SOM-iMX7 is available with three options of operating temperature range.

Table 76 CL-SOM-iMX7 Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.

Range	Temp.	Description
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CL-SOM-iMX7 operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-iMX7.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CL-SOM-iMX7 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CL-SOM-iMX7.
- Refer to the SB-SOM-iMX7 carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect

- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX7, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-SOM-iMX7 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of "Qualified Magnetics" contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 77 Qualified Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-SOM-iMX7 reference design schematics