UCM-iMX8

Reference Guide

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Table 1 Revision Notes

Date	Description
Nov 2018	First release

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab UCM-iMX8 Computer-on-Module.

1.2 UCM-iMX8 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the UCM-iMX8 part number: https://www.compulab.com/products/computer-on-modules/ucm-imx8-nxp-i-mx-8m-som-system-on-module-computer/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
UCM-iMX8 Developer Resources	https://www.compulab.com/products/computer-on-modules/ucm-imx8-nxp-i-mx-8m-som-system-on-module-computer/#devres
iMX8M Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-family-armcortex-a53-cortex-m4-audio-voice-video:i.MX8M?tab=Documentation_Tab
iMX8M Datasheet	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-family-armcortex-a53-cortex-m4-audio-voice-video:i.MX8M?tab=Documentation_Tab

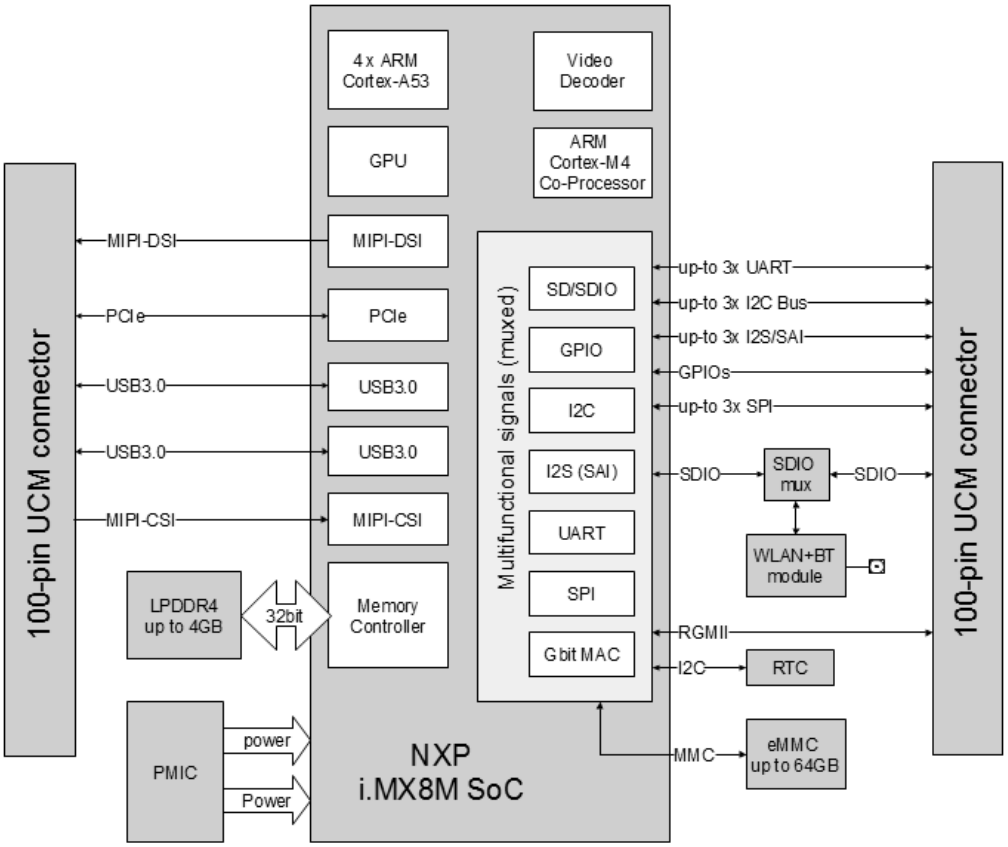
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M ARM Cortex-A53 MPCore 1.5GHz
- Real-time ARM Cortex-M4 co-processor
- Up to 4GB LPDDR4 and 64GB eMMC
- HDMI 2.0a, MIPI-DSI, up to 4096 x 2160
- Gbit Ethernet, certified WiFi 802.11ac, BT 4.1
- 2x PCIe, 2x USB3.0, 4x UART, 95x GPIO
- Miniature size: 28 x 40 x 5 mm

2.2 Block Diagram

Figure 1 UCM-iMX8 Block Diagram



2.3 UCM-iMX8 Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Quad, quad-core ARM Cortex-A53, 1.5GHz	C1500Q
	NXP i.MX8M Dual, dual-core ARM Cortex-A53, 1.5GHz	C1500D
Memory and Storage		
RAM	1GB – 4GB, LPDDR4	D
Storage	eMMC flash, 4GB - 64GB	N
Display and Camera		
Display	HDMI 2.0a, up-to 4096 x 2160 @60Hz	+
	MIPI-DSI 4 lanes up to FHD (1920 x 1080) @60Hz	+
Camera	MIPI-CSI, 4 lanes	+
Network		
Ethernet	1x 10/100/1000Mbps Ethernet port (RGMII)	+
WiFi	802.11ac WiFi interface, Broadcom BCM43353 chipset *precludes MMC/SD/SDIO port	WB
Bluetooth	Bluetooth 4.2 BLE	
Audio		
Digital Audio	Up-to 3x I2S / SAI	+
	S/PDIF input/output	+
I/O		
PCI Express	2x PCIe x1 Gen. 2.1	+
USB	2x USB3.0 dual-role ports	+
Serial Ports (UARTs)	1x UART debug port - TX, RX Only, levels (UART3)	+
	Up to 2x UART ports, up to 4 Mbps	+
	1x UART port - TX, RX, CTS, RTS	~~WB~~
MMC/SD/SDIO	Up to 1x MMC/SD/SDIO *mutually exclusive with WiFi module	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 95x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

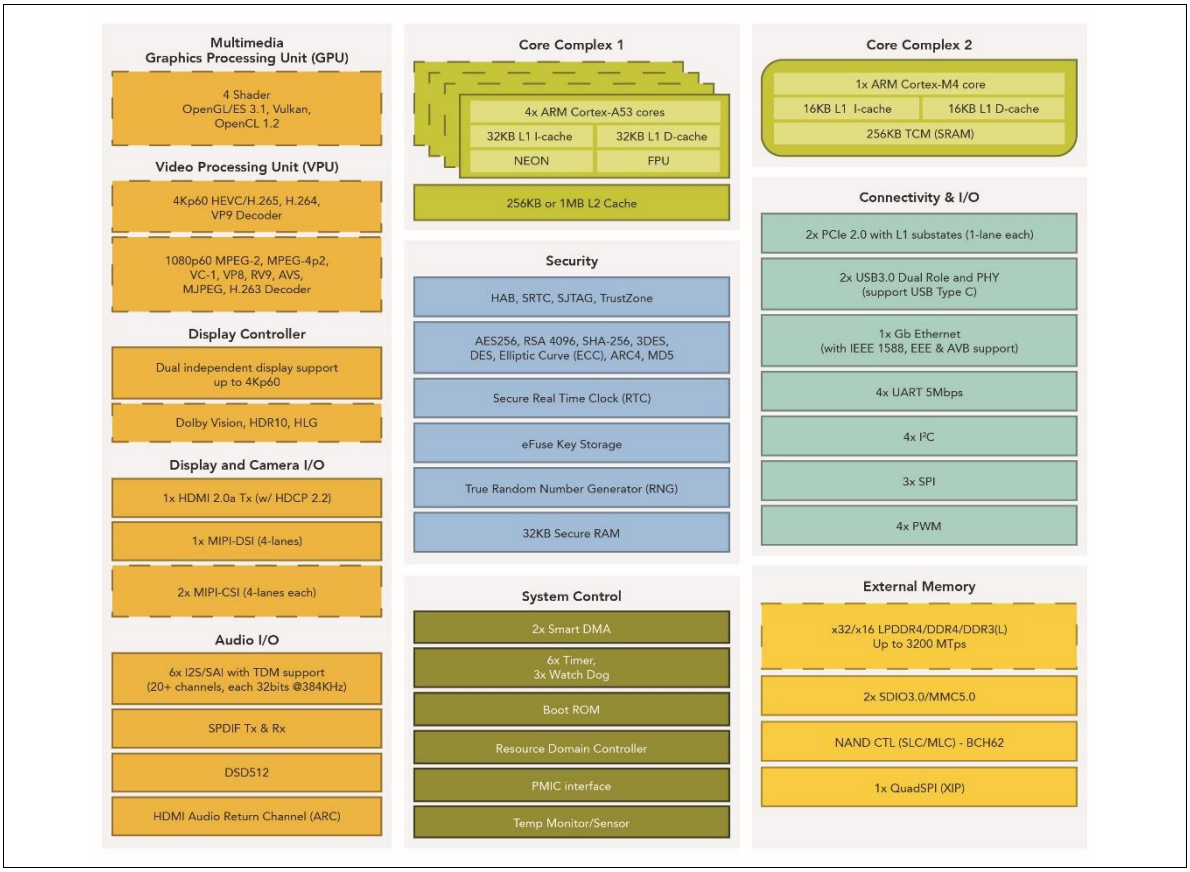
Electrical Specifications	
Supply Voltage	3.6V to 4.4V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	28 x 40 x 5 mm
Weight	8 gram
Connectors	2 x 100 pin, 0.4mm pitch
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 iMX8M SoC

The i.MX 8M family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general purpose Cortex®-M4 core processor is for low-power processing.

Figure 2 i.MX8M Block Diagram



3.2 Memory

3.2.1 DRAM

UCM-iMX8 is equipped with up to 4GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide and operates at 1600 MHz clock frequency (LPDDR4-3200).

3.2.2 Bootloader and General Purpose Storage

The UCM-iMX8 uses on-board non-volatile memory (eMMC) storage as its bootloader host. The remaining eMMC space is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

UCM-iMX8 implements a variety of peripheral interfaces through 2 x 100-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the 2 x 100-pin interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX8 SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the UCM-iMX8 carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5.
- All of the UCM-iMX8 digital interfaces operate at 3.3V voltage levels unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Connector#" –** The carrier board connector number (P1/P2) where the discussed signal is available.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on UCM-iMX8 Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board UCM-iMX8. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard UCM-IMX8, followed by pull value.
- **"PU" -** Always pulled up onboard UCM-IMX8, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 HDMI

UCM-iMX8 HDMI 2.0 interface is derived from the i.MX8M HD Display Transmitter Controller IP. For more detailed information, please refer to the i.MX8M TRM chapter 13: HD Display Transmitter Controller (HDMI TX).

The controller supports the following protocols:

- HDMI 1.4 Specification.
- HDMI 2.0a Specification.
- High-bandwidth Digital Content Protection system, Mapping HDCP to HDMI, Revision 2.2.
- High-bandwidth Digital Content Protection system, Mapping HDCP to HDMI, Revision 1.4.
- CEA-861-F.

The table below summarizes the HDMI interface signals

Table 5 HDMI Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
HDMI_AUXN	P1	61	IO	HEAC -	Always available
HDMI_AUXP	P1	59	IO	HEAC +	Always available
HDMI_CEC	P1	62	I	Consumer Electronics Control	Always available
HDMI_CLKN_CM	P1	52	O	TMDS Clock-	Always available
HDMI_CLKP_CM	P1	50	O	TMDS Clock+	Always available
HDMI_DDC_SCL	P1	58	O	Data Display Channel clock	Always available
HDMI_DDC_SDA	P1	56	IO	Data Display Channel data signal	Always available
HDMI_HPD	P1	60	I	Hot Plug Detect	Always available
HDMI_TXN0_CM	P1	49	O	TMDS Data0-	Always available
HDMI_TXN1_CM	P1	55	O	TMDS Data1-	Always available
HDMI_TXN2_CM	P1	45	O	TMDS Data2-	Always available
HDMI_TXP0_CM	P1	51	O	TMDS Data0+	Always available
HDMI_TXP1_CM	P1	53	O	TMDS Data1+	Always available
HDMI_TXP2_CM	P1	47	O	TMDS Data2+	Always available

4.2 MIPI-DSI Interface

The UCM-iMX8 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the iMX8M SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 Data Lanes.
- Supports MIPI Standard for D-PHY.
- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz).
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
DSI_CKN	P2	21	O	Negative part of MIPI-DSI clock diff-pair	Always available
DSI_CKP	P2	23	O	Positive part of MIPI-DSI clock diff-pair	Always available
DSI_DN0	P2	1	O	Negative part of MIPI-DSI data diff-pair 0	Always available
DSI_DN1	P2	15	O	Negative part of MIPI-DSI data diff-pair 2	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
DSI_DN2	P2	5	O	Negative part of MIPI-DSI data diff-pair 2	Always available
DSI_DN3	P2	11	O	Negative part of MIPI-DSI data diff-pair 2	Always available
DSI_DP0	P2	3	O	Positive part of MIPI-DSI data diff-pair 0	Always available
DSI_DP1	P2	17	O	Positive part of MIPI-DSI data diff-pair 1	Always available
DSI_DP2	P2	7	O	Positive part of MIPI-DSI data diff-pair 2	Always available
DSI_DP3	P2	13	O	Positive part of MIPI-DSI data diff-pair 3	Always available

4.3 Camera Serial Interface

UCM-iMX8 MIPI-CSI interface is derived from the four-lane MIPI CSI1 host controller (MIPI_CSI1) integrated into the iMX8M SoC. The CSI1 host controller is a digital core that implements all protocol functions defined in the MIPI CSI-1 specification, providing an interface between UCM-iMX8 and a MIPI CSI-1 compliant camera sensor. The following main features are supported:

- Up-to four data lanes and one clock lane.
- Maximum bit rate of 1.5 Gbps.
- Compliant with MIPI D-PHY standard specification V1.1 and Samsung D-PHY.
- Compliant to MIPI CSI2 Standard Specification V1.01r06.
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits.
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 7 MIPI-CSI Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
CSI_P1_CKN	P2	2	O	Negative part of MIPI-CSI clock diff-pair	Always available
CSI_P1_CKP	P2	4	O	Positive part of MIPI-CSI clock diff-pair	Always available
CSI_P1_DN0	P2	6	I	Negative part of MIPI-CSI data diff-pair 0	Always available
CSI_P1_DN1	P2	31	I	Negative part of MIPI-CSI data diff-pair 1	Always available
CSI_P1_DN2	P2	25	I	Negative part of MIPI-CSI data diff-pair 2	Always available
CSI_P1_DN3	P2	35	I	Negative part of MIPI-CSI data diff-pair 3	Always available
CSI_P1_DP0	P2	8	I	Positive part of MIPI-CSI data diff-pair 0	Always available
CSI_P1_DP1	P2	33	I	Positive part of MIPI-CSI data diff-pair 1	Always available
CSI_P1_DP2	P2	27	I	Positive part of MIPI-CSI data diff-pair 2	Always available
CSI_P1_DP3	P2	37	I	Positive part of MIPI-CSI data diff-pair 3	Always available

4.4 Ethernet

iMX8M incorporates an internal MAC controller that can be used with an external PHY to implement 10/100/1000 Mbps Ethernet interface.

4.4.1 RGMII

The iMX8M Ethernet MAC RGMII and MDIO lines are routed directly to the carrier board interface. Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the Ethernet RGMII interface signals

Table 8 Ethernet RGMII Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
ENET_MDC	P2	76*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always available
ENET_MDC	P1	100*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always available
ENET_MDIO	P2	88*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always available
ENET_MDIO	P1	96*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always available
ENET_RD0	P2	86*	I	Ethernet input data from the PHY	Always available
ENET_RD1	P2	83*	I	Ethernet input data from the PHY	Always available
ENET_RD2	P2	84*	I	Ethernet input data from the PHY	Always available
ENET_RD3	P2	85*	I	Ethernet input data from the PHY	Always available
ENET_RX_CTL	P2	79*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode).	Always available
ENET_RXC	P2	80*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Always available
ENET_TD0	P2	75*	O	Ethernet output data to PHY	Always available
ENET_TD1	P2	78*	O	Ethernet output data to PHY	Always available
ENET_TD2	P2	77*	O	Ethernet output data to PHY	Always available
ENET_TD3	P2	73*	O	Ethernet output data to PHY	Always available
ENET_TXC	P2	81*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Always available
ENET_TX_CTL	P2	74*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode).	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.5 Wireless Interface

UCM-iMX8 optional 802.11a/b/g/n/ac WLAN and Bluetooth 4.2/EDR functions are implemented with the Cypress BCM43353 chipset. i.MX8M SoC is interfaced with the WLAN Cypress subsystem over i.MX8M SDIO interface, while UART4 is dedicated to Bluetooth functionality.

UCM-iMX8 is equipped with a MHF4 high-frequency connector allowing easy integration with an external WLAN/BT antenna.

Table 9 J5 MHF4 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	W.FL2-R-MT(60)	Hirose W.FL2-LP-062HF

NOTE: UCM-iMX8 WiFi 802.11 a/b/g/n and Bluetooth functionality is available only with the 'WB' ordering option.

4.6 PCI-Express

iMX8M SoC is equipped with two single lane PCI Express port (PCIe) Gen 2.1 ports. UCM-iMX8 enables access to the iMX8M PCI-Express ports (PCIe 1 & 2) through the carrier board interface. PCIe #1 has a built in PCIe reference clock and does not require an external clock source, while PCIe #2 requires an external PCIe clock to be supplied in order to utilize the interface. The PCI Express ports support the following main features:

- Single lane compliant with PCI Express base specification Gen 2.1 (5.0Gbps).
- Dual mode operation to function as root complex or endpoint.
- Integrated PHY interface.
- Supports spread spectrum clocking in transmitter and receiver.

Please refer to the iMX8M Reference manual for additional details. The tables below summarize the PCI Express interface signals

Table 10 PCIE 1 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
PCIE1_CLKREQ_B	P1	87*	I	PCIe clock request signal	Always available
PCIE1_CLKREQ_B	P1	84*	I	PCIe clock request signal	Always available
PCIE1_REF_CLKN	P2	44	O	100 MHz negative-side reference clock differential output for PCIe	Always available
PCIE1_REF_CLKP	P2	42	O	100 MHz positive-side reference clock differential output for PCIe	Always available
PCIE1_RXN_N	P2	30	I	PCI Express receive data negative	Always available
PCIE1_RXN_P	P2	32	I	PCI Express receive data positive	Always available
PCIE1_TXN_N	P2	36	O	PCI Express transmit data negative	Always available
PCIE1_TXN_P	P2	38	O	PCI Express transmit data positive	Always available

Table 11 PCIE 2 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
PCIE2_CLKREQ_B	P1	89*	I	PCIe clock request signal	Always available
PCIE2_CLKREQ_B	P1	86*	I	PCIe clock request signal	Always available
PCIE2_REF_CLKN	P2	26	I	100 MHz negative-side reference clock differential output for PCIe. Must be pulled low through 49.9Ω resistor on carrier board.	Always available
PCIE2_REF_CLKP	P2	24	I	100 MHz positive-side reference clock differential output for PCIe. Must be pulled low through 49.9Ω resistor on carrier board.	Always available
PCIE2_RXN_N	P2	12	I	PCI Express receive data negative	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
PCIE2_RXN_P	P2	14	I	PCI Express receive data positive	Always available
PCIE2_TXN_N	P2	18	O	PCI Express transmit data negative	Always available
PCIE2_TXN_P	P2	20	O	PCI Express transmit data positive	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.7 Sony/Philips Digital Interface (SPDIF)

UCM-iMX8 provides one SPDIF transmitter with one output and one SPDIF receiver with one input.

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the SPDIF interface signals

Table 12 SPDIF Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	P1	77*	I	External clock signal	Always available
SPDIF_RX	P1	79*	I	SPDIF input data line signal	Always available
SPDIF_TX	P1	81*	O	SPDIF output data line signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Digital Audio (SAI)

UCM-iMX8 enables access to 3 of the iMX8M integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the iMX8M Reference manual for additional details. The tables below summarize the SAI interface signals

Table 13 SAI 2 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
SAI2_MCLK	P1	30*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI2_RXD	P1	28*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI2_RXC	P1	32*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
SAI2_RXFS	P1	34*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI2_TXD	P1	26*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI2_TXC	P1	36*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI2_TXFS	P1	38*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 14 SAI 3 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
SAI3_MCLK	P1	17*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXD	P1	19*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI3_RXC	P1	21*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXFS	P1	25*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI3_TXD	P1	13*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI3_TXC	P1	15*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_TXFS	P1	23*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 15 SAI 5 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
SAI5_MCLK	P1	41*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI5_MCLK	P1	30*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI5_MCLK	P1	17*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RX_BCLK	P1	21*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RXD0	P1	35*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD0	P1	19*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD1	P1	33*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD1	P1	23*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD2	P1	37*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD2	P1	15*	I	Receive data, sampled synchronously by the bit clock	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
SAI5_RXD3	P1	29*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXD3	P1	13*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI5_RXC	P1	31*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RXFS	P1	39*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI5_RX_SYNC	P1	25*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI5_TX_BCLK	P1	37*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_TX_BCLK	P1	32*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_TX_DATA[0]	P1	29*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_DATA[0]	P1	28*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_DATA[1]	P1	38*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_DATA[2]	P1	36*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_DATA[3]	P1	26*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_SYNC	P1	34*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI5_TX_SYNC	P1	33*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.9 USB3.0 ports

iMX8M SoC is equipped with two USB controllers and PHYs that support USB 3.0 and USB 2.0. Each USB instance contains USB 3.0 core, which can operate in both 3.0 and 2.0 mode. One port supports dual-role functionality, while the second port is configured permanently for host mode. USB ports support the following main features:

- SuperSpeed, Hi Speed and Full Speed support.
- USB3 U1/U2/U3 Support.
- 32 endpoints per slot.
- Separate Power Domains for Host and Peripheral Device logic.
- Full Power Management capabilities (U1, U2 and U3) with LFPS support for

SuperSpeed.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the USB3.0 interface signals

Table 16 USB3.0 1 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
USB1_DN	P1	14	IO	USB2.0 negative data	Always available
USB1_DP	P1	12	IO	USB2.0 positive data	Always available
USB1_ID	P1	22	I	USB1 OTG ID signal	Always available
USB1_RX_N	P1	18	I	USB3.0 receive negative lane	Always available
USB1_RX_P	P1	16	I	USB3.0 receive positive lane	Always available
USB1_TX_N	P1	8	O	USB3.0 transmit negative lane	Always available
USB1_TX_P	P1	6	O	USB3.0 transmit positive lane	Always available
USB1_VBUS_DET	P1	24	I	USB1 VBUS detect	Always available

Table 17 USB3.0 2 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
USB2_DN	P1	5	IO	USB2.0 negative data	Always available
USB2_DP	P1	3	IO	USB2.0 positive data	Always available
USB2_RX_N	P1	9	I	USB3.0 receive negative lane	Always available
USB2_RX_P	P1	7	I	USB3.0 receive positive lane	Always available
USB2_TX_N	P1	2	O	USB3.0 transmit negative lane	Always available
USB2_TX_P	P1	4	O	USB3.0 transmit positive lane	Always available
USB2_VBUS_DET	P1	1	I	USB2 VBUS detect	Always available

4.10 MMC / SD /SDIO

UCM-iMX8 features one MMC/SD/SDIO port which is mutually functionally exclusive with the on-board WiFi module. The i.MX8M SDIO interface is routed by on-board multiplexing circuitry either to the on-board WiFi module or to the carrier-board interface connector. SDIO multiplexing is controlled by GPIO_IO13. If “WB” option is not populated, the SDIO interface is always available.

The port is derived from the iMX8M on-chip MMC/SD/SDIO controller (uSDHC). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS400 (8-bit transfer mode is only available on uSDHC port 1).
- Dedicated card detection, write protection and Reset signals.

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals

Table 18 MMC/SD/SDIO Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
SD2_nCD	P2	92*	I	Card detection pin	Always available
EXT_SD2_CLK	P2	96*	O	Clock for MMC/SD/SDIO card	GPIO_IO13 is low or not WB

Signal Name	Connector #	Pin #	Type	Description	Availability
EXT_SD2_CMD	P2	100*	IO	CMD line connect to card	GPIO_IO13 is low or not WB
EXT_SD2_DATA0	P2	97*	IO	DATA0 line in all modes. Also used to detect busy state	GPIO_IO13 is low or not WB
EXT_SD2_DATA1	P2	99*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	GPIO_IO13 is low or not WB
EXT_SD2_DATA2	P2	94*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	GPIO_IO13 is low or not WB
EXT_SD2_DATA3	P2	98*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	GPIO_IO13 is low or not WB
SD2_nRST	P2	51*	O	Card hardware reset signal, active LOW	Always available
SD2_WP	P2	49*	I	Card write protect detection	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 UART

UCM-iMX8 enables access to up-to four iMX8M universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The iMX8M UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: The UART4 is used for the on-board Bluetooth module. Using UART4 interface signals available through the carrier board interface precludes on-board Bluetooth operation.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the UART interface signals

Table 19 UART 1 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
UART1_CTS_B	P1	76*	O	UART-1 clear to send	Always available
UART1_RTS_B	P1	74*	I	UART-1 request to send	Always available
UART1_RXD	P1	70*	I	UART-1 serial data receive	Always available
UART1_TXD	P1	72*	O	UART-1 serial data transmit	Always available

Table 20 UART 2 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
UART2_CTS_B	P1	84*	O	UART-2 clear to send	Always available
UART2_RTS_B	P1	86*	I	UART-2 request to send	Always available
UART2_RXD	P1	80*	I	UART-2 serial data receive	Always available
UART2_TXD	P1	82*	O	UART-2 serial data transmit	Always available

Table 21 UART 3 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
DBG_UART_RXD	P1	76*	I	UART-3 serial data receive	Always available
DBG_UART_TXD	P1	74*	O	UART-3 serial data transmit	Always available

Table 22 UART 4 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
UART4_RXD	P1	84*	I	UART-4 serial data receive	Always available, precludes Bluetooth
	P2	93*	I	UART-4 serial data receive	Only w/o "WB" option
UART4_TXD	P1	86*	O	UART-4 serial data transmit	Always available, precludes Bluetooth
	P2	95*	O	UART-4 serial data transmit	Only w/o "WB" option
UART4_CTS_B	P2	89*	O	UART-4 clear to send	Only w/o "WB" option
UART4_RTS_B	P2	91*	I	UART-4 request to send	Only w/o "WB" option

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 I2C

UCM-iMX8 is equipped with up-to three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the I2C interface signals

Table 23 I2C 1 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
I2C1_SCL	P1	100*	O	I2C serial clock line	Always available
I2C1_SDA	P1	96*	IO	I2C serial data line	Always available

Table 24 I2C 3 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
I2C3_SCL	P1	94*	O	I2C serial clock line	Always available
I2C3_SDA	P1	91*	IO	I2C serial data line	Always available

Table 25 I2C 4 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
I2C4_SCL	P1	87*	O	I2C serial clock line	Always available
I2C4_SDA	P1	89*	IO	Always available	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 ECSPI

Up-to three SPI interfaces are accessible through the UCM-iMX8 carrier board interface. The SPI interfaces are derived from iMX8M integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the ECSPI interface signals

Table 26 ECSPI 1 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
ECSPI1_MISO	P1	44*	I	SPI-1 Master data in; slave data out	Always available
ECSPI1_MOSI	P1	42*	O	SPI-1 Master data out; slave data in	Always available
ECSPI1_SCLK	P1	48*	O	SPI-1 Master clock out; slave clock in	Always available
ECSPI1_SS0	P1	46*	O	SPI-1 Chip select 0	Always available

Table 27 ECSPI 2 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
ECSPI2_MISO	P2	89*	I	SPI-2 Master data in; slave data out	Only w/o "WB" option
ECSPI2_MOSI	P2	95*	O	SPI-2 Master data out; slave data in	Only w/o "WB" option
ECSPI2_SCLK	P2	93*	O	SPI-2 Master clock out; slave clock in	Only w/o "WB" option
ECSPI2_SS0	P2	91*	O	SPI-2 Chip select 0	Only w/o "WB" option

Table 28 ECSPI 3 Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
ECSPI3_MISO	P1	80*	I	SPI-3 Master data in; slave data out	Always available
ECSPI3_MOSI	P1	72*	O	SPI-3 Master data out; slave data in	Always available
ECSPI3_SCLK	P1	70*	O	SPI-3 Master clock out; slave clock in	Always available
ECSPI3_SS0	P1	82*	O	SPI-3 Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 JTAG

UCM-iMX8 enables access to the iMX8M JTAG port through the carrier board interface.

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the JTAG interface signals

Table 29 JTAG Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
JTAG_MOD	P1	75	I	JTAG MODE	Always available
JTAG_nTRST	P1	63	I	Test Reset	Always available
JTAG_TCK	P1	73	I	Test Clock	Always available
JTAG_TDI	P1	71	I	Test Data In	Always available
JTAG_TDO	P1	67	O	Test Data Out	Always available
JTAG_TMS	P1	65	I	Test Mode Select	Always available

4.15 QSPI

UCM-iMX8 is equipped with two instances of the Quad SPI interface. The interface is implemented with the iMX8M integrated QSPI controller. The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Parallel Flash mode.
- Direct Memory Access (DMA) support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the iMX8M Reference manual for additional details.

The tables below summarize the QSPI interface signals

Table 30 QSPI A Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
QSPI_A_DATA0	P2	61*	IO	Data IO 0	Always available
QSPI_A_DATA1	P2	56*	IO	Data IO 1	Always available
QSPI_A_DATA2	P2	43*	IO	Data IO 2	Always available
QSPI_A_DATA3	P2	58*	IO	Data IO 3	Always available
QSPI_A_DQS	P2	67*	O	Data strobe signal to serial flash device A	Always available
QSPI_A_SCLK	P2	55*	O	Serial clock	Always available
QSPI_A_SS0_B	P2	65*	O	Chip select 0	Always available
QSPI_A_SS1_B	P2	53*	O	Chip select 1	Always available

Table 31 QSPI B Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
QSPI_B_DATA0	P2	48*	IO	Data IO 0	Always available
QSPI_B_DATA1	P2	59*	IO	Data IO 1	Always available
QSPI_B_DATA2	P2	63*	IO	Data IO 2	Always available
QSPI_B_DATA3	P2	69*	IO	Data IO 3	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
QSPI_B_DQS	P2	50*	O	Data strobe signal to serial flash device B	Always available
QSPI_B_SCLK	P2	62*	O	Serial clock	Always available
QSPI_B_SS0_B	P2	41*	O	Chip select 0	Always available
QSPI_B_SS1_B	P2	60*	O	Chip select 1	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 NAND

8-bit NAND-Flash is implemented with the iMX8M GPMI controller.

The table below summarizes the NAND interface signals

Table 32 NAND Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
NAND_ALE	P2	55*	O	NAND address latch enable	Always available
NAND_nCE0	P2	65*	O	NAND chip enable 0	Always available
NAND_nCE1	P2	53*	O	NAND chip enable 1	Always available
NAND_nCE2	P2	41*	O	NAND chip enable 2	Always available
NAND_nCE3	P2	60*	O	NAND chip enable 3	Always available
NAND_CLE	P2	62*	O	NAND command latch enable	Always available
NAND_DATA0	P2	61*	IO	NAND data IO 0	Always available
NAND_DATA1	P2	56*	IO	NAND data IO 1	Always available
NAND_DATA2	P2	43*	IO	NAND data IO 2	Always available
NAND_DATA3	P2	58*	IO	NAND data IO 3	Always available
NAND_DATA4	P2	48*	IO	NAND data IO 4	Always available
NAND_DATA5	P2	59*	IO	NAND data IO 5	Always available
NAND_DATA6	P2	63*	IO	NAND data IO 6	Always available
NAND_DATA7	P2	69*	IO	NAND data IO 7	Always available
NAND_DQS	P2	67*	I	NAND DQS strobe	Always available
NAND_nRE	P2	50*	O	NAND read enable	Always available
NAND_nREADY	P2	52*	I	NAND ready ready/busy	Always available
NAND_nWE	P2	47*	O	NAND write enable	Always available
NAND_nWP	P2	45*	O	NAND write protect	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.17 PWM

Up to four independent PWM output signals are available at the UCM-iMX8 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the PWM interface signals

Table 33 PWM Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
PWM1_OUT	P1	77*	O	PWM functional output	Always available
	P1	89*	O	PWM functional output	Always available
PWM2_OUT	P1	79*	O	PWM functional output	Always available
	P1	87*	O	PWM functional output	Always available
PWM3_OUT	P1	81*	O	PWM functional output	Always available
	P1	91*	O	PWM functional output	Always available
PWM4_OUT	P1	17*	O	PWM functional output	Always available
	P1	94*	O	PWM functional output	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.18 GPIO

Up-to 95 of the iMX8M general purpose input/output (GPIO) signals are available through the UCM-iMX8 carrier board interface. When configured as an output, it is possible to write to an iMX8M register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an iMX8M register. In addition, GPIOs peripheral can produce interrupts.

Please refer to the iMX8M Reference manual for additional details.

The table below summarizes the GPIO interface signals

Table 34 GPIO Interface Signals

Signal Name	Connector #	Pin #	Type	Description	Availability
GPIO1_IO[09]	P2	68	IO	GPIO	Always available
GPIO1_IO[10]	P2	90	IO	GPIO	Always available
GPIO1_IO[11]	P2	70	IO	GPIO	Always available
GPIO1_IO[15]	P1	85	IO	GPIO	Always available
GPIO1_IO[16]	P2	76*	IO	GPIO	Always available
GPIO1_IO[17]	P2	88*	IO	GPIO	Always available
GPIO1_IO[18]	P2	73*	IO	GPIO	Always available
GPIO1_IO[19]	P2	77*	IO	GPIO	Always available
GPIO1_IO[20]	P2	78*	IO	GPIO	Always available
GPIO1_IO[21]	P2	75*	IO	GPIO	Always available
GPIO1_IO[22]	P2	74*	IO	GPIO	Always available
GPIO1_IO[23]	P2	81*	IO	GPIO	Always available
GPIO1_IO[24]	P2	79*	IO	GPIO	Always available
GPIO1_IO[25]	P2	80*	IO	GPIO	Always available
GPIO1_IO[26]	P2	86*	IO	GPIO	Always available
GPIO1_IO[27]	P2	83*	IO	GPIO	Always available
GPIO1_IO[28]	P2	84*	IO	GPIO	Always available
GPIO1_IO[29]	P2	85*	IO	GPIO	Always available
GPIO2_IO[12]	P2	92*	IO	GPIO	Always available
GPIO2_IO[13]	P2	96*	IO	GPIO	Always available
GPIO2_IO[14]	P2	100*	IO	GPIO	Always available
GPIO2_IO[15]	P2	97*	IO	GPIO	Always available
GPIO2_IO[16]	P2	99*	IO	GPIO	Always available
GPIO2_IO[17]	P2	94*	IO	GPIO	Always available
GPIO2_IO[18]	P2	98*	IO	GPIO	Always available
GPIO2_IO[19]	P2	51*	IO	GPIO	Always available
GPIO2_IO[20]	P2	49*	IO	GPIO	Always available
GPIO3_IO[0]	P2	55*	IO	GPIO	Always available
GPIO3_IO[1]	P2	65*	O	GPIO	Always available
GPIO3_IO[2]	P2	53*	IO	GPIO	Always available
GPIO3_IO[3]	P2	41*	IO	GPIO	Always available
GPIO3_IO[4]	P2	60*	IO	GPIO	Always available
GPIO3_IO[5]	P2	62*	IO	GPIO	Always available
GPIO3_IO[6]	P2	61*	O	GPIO	Always available
GPIO3_IO[7]	P2	56*	IO	GPIO	Always available

Signal Name	Connector #	Pin #	Type	Description	Availability
GPIO3_IO[8]	P2	43*	IO	GPIO	Always available
GPIO3_IO[9]	P2	58*	IO	GPIO	Always available
GPIO3_IO[10]	P2	48*	IO	GPIO	Always available
GPIO3_IO[11]	P2	59*	IO	GPIO	Always available
GPIO3_IO[12]	P2	63*	IO	GPIO	Always available
GPIO3_IO[13]	P2	69*	IO	GPIO	Always available
GPIO3_IO[14]	P2	67*	IO	GPIO	Always available
GPIO3_IO[15]	P2	50*	IO	GPIO	Always available
GPIO3_IO[16]	P2	52*	IO	GPIO	Always available
GPIO3_IO[17]	P2	47*	IO	GPIO	Always available
GPIO3_IO[18]	P2	45*	IO	GPIO	Always available
GPIO3_IO[19]	P1	39*	IO	GPIO	Always available
GPIO3_IO[20]	P1	31*	IO	GPIO	Always available
GPIO3_IO[21]	P1	35*	IO	GPIO	Always available
GPIO3_IO[22]	P1	33*	IO	GPIO	Always available
GPIO3_IO[23]	P1	37*	IO	GPIO	Always available
GPIO3_IO[24]	P1	29*	IO	GPIO	Always available
GPIO3_IO[25]	P1	41*	IO	GPIO	Always available
GPIO4_IO[10]	P1	95	IO	GPIO	Always available
GPIO4_IO[21]	P1	34*	IO	GPIO	Always available
GPIO4_IO[22]	P1	32*	IO	GPIO	Always available
GPIO4_IO[23]	P1	28*	IO	GPIO	Always available
GPIO4_IO[24]	P1	38*	IO	GPIO	Always available
GPIO4_IO[25]	P1	36*	IO	GPIO	Always available
GPIO4_IO[26]	P1	26*	IO	GPIO	Always available
GPIO4_IO[27]	P1	30*	IO	GPIO	Always available
GPIO4_IO[28]	P1	25*	IO	GPIO	Always available
GPIO4_IO[29]	P1	21*	IO	GPIO	Always available
GPIO4_IO[30]	P1	19*	IO	GPIO	Always available
GPIO4_IO[31]	P1	23*	IO	GPIO	Always available
GPIO5_IO[0]	P1	15*	IO	GPIO	Always available
GPIO5_IO[1]	P1	13*	IO	GPIO	Always available
GPIO5_IO[2]	P1	17*	IO	GPIO	Always available
GPIO5_IO[3]	P1	81*	IO	GPIO	Always available
GPIO5_IO[4]	P1	79*	IO	GPIO	Always available
GPIO5_IO[5]	P1	77*	IO	GPIO	Always available
GPIO5_IO[6]	P1	48*	IO	GPIO	Always available
GPIO5_IO[7]	P1	42*	IO	GPIO	Always available
GPIO5_IO[8]	P1	44*	IO	GPIO	Always available
GPIO5_IO[9]	P1	46*	IO	GPIO	Always available
GPIO5_IO[10]	P2	93*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[11]	P2	95*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[12]	P2	89*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[13]	P2	91*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[14]	P1	100*	IO	GPIO	Always available
GPIO5_IO[15]	P1	96*	IO	GPIO	Always available
GPIO5_IO[16]	P1	99	IO	GPIO	Always available
GPIO5_IO[17]	P1	97	IO	GPIO	Always available
GPIO5_IO[18]	P1	94*	IO	GPIO	Always available
GPIO5_IO[19]	P1	91*	IO	GPIO	Always available
GPIO5_IO[20]	P1	87*	IO	GPIO	Always available
GPIO5_IO[21]	P1	89*	IO	GPIO	Always available
GPIO5_IO[22]	P1	70*	IO	GPIO	Always available
GPIO5_IO[23]	P1	72*	IO	GPIO	Always available
GPIO5_IO[24]	P1	80*	IO	GPIO	Always available
GPIO5_IO[25]	P1	82*	IO	GPIO	Always available
GPIO5_IO[26]	P1	76*	IO	GPIO	Always available
GPIO5_IO[27]	P1	74*	IO	GPIO	Always available
GPIO5_IO[28]	P1	84*	IO	GPIO	Always available
GPIO5_IO[29]	P1	86*	IO	GPIO	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

5 SYSTEM LOGIC

5.1 Power Supply

Table 35 Power signals

Signal Name	Connector #	Pin#	Type	Description
V_SOM	P1	11,27,43,57,69,83	P	Main power supply. Connect to a regulated DC supply or Li-iON battery
	P2	9,19,29,39,57,71,87		
VCC_RTC	P1	93	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Use 4.7uF capacitor instead of a coin-cell battery if RTC back-up is not required.
GND	P1	10,20,40,54,64,78,88	P	Common ground.
	P2	10,16,22,28,34,40,46,54,72,82		

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

UCM-iMX8 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the iMX8M SoC. The logic that controls both signals is supplied by the iMX8M SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that UCM-iMX8 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the iMX8M Reference manual for additional details. The table below summarizes the external regulator control signals

Table 36 External regulator control signals

Signal Name	Connector #	Pin #	Type	Description	Availability
PMIC_STBY_REQ	P1	66	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	P1	68	O	Active high power-up request output from iMX8M SoC.	Always available
PWRBTN	P2	64	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX8. Please refer to the iMX8M Reference manual for additional details.

Table 37 Reset signals

Signal Name	Connector #	Pin #	Type	Description	Availability
POR_B	P2	66	I	Active Low cold reset input signal. Should be used as main system reset Maximum rise/fall time is 5.0nS.	Always available

5.4 Boot Sequence

UCM-iMX8 boot sequence defines which interface/media is used by UCM-iMX8 to load and execute the initial software (such as U-boot). UCM-iMX8 can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD/MMC card using the MMC/SD/SDIO 2 interface

UCM-iMX8 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by UCM-iMX8:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows UCM-iMX8 to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 38 Alternative Boot selection signal

Signal Name	Connector #	Pin #	Type	Description	Availability
ALT_BOOT	P1	90	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 39 UCM-iMX8 Boot sequences

sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (Primary boot storage)
Alternate	High	SD card on MMC/SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 90 of the UCM-iMX8 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX8 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 5 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX8 pins are derived from the iMX8M SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 40 Multifunctional Signals

Connector #	Pin #	i.MX8 signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
P1	13*	SAI3_TXD	GPT1_COMPARE3	SAI5_RXD3			GPIO5_IO[1]	Always available
P1	15*	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2			GPIO5_IO[0]	Always available
P1	17*	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO[2]	Always available
P1	19*	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0			GPIO4_IO[30]	Always available
P1	21*	SAI3_RXC	GPT1_CAPTURE1	SAI5_RX_BCLK			GPIO4_IO[29]	Always available
P1	23*	SAI3_TXFS	GPT1_CLK	SAI5_RXD1			GPIO4_IO[31]	Always available
P1	25*	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RX_SYNC			GPIO4_IO[28]	Always available
P1	26*	SAI2_TXD	SAI5_TX_DATA[3]				GPIO4_IO[26]	Always available
P1	28*	SAI2_RXD	SAI5_TX_DATA[0]				GPIO4_IO[23]	Always available
P1	29*	SAI5_RXD3			SAI5_TX_DATA[0]		GPIO3_IO[24]	Always available
P1	30*	SAI2_MCLK	SAI5_MCLK				GPIO4_IO[27]	Always available
P1	31*	SAI5_RXC					GPIO3_IO[20]	Always available
P1	32*	SAI2_RXC	SAI5_TX_BCLK				GPIO4_IO[22]	Always available
P1	33*	SAI5_RXD1			SAI5_TX_SYNC		GPIO3_IO[22]	Always available
P1	34*	SAI2_RXFS	SAI5_TX_SYNC				GPIO4_IO[21]	Always available
P1	35*	SAI5_RXD0					GPIO3_IO[21]	Always available
P1	36*	SAI2_TXC	SAI5_TX_DATA[2]				GPIO4_IO[25]	Always available
P1	37*	SAI5_RXD2			SAI5_TX_BCLK		GPIO3_IO[23]	Always available
P1	38*	SAI2_TXFS	SAI5_TX_DATA[1]				GPIO4_IO[24]	Always available
P1	39*	SAI5_RXFS					GPIO3_IO[19]	Always available
P1	41*	SAI5_MCLK					GPIO3_IO[25]	Always available
P1	42*	ECSPI1_MOSI	UART3				GPIO5_IO[7]	Always available
P1	44*	ECSPI1_MISO	UART3				GPIO5_IO[8]	Always available
P1	46*	ECSPI1_SS0	UART3				GPIO5_IO[9]	Always available
P1	48*	ECSPI1_SCLK	UART3				GPIO5_IO[6]	Always available
P1	70*	UART1_RXD	ECSPI3_SCLK				GPIO5_IO[22]	Always available
P1	72*	UART1_TXD	ECSPI3_MOSI				GPIO5_IO[23]	Always available
P1	74*	DBG_UART_TXD					GPIO5_IO[27]	Always available
P1	76*	DBG_UART_RXD					GPIO5_IO[26]	Always available
P1	77*	SPDIF_EXT_CLK	PWM1_OUT				GPIO5_IO[5]	Always available
P1	79*	SPDIF_RX	PWM2_OUT				GPIO5_IO[4]	Always available
P1	80*	UART2_RXD	ECSPI3_MISO				GPIO5_IO[24]	Always available
P1	81*	SPDIF_TX	PWM3_OUT				GPIO5_IO[3]	Always available
P1	82*	UART2_TXD	ECSPI3_SS0				GPIO5_IO[25]	Always available
P1	84*	UART4_RXD	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO[28]	Always available
P1	85	INT_I2C_EXP					GPIO1_IO[15]	Always available
P1	86*	UART4_TXD	UART2_RTS_B	PCIE2_CLKREQ_B			GPIO5_IO[29]	Always available
P1	87*	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO[20]	Always available
P1	89*	I2C4_SDA	PWM1_OUT	PCIE2_CLKREQ_B			GPIO5_IO[21]	Always available
P1	91*	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]	Always available
P1	94*	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]	Always available
P1	95	GPIO4_IO10					GPIO4_IO[10]	Always available
P1	96*	I2C1_SDA	ENET_MDIO				GPIO5_IO[15]	Always available
P1	97	SYS_I2C_SDA					GPIO5_IO[17]	Always available
P1	99	SYS_I2C_SCL					GPIO5_IO[16]	Always available
P1	100*	I2C1_SCL	ENET_MDC				GPIO5_IO[14]	Always available
P2	41*	NAND_nCE2	QSPI_B_SS0_B				GPIO3_IO[3]	Always available
P2	43*	NAND_DATA2	QSPI_A_DATA2				GPIO3_IO[8]	Always available

Connector #	Pin #	i.MX8 signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
P2	45*	NAND_nWP					GPIO3_IO[18]	Always available
P2	47*	NAND_nWE					GPIO3_IO[17]	Always available
P2	48*	NAND_DATA4	QSPI_B_DATA0				GPIO3_IO[10]	Always available
P2	49*	SD2_WP					GPIO2_IO[20]	Always available
P2	50*	NAND_nRE	QSPI_B_DQS				GPIO3_IO[15]	Always available
P2	51*	SD2_nRST					GPIO2_IO[19]	Always available
P2	52*	NAND_nREADY					GPIO3_IO[16]	Always available
P2	53*	NAND_nCE1	QSPI_A_SS1_B				GPIO3_IO[2]	Always available
P2	55*	NAND_ALE	QSPI_A_SCLK				GPIO3_IO[0]	Always available
P2	56*	NAND_DATA1	QSPI_A_DATA1				GPIO3_IO[7]	Always available
P2	58*	NAND_DATA3	QSPI_A_DATA3				GPIO3_IO[9]	Always available
P2	59*	NAND_DATA5	QSPI_B_DATA1				GPIO3_IO[11]	Always available
P2	60*	NAND_nCE3	QSPI_B_SS1_B				GPIO3_IO[4]	Always available
P2	61*	NAND_DATA0	QSPI_A_DATA0				GPIO3_IO[6]	Always available
P2	62*	NAND_CLE	QSPI_B_SCLK				GPIO3_IO[5]	Always available
P2	63*	NAND_DATA6	QSPI_B_DATA2				GPIO3_IO[12]	Always available
P2	65*	NAND_nCE0	QSPI_A_SS0_B				GPIO3_IO[1]	Always available
P2	67*	NAND_DQS	QSPI_A_DQS				GPIO3_IO[14]	Always available
P2	68	GPIO_PHY1_WOL					GPIO1_IO[09]	Always available
P2	69*	NAND_DATA7	QSPI_B_DATA3				GPIO3_IO[13]	Always available
P2	70	GPIO_PHY1_INT					GPIO1_IO[11]	Always available
P2	73*	ENET_TD3					GPIO1_IO[18]	Always available
P2	74*	ENET_TX_CTL					GPIO1_IO[22]	Always available
P2	75*	ENET_TD0					GPIO1_IO[21]	Always available
P2	76*	ENET_MDC					GPIO1_IO[16]	Always available
P2	77*	ENET_TD2					GPIO1_IO[19]	Always available
P2	78*	ENET_TD1					GPIO1_IO[20]	Always available
P2	79*	ENET_RX_CTL					GPIO1_IO[24]	Always available
P2	80*	ENET_RXC					GPIO1_IO[25]	Always available
P2	81*	ENET_TXC					GPIO1_IO[23]	Always available
P2	83*	ENET_RD1					GPIO1_IO[27]	Always available
P2	84*	ENET_RD2					GPIO1_IO[28]	Always available
P2	85*	ENET_RD3					GPIO1_IO[29]	Always available
P2	86*	ENET_RD0					GPIO1_IO[26]	Always available
P2	88*	ENET_MDIO					GPIO1_IO[17]	Always available
P2	89*	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO[12]	Only w/o "WB" option
P2	90	GPIO_USB_ID					GPIO1_IO[10]	Always available
P2	91*	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO[13]	Only w/o "WB" option
P2	92*	SD2_nCD					GPIO2_IO[12]	Always available
P2	93*	ECSPI2_SCLK	UART4_RXD				GPIO5_IO[10]	Only w/o "WB" option
P2	94*	EXT_SD2_DATA2					GPIO2_IO[17]	Always available
P2	95*	ECSPI2_MOSI	UART4_TXD				GPIO5_IO[11]	Only w/o "WB" option
P2	96*	EXT_SD2_CLK					GPIO2_IO[13]	Always available
P2	97*	EXT_SD2_DATA0					GPIO2_IO[15]	Always available
P2	98*	EXT_SD2_DATA3					GPIO2_IO[18]	Always available
P2	99*	EXT_SD2_DATA1					GPIO2_IO[16]	Always available
P2	100*	EXT_SD2_CMD					GPIO2_IO[14]	Always available

5.6 RTC

UCM-iMX8 features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

At main power supply absence, in order to maintain activities of the RTC, i.e. clock advancement and data storage, use of a backup power supply is essential. External backup battery should be used in order to maintain clock and time information when main supply is not present. A rechargeable battery can be charged from the V_SOM voltage using an internal trickle charger of the RTC.

For more information about UCM-iMX8 RTC please refer to the AM1805 datasheet.

5.7 LED

UCM-iMX8 features a single general purpose green LED controlled by GPIO1_12 signal of the iMX8M. The LED is ON when GPIO1_12 is logic LOW.

6 CARRIER BOARD INTERFACE

The UCM-iMX8 CoM/SoM carrier board interface uses 2 x 100 Pin carrier board connectors. The SoM pinout is detailed in the table below.

6.1 Connectors Pinout

Table 41 Connector P1

Pin #	UCM-iMX8 Signal Name	Ref.		Pin #	UCM-iMX8 Signal Name	Ref.
2	USB2_TX_N	4.9		1	USB2_VBUS_DET	4.9
4	USB2_TX_P	4.9		3	USB2_DP	4.9
6	USB1_TX_P	4.9		5	USB2_DN	4.9
8	USB1_TX_N	4.9		7	USB2_RX_P	4.9
10	GND	5.1		9	USB2_RX_N	4.9
12	USB1_DP	4.9		11	V_SOM	5.1
14	USB1_DN	4.9		13	SAI3_TXD GPT1_COMPARE3 SAI5_RXD3 GPIO5_IO[1]	04.8 - 04.8 04.18
16	USB1_RX_P	4.9		15	SAI3_TXC GPT1_COMPARE2 SAI5_RXD2 GPIO5_IO[0]	04.8 - 04.8 04.18
18	USB1_RX_N	4.9		17	SAI3_MCLK PWM4_OUT SAI5_MCLK GPIO5_IO[2]	04.8 4.17 04.8 04.18
20	GND	5.1		19	SAI3_RXD GPT1_COMPARE1 SAI5_RXD0 GPIO4_IO[30]	04.8 - 04.8 04.18
22	USB1_ID	4.9		21	SAI3_RXC GPT1_CAPTURE1 SAI5_RX_BCLK GPIO4_IO[29]	04.8 - 04.8 04.18
24	USB1_VBUS_DET	4.9		23	SAI3_TXFS GPT1_CLK SAI5_RXD1 GPIO4_IO[31]	04.8 - 04.8 04.18
26	SAI2_TXD SAI5_TX_DATA[3] GPIO4_IO[26]	04.8 4.8 04.18		25	SAI3_RXFS GPT1_CAPTURE1 SAI5_RX_SYNC GPIO4_IO[28]	04.8 - 04.8 04.18
28	SAI2_RXD SAI5_TX_DATA[0] GPIO4_IO[23]	04.8 04.8 04.18		27	V_SOM	5.1
30	SAI2_MCLK SAI5_MCLK GPIO4_IO[27]	04.8 04.8 04.18		29	SAI5_RXD3 SAI5_TX_DATA[0] GPIO3_IO[24]	04.8 04.8 04.18
32	SAI2_RXC SAI5_TX_BCLK GPIO4_IO[22]	04.8 04.8 04.18		31	SAI5_RXC GPIO3_IO[20]	04.8 04.18
34	SAI2_RXFS SAI5_TX_SYNC GPIO4_IO[21]	04.8 04.8 04.18		33	SAI5_RXD1 SAI5_TX_SYNC GPIO3_IO[22]	04.8 04.8 04.18
36	SAI2_TXC SAI5_TX_DATA[2] GPIO4_IO[25]	04.8 04.8 04.18		35	SAI5_RXD0 GPIO3_IO[21]	04.8 04.18
38	SAI2_TXFS SAI5_TX_DATA[1] GPIO4_IO[24]	04.8 04.8 04.18		37	SAI5_RXD2 SAI5_TX_BCLK GPIO3_IO[23]	04.8 04.8 04.18
40	GND	5.1		39	SAI5_RXFS GPIO3_IO[19]	04.8 04.18
42	ECSPI1_MOSI UART3 GPIO5_IO[7]	4.13 4.11 04.18		41	SAI5_MCLK GPIO3_IO[25]	04.8 4.18
44	ECSPI1_MISO UART3 GPIO5_IO[8]	4.13 4.11 04.18		43	V_SOM	5.1

46	ECSPI1_SS0 UART3 GPIO5_IO[9]	4.13 4.11 04.18		45	HDMI_TXN2_CM	4.1
48	ECSPI1_SCLK UART3 GPIO5_IO[6]	4.13 4.11 04.18		47	HDMI_TXP2_CM	4.1
50	HDMI_CLKP_CM	4.1		49	HDMI_TXN0_CM	4.1
52	HDMI_CLKN_CM	4.1		51	HDMI_TXP0_CM	4.1
54	GND	5.1		53	HDMI_TXP1_CM	4.1
4.1	HDMI_DDC_SDA 4.1	4.1		4.1	HDMI_TXN1_CM	4.1
58	HDMI_DDC_SCL	4.1		57	V_SOM	5.1
60	HDMI_HPD	4.1		59	HDMI_AUXP	4.1
62	HDMI_CEC	4.1		61	HDMI_AUXN	4.1
64	GND	5.1		63	JTAG_nTRST	4.14
66	PMIC_STBY_REQ	5.2.1		65	JTAG_TMS	4.14
68	PMIC_ON_REQ	5.2.1		67	JTAG_TDO	4.14
70	UART1_RXD ECSPI3_SCLK GPIO5_IO[22]	4.11 4.13 4.18		69	V_SOM	5.1
72	UART1_TXD ECSPI3_MOSI GPIO5_IO[23]	4.11 4.13 4.18		71	JTAG_TDI	4.14
74	DBG_UART_TXD UART1_RTS_B GPIO5_IO[27]	4.11 4.13 4.18		73	JTAG_TCK	4.14
76	DBG_UART_RXD UART1_CTS_B GPIO5_IO[26]	4.11 4.13 4.18		75	JTAG_MOD	4.14
78	GND	5.1		77	SPDIF_EXT_CLK PWM1_OUT GPIO5_IO[5]	4.7 4.17 4.18
80	UART2_RXD ECSPI3_MISO GPIO5_IO[24]	4.11 4.13 4.18		79	SPDIF_RX PWM2_OUT GPIO5_IO[4]	4.7 4.17 4.18
82	UART2_TXD ECSPI3_SS0 GPIO5_IO[25]	4.11 4.13 4.18		81	SPDIF_TX PWM3_OUT GPIO5_IO[3]	4.7 4.17 4.18
84	UART4_RXD UART2_CTS_B PCIE1_CLKREQ_B GPIO5_IO[28]	4.11 4.11 4.6 4.18		83	V_SOM	5.1
86	UART4_TXD UART2_RTS_B PCIE2_CLKREQ_B GPIO5_IO[29]	4.11 4.11 4.6 4.18		85	GPIO1_IO[15]	4.18
88	GND	5.1		87	I2C4_SCL PWM2_OUT PCIE1_CLKREQ_B GPIO5_IO[20]	4.12 4.17 4.6 4.18
90	ALT_BOOT	5.4		89	I2C4_SDA PWM1_OUT PCIE2_CLKREQ_B GPIO5_IO[21]	4.12 4.17 4.6 4.18
92	TP5	-		91	I2C3_SDA PWM3_OUT GPT3_CLK GPIO5_IO[19]	4.12 4.17 - 4.18
94	I2C3_ SCL PWM4_OUT GPT2_CLK GPIO5_IO[18]	4.12 4.17 - 4.18		93	VCC_RTC	5.1
96	I2C1_SDA ENET_MDIO GPIO5_IO[15]	4.12 4.4.1 4.18		95	GPIO4_IO[10]	4.18
98	TP6	-		97	GPIO5_IO[17]	4.18
100	I2C1_SCL ENET_MDC GPIO5_IO[14]	4.12 4.4.1 4.18		99	GPIO5_IO[16]	4.18

Table 42 Connector P2

Pin #	UCM-iMX8 Signal Name	Ref.		Pin #	UCM-iMX8 Signal Name	Ref.

2	CSI_P1_CKN	4.3		1	DSI_DN0	4.2
4	CSI_P1_CKP	4.3		3	DSI_DP0	4.2
6	CSI_P1_DN0	4.3		5	DSI_DN2	4.2
8	CSI_P1_DP0	4.3		7	DSI_DP2	4.2
10	GND	5.1		9	V_SOM	5.1
12	PCIE2_RXN_N	4.6		11	DSI_DN3	4.2
14	PCIE2_RXN_P	4.6		13	DSI_DP3	4.2
16	GND	5.1		15	DSI_DN1	4.2
18	PCIE2_TXN_N	4.6		17	DSI_DP1	4.2
20	PCIE2_TXN_P	4.6		19	V_SOM	5.1
22	GND	5.1		21	DSI_CKN	4.2
24	PCIE2_REF_CLKP	4.6		23	DSI_CKP	4.2
26	PCIE2_REF_CLKN	4.6		25	CSI_P1_DN2	4.3
28	GND	5.1		27	CSI_P1_DP2	4.3
30	PCIE1_RXN_N	4.6		29	V_SOM	5.1
32	PCIE1_RXN_P	4.6		31	CSI_P1_DN1	4.3
34	GND	5.1		33	CSI_P1_DP1	4.3
36	PCIE1_TXN_N	4.6		35	CSI_P1_DN3	4.3
38	PCIE1_TXN_P	4.6		37	CSI_P1_DP3	4.3
40	GND	5.1		39	V_SOM	5.1
42	PCIE1_REF_CLKP	4.6		41	NAND_nCE2 QSPI_B_SS0_B GPIO3_IO[3]	4.16 4.15 4.18
44	PCIE1_REF_CLKN	4.6		43	NAND_DATA2 QSPI_A_DATA2 GPIO3_IO[8]	4.16 4.15 4.18
46	GND	5.1		45	NAND_nWP GPIO3_IO[18]	4.16 4.18
48	NAND_DATA4 QSPI_B_DATA0 GPIO3_IO[10]	4.16 4.15 4.18		47	NAND_nWE GPIO3_IO[17]	4.16 4.18
50	NAND_nRE QSPI_B_DQS GPIO3_IO[15]	4.16 4.15 4.18		49	SD2_WP GPIO2_IO[20]	4.10 4.18
52	NAND_nREADY GPIO3_IO[16]	4.16 4.18		51	SD2_nRST GPIO2_IO[19]	4.10 4.18
54	GND	5.1		53	NAND_nCE1 QSPI_A_SS1_B GPIO3_IO[2]	4.16 4.15 4.18
56	NAND_DATA1 QSPI_A_DATA1 GPIO3_IO[7]	4.16 4.15 4.18		55	NAND_ALE QSPI_A_SCLK GPIO3_IO[0]	4.16 4.15 4.18
58	NAND_DATA3 QSPI_A_DATA3 GPIO3_IO[9]	4.16 4.15 4.18		57	V_SOM	5.1
60	NAND_nCE3 QSPI_B_SS1_B GPIO3_IO[4]	4.16 4.15 4.18		59	NAND_DATA5 QSPI_B_DATA1 GPIO3_IO[11]	4.16 4.15 4.18
62	NAND_CLE QSPI_B_SCLK GPIO3_IO[5]	4.16 4.15 4.18		61	NAND_DATA0 QSPI_A_DATA0 GPIO3_IO[6]	4.16 4.15 4.18
64	PWRBTN	5.2.1		63	NAND_DATA6 QSPI_B_DATA2 GPIO3_IO[12]	4.16 4.15 4.18
66	POR_B	5.3		65	NAND_nCE0 QSPI_A_SS0_B GPIO3_IO[1]	4.16 4.15 4.18
68	GPIO1_IO[09]	4.18		67	NAND_DQS QSPI_A_DQS GPIO3_IO[14]	4.16 4.15 4.18
70	GPIO1_IO[11]	4.18		69	NAND_DATA7 QSPI_B_DATA3 GPIO3_IO[13]	4.16 4.15 4.18
72	GND	5.1		71	V_SOM	5.1
74	ENET_TX_CTL GPIO1_IO[22]	4.4.1 4.18		73	ENET_TD3 GPIO1_IO[18]	4.4.1 4.18
76	ENET_MDC GPIO1_IO[16]	4.4.1 4.18		75	ENET_TD0 GPIO1_IO[21]	4.4.1 4.18
78	ENET_TD1 GPIO1_IO[20]	4.4.1 4.18		77	ENET_TD2 GPIO1_IO[19]	4.4.1 4.18
80	ENET_RXC GPIO1_IO[25]	4.4.1 4.18		79	ENET_RX_CTL GPIO1_IO[24]	4.4.1 4.18

82	GND	5.1		81	ENET_TXC GPIO1_IO[23]	4.4.1 4.18
84	ENET_RD2 GPIO1_IO[28]	4.4.1 4.18		83	ENET_RD1 GPIO1_IO[27]	4.4.1 4.18
86	ENET_RD0 GPIO1_IO[26]	4.4.1 4.18		85	ENET_RD3 GPIO1_IO[29]	4.4.1 4.18
88	ENET_MDIO GPIO1_IO[17]	4.4.1 4.18		87	V_SOM	5.1
90	GPIO1_IO[10]	4.18		89	ECSPI2_MISO UART4_CTS_B GPIO5_IO[12]	4.13 4.11 4.18
92	SD2_nCD GPIO2_IO[12]	4.10 4.18		91	ECSPI2_SS0 UART4_RTS_B GPIO5_IO[13]	4.13 4.11 4.18
94	EXT_SD2_DATA2 GPIO2_IO[17]	4.10 4.18		93	ECSPI2_SCLK UART4_RXD GPIO5_IO[10]	4.13 4.11 4.18
96	EXT_SD2_CLK GPIO2_IO[13]	4.10 4.18		95	ECSPI2_MOSI UART4_TXD GPIO5_IO[11]	4.13 4.11 4.18
98	EXT_SD2_DATA3 GPIO2_IO[18]	4.10 4.18		97	EXT_SD2_DATA0 GPIO2_IO[15]	4.10 4.18
100	EXT_SD2_CMD GPIO2_IO[14]	4.10 4.18		99	EXT_SD2_DATA1 GPIO2_IO[16]	4.10 4.18

6.2 Mating Connectors

Table 43 Connector type

UCM-iMX8 connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1,P2	2x B2B, 2x50 cont., 0.4mm pitch, Plug connector	Hirose	DF40HC(3.0)-100DS-0.4V(51)

6.3 Mechanical Drawings

Figure 3 UCM-iMX8 top

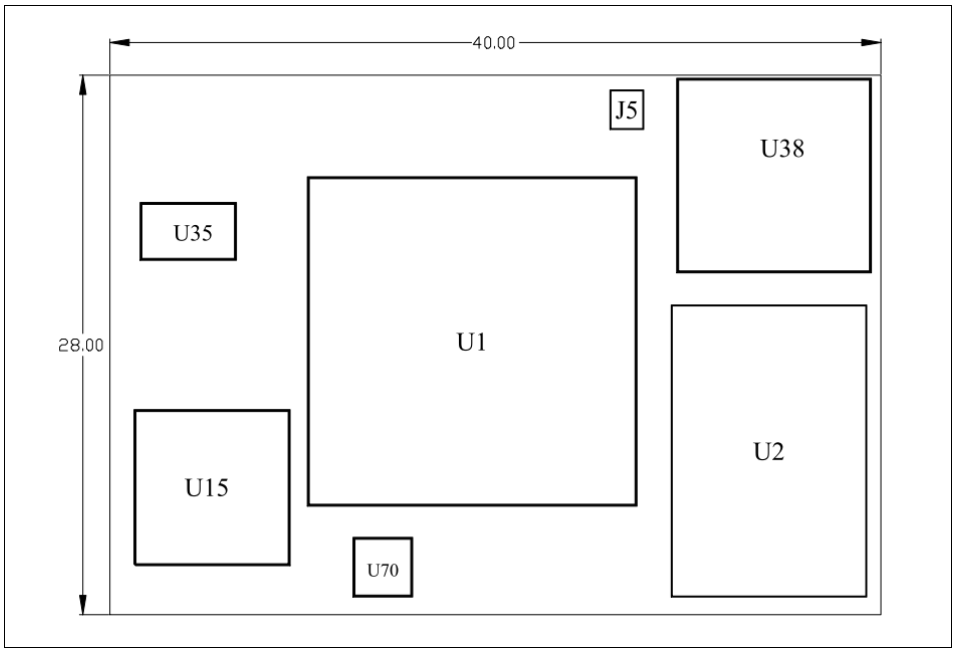
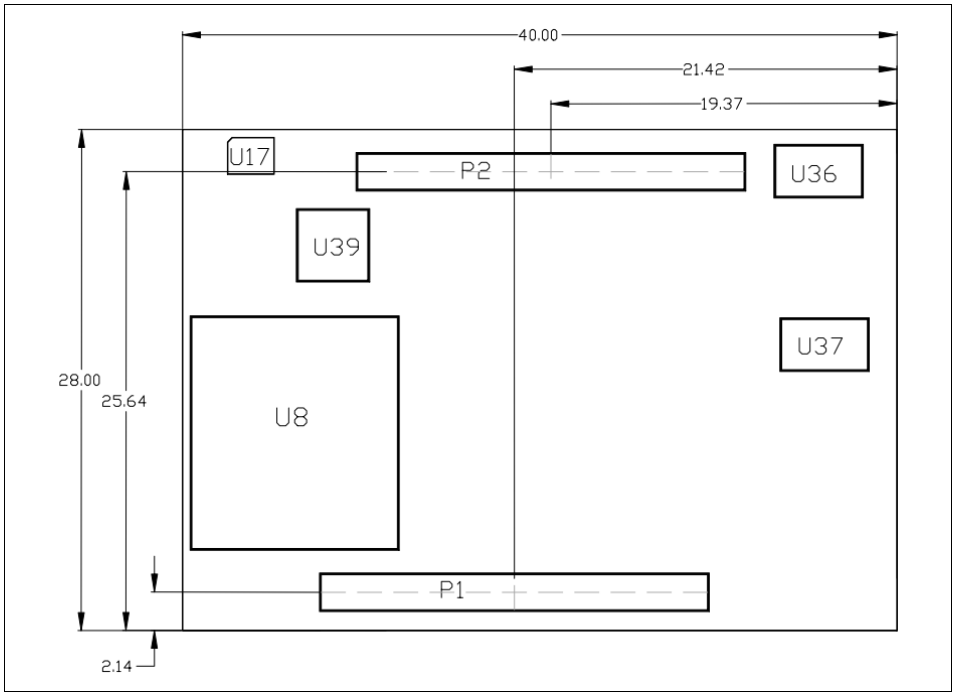


Figure 4 UCM-iMX8 bottom



1. All dimensions are in millimeters.
2. The height of all components is < 2.2mm.
3. Baseboard connectors provide 3 ± 0.15mm board-to-board clearance.
4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format at https://www.compulab.com/products/computer-on-modules/ucm-imx8-nxp-i-mx-8m-som-system-on-module-computer/#devres

6.4 Heat Spreader and Cooling Solutions

CompuLab provides UCM-iMX8 with an optional heat-spreader assembly. The UCM-iMX8 heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the UCM-iMX8 temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 44 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 45 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.6	3.8	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 ESD Performance

Table 46 ESD Performance

Interface	ESD Performance
iMX8M pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)
SD pins	2kV Human Body Model (HBM), 1500V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX8 operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX8.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB3.0: DP/DM and SS_TX/SS_RX have impedance requirement of 90 ohms.
  - All single-ended signals: have impedance requirement of 50 ohms.
  - PCIe TX/RX data pairs: have impedance requirement of 85 ohms.
  - Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI): have impedance requirement of 100 ohms.
- Be careful when placing components under the UCM-iMX8 module. The carrier board interface connector provides 3mm mating height. Bear in mind that there are components on the underside of the UCM-iMX8.
- Refer to the SB-UCMIMX8 carrier board reference design schematics.
- It is recommended to send custom carrier board schematics to the Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX8, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX8 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.