# CL-SOM-iMX8X

Reference Guide

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# Table of Contents

**Table 1 Revision Notes**

| Date | Description |
|---|---|
| Aug 2019 | • First release |
| Sept 2019 | • Updated alternative signal multiplexing in tables 15, 22, 25, 26, 27, 30, 31, 33 and 34<br>• Added operating voltage information into sections 4.2, 4.15, 4.16 and 4.17<br>• Updated differential impedance requirements in section 8.1 |

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

# 1 INTRODUCTION

## 1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX8X System-on-Module.

## 1.2 CL-SOM-iMX8X Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-iMX8X part number: https://www.compulab.com/products/computer-on-modules/cl-som-imx8x-nxp-i-mx-8x-system-on-module-computer/#ordering.

## 1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

**Table 2 Related Documents**

| Document | Location |
|---|---|
| CL-SOM-iMX8X Developer Resources | https://www.compulab.com/products/computer-on-modules/cl-som-imx8x-nxp-i-mx-8x-system-on-module-computer/#devres |
| i.MX8X Reference Manual | https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i.mx-applications-processors/i.mx-8-processors/i.mx-8x-family-arm-cortex-a35-3d-graphics-4k-video-dsp-error-correcting-code-on-ddr:i.MX8X?tab=Documentation_Tab |
| i.MX8X Datasheet | |

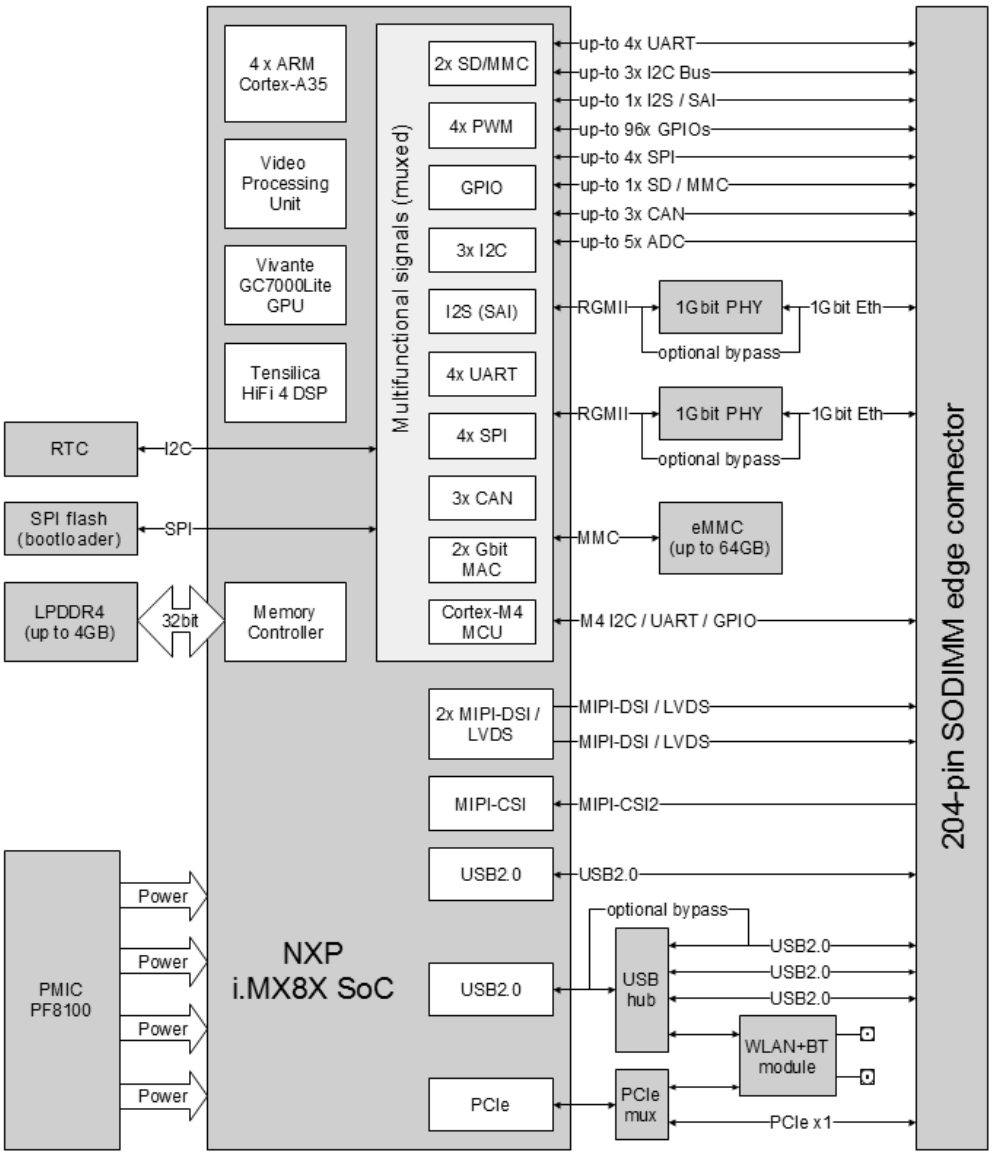
# 2 OVERVIEW

## 2.1 Highlights

- NXP i.MX 8QuadXPlus or NXP i.MX 8DualXPlus processors, up-to 1.2 GHz
- Integrated 2D/3D GPU and 4K VPU
- Real-time ARM Cortex-M4 co-processor
- Up to 4GB LPDDR4 and 64GB eMMC
- 2x MIPI-DSI / LVDS, up-to 1080p60
- Certified WiFi 802.11ac, BT 4.2
- 2x GbE, PCIe, 4x USB, 3x CAN-FD, 4x UART, 96x GPIO

## 2.2 Block Diagram

**Figure 1 CL-SOM-iMX8X Block Diagram**



## 2.3 CL-SOM-iMX8X Features

The "Option" column specifies the SoM configuration option required to have the particular feature. When a SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

**Table 3 Features and Configuration options**

| Feature | Description | Option |
|---|---|---|
| CPU Core | | |
| CPU | NXP i.MX 8QuadXPlus, quad-core ARM Cortex-A35, 1.2GHz | + |
| Video Decode | 4k H.265, 1080p H.264, VP8, MPEG4, RealVideo | C1200QM |
| Video Encode | 1080p H.264 | |
| GPU | GC7000Lite GPU<br>OpenGL 3.0, OpenGL ES 3.1, OpenCL 1.2 FP, OpenVG 1.1, Vulkan | C1200QM |
| DSP | Tensilica® HiFi 4 DSP | |
| Real-Time Coprocessor | ARM Cortex-M4F, 266 MHz | + |
| Memory and Storage | | |
| RAM | 1GB – 4GB, LPDDR4 | D |
| Storage | eMMC flash, 4GB - 64GB | N |
| Display and Camera | | |
| Display | 2x MIPI-DSI, 4 data lanes, up to 1080p60 | C1200QM |
| | Dual-channel / 2x single-channel LVDS, up to 1080p60 | |
| Touchscreen | Capacitive touch-screen support through SPI and I2C interfaces | + |
| Camera | MIPI-CSI, 4 data lanes | + |
| Network | | |
| Gigabit Ethernet | 1x Gigabit Ethernet port (MAC+PHY) | E1 |
| | 2x Gigabit Ethernet ports (MAC+PHY) | E2 |
| WiFi | Certified 802.11ac WiFi interface<br>Intel 8265 chipset<br>* mutually exclusive with PCIe port | WB |
| Bluetooth | Bluetooth 4.2 BLE | WB |
| Audio | | |
| Digital Audio | Up-to 1x I2S/SAI | + |
| | S/PDIF input/output | + |
| I/O | | |
| PCI Express | 1x PCIe Gen. 3.0<br>* mutually exclusive with WiFi | + |
| USB | 1x USB2.0 dual-role port | + |
| | Additional 1x USB2.0 host ports | Not WB and not UH |
| | Additional 3x USB2.0 host ports | UH |
| UART | Up to 4x UART | + |
| CAN bus | Up to 3x CAN-FD | + |
| MMC/SD/SDIO | Up to 1x SD / MMC | + |
| SPI | Up to 4x SPI | + |
| I2C | Up to 3x I2C | + |
| PWM | Up to 4x general purpose PWM signals | + |
| GPIO | Up to 96x GPIO (multifunctional signals shared with other functions) | + |
| ADC | 5x general-purpose ADC channels | + |
| System Logic and Debug | | |
| RTC | Real time clock, powered by external battery | + |
| JTAG | JTAG debug interface | + |

## Table 4 Electrical, Mechanical and Environmental Specifications

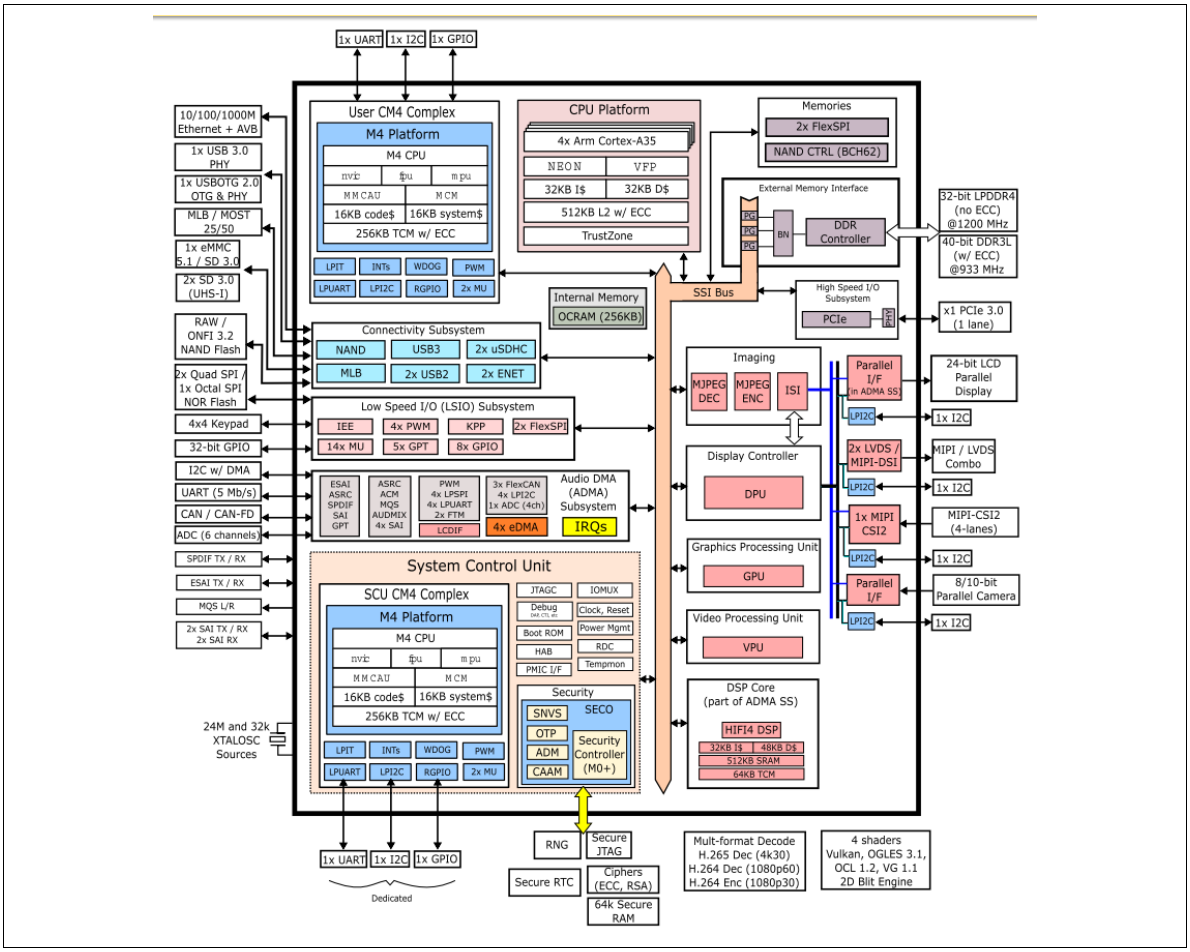
| | |
|---|---|
| Electrical Specifications | |
| Supply Voltage | 4.0V to 4.5V |
| Digital I/O voltage | 3.3V |
| Mechanical Specifications | |
| Dimensions | 38 x 68 x 5 mm |
| Weight | 14 gram |
| Connectors | 204-pin SO-DIMM edge connector |
| Environmental and Reliability | |
| MTTF | > 200,000 hours |
| Operation temperature (case) | Commercial: 0° to 70° C |
| | Extended: -20° to 70° C |
| | Industrial: -40° to 85° C |
| Storage temperature | -40° to 85° C |
| Relative humidity | 10% to 90% (operation) |
| | 05% to 95% (storage) |
| Shock | 50G / 20 ms |
| Vibration | 20G / 0 - 600 Hz |

# 3 CORE SYSTEM COMPONENTS

## 3.1 i.MX8X SoC

The i.MX8X family of processors features advanced implementation of up to quad ARM® Cortex®-A35 core which operate at speeds of up to 1.2 GHz. A general purpose Cortex®-M4 core processor enables low-power processing.

**Figure 2 i.MX8X Block Diagram**




## 3.2 Memory

### 3.2.1 DRAM

CL-SOM-iMX8X is equipped with up to 4GB of on-board LPDDR4 memory. The LPDDR4 channel is 32-bits wide and operates at 1200 MHz clock frequency (LPDDR4-2400).

### 3.2.2 Bootloader Storage

CL-SOM-iMX8X is assembled with 2MBytes of SPI NOR flash. SPI NOR flash is used to store the boot-loader and configuration blocks.

### 3.2.3 General Purpose Storage

CL-SOM-iMX8X is available with optional on-board eMMC flash of up to 64GB which can be used to store the operating system (kernel and root filesystem) and user data.

# 4 PERIPHERAL INTERFACES

CL-SOM-iMX8X implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-iMX8X SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the CL-SOM-iMX8X carrier board interface pins are multifunctional. Up to 5 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 05.5.
- All of the CL-SOM-iMX8X digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-iMX8X configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard CL-SOM-iMX8X, followed by pull value.
- **"PU" -** Always pulled up onboard CL-SOM-iMX8X, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

## 4.1 MIPI-DSI / LVDS

CL-SOM-iMX8X features two MIPI / LVDS display interfaces available on the i.MX8X SoC. The following main features are supported:

MIPI-DSI:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Programmable display resolutions, up to 1920x1200(WUXGA) @ 60 fps, 24bpp
- Multiple Peripheral Support capability, configurable virtual channels
- Video Mode Pixel Formats supported are 16bpp (RGB565), 18bpp (RGB666) packed, 18bpp (RGB666) loosely packed, 24bpp (RGB888).

LVDS:

- 4-lane LVDS Interface
- Support display resolutions up to 1920x1080 (FHD) @ 60fps, 24bpp
- Supports 18 bpp pixel format (RGB666) and 24 bpp pixel format (RGB888)

The tables below summarize the MIPI-DSI / LVDS interface signals.

**Table 5 MIPI-DSI / LVDS 0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| MIPI_DSI0_CLK_P | 33 | O | Positive part of MIPI-DSI / LVDS clock diff-pair | Always available |
| MIPI_DSI0_CLK_N | 35 | O | Negative part of MIPI-DSI / LVDS clock diff-pair | Always available |
| MIPI_DSI0_DATA0_P | 39 | O | Positive part of MIPI-DSI / LVDS 0 data diff-pair 0 | Always available |
| MIPI_DSI0_DATA0_N | 41 | O | Negative part of MIPI-DSI / LVDS 0 data diff-pair 0 | Always available |
| MIPI_DSI0_I2C0_SCL | 43* | O | Dedicated display 0 I2C clock | Always available |
| MIPI_DSI0_I2C0_SDA | 49* | IO | Dedicated display 0 I2C data | Always available |
| MIPI_DSI0_DATA1_P | 45 | O | Positive part of MIPI-DSI / LVDS 0 data diff-pair 1 | Always available |
| MIPI_DSI0_DATA1_N | 47 | O | Negative part of MIPI-DSI / LVDS 0 data diff-pair 1 | Always available |
| MIPI_DSI0_DATA2_P | 51 | O | Positive part of MIPI-DSI / LVDS 0 data diff-pair 2 | Always available |
| MIPI_DSI0_DATA2_N | 53 | O | Negative part of MIPI-DSI / LVDS 0 data diff-pair 2 | Always available |
| MIPI_DSI0_DATA3_P | 57 | O | Positive part of MIPI-DSI / LVDS 0 data diff-pair 3 | Always available |
| MIPI_DSI0_DATA3_N | 59 | O | Negative part of MIPI-DSI / LVDS 0 data diff-pair 3 | Always available |
| MIPI_DSI0_GPIO0_01 | 74* | IO | Dedicated GPIO signal for display interface 0 | Always available |
| MIPI_DSI0_GPIO0_00 | 76* | IO | Dedicated GPIO signal for display interface 0 | Always available |

**Table 6 MIPI-DSI / LVDS 1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| MIPI_DSI1_DATA0_P | 21 | O | Positive part of MIPI-DSI / LVDS 1 clock diff-pair 0 | Always available |
| MIPI_DSI1_DATA0_N | 23 | O | Negative part of MIPI-DSI / LVDS 1 clock diff-pair 0 | Always available |
| MIPI_DSI1_GPIO0_01 | 27* | IO | Dedicated GPIO signal for display interface 1 | Always available |
| MIPI_DSI1_GPIO0_00 | 29* | IO | Dedicated GPIO signal for display interface 1 | Always available |
| MIPI_DSI1_CLK_P | 77 | O | Positive part of MIPI-DSI / LVDS 1 clock diff-pair | Always available |

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| MIPI_DSI1_CLK_N | 79 | O | Negative part of MIPI-DSI / LVDS 1 clock diff-pair | Always available |
| MIPI_DSI1_DATA1_P | 93 | O | Positive part of MIPI-DSI / LVDS 1 data diff-pair 1 | Always available |
| MIPI_DSI1_DATA1_N | 95 | O | Negative part of MIPI-DSI / LVDS 1 data diff-pair 1 | Always available |
| MIPI_DSI1_I2C0_SCL | 151* | O | Dedicated display 1 I2C clock | Always available |
| MIPI_DSI1_I2C0_SDA | 153* | IO | Dedicated display 1 I2C data | Always available |
| MIPI_DSI1_DATA2_P | 155 | O | Positive part of MIPI-DSI / LVDS 1 data diff-pair 2 | Always available |
| MIPI_DSI1_DATA2_N | 157 | O | Negative part of MIPI-DSI / LVDS 1 data diff-pair 2 | Always available |
| MIPI_DSI1_DATA3_P | 161 | O | Positive part of MIPI-DSI / LVDS 1 data diff-pair 3 | Always available |
| MIPI_DSI1_DATA3_N | 163 | O | Negative part of MIPI-DSI / LVDS 1 data diff-pair 3 | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.2 MIPI-CSI

CL-SOM-iMX8X MIPI-CSI interface is derived from the four-lane MIPI CSI host controller integrated into the i.MX8X SoC. The controller supports the following main features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol, Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Up-to four data lanes and one clock lane
- Supports high speed mode(80Mbps - 1.5Gbps) per lane
- Includes high speed deserializers
- Supports primary and secondary image format:
  - YUV420, YUV422, YUV444 of 8-bits and 12-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14

Please refer to the i.MX8X Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

**Table 6 MIPI-CSI Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| MIPI_CSI0_GPIO0_00 | 73* | IO | Dedicated GPIO signal for MIPI-CSI | Always available |
| MIPI_CSI0_GPIO0_01 | 75* | IO | Dedicated GPIO signal for MIPI-CSI | Always available |
| MIPI_CSI0_DATA0_P | 83 | I | Positive part of MIPI-CSI data diff-pair 0 | Always available |
| MIPI_CSI0_DATA0_N | 85 | I | Negative part of MIPI-CSI data diff-pair 0 | Always available |
| MIPI_CSI0_DATA1_P | 89 | I | Positive part of MIPI-CSI data diff-pair 1 | Always available |
| MIPI_CSI0_DATA1_N | 91 | I | Negative part of MIPI-CSI data diff-pair 1 | Always available |
| MIPI_CSI0_DATA2_P | 101 | I | Positive part of MIPI-CSI data diff-pair 2 | Always available |
| MIPI_CSI0_DATA2_N | 103 | I | Negative part of MIPI-CSI data diff-pair 2 | Always available |

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| MIPI_CSI0_CLK_P | 107 | I | Positive part of MIPI-CSI clock diff-pair | Always available |
| MIPI_CSI0_CLK_N | 109 | I | Negative part of MIPI-CSI clock diff-pair | Always available |
| MIPI_CSI0_DATA3_N | 113 | I | Negative part of MIPI-CSI data diff-pair 3 | Always available |
| MIPI_CSI0_DATA3_P | 115 | I | Positive part of MIPI-CSI data diff-pair 3 | Always available |
| MIPI_CSI0_I2C0_SCL | 167*^ | O | Dedicated camera I2C clock | Always available |
| MIPI_CSI0_I2C0_SDA | 169*^ | IO | Dedicated camera I2C data | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

**NOTE: Pins denoted with "^" operate at 1.8V voltage level**

## 4.3 Ethernet

CL-SOM-iMX8X incorporates two optional full-featured 10/100/1000 Ethernet interfaces, implemented with the i.MX8X MAC.

### 4.3.1 Gigabit Ethernet

CL-SOM-iMX8X features one (“E1” configuration option) or two (“E2” configuration option) onboard AR8033 PHYs which support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports all IEEE 1588 frames - inside the MAC
- Automatic channel swap (ACS)

The tables below summarize the GbE interface signals.

**Table 8 GbE 1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ETH1_LED2_ACT | 4 | O;PD | Activity LED driver. 2.5V signal | E1 or E2 |
| ETH1_MDI0N | 6 | IO | Negative part of 100ohm diff-pair 0 | E1 or E2 |
| ETH1_MDI0P | 8 | IO | Positive part of 100ohm diff-pair 0 | E1 or E2 |
| ETH1_MDI1N | 12 | IO | Negative part of 100ohm diff-pair 1 | E1 or E2 |
| ETH1_MDI1P | 14 | IO | Positive part of 100ohm diff-pair 1 | E1 or E2 |
| ETH1_LED1_1000 | 16 | O;PD | Activity LED driver. 2.5V signal | E1 or E2 |
| ETH1_MDI2N | 18 | IO | Negative part of 100ohm diff-pair 2 | E1 or E2 |
| ETH1_MDI2P | 20 | IO | Positive part of 100ohm diff-pair 2 | E1 or E2 |
| ETH1_LED3_10_100 | 22 | O;PD | Activity LED driver. 2.5V signal | E1 or E2 |
| ETH1_MDI3N | 24 | IO | Negative part of 100ohm diff-pair 3 | E1 or E2 |
| ETH1_MDI3P | 26 | IO | Positive part of 100ohm diff-pair 3 | E1 or E2 |

**Table 9 GbE 2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ETH2_LED5_ACT | 25 | O;PD | Activity LED driver. 2.5V signal | E2 |
| ETH2_MDI0N | 30 | IO | Negative part of 100ohm diff-pair 0 | E2 |
| ETH2_MDI0P | 32 | IO | Positive part of 100ohm diff-pair 0 | E2 |
| ETH2_MDI1N | 36 | IO | Negative part of 100ohm diff-pair 1 | E2 |
| ETH2_MDI1P | 38 | IO | Positive part of 100ohm diff-pair 1 | E2 |
| ETH2_LED6_10_100 | 34 | O;PU | Activity LED driver. 2.5V signal | E2 |
| ETH2_MDI2N | 42 | IO | Negative part of 100ohm diff-pair 2 | E2 |
| ETH2_MDI2P | 44 | IO | Positive part of 100ohm diff-pair 2 | E2 |
| ETH2_LED4_1000 | 40 | O;PD | Activity LED driver. 2.5V signal | E2 |
| ETH2_MDI3N | 48 | IO | Negative part of 100ohm diff-pair 3 | E2 |
| ETH2_MDI3P | 50 | IO | Positive part of 100ohm diff-pair 3 | E2 |

### 4.3.2 RGMII

When CL-SOM-iMX8X is assembled without the “E1” or “E2” configuration options, the i.MX8X RGMII and MDIO signals are routed to the carrier board interface.

Please refer to the i.MX8X Reference manual for additional details.

The tables below summarize the RGMII interface signals.

**Table 7 MDIO Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ENET_MDC | 52* | O | Provides a timing reference to the PHY for data transfers on the MDIO signal | Not E2 |
| ENET_MDIO | 97* | IO | Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset | Not E2 |

**Table 8 RGMII 1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ENET1_RGMII_RXD0 | 20* | I | Ethernet input data from the PHY | Not E1 and not E2 |
| ENET1_RGMII_RXD1 | 4* | I | Ethernet input data from the PHY | Not E1 and not E2 |
| ENET1_RGMII_RXD2 | 18* | I | Ethernet input data from the PHY | Not E1 and not E2 |
| ENET1_RGMII_RXD3 | 20* | I | Ethernet input data from the PHY | Not E1 and not E2 |
| ENET1_RGMII_RX_CTL | 26* | I | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode) | Not E1 and not E2 |
| ENET1_RGMII_RXC | 24* | I | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE | Not E1 and not E2 |
| ENET1_RGMII_TXD0 | 16* | O | Ethernet output data to PHY | Not E1 and not E2 |
| ENET1_RGMII_TXD1 | 12* | O | Ethernet output data to PHY | Not E1 and not E2 |
| ENET1_RGMII_TXD2 | 62* | O | Ethernet output data to PHY | Not E1 and not E2 |
| ENET1_RGMII_TXD3 | 14* | O | Ethernet output data to PHY | Not E1 and not E2 |
| ENET1_RGMII_TXC | 8* | O | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE | Not E1 and not E2 |
| ENET1_RGMII_TX_CTL | 6* | O | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode) | Not E1 and not E2 |
| EPHY1_RGMII_VDDH | 2 | P | RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements | Not E1 and not E2 |

**Table 9 RGMII 2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ENET2_RGMII_RXD0 | 34* | I | Ethernet input data from the PHY | Not E2 |
| ENET2_RGMII_RXD1 | 25* | I | Ethernet input data from the PHY | Not E2 |
| ENET2_RGMII_RXD2 | 42* | I | Ethernet input data from the PHY | Not E2 |
| ENET2_RGMII_RXD3 | 44* | I | Ethernet input data from the PHY | Not E2 |
| ENET2_RGMII_RX_CTL | 50* | I | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode) | Not E2 |
| ENET2_RGMII_RXC | 48* | I | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE | Not E2 |
| ENET2_RGMII_TXD0 | 40* | O | Ethernet output data to PHY | Not E2 |
| ENET2_RGMII_TXD1 | 36* | O | Ethernet output data to PHY | Not E2 |
| ENET2_RGMII_TXD2 | 31* | O | Ethernet output data to PHY | Not E2 |
| ENET2_RGMII_TXD3 | 38* | O | Ethernet output data to PHY | Not E2 |
| ENET2_RGMII_TXC | 32* | O | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE | Not E2 |
| ENET2_RGMII_TX_CTL | 30* | O | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode) | Not E2 |
| EPHY2_RGMII_VDDH | 54* | P | RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements | Not E2 |

**NOTE: 2.5V or 3.3V power must be supplied via the EPHY_RGMII_VDDH pins if any of the RGMII signals are used on the carrier-board**

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.4 Wireless Interfaces

CL-SOM-iMX8X optional 802.11ac WLAN and Bluetooth 4.2 functions are implemented with Intel Dual Band Wireless-AC 8265 chipset (M.2 1216 module).

The WLAN sub-system is interfaced with the i.MX8X SoC through a multiplexed PCIe interface. On-board multiplexing allows to route the PCIe interface either to the WLAN module or to the SODIMM connector. Multiplexing is controlled by signal PCIE_DEV_SEL (SODIMM pin #81).

**Table 10 WiFi and PCIe multiplexing logic**

| PCIE_DEV_SEL | PCIe routing | Operation mode |
|---|---|---|
| High | WLAN | Utilize on-board WLAN modules |
| Low | SODIMM interface connector | Utilize PCIe interface for an external device |

The Bluetooth sub-system is interfaced with the i.MX8X SoC via USB interface.

Depending on USB hub configuration options, Bluetooth is connected either directly to i.MX8X SoC or via USB hub.

**Table 11 Bluetooth and USB ports**

| On-board USB hub ("UH" option) | Bluetooth USB port connection | Number of external USB |
|---|---|---|
| Present | Connected to hub | 1 SoC port + 3 hub ports |
| Not present | Connected to SoC | 1 SoC port |

CL-SOM-iMX8X is equipped with two MHF4 high-frequency connectors allowing easy integration with external antennas:

- Primary (MAIN) WLAN/BT antenna connector ANT2. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality.
- Secondary (AUX) WLAN antenna connector ANT1. Can be used with any type of 2.4GHz/5.0GHz antenna for dual-band WLAN functionality

**Table 12 ANT1 and ANT2 connector data**

| Manufacturer | Mfg. P/N | Mating Connector |
|---|---|---|
| Hirose | W.FL2-R-MT(60) | Hirose W.FL2-LP-062HF |

### 4.4.1 Wireless certification

Intel 8265 M.2 1216 module is certified for usage in most world regions. For Intel 8265 certification documentation:

- Follow https://www.intel.com/content/www/us/en/support/articles/000007443/network-and-i-o/wireless-networking.html
- Expand the "Current Adapter" section
- Expand the "Intel® Dual Band Wireless-AC 8265" sub-section
- Download 8265D2W documents

**NOTE: CL-SOM-iMX8X WiFi and Bluetooth functions are available only with the 'WB' ordering option**

**NOTE: CL-SOM-iMX8X WiFi and PCIe functions are mutually exclusive**

## 4.5 PCI Express

CL-SOM-iMX8X provides one PCI Express port. The port is routed to the carrier board interface connector via on-board multiplexer.

On CL-SOM-iMX8X assembled with on-board WiFi/Bluetooth ("WB" option) PCIe interface can be routed either to the WLAN module or to the SODIMM connector. Multiplexing is controlled by signal PCIE_DEV_SEL (SODIMM pin #81).

On CL-SOM-iMX8X assembled without on-board WiFi/Bluetooth, PCIe interface is always available on the SODIMM connector.

The table below summarizes PCIe interface signals.

**Table 13 PCIe Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| PCIE_CTRL0_PERST_B | 192 | AO | PCI Express reset signal | Always available |
| PCIE_CTRL0_CLKREQ_B | 173 | AI | PCI Express clock request signal | Always available |
| PCIE_CTRL0_WAKE_B | 194 | AI | PCI Express wake signal | Always available |
| PCIE0_TX0_P | 125 | AO | PCI Express transmit data positive | Always available |
| PCIE0_TX0_N | 127 | AO | PCI Express transmit data negative | Always available |
| PCIE0_RX0_P | 131 | AI | PCI Express receive data positive | Always available |
| PCIE0_RX0_N | 133 | AI | PCI Express receive data negative | Always available |
| PCIE_REFCLK100M_P | 119 | AO | PCI Express clock positive signal | Always available |
| PCIE_REFCLK100M_N | 121 | AO | PCI Express clock negative signal | Always available |
| PCIE_DEV_SEL | 81 | I | PCIe multiplexing select signal | Always available |

**NOTE: CL-SOM-iMX8X WiFi and PCIe functions are mutually exclusive**

## 4.6 S/PDIF

CL-SOM-iMX8X provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8X Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

**Table 14 S/PDIF Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SPDIF0_EXT_CLK | 200* | IO | External clock signal | Always available |
| SPDIF0_RX | 20* | I | SPDIF input data line signal | Always available |
| SPDIF0_TX | 26* | O | SPDIF output data line signal | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.7 Digital Audio (SAI)

CL-SOM-iMX8X enables access to the i.MX8X integrated synchronous audio interface (SAI) module. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line.
- One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Asynchronous 64 × 32-bit FIFO for each transmit and receive data line

Please refer to the i.MX8X Reference manual for additional details. The table below summarizes the SAI interface signals.

**Table 15 SAI1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SAI1_TXC | 137* | O | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | Always available |
| | 108* | | | Always available |
| SAI1_TXD | 139* | O | Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word | Always available |
| | 60* | | | Always available |
| | 102* | | | Always available |
| SAI1_RXD | 143* | I | Receive data, sampled synchronously by the bit clock | Always available |
| | 106* | | | Always available |

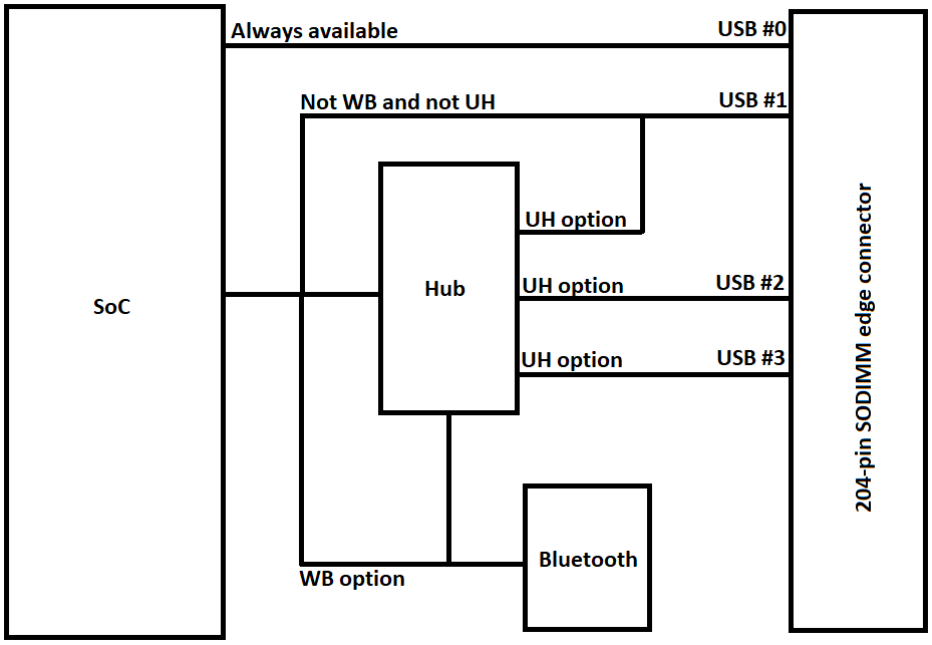
| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SAI1_RXFS | 145* | O | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | Always available |
| | 126* | | | Always available |
| | 104* | | | Always available |
| SAI1_RXC | 100* | O | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | Always available |
| | 128* | | | Always available |
| | 137* | | | Always available |
| SAI1_TXFS | 110* | O | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | Always available |
| | 145* | | | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.8 USB

CL-SOM-iMX8X features up-to four USB ports. One port is implemented directly with USB interface of the i.MX8X SoC. Additional ports are implemented with an optional USB2.0 hub.

**Figure 3 CL-SOM-iMX8X USB options diagram**




The table below summarizes availability of USB ports with different configuration options.

**Table 16 USB ports with different configuration options**

| Interface\Configuration | not UH and not WB | UH, not WB | WB, not UH | WB and UH |
|---|---|---|---|---|
| USB port #0 | Available | Available | Available | Available |
| USB port #1 | Available | Available | Not available | Available |
| USB port #2 | Not available | Available | Not available | Available |
| USB port #3 | Not available | Available | Not available | Available |

The tables below summarize the USB interface signals.

**Table 17 USB2.0 port #0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| USB_OTG_DN | 178* | IO | USB2.0 negative data | Always available |
| USB_OTG_DP | 176* | IO | USB2.0 positive data | Always available |

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| USB_OTG_ID | 174 | I | USB2.0 ID signal | Always available |
| USB_OTG_VBUS | 180 | I | USB2.0 VBUS detect | Always available |

**Table 18 USB2.0 port #1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| HUBUSB_DN1 | 170 | IO | USB2.0 negative data 1 | see table 19 |
| HUBUSB_DP1 | 172 | IO | USB2.0 positive data 1 | see table 19 |

**Table 19 USB2.0 port #2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| HUBUSB_DN2 | 164 | IO | USB2.0 negative data 2 | Only with 'UH' option |
| HUBUSB_DP2 | 166 | IO | USB2.0 positive data 2 | Only with 'UH' option |

**Table 20 USB2.0 port #3 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| HUBUSB_DN3 | 158 | IO | USB2.0 negative data 3 | Only with 'UH' option |
| HUBUSB_DP3 | 160 | IO | USB2.0 positive data 3 | Only with 'UH' option |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.9 MMC / SD /SDIO

One MMC/SD/SDIO port is available through the CL-SOM-iMX8X carrier board interface. The port is derived from the i.MX8X on-chip MMC / SD / SDIO controller (uSDHC). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v4.2/v4.3/v4.4/v4.41/v5.0/v5.1.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to 25MB/s.
- 1-bit or 4-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes.
- Dedicated card detection, write protection and Reset signals.

Please refer to the i.MX8X Reference manual for additional details.

The table below summarizes the MMC / SD / SDIO interface signals.

**Table 21 MMC/SD/SDIO Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| USDHC1_CD_B | 61* | I | Card detection pin | Always available |
| USDHC1_WP | 67* | I | Card write protect detection | Always available |
| USDHC1_CLK | 80* | O | Clock for MMC/SD/SDIO card | Always available |
| USDHC1_CMD | 82* | O | CMD line connect to card | Always available |
| USDHC1_DATA0 | 84* | IO | DATA0 line in all modes. Also used to detect busy state | Always available |
| USDHC1_DATA1 | 86* | IO | DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode | Always available |
| USDHC1_DATA2 | 88* | IO | DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode | Always available |
| USDHC1_DATA3 | 90* | IO | DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode. | Always available |
| USDHC1_RESET_B | 154* | O | Card hardware reset signal, active LOW | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.10 UART

CL-SOM-iMX8X enables access to up-to four i.MX8X UART interfaces. The i.MX8X UART module supports the following key features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- 7, 8, 9, or 10-bit data characters (7-bits only with parity)
- Hardware flow control support for a request to send and clear to send signals.

**NOTE: By default UART0 is assigned to be used as the main debug console port**

Please refer to the i.MX8X Reference manual for additional details.

The tables below summarize the UART interface signals.

**Table 22 UART0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| UART0_RX | 117* | I | UART-0 serial data receive | Always available |
| UART0_TX | 111* | O | UART-0 serial data transmit | Always available |
| UART0_RTS_B | 108* | I | UART-0 request to send | Always available |
| UART0_CTS_B | 110* | O | Clear to send | Always available |

**Table 23 UART1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| UART1_CTS_B | 15* | I | UART-1 clear to send | Always available |
| UART1_RTS_B | 17* | O | UART-1 request to send | Always available |
| UART1_RX | 13* | I | UART-1 serial data receive | Always available |
| UART1_TX | 11* | O | UART-1 serial data transmit | Always available |

**Table 24 UART2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| UART2_TX | 3* | O | UART-2 serial data transmit | Always available |
| UART2_RX | 5* | I | UART-2 serial data receive | Always available |

**Table 25 UART3 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| UART3_TX | 7* | I | UART-3 serial data transmit | Always available |
| | 86* | | | Always available |
| | 128* | | | Always available |
| UART3_RX | 9* | O | UART-3 serial data receive | Always available |
| | 80* | | | Always available |
| | 126* | | | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.11 CAN Bus

CL-SOM-iMX8X provides up to three CAN bus interfaces implemented with the i.MX8X integrated FlexCAN module. The following features are supported by the FlexCAN module:

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B
- Flexible mailboxes configurable to store 0 to 8, 16, 32 or 64 bytes data length
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8X reference manual for additional details.

**Table 26 CAN bus #0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| FLEXCAN0_RX | 108* | I | FLEXCAN receive pin | Always available |
| | 117* | | | Always available |
| FLEXCAN0_TX | 110* | O | FLEXCAN transmit pin | Always available |
| | 111* | | | |

**Table 27 CAN bus #1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| FLEXCAN1_RX | 139* | I | FLEXCAN receive pin | Always available |
| | 5* | | | Always available |
| FLEXCAN1_TX | 143* | O | FLEXCAN transmit pin | Always available |
| | 3* | | | Always available |

**Table 28 CAN bus #2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| FLEXCAN2_RX | 126* | I | FLEXCAN receive pin | Always available |
| FLEXCAN2_TX | 128* | O | FLEXCAN transmit pin | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.12 I2C

CL-SOM-iMX8X features up-to three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Support the original 100KHz mode, 400KHz fast-mode, 3.4MHz high-speed mode
- and 5MHz ultra fast-mode (with appropriate pads) Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Direct Memory Access (DMA) support

Please refer to the i.MX8X Reference manual for additional details.

The tables below summarize the I2C interface signals.

**Table 29 I2C0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| I2C0_SCL | 73* | O | I2C serial clock line | Always available |
| I2C0_SDA | 75* | IO | I2C serial data line | Always available |

**Table 30 I2C1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| I2C1_SCL | 129* | O | I2C serial clock line | Always available |
| | 74* | | | Always available |
| I2C1_SDA | 135* | IO | I2C serial data line | Always available |
| | 76* | | | Always available |

**Table 31 I2C3 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| I2C3_SCL | 179* | O | I2C serial clock line | Always available |
| | 142* | | | Always available |
| I2C3_SDA | 181* | IO | Always available | Always available |
| | 144* | | | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.13 SPI

Up-to four SPI interfaces are accessible through the CL-SOM-iMX8X carrier board interface. The SPI interfaces are derived from i.MX8X integrated low power Serial Peripheral Interface (LPSPI). Each instance of the LPSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Master operation supporting up to 4 peripheral chip select
- Slave operation
- Command/transmit FIFO of 64 words
- Receive FIFO of 64 words
- Support for full and half duplex transfers supporting 1-bit transmit and receive on each clock edge
- Support for half duplex transfers supporting 2-bit or 4-bit transmit or receive on each clock edge (master only)

Please refer to the i.MX8X Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

**Table 32 SPI0 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SPI0_CS0 | 58* | O | SPI0 chip select 0 | Always available |
| SPI0_CS1 | 60* | O | SPI0 chip select 1 | Always available |
| SPI0_SDI | 63* | I | SPI0 slave data in | Always available |
| SPI0_SDO | 65* | O | SPI0 slave data out | Always available |
| SPI0_SCK | 69* | O | SPI0 slave clock | Always available |

**Table 33 SPI1 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SPI1_SCK | 98* | O | SPI1 slave clock | Always available |
| | 124* | | | Always available |
| SPI1_SDO | 100* | O | SPI1 slave data out | Always available |
| SPI1_SDI | 102* | I | SPI1 slave data in | Always available |
| | 179* | | | Always available |
| SPI1_CS0 | 104* | O | SPI1 chip select 0 | Always available |
| | 181* | | | Always available |
| SPI1_CS1 | 106* | O | SPI1 chip select 1 | Always available |

**Table 34 SPI2 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SPI2_SCK | 116* | O | SPI2 slave clock | Always available |
| | 144* | | | Always available |
| | 154* | | | Always available |
| SPI2_SDO | 118* | O | SPI2 slave data out | Always available |
| | 148* | | | Always available |
| SPI2_SDI | 120* | I | SPI2 slave data in | Always available |
| | 67* | | | Always available |
| | 146* | | | Always available |
| SPI2_CS0 | 122* | O | SPI2 chip select 0 | Always available |
| | 61* | | | Always available |
| | 142* | | | Always available |
| SPI2_CS1 | 124* | O | SPI2 chip select 1 | Always available |

**Table 35 SPI3 Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| SPI3_SCK | 134* | O | SPI3 slave clock | Always available |
| SPI3_SDO | 136* | O | SPI3 slave data out | Always available |
| SPI3_SDI | 138* | I | SPI3 slave data in | Always available |
| SPI3_CS0 | 140* | O | SPI3 chip select 0 | Always available |
| SPI3_CS1 | 142* | O | SPI3 chip select 1 | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.14 PWM

CL-SOM-iMX8X features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8X Reference manual for additional details.

The table below summarizes the PWM interface signals.

**Table 36 PWM Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| PWM0_OUT | 11* | O | PWM functional output | Always available |
| PWM1_OUT | 13* | O | PWM functional output | Always available |
| PWM2_OUT | 17* | O | PWM functional output | Always available |
| PWM3_OUT | 15* | O | PWM functional output | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

## 4.15 ADC

CL-SOM-iMX8X enables access to the i.MX8X integrated 12-bit Analog-to-Digital Converter. Following main features are supported:

- Linear successive approximation algorithm
- Channel support for up to 64 analog input channels for conversion of external pins and from internal sources
- Channel scaling allows input voltage levels higher than the ADC reference voltage
- Configurable analog input sample time
- Trigger detect with up to 8 trigger sources with priority level configuration. Software or hardware trigger option for each.
- Automatic compare for less-than, greater-than, within range, or out-of-range with "store on true" and "repeat until true" options
- 16-entry conversion result data FIFO with configurable watermark and overflow detection
- Interrupt, DMA or polled operation

Please refer to the i.MX8X Reference manual for additional details. The table below summarizes the ADC interface signals.

**Table 37 ADC Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ADC_IN0 | 191* | AI | ADC interface input | Always available |
| ADC_IN1 | 193* | AI | ADC interface input | Always available |
| ADC_IN2 | 197* | AI | ADC interface input | Always available |
| ADC_IN3 | 199* | AI | ADC interface input | Always available |
| ADC_IN4 | 201* | AI | ADC interface input | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document**

**NOTE: All ADC signals operate at 1.8V voltage level**

## 4.16 JTAG

CL-SOM-iMX8X enables access to the i.MX8X JTAG port through the carrier board interface.

Please refer to the i.MX8X Reference manual for additional details.

The table below summarizes the JTAG interface signals.

**Table 38 JTAG Signals**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| JTAG_NTRST | 56 | I | Test Reset | Always available |
| JTAG_TCK | 66 | O | Test Clock | Always available |
| JTAG_TDI | 70 | I | Test Data In | Always available |
| JTAG_TDO | 72 | O | Test Data Out | Always available |
| JTAG_TMS | 68 | O | Test Mode Select | Always available |

**NOTE: All JTAG signals operate at 1.8V voltage level**

## 4.17 GPIO

Up-to 96 of the i.MX8X general purpose input/output (GPIO) signals are available through the CL-SOM-iMX8X carrier board interface.
Please refer to the i.MX8X Reference manual for additional details.
The table below summarizes the GPIO interface signals.

**Table 39 GPIO Signals**

| Signal Name | Pin # | Type | Description | Voltage domain | Availability |
|---|---|---|---|---|---|
| GPIO0_IO01 | 62*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO0_IO02 | 6*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO03 | 14*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO04 | 24*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO05 | 20*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO06 | 18*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO07 | 4*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO08 | 16*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO09 | 12*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO10 | 22*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO11 | 26*^ | IO | GPIO | EPHY1_RGMII_VDDH | Not E1 and not E2 |
| GPIO0_IO12 | 200* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO13 | 134* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO14 | 136* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO15 | 138* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO16 | 140* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO19 | 146* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO20 | 148* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO21 | 11* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO22 | 13* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO24 | 15* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO25 | 100* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO26 | 102* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO27 | 104* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO28 | 124* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO29 | 106* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO30 | 137* | IO | GPIO | 3.3V | Always available |
| GPIO0_IO31 | 145* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO00 | 122* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO01 | 118* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO02 | 120* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO03 | 116* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO04 | 69* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO05 | 63* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO06 | 65* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO07 | 60* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO08 | 58* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO09 | 193* | IO | GPIO | 1.8V | Always available |
| GPIO1_IO10 | 191* | IO | GPIO | 1.8V | Always available |
| GPIO1_IO11 | 199* | IO | GPIO | 1.8V | Always available |
| GPIO1_IO12 | 197* | IO | GPIO | 1.8V | Always available |
| GPIO1_IO15 | 108* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO16 | 110* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO17 | 139* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO18 | 143* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO19 | 126* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO20 | 128* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO21 | 117* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO22 | 111* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO23 | 3* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO24 | 5* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO25 | 43* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO26 | 49* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO27 | 76* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO28 | 74* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO29 | 151* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO30 | 153* | IO | GPIO | 3.3V | Always available |
| GPIO1_IO31 | 29* | IO | GPIO | 3.3V | Always available |
| GPIO2_IO00 | 27* | IO | GPIO | 3.3V | Always available |
| GPIO2_IO03 | 9* | IO | GPIO | 3.3V | Always available |

| Signal Name | Pin # | Type | Description | Voltage domain | Availability |
|---|---|---|---|---|---|
| GPIO3_IO00 | 98* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO01 | 112* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO02 | 179* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO03 | 181* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO04 | 175* | IO | GPIO | 1.8V | Always available |
| GPIO3_IO05 | 167* | IO | GPIO | 1.8V | Always available |
| GPIO3_IO06 | 169* | IO | GPIO | 1.8V | Always available |
| GPIO3_IO07 | 75* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO08 | 73* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO13 | 130* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO17 | 92* | IO | GPIO | 3.3V | Always available |
| GPIO3_IO18 | 94* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO01 | 173* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO03 | 156* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO05 | 162* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO19 | 154* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO21 | 67* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO22 | 61* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO23 | 80* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO24 | 82* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO25 | 84* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO26 | 86* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO27 | 88* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO28 | 90* | IO | GPIO | 3.3V | Always available |
| GPIO4_IO29 | 32*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO4_IO30 | 30*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO4_IO31 | 40*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO00 | 36*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO01 | 31*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO02 | 38*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO03 | 48*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO04 | 50*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO05 | 34*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO06 | 25*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO07 | 42*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO08 | 44*^ | IO | GPIO | EPHY2_RGMII_VDDH | Not E2 |
| GPIO5_IO09 | 152* | IO | GPIO | 3.3V | Always available |

**NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document**

**NOTE: 3.3V power must be supplied via the EPHY_RGMII_VDDH pins if any of the GPIO signals denoted with "^" are used on the carrier-board**

# 5 SYSTEM LOGIC

## 5.1 Power Supply

**Table 40 Power signals**

| Signal Name | Pin# | Type | Description |
|---|---|---|---|
| V_SOM | 19, 10, 19, 28, 37, 46, 55, 64, 71, 78, 87, 96, 105, 114, 123, 132, 141, 150, 159, 168, 177, 186, 195 | P | Main power supply. Connect to a regulated DC supply |
| V_RTC | 183 | P | RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND. |
| GND | 19, 37, 55, 71, 87, 105, 123, 141, 159, 177, 195 | P | Common ground |
| EXT_PHY0_VDDH | 2 | P | RGMII interface power supply input. When on-board PHY is not present, this pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements |
| EXT_PHY1_VDDH | 54 | P | RGMII interface power supply input. When on-board PHY is not present, this pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements |

## 5.2 System and Miscellaneous Signals

To be added in a future version of this document.

## 5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX8X. Please refer to the i.MX8X Reference manual for additional details.

**Table 41 Reset signal**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| COLD_RESET_IN | 171 | I | Pulled-Up Active low SoC reset signal | Always available |

## 5.4 Boot Sequence

CL-SOM-iMX8X boot sequence defines which interface/media is used by CL-SOM-iMX8X to load and execute the initial software (such as SPL or/and U-boot). CL-SOM-iMX8X can load initial software from the following interfaces/media:

- On-board boot-loader storage (SPI NOR with pre-flashed boot-loader)
- External SD card using the SD/SDIO 1 interface

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

**Table 42 Alternative Boot selection signal**

| Signal Name | Pin # | Type | Description | Availability |
|---|---|---|---|---|
| ALT_BOOT | 185 | I | Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence | Always available |
| QSPI_BOOT | 149 | I | | Always available |

**Table 43 CL-SOM-iMX8X Boot sequences**

| Sequence | ALT_BOOT (pin 185) | QSPI_BOOT (pin 149) |
|---|---|---|
| Standard (on-board SPI) | Low | High (1.8V) |
| Alternate (external SD card) | High (1.8V) | Low |

**NOTE: ALT_BOOT and QSPI_BOOT signals must be operated at 1.8V voltage levels.**

## 5.5 Signal Multiplexing Characteristics

Up to 97 of the CL-SOM-iMX8X carrier board interface pins are multifunctional. Multifunctional pins allow extensive functional flexibility by allowing usage of a single carrier board interface pin for one of several functions. Up-to 5 functions (ALT MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX8X pins are derived from the i.MX8X SoC control module.

**NOTE: Pin function selection is controlled by software.**

**NOTE: Each pin can be used for a single function at a time.**

**NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).**

**NOTE: An empty MUX mode is a "RESERVED" function and must not be used.**

### Table 44 Multifunctional Signals

| Pin# | Pin Name / ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | Availability |
|---|---|---|---|---|---|---|
| 3 | UART2_TX | FTM_CH1 | FLEXCAN1_TX | | GPIO1_IO23 | Always available |
| 4 | ESAI0_TX3_RX2 | | | ENET1_RGMII_RXD1 | GPIO0_IO07 | Not E1 and not E2 |
| 5 | UART2_RX | FTM_CH0 | FLEXCAN1_RX | | GPIO1_IO24 | Always available |
| 7 | SCU_GPIO0_01 | | | UART3_TX | SCU_WDOG0 _OUT | Always available |
| 6 | ESAI0_SCKR | | | ENET1_RGMII_TX_CTL | GPIO0_IO02 | Not E1 and not E2 |
| 8 | ESAI0_FSR | | | ENET1_RGMII_TXC | | Not E1 and not E2 |
| 9 | SCU_GPIO0_00 | | | UART3_RX | GPIO2_IO03 | Always available |
| 11 | UART1_TX | PWM0_OUT | GPT0_CAPTURE | | GPIO0_IO21 | Always available |
| 12 | ESAI0_TX5_RX0 | | | ENET1_RGMII_TXD1 | GPIO0_IO09 | Not E1 and not E2 |
| 13 | UART1_RX | PWM1_OUT | GPT0_COMPARE | GPT1_CLK | GPIO0_IO22 | Always available |
| 14 | ESAI0_SCKT | | | ENET1_RGMII_TXD3 | GPIO0_IO03 | Not E1 and not E2 |
| 15 | UART1_CTS_B | PWM3_OUT | | GPT1_COMPARE | GPIO0_IO24 | Always available |
| 16 | ESAI0_TX4_RX1 | | | ENET1_RGMII_TXD0 | GPIO0_IO08 | Not E1 and not E2E2 |
| 17 | UART1_RTS_B | PWM2_OUT | | GPT1_CAPTURE | GPT0_CLK | Always available |
| 18 | ESAI0_TX2_RX3 | | | ENET1_RGMII_RXD2 | GPIO0_IO06 | Not E1 and not E2 |
| 20 | ESAI0_TX1 | | | ENET1_RGMII_RXD3 | GPIO0_IO05 | Not E1 and not E2 |
| 22 | SPDIF0_RX | | | ENET1_RGMII_RXD0 | GPIO0_IO10 | Not E1 and not E2 |
| 24 | ESAI0_TX0 | | | ENET1_RGMII_RXC | GPIO0_IO04 | Not E1 and not E2 |
| 25 | ENET2_RGMII_RXD1 | | | | GPIO5_IO06 | Not E2 |
| 26 | SPDIF0_TX | | | ENET1_RGMII_RX_CTL | GPIO0_IO11 | Not E1 and not E2 |
| 27 | MIPI_DSI1_GPIO0_01 | I2C2_SDA | | | GPIO2_IO00 | Always available |
| 29 | MIPI_DSI1_GPIO0_00 | I2C2_SCL | MIPI_DSI1_PWM0_OUT | | GPIO1_IO31 | Always available |
| 30 | ENET2_RGMII_TX_CTL | | | | GPIO4_IO30 | Not E2 |
| 31 | ENET2_RGMII_TXD2 | | | | GPIO5_IO01 | Not E2 |
| 32 | ENET2_RGMII_TXC | | | | GPIO4_IO29 | Not E2 |
| 34 | ENET2_RGMII_RXD0 | | | | GPIO5_IO05 | Not E2 |
| 36 | ENET2_RGMII_TXD1 | | | | GPIO5_IO00 | Not E2 |
| 38 | ENET2_RGMII_TXD3 | | | | GPIO5_IO02 | Not E2 |
| 40 | ENET2_RGMII_TXD0 | | | | GPIO4_IO31 | Not E2 |
| 42 | ENET2_RGMII_RXD2 | | | | GPIO5_IO07 | Not E2 |
| 43 | MIPI_DSI0_I2C0_SCL | MIPI_DSI1_GPIO0_IO02 | | | GPIO1_IO25 | Always available |
| 44 | ENET2_RGMII_RXD3 | | | | GPIO5_IO08 | Not E2 |
| 48 | ENET2_RGMII_RXC | | | | GPIO5_IO03 | Not E2 |
| 49 | MIPI_DSI0_I2C0_SDA | MIPI_DSI1_GPIO0_IO03 | | | GPIO1_IO26 | Always available |
| 50 | ENET2_RGMII_RX_CTL | | | | GPIO5_IO04 | Not E2 |
| 58 | SPI0_CS0 | SAI0_RXD | M40_TPM0_CH1 | M40_GPIO0_IO03 | GPIO1_IO08 | Always available |
| 60 | SPI0_CS1 | SAI0_RXC | SAI1_TXD | LCD_PWM0 | GPIO1_IO07 | Always available |
| 61 | USDHC1_CD_B | | SPI2_CS0 | | GPIO4_IO22 | Always available |
| 62 | ESAI0_FST | | | ENET2_RGMII_TXD2 | GPIO0_IO01 | Not E2 |
| 63 | SPI0_SDI | SAI0_TXD | M40_TPM0_CH0 | M40_GPIO0_IO02 | GPIO1_IO05 | Always available |
| 65 | SPI0_SDO | SAI0_TXFS | M40_I2C0_SDA | M40_GPIO0_IO01 | GPIO1_IO06 | Always available |
| 67 | USDHC1_WP | | SPI2_SDI | | GPIO4_IO21 | Always available |
| 69 | SPI0_SCK | SAI0_TXC | M40_I2C0_SCL | M40_GPIO0_IO00 | GPIO1_IO04 | Always available |
| 73 | MIPI_CSI0_GPIO0_00 | I2C0_SCL | | | GPIO3_IO08 | Always available |
| 74 | MIPI_DSI0_GPIO0_01 | I2C1_SDA | | | GPIO1_IO28 | Always available |
| 75 | MIPI_CSI0_GPIO0_01 | I2C0_SDA | | | GPIO3_IO07 | Always available |
| 76 | MIPI_DSI0_GPIO0_00 | I2C1_SCL | MIPI_DSI0_PWM0_OUT | | GPIO1_IO27 | Always available |
| 80 | USDHC1_CLK | | UART3_RX | | GPIO4_IO23 | Always available |

| | | | | | | |
|---|---|---|---|---|---|---|
| 82 | USDHC1_CMD | | MQS_R | | GPIO4_IO24 | Always available |
| 84 | USDHC1_DATA0 | | MQS_L | | GPIO4_IO25 | Always available |
| 86 | USDHC1_DATA1 | | UART3_TX | | GPIO4_IO26 | Always available |
| 88 | USDHC1_DATA2 | | UART3_CTS_B | | GPIO4_IO27 | Always available |
| 90 | USDHC1_DATA3 | | UART3_RTS_B | | GPIO4_IO28 | Always available |
| 92 | QSPI0B_SCLK | QSPI1A_SCLK | KPP0_COL0 | | GPIO3_IO17 | Always available |
| 94 | QSPI0B_DATA0 | QSPI1A_DATA0 | KPP0_COL1 | | GPIO3_IO18 | Always available |
| 98 | CSI_PCLK | MIPI_CSI0_I2C0_SCL | | SPI1_SCK | GPIO3_IO00 | Always available |
| 100 | SAI0_TXD | SAI1_RXC | SPI1_SDO | | GPIO0_IO25 | Always available |
| 102 | SAI0_TXC | SAI1_TXD | SPI1_SDI | | GPIO0_IO26 | Always available |
| 104 | SAI0_RXD | SAI1_RXFS | SPI1_CS0 | | GPIO0_IO27 | Always available |
| 106 | SAI1_RXD | SAI0_RXFS | SPI1_CS1 | | GPIO0_IO29 | Always available |
| 108 | FLEXCAN0_RX | SAI2_RXC | UART0_RTS_B | SAI1_TXC | GPIO1_IO15 | Always available |
| 110 | FLEXCAN0_TX | SAI2_RXD | UART0_CTS_B | SAI1_TXFS | GPIO1_IO16 | Always available |
| 111 | UART0_TX | MQS_L | FLEXCAN0_TX | | GPIO1_IO22 | Always available |
| 112 | CSI_MCLK | MIPI_CSI0_I2C0_SDA | | SPI1_SDO | GPIO3_IO01 | Always available |
| 116 | SPI2_SCK | | | | GPIO1_IO03 | Always available |
| 117 | UART0_RX | MQS_R | FLEXCAN0_RX | | GPIO1_IO21 | Always available |
| 118 | SPI2_SDO | | | | GPIO1_IO01 | Always available |
| 120 | SPI2_SDI | | | | GPIO1_IO02 | Always available |
| 122 | SPI2_CS0 | | | | GPIO1_IO00 | Always available |
| 124 | SAI0_TXFS | SPI2_CS1 | SPI1_SCK | | GPIO0_IO28 | Always available |
| 126 | FLEXCAN2_RX | SAI3_RXD | UART3_RX | SAI1_RXFS | GPIO1_IO19 | Always available |
| 128 | FLEXCAN2_TX | SAI3_RXFS | UART3_TX | SAI1_RXC | GPIO1_IO20 | Always available |
| 130 | QSPI0A_DQS | | | | GPIO3_IO13 | Always available |
| 134 | SPI3_SCK | | | | GPIO0_IO13 | Always available |
| 136 | SPI3_SDO | | | | GPIO0_IO14 | Always available |
| 137 | SAI1_RXC | SAI1_TXC | | | GPIO0_IO30 | Always available |
| 138 | SPI3_SDI | | | | GPIO0_IO15 | Always available |
| 139 | FLEXCAN1_RX | SAI2_RXFS | FTM_CH2 | SAI1_TXD | GPIO1_IO17 | Always available |
| 140 | SPI3_CS0 | ACM_MCLK_OUT1 | | | GPIO0_IO16 | Always available |
| 142 | SPI3_CS1 | I2C3_SCL | | SPI2_CS0 | | Always available |
| 143 | FLEXCAN1_TX | SAI3_RXC | DMA0_REQ_IN0 | SAI1_RXD | GPIO1_IO18 | Always available |
| 144 | MCLK_IN1 | I2C3_SDA | | SPI2_SCK | | Always available |
| 145 | SAI1_RXFS | SAI1_TXFS | | | GPIO0_IO31 | Always available |
| 146 | MCLK_IN0 | ESAI0_RX_HF_CLK | | SPI2_SDI | GPIO0_IO19 | Always available |
| 148 | MCLK_OUT0 | ESAI0_TX_HF_CLK | | SPI2_SDO | GPIO0_IO20 | Always available |
| 151 | MIPI_DSI1_I2C0_SCL | MIPI_DSI0_GPIO0_IO02 | | | GPIO1_IO29 | Always available |
| 152 | ENET1_REFCLK_125M_25M | ENET1_PPS | ENET2_PPS | | GPIO5_IO09 | Always available |
| 153 | MIPI_DSI1_I2C0_SDA | MIPI_DSI0_GPIO0_IO03 | | | GPIO1_IO30 | Always available |
| 154 | USDHC1_RESET_B | | SPI2_SCK | | GPIO4_IO19 | Always available |
| 167 | MIPI_CSI0_I2C0_SCL | MIPI_CSI0_GPIO0_IO02 | | | GPIO3_IO05 | Always available |
| 169 | MIPI_CSI0_I2C0_SDA | MIPI_CSI0_GPIO0_IO03 | | | GPIO3_IO06 | Always available |
| 175 | MIPI_CSI0_MCLK_OUT | | | | GPIO3_IO04 | Always available |
| 179 | CSI_EN | CI_PI_CSI_I2C_SCL | I2C3_SCL | SPI1_SDI | GPIO3_IO02 | Always available |
| 181 | CSI_RESET | CI_PI_CSI_I2C_SDA | I2C3_SDA | SPI1_CS0 | GPIO3_IO03 | Always available |
| 191 | ADC_IN0 | M40_I2C0_SCL | M40_GPIO0_IO00 | | GPIO1_IO10 | Always available |
| 193 | ADC_IN1 | M40_I2C0_SDA | M40_GPIO0_IO01 | | GPIO1_IO09 | Always available |
| 197 | ADC_IN2 | M40_UART0_RX | M40_GPIO0_IO02 | ACM_MCLK_IN0 | GPIO1_IO12 | Always available |
| 199 | ADC_IN3 | M40_UART0_TX | M40_GPIO0_IO03 | ACM_MCLK_OUT0 | GPIO1_IO11 | Always available |
| 201 | ADC_IN4 | M40_TPM0_CH0 | M40_GPIO0_IO04 | | GPIO1_IO14 | Always available |
| 200 | SPDIF0_EXT_CLK | | | ENET2_REFCLK_125M_25M | GPIO0_IO12 | Always available |

## 5.6 RTC

CL-SOM-iMX8X features an on-board ultra-low-power EM3027 real time clock (RTC). The RTC is connected to the i.MX8X SoC using I2C1 interface at address 56h.

Back-up power supply should be connected to V_RTC power rail in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about CL-SOM-iMX8X RTC please refer to the EM3027 datasheet.

## 5.7 LED

CL-SOM-iMX8X features a single general purpose green LED controlled by GPIO1_IO13 signal of the i.MX8X. The LED is ON when GPIO1_IO13 is logic LOW. During CL-SOM-iMX8X boot, the system LED is powered on by SCFW firmware.

## 5.8 Reserved Signals

The following CL-SOM-iMX8X signals are reserved and must be left unconnected.

**Table 45 Reserved Signals**

| Signal Name | Pin# | Description |
|---|---|---|
| RESERVED | 182 ,184, 188, 190 | Signals reserved for future implementation of USB3.0 interface |
| RESERVED | 189, 196, 203 | Signals reserved for future use |

# 6 CARRIER BOARD INTERFACE

The CL-SOM-iMX8X CoM/SoM carrier board interface uses 2 x 100 Pin carrier board connectors. The SoM pinout is detailed in the table below.

## 6.1 Connectors Pinout

**Table 46 Connector P1**

| Pin # | CL-SOM-iMX8X Signal Functions | Ref. | | Pin # | CL-SOM-iMX8X Signal Functions | Ref. |
|---|---|---|---|---|---|---|
| 1 | GND | | | 2 | EPHY2_RGMII_VDDH<br>EXT_PHY0_VDDH | |
| 3 | UART2_TX<br>FLEXCAN1_TX<br>GPIO1_IO23 | | | 4 | ESAI0_TX3_RX2<br>ETH1_LED2_ACT<br>ENET2_RGMII_RXD1<br>GPIO0_IO07 | |
| 5 | UART2_RX<br>FLEXCAN1_RX<br>GPIO1_IO24 | | | 6 | ESAI0_SCKR<br>ETH1_MDI0N<br>ENET2_RGMII_TX_CTL | |
| 7 | SCU_GPIO0_01<br>UART3_TX<br>SCU_WDOG0 _OUT | | | 8 | ESAI0_FSR<br>ETH1_MDI0P<br>ENET2_RGMII_TXC<br>GPIO0_IO02 | |
| 9 | SCU_GPIO0_00<br>UART3_RX<br>GPIO2_IO03 | | | 10 | V_SOM | |
| 11 | UART1_TX<br>PWM0_OUT<br>GPIO0_IO21 | | | 12 | ESAI0_TX5_RX0<br>ETH1_MDI1N<br>ENET2_RGMII_TXD1<br>GPIO0_IO09 | |
| 13 | UART1_RX<br>PWM1_OUT<br>GPIO0_IO22 | | | 14 | ESAI0_SCKT<br>ETH1_MDI1P<br>ENET2_RGMII_TXD3<br>GPIO0_IO03 | |
| 15 | UART1_CTS_B<br>PWM3_OUT<br>GPIO0_IO24 | | | 16 | ESAI0_TX4_RX1<br>ETH1_LED1_1000<br>ENET2_RGMII_TXD0<br>GPIO0_IO08 | |
| 17 | UART1_RTS_B<br>PWM2_OUT<br>GPT0_CLK | | | 18 | ESAI0_TX2_RX3<br>ETH1_MDI2N<br>ENET2_RGMII_RXD2<br>GPIO0_IO06 | |
| 19 | GND | | | 20 | ESAI0_TX1<br>ETH1_MDI2P<br>ENET2_RGMII_RXD3<br>SPDIF0_RX<br>GPIO0_IO05 | |
| 21 | MIPI_DSI1_DATA0_P | | | 22 | SPDIF0_RX<br>ETH1_LED3_10_100<br>GPIO0_IO10 | |
| 23 | MIPI_DSI1_DATA0_N | | | 24 | ESAI0_TX0<br>ETH1_MDI3N<br>ENET2_RGMII_RXC<br>GPIO0_IO04 | |
| 25 | ENET1_RGMII_RXD1<br>ETH2_LED5_ACT<br>GPIO5_IO06 | | | 26 | SPDIF0_TX<br>ETH1_MDI3P<br>ENET2_RGMII_RX_CTL<br>SPDIF0_TX<br>GPIO0_IO11 | |
| 27 | MIPI_DSI1_GPIO0_01<br>GPIO2_IO00 | | | 28 | V_SOM | |
| 29 | MIPI_DSI1_GPIO0_00<br>GPIO1_IO31 | | | 30 | ENET1_RGMII_TX_CTL<br>ETH2_MDI0N<br>GPIO4_IO30 | |
| 31 | ENET1_RGMII_TXD2<br>GPIO5_IO01 | | | 32 | ENET1_RGMII_TXC<br>ETH2_MDI0P<br>GPIO4_IO29 | |
| 33 | MIPI_DSI0_CLK_P | | | 34 | ENET1_RGMII_RXD0<br>ETH2_LED6_10_100 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | GPIO5_IO05 | |
| 35 | MIPI_DSI0_CLK_N | | | 36 | ENET1_RGMII_TXD1<br>ETH2_MDI1N<br>GPIO5_IO00 | |
| 37 | GND | | | 38 | ENET1_RGMII_TXD3<br>ETH2_MDI1P<br>GPIO5_IO02 | |
| 39 | MIPI_DSI0_DATA0_P | | | 40 | ENET1_RGMII_TXD0<br>ETH2_LED4_1000<br>GPIO4_IO31 | |
| 41 | MIPI_DSI0_DATA0_N | | | 42 | ENET1_RGMII_RXD2<br>ETH2_MDI2N<br>GPIO5_IO07 | |
| 43 | MIPI_DSI0_I2C0_SCL<br>GPIO1_IO25 | | | 44 | ENET1_RGMII_RXD3<br>ETH2_MDI2P<br>GPIO5_IO08 | |
| 45 | MIPI_DSI0_DATA1_P | | | 46 | V_SOM | |
| 47 | MIPI_DSI0_DATA1_N | | | 48 | ENET1_RGMII_RXC<br>ETH2_MDI3N<br>GPIO5_IO03 | |
| 49 | MIPI_DSI0_I2C0_SDA<br>GPIO1_IO26 | | | 50 | ENET1_RGMII_RX_CTL<br>ETH2_MDI3P<br>GPIO5_IO04 | |
| 51 | MIPI_DSI0_DATA2_P | | | 52 | ENET0_MDC | |
| 53 | MIPI_DSI0_DATA2_N | | | 54 | EPHY1_RGMII_VDDH | |
| 55 | GND | | | 56 | SBC_JTAG_NTRST | |
| 57 | MIPI_DSI0_DATA3_P | | | 58 | SPI0_CS0<br>GPIO1_IO08 | |
| 59 | MIPI_DSI0_DATA3_N | | | 60 | SPI0_CS1<br>SAI1_TXD<br>GPIO1_IO07 | |
| 61 | USDHC1_CD_B<br>SPI2_CS0<br>GPIO4_IO22 | | | 62 | ESAI0_FST<br>ENET2_RGMII_TXD2<br>GPIO0_IO01 | |
| 63 | SPI0_SDI<br>GPIO1_IO05 | | | 64 | V_SOM | |
| 65 | SPI0_SDO<br>GPIO1_IO06 | | | 66 | JTAG_TCK | |
| 67 | USDHC1_WP<br>SPI2_SDI<br>GPIO4_IO21 | | | 68 | JTAG_TMS | |
| 69 | SPI0_SCK<br>GPIO1_IO04 | | | 70 | JTAG_TDI | |
| 71 | GND | | | 72 | JTAG_TDO | |
| 73 | MIPI_CSI0_GPIO0_00<br>I2C0_SCL<br>GPIO3_IO08 | | | 74 | MIPI_DSI0_GPIO0_01<br>I2C1_SCL<br>GPIO1_IO28 | |
| 75 | MIPI_CSI0_GPIO0_01<br>I2C0_SDA<br>GPIO3_IO07 | | | 76 | MIPI_DSI0_GPIO0_00<br>I2C1_SDA<br>GPIO1_IO27 | |
| 77 | MIPI_DSI1_CLK_P | | | 78 | V_SOM | |
| 79 | MIPI_DSI1_CLK_N | | | 80 | USDHC1_CLK<br>UART3_RX<br>GPIO4_IO23 | |
| 81 | PCIE_DEV_SEL | | | 82 | USDHC1_CMD<br>GPIO4_IO24 | |
| 83 | MIPI_CSI0_DATA0_P | | | 84 | USDHC1_DATA0<br>GPIO4_IO25 | |
| 85 | MIPI_CSI0_DATA0_N | | | 86 | USDHC1_DATA1<br>UART3_TX<br>GPIO4_IO26 | |
| 87 | GND | | | 88 | USDHC1_DATA2<br>GPIO4_IO27 | |
| 89 | MIPI_CSI0_DATA1_P | | | 90 | USDHC1_DATA3<br>GPIO4_IO28 | |
| 91 | MIPI_CSI0_DATA1_N | | | 92 | QSPI0B_SCLK<br>GPIO3_IO17 | |
| 93 | MIPI_DSI1_DATA1_P | | | 94 | QSPI0B_DATA0<br>GPIO3_IO18 | |
| 95 | MIPI_DSI1_DATA1_N | | | 96 | V_SOM | |
| 97 | ENET0_MDIO | | | 98 | CSI_PCLK<br>SPI1_SCK<br>GPIO3_IO00 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 99 | TAMPER_IN0 | | | 100 | SAI0_TXD<br>SAI1_RXC<br>SPI1_SDO<br>GPIO0_IO25 | |
| 101 | MIPI_CSI0_DATA2_P | | | 102 | SAI0_TXC<br>SAI1_TXD<br>SPI1_SDI<br>GPIO0_IO26 | |
| 103 | MIPI_CSI0_DATA2_N | | | 104 | SAI0_RXD<br>SAI1_RXFS<br>SPI1_CS0<br>GPIO0_IO27 | |
| 105 | GND | | | 106 | SAI1_RXD<br>SPI1_CS1<br>GPIO0_IO29 | |
| 107 | MIPI_CSI0_CLK_P | | | 108 | FLEXCAN0_RX<br>SAI1_TXC<br>UART0_RTS_B<br>GPIO1_IO15 | |
| 109 | MIPI_CSI0_CLK_N | | | 110 | FLEXCAN0_TX<br>SAI1_TXFS<br>UART0_CTS_B<br>GPIO1_IO16 | |
| 111 | UART0_TX<br>FLEXCAN0_TX<br>GPIO1_IO22 | | | 112 | CSI_MCLK<br>GPIO3_IO01 | |
| 113 | MIPI_CSI0_DATA3_N | | | 114 | V_SOM | |
| 115 | MIPI_CSI0_DATA3_P | | | 116 | SPI2_SCK<br>GPIO1_IO03 | |
| 117 | UART0_RX<br>FLEXCAN0_RX<br>GPIO1_IO21 | | | 118 | SPI2_SDO<br>GPIO1_IO01 | |
| 119 | PCIE_REFCLK100M_P | | | 120 | SPI2_SDI<br>GPIO1_IO02 | |
| 121 | PCIE_REFCLK100M_N | | | 122 | SPI2_CS0<br>GPIO1_IO00 | |
| 123 | GND | | | 124 | SAI0_TXFS<br>SPI2_CS1<br>SPI1_SCK<br>GPIO0_IO28 | |
| 125 | PCIE0_TX0_P | | | 126 | FLEXCAN2_RX<br>SAI1_RXFS<br>UART3_RX<br>GPIO1_IO19 | |
| 127 | PCIE0_TX0_N | | | 128 | FLEXCAN2_TX<br>SAI1_RXC<br>UART3_TX<br>GPIO1_IO20 | |
| 129 | I2C1_SCL | | | 130 | QSPI0A_DQS<br>GPIO3_IO13 | |
| 131 | PCIE0_RX0_P | | | 132 | V_SOM | |
| 133 | PCIE0_RX0_N | | | 134 | SPI3_SCK<br>GPIO0_IO13 | |
| 135 | I2C1_SDA | | | 136 | SPI3_SDO<br>GPIO0_IO14 | |
| 137 | SAI1_RXC<br>SAI1_TXC<br>GPIO0_IO30 | | | 138 | SPI3_SDI<br>GPIO0_IO15 | |
| 139 | FLEXCAN1_RX<br>SAI1_TXD<br>GPIO1_IO17 | | | 140 | SPI3_CS0<br>GPIO0_IO16 | |
| 141 | GND | | | 142 | SPI3_CS1<br>I2C3_SCL<br>SPI2_CS0 | |
| 143 | FLEXCAN1_TX<br>SAI1_RXD<br>GPIO1_IO18 | | | 144 | MCLK_IN1<br>I2C3_SDA<br>SPI2_SCK | |
| 145 | SAI1_RXFS<br>SAI1_TXFS<br>GPIO0_IO31 | | | 146 | MCLK_IN0<br>SPI2_SDI<br>GPIO0_IO19 | |
| 147 | PMIC_STANDBY | | | 148 | MCLK_OUT0<br>SPI2_SDO<br>GPIO0_IO20 | |
| 149 | QSPI_BOOT | | | 150 | V_SOM | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 151 | MIPI_DSI1_I2C0_SCL<br>GPIO1_IO29 | | | 152 | ENET1_REFCLK_125M_25M<br>GPIO5_IO09 | |
| 153 | MIPI_DSI1_I2C0_SDA<br>GPIO1_IO30 | | | 154 | USDHC1_RESET_B<br>SPI2_SCK<br>GPIO4_IO19 | |
| 155 | MIPI_DSI1_DATA2_P | | | 156 | GPIO4_IO03 | |
| 157 | MIPI_DSI1_DATA2_N | | | 158 | HUBUSB_DN3 | |
| 159 | GND | | | 160 | HUBUSB_DP3 | |
| 161 | MIPI_DSI1_DATA3_P | | | 162 | GPIO4_IO05 | |
| 163 | MIPI_DSI1_DATA3_N | | | 164 | HUBUSB_DN2 | |
| 165 | SOC_ON_OFF | | | 166 | HUBUSB_DP2 | |
| 167 | MIPI_CSI0_I2C0_SCL<br>GPIO3_IO05 | | | 168 | V_SOM | |
| 169 | MIPI_CSI0_I2C0_SDA<br>GPIO3_IO06 | | | 170 | HUBUSB_DN1 | |
| 171 | COLD_RESET_IN | | | 172 | HUBUSB_DP1 | |
| 173 | PCIE_CTRL0_CLKREQ_B | | | 174 | USB_OTG_ID | |
| 175 | MIPI_CSI0_MCLK_OUT<br>GPIO3_IO04 | | | 176 | USB_OTG_DP | |
| 177 | GND | | | 178 | USB_OTG_DN | |
| 179 | CSI_EN<br>I2C3_SCL<br>SPI1_SDI<br>GPIO3_IO02 | | | 180 | USB_OTG_VBUS | |
| 181 | CSI_RESET<br>I2C3_SDA<br>SPI1_CS0<br>GPIO3_IO03 | | | 182 | RESERVED | |
| 183 | V_RTC | | | 184 | RESERVED | |
| 185 | ALT_BOOT | | | 186 | V_SOM | |
| 187 | TAMPER_OUT0 | | | 188 | RESERVED | |
| 189 | RESERVED | | | 190 | RESERVED | |
| 191 | ADC_IN0<br>GPIO1_IO10 | | | 192 | PCIE_CTRL0_PERST_B | |
| 193 | ADC_IN1<br>GPIO1_IO09 | | | 194 | PCIE_CTRL0_WAKE_B | |
| 195 | GND | | | 196 | RESERVED | |
| 197 | ADC_IN2<br>GPIO1_IO12 | | | 198 | SOC_RESET_OUT | |
| 199 | ADC_IN3<br>GPIO1_IO11 | | | 200 | SPDIF0_EXT_CLK<br>GPIO0_IO12 | |
| 201 | ADC_IN4<br>GPIO1_IO14 | | | 202 | PMIC_PWRON | |
| 203 | RESERVED | | | 204 | V_SOM | |

## 6.2 Mating Connectors

### Table 47 Connector type

| CL-SOM-iMX8X connector | | Carrier board (mating) connector P/N | |
|---|---|---|---|
| Ref. | Implementation | Mfg. | P/N |
| P1 | 2-sides PCB based SODIMM-204 edge connector | Lotes | AAA-DDR-109-K01 |

## 6.3 Mechanical Drawings

**Figure 4 CL-SOM-iMX8X top**

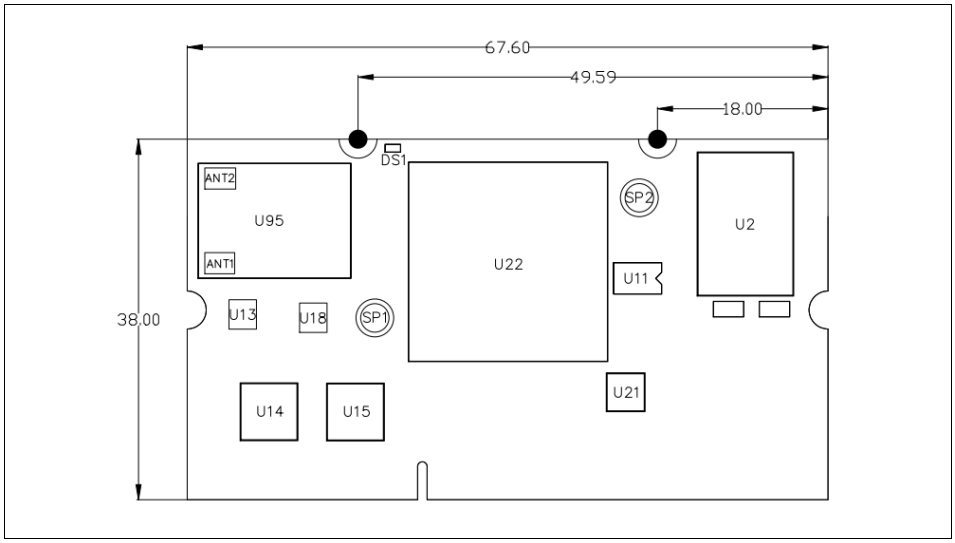
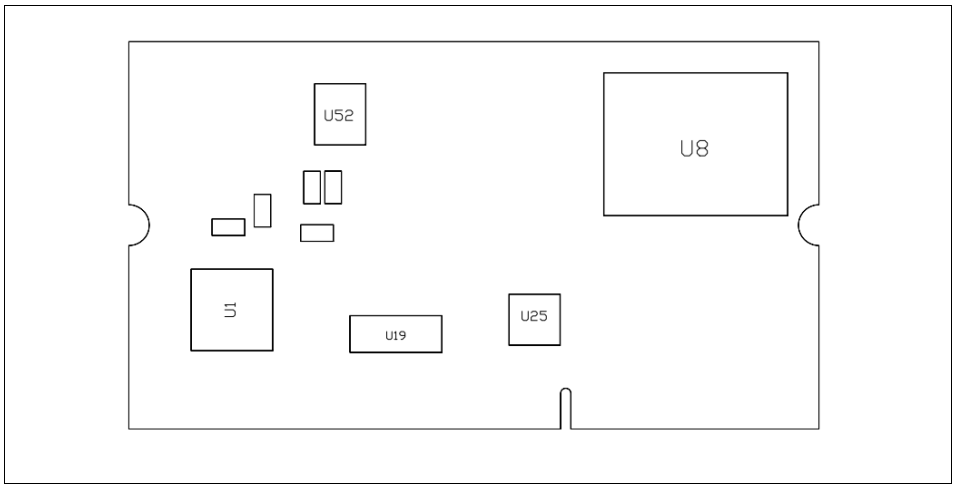



**Figure 5 CL-SOM-iMX8X bottom**




1. All dimensions are in millimeters.
2. The height of components on top side is < 3.0mm.
3. The height of components on bottom side is < 2.0mm.
4. Carrier-board connectors provide 2.8 ± 0.25mm board-to-board clearance.
5. Board thickness is 1.0mm.

Mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/cl-som-imx8x-nxp-i-mx-8x-system-on-module-computer/#devres

## 6.4 Standoffs/Spacers

CL-SOM-iMX8X has two semi-circular mounting holes to physically secure the SoM to the carrier board. Secure CL-SOM-iMX8X to the carrier board by mounting two spacers with any adequate screws and nuts.

## 6.5 Heat Spreader and Cooling Solutions

CompuLab provides CL-SOM-iMX8X with an optional heat-spreader assembly. The CL-SOM-iMX8X heat-spreader is designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the CL-SOM-iMX8X temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

# 7 OPERATIONAL CHARACTERISTICS

## 7.1 Absolute Maximum Ratings

**Table 48 Absolute Maximum ratings**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Main power supply voltage (V_SOM) | -0.3 | 4.8 | V |
| Voltage on any non-power supply pin | -0.5 | 3.6 | V |
| Backup battery supply voltage (V_RTC) | -0.3 | 3.6 | V |

**NOTE: Exceeding absolute maximum ratings may damage the device.**

## 7.2 Recommended Operating Conditions

**Table 49 Recommended Operating Conditions**

| Parameter | Min | Typ. | Max | Unit |
|---|---|---|---|---|
| Main power supply voltage (V_SOM) | 4.0 | 4.2 | 4.5 | V |
| Backup battery supply voltage (V_RTC) | 1.8 | 3.0 | 3.3 | V |

## 7.3 ESD Performance

**Table 50 ESD Performance**

| Interface | ESD Performance |
|---|---|
| i.MX8X pins | 2kV Human Body Model (HBM), 500V Charge Device Model (CDM) |

# 8 APPLICATION NOTES

## 8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between V_SOM and GND near the carrier-board connector.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI, MIPI-DSI and PCIe clocks signals require 100 ohm differential impedance.
- The carrier board interface connectors provide 2.8mm mating height. Bear in mind that there are components on the bottom side of CL-SOM-iMX8X. It is not recommended to place any components underneath the CL-SOM-iMX8X module.
- Refer to the SB-iMX8X carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

## 8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check whether the system starts properly. In system larger than the minimum, check the following potential issues:

- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX8X, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-iMX8X carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.