UCM-iMX8M-Mini

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
Jan 2019	• First release
May 2019	• Added section 7.3 (typical power consumption) • Updated PCI Express signal description in section 4.5
June 2019	• Fixed VCC_RTC description in section 5.1
July 2019	• Fixed MMC / SD / SDIO feature description in section 4.9 • Added notes on internal pull up/down limitation in sections 4.16 and 5.5
Aug 2019	• Fixed signals types in sections 4.1 and 4.2
Feb 2020	• Removed P1-97 and P1-99 from table 32 in section 4.16
May 2020	• Fixed antenna connector type in section 4.4
Jan 2021	• Added deep sleep power consumption in section 7.3
Feb 2021	• Updated reset description in table 35 in section 5.3 • Added voltage level information in table 34 in section 5.2.1

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab UCM-iMX8M-Mini System-on-Module.

1.2 UCM-iMX8M-Mini Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the UCM-iMX8M-Mini part number: https://www.compulab.com/products/computer-on-modules/ucm-imx8m-mini-nxp-i-mx-8m-mini-som-system-on-module-computer/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
UCM-iMX8M-Mini Developer Resources	https://www.compulab.com/products/computer-on-modules/ucm-imx8m-mini-nxp-i-mx-8m-mini-som-system-on-module-computer/#devres
i.MX8M Mini Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-mini-family-arm-cortex-a53-cortex-m4-audio-voice-video:i.MX8MMINI?tab=Documentation_Tab
i.MX8M Mini Datasheet	

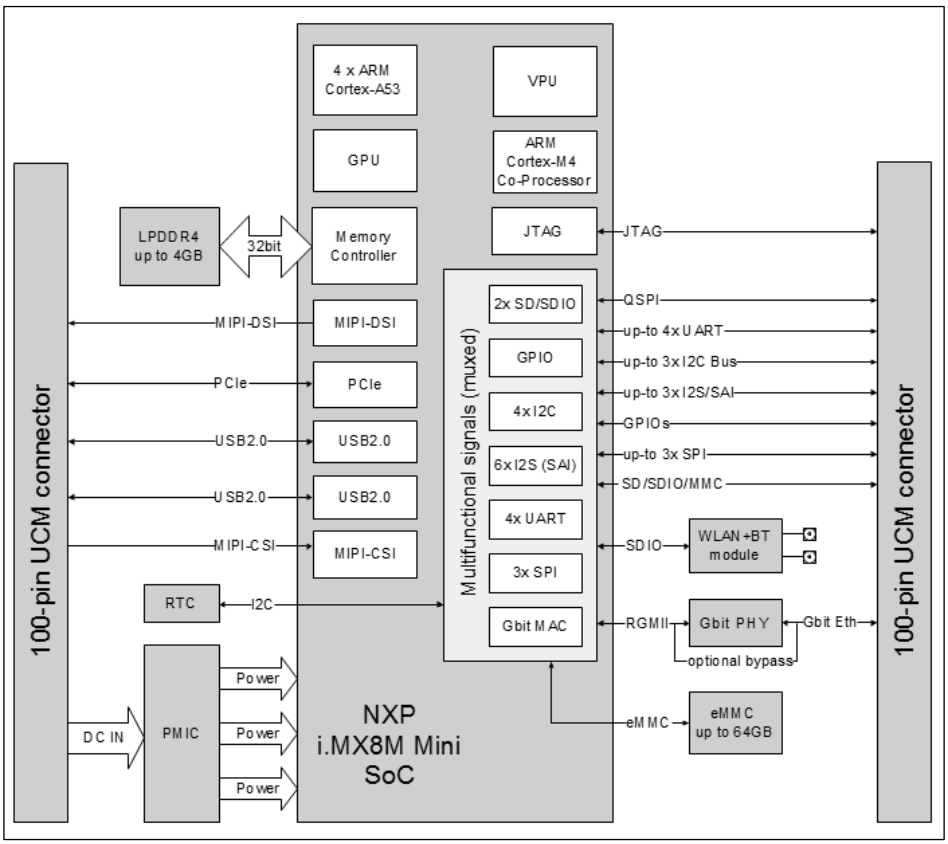
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Mini Processor, up-to 1.8GHz
- Up to 4GB LPDDR4 and 64GB eMMC
- Integrated 2D/3D GPU and 1080p VPU
- MIPI-DSI, up to 1080p60, MIPI-CSI camera input
- PCIe, GbE, 2x USB, 4x UART, 85x GPIO
- Certified dual-band WiFi 802.11ac, BT 4.2
- Tiny size and weight - 28 x 38 x 4 mm, 7 gram

2.2 Block Diagram

Figure 1 UCM-iMX8M-Mini Block Diagram



2.3 UCM-iMX8M-Mini Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Mini DualLite, dual-core ARM Cortex-A53, 1.8GHz	C1800D
	NXP i.MX8M Mini Dual, dual-core ARM Cortex-A53, 1.8GHz	C1800DM
	NXP i.MX8M Mini Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
Video Decode	1080p60 H.265, H.264, VP8, VP9	C1800DM or 1800QM
Video Encode	1080p60 H.264, VP8	C1800DM or 1800QM
GPU	GC NanoUltra GPU OpenGL ES 2.0, Open VG 1.1	+
Real-Time Co-processor	ARM Cortex-M4	+
Memory and Storage		
RAM	1GB – 4GB, LPDDR4	D
Storage	eMMC flash, 4GB - 64GB	N
Display and Camera		
Display	MIPI-DSI, 4 data lanes, up to 1080p60	+
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	MIPI-CSI, 4 lanes	+
Network		
Ethernet	Gigabit Ethernet port (MAC+PHY)	+
WiFi	Certified 802.11ac WiFi interface Broadcom BCM43353 chipset	WB
Bluetooth	Bluetooth 4.2 BLE	
Audio		
Digital Audio	Up-to 3x I2S / SAI	+
	S/PDIF input/output	+
I/O		
PCI Express	PCIe x1 Gen. 2.1	+
USB	2x USB2.0 dual-role ports	+
Serial Ports (UARTs)	Up to 4x UART	+
MMC/SD/SDIO	Up to 1x MMC/SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 85x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

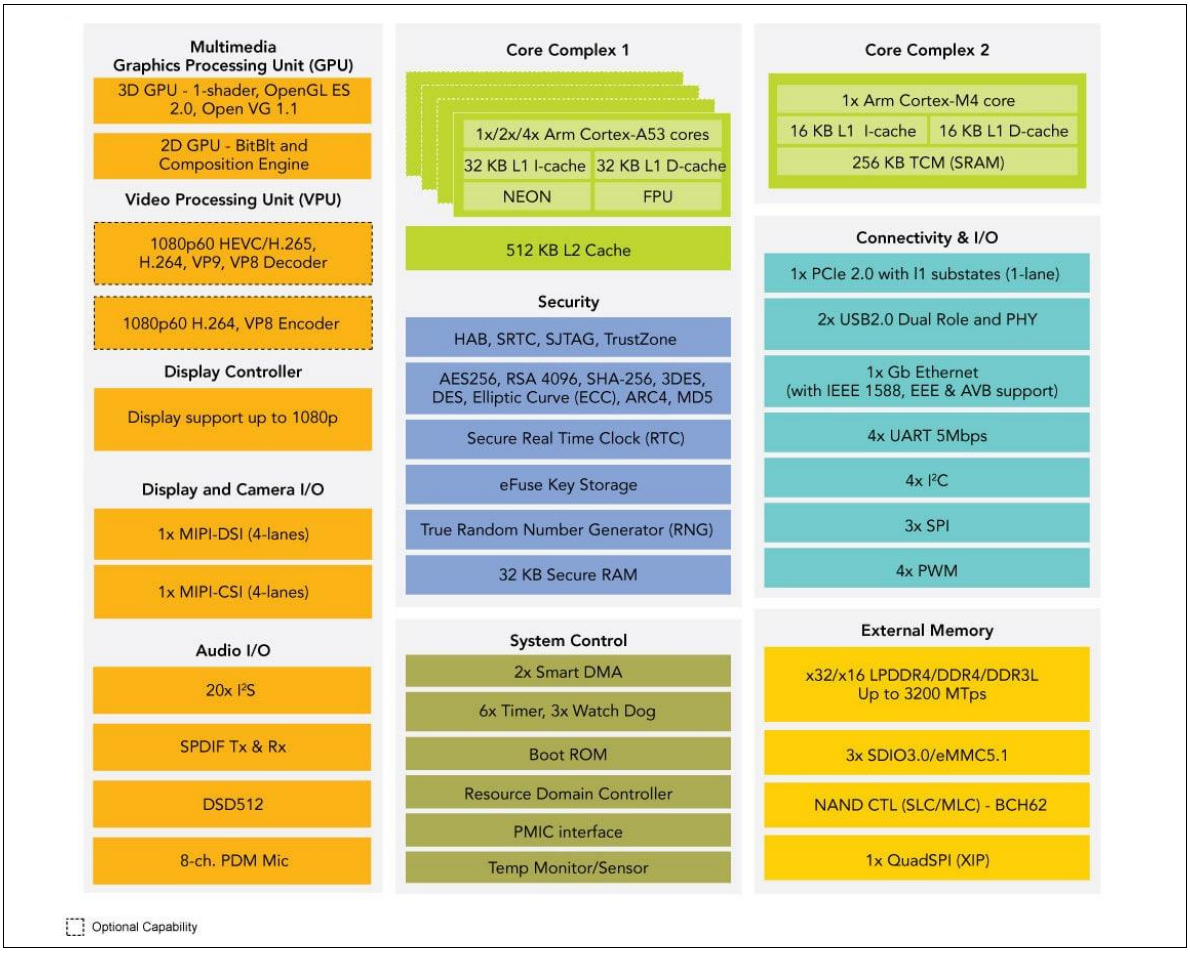
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	28 x 38 x 4 mm
Weight	7 gram
Connectors	2 x 100 pin, 0.4mm pitch
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Mini SoC

The i.MX8M Mini family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M4 core processor enables low-power processing.

Figure 2 i.MX8M Mini Block Diagram



3.2 Memory

3.2.1 DRAM

UCM-iMX8M-Mini is equipped with up to 4GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide and operates at 1600 MHz clock frequency (LPDDR4-3200).

3.2.2 Bootloader and General Purpose Storage

UCM-iMX8M-Mini uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

UCM-iMX8M-Mini implements a variety of peripheral interfaces through 2 x 100-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX8M-Mini SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the UCM-iMX8M-Mini carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5.
- All of the UCM-iMX8M-Mini digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on UCM-iMX8M-Mini configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard UCM-IMX8, followed by pull value.
- **"PU" -** Always pulled up onboard UCM-IMX8, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 MIPI-DSI Interface

The UCM-iMX8M-Mini MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Mini SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals

Table 5 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI_CKN	P2-21	AO	Negative part of MIPI-DSI clock diff-pair	Always available
DSI_CKP	P2-23	AO	Positive part of MIPI-DSI clock diff-pair	Always available
DSI_DN0	P2-1	AO	Negative part of MIPI-DSI data diff-pair 0	Always available
DSI_DP0	P2-3	AO	Positive part of MIPI-DSI data diff-pair 0	Always available
DSI_DN1	P2-15	AO	Negative part of MIPI-DSI data diff-pair 1	Always available
DSI_DP1	P2-17	AO	Positive part of MIPI-DSI data diff-pair 1	Always available
DSI_DN2	P2-5	AO	Negative part of MIPI-DSI data diff-pair 2	Always available
DSI_DP2	P2-7	AO	Positive part of MIPI-DSI data diff-pair 2	Always available
DSI_DN3	P2-11	AO	Negative part of MIPI-DSI data diff-pair 3	Always available
DSI_DP3	P2-13	AO	Positive part of MIPI-DSI data diff-pair 3	Always available

4.2 Camera Serial Interface

UCM-iMX8M-Mini MIPI-CSI interface is derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Mini SoC. The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 6 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI_P1_CKN	P2-2	AI	Negative part of MIPI-CSI clock diff-pair	Always available
CSI_P1_CKP	P2-4	AI	Positive part of MIPI-CSI clock diff-pair	Always available
CSI_P1_DN0	P2-6	AI	Negative part of MIPI-CSI data diff-pair 0	Always available
CSI_P1_DP0	P2-8	AI	Positive part of MIPI-CSI data diff-pair 0	Always available
CSI_P1_DN1	P2-31	AI	Negative part of MIPI-CSI data diff-pair 1	Always available
CSI_P1_DP1	P2-33	AI	Positive part of MIPI-CSI data diff-pair 1	Always available
CSI_P1_DN2	P2-25	AI	Negative part of MIPI-CSI data diff-pair 2	Always available
CSI_P1_DP2	P2-27	AI	Positive part of MIPI-CSI data diff-pair 2	Always available
CSI_P1_DN3	P2-35	AI	Negative part of MIPI-CSI data diff-pair 3	Always available

Signal Name	Pin #	Type	Description	Availability
CSI_P1_DP3	P2-37	AI	Positive part of MIPI-CSI data diff-pair 3	Always available

4.3 Ethernet

UCM-iMX8M-Mini incorporates an optional full-featured 10/100/1000 Ethernet interface, implemented with the i.MX8M Mini MAC coupled with an optional onboard Atheros AR8033 GbE PHY.

4.3.1 Gigabit Ethernet

UCM-iMX8M-Mini with onboard AR8033 PHY ("E" configuration option) supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The table below summarizes the GbE interface signals.

Table 7 GbE Interface Signals

Signal Name	Pin #	Type	Description	Availability
AVDD33_ETH	P1-62	P	Center tap supply for Ethernet magnetics	Only with 'E' option
ETH1_LED_ACT	P2-83^	IO;PD8K2	Active High, activity LED driver. 2.5V signal, PHY strap	Only with 'E' option
ETH1_LINK-LED_10_100	P2-86	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	Only with 'E' option
ETH1_LINK-LED_1000	P2-75^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal, PHY strap	Only with 'E' option
ETH1_MDI0N	P2-73	AIO	Negative part of 100ohm diff-pair 0	Only with 'E' option
ETH1_MDI0P	P2-74	AIO	Positive part of 100ohm diff-pair 0	Only with 'E' option
ETH1_MDI1N	P2-80	AIO	Negative part of 100ohm diff-pair 1	Only with 'E' option
ETH1_MDI1P	P2-78	AIO	Positive part of 100ohm diff-pair 1	Only with 'E' option
ETH1_MDI2N	P2-81	AIO	Negative part of 100ohm diff-pair 2	Only with 'E' option
ETH1_MDI2P	P2-79	AIO	Positive part of 100ohm diff-pair 2	Only with 'E' option
ETH1_MDI3N	P2-85	AIO	Negative part of 100ohm diff-pair 3	Only with 'E' option
ETH1_MDI3P	P2-84	AIO	Positive part of 100ohm diff-pair 3	Only with 'E' option

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

4.3.2 RGMII

When UCM-iMX8M-Mini is assembled without the "E" configuration option, the i.MX8M Mini Ethernet MAC RGMII and MDIO signals are routed directly to the carrier board interface. Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the Ethernet RGMII interface signals.

Table 8 RGMII Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET_MDC	P2-76*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Only w/o 'E' option
	P1-85*			Always available
ENET_MDIO	P2-88*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Only w/o 'E' option
	P2-90*			Always available
	P1-96*			Always available
ENET_RD0	P2-86*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET_RD1	P2-83*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET_RD2	P2-84*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET_RD3	P2-85*	I	Ethernet input data from the PHY	Only w/o 'E' option
ENET_RX_CTL	P2-79*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	Only w/o 'E' option
ENET_RXC	P2-80*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Only w/o 'E' option
ENET_TD0	P2-75*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET_TD1	P2-78*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET_TD2	P2-77*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET_TD3	P2-73*	O	Ethernet output data to PHY	Only w/o 'E' option
ENET_TXC	P2-81*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Only w/o 'E' option
ENET_TX_CTL	P2-74*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Only w/o 'E' option
RGMII_VIO	P1-55	P	RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements	Only w/o 'E' option

NOTE: 2.5V or 3.3V power must be supplied via the RGMII_VIO pin if any of the RGMII signals are used on the carrier-board

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.4 Wireless Interfaces

UCM-iMX8M-Mini optional 802.11ac WLAN and Bluetooth 4.2/EDR functions are implemented with the certified Laird Sterling-LWB5 Module based on Cypress BCM43353 chipset. i.MX8M Mini SoC is interfaced with the WLAN subsystem over SDIO1 interface, while UART4 is dedicated to Bluetooth functionality.

UCM-iMX8M-Mini is equipped with a MHF4 high-frequency connector allowing easy integration with an external WLAN/BT antenna.

Table 9 J1 MHF4 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	W.FL2-R-SMT1(60)	Hirose W.FL2-LP-062HF

NOTE: UCM-iMX8M-Mini WiFi and Bluetooth functions are available only with the 'WB' ordering option.

4.5 PCI-Express

UCM-iMX8M-Mini provides one PCI Express port. The port requires an external PCIe reference clock to be supplied from the carrier-board.

Table 10 PCIE Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE1_REF_CLKN	P2-44	AI	100 MHz PCIe reference clock differential input negative	Always available
PCIE1_REF_CLKP	P2-42	AI	100 MHz PCIe reference clock differential input positive	Always available
PCIE1_RXN_N	P2-30	I	PCI Express receive data negative	Always available
PCIE1_RXN_P	P2-32	I	PCI Express receive data positive	Always available
PCIE1_TXN_N	P2-36	O	PCI Express transmit data negative	Always available
PCIE1_TXN_P	P2-38	O	PCI Express transmit data positive	Always available

4.6 Sony/Philips Digital Interface (S/PDIF)

UCM-iMX8M-Mini provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 11 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	P1-77*	I	External clock signal	Always available
SPDIF_RX	P1-79*	I	SPDIF input data line signal	Always available
SPDIF_TX	P1-81*	O	SPDIF output data line signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.7 Digital Audio (SAI)

UCM-iMX8M-Mini enables access to 4 of the i.MX8M Mini integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Mini Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 12 SAI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1_MCLK	P2-62*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI1_RXC	P2-69*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI1_RXD0	P2-48*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RXD1	P2-50*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RXD2	P2-52*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RXD3	P2-60*^	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RXFS	P2-47*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI1_TXC	P2-45*	O	Transmit bit clock. An input when generated externally and an output when generated internally	Always available
	P1-41*			Always available
	P2-62*			Always available
SAI1_TXD0	P2-53*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-39*			Always available
SAI1_TXD1	P2-59*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-31*			Always available
	P2-48*^			Always available
SAI1_TXD2	P2-63*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-35*			Always available
SAI1_TXD3	P2-67*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-33*			Always available
SAI1_TXD4	P1-37*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TXD5	P1-29*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_TXFS	P2-41*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI1_TX_SYNC	P1-29*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P1-33*			Always available
	P1-37*			Always available

Table 13 SAI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2_MCLK	P1-30*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI2_RXD	P1-28*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI2_RXC	P1-32*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI2_RXFS	P1-34*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI2_TXD	P1-26*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI2_TXC	P1-36*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI2_TXFS	P1-38*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 14 SAI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI3_MCLK	P1-17*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXD	P1-19*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI3_RXC	P1-21*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXFS	P1-25*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI3_TXD0	P1-13*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI3_TXC	P1-15*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_TXFS	P1-23*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 15 SAI5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI5_MCLK	P1-41*	IO	Audio master clock. An input when generated externally and an output when generated internally	Always available
	P1-30*			Always available
	P1-17*			Always available
	P2-62*			Always available
SAI5_RX_BCLK	P1-21*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
	P2-69*			Always available
SAI5_RXD0	P1-35*	I	Receive data, sampled synchronously by the bit clock	Always available
	P1-19*			Always available
	P2-48*^			Always available
SAI5_RXD1	P1-33*	I	Receive data, sampled synchronously by the bit clock	Always available
	P1-23*			Always available
	P2-50*^			Always available
SAI5_RXD2	P1-37*	I	Receive data, sampled synchronously by the bit clock	Always available
	P1-15*			Always available
	P2-52*^			Always available
SAI5_RXD3	P1-29*	I		Always available

Signal Name	Pin #	Type	Description	Availability
	P1-13*		Receive data, sampled synchronously by the bit clock	Always available
	P2-60*^			Always available
SAI5_RXC	P1-31*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI5_RXFS	P1-39*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P2-47*			Always available
SAI5_RX_SYNC	P1-25*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI5_TX_BCLK	P1-32*	O	Transmit bit clock. An input when generated externally and an output when generated internally	Always available
SAI5_TXD0	P1-29*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-28*			Always available
	P2-53*^			Always available
SAI5_TXD1	P1-38*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-34*			Always available
	P2-59*^			Always available
SAI5_TXD2	P1-36*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P2-63*^			Always available
SAI5_TXD3	P1-26*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI5_TX_SYNC	P1-34*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI5_TX_SYNC	P1-33*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI5_TXFS	P2-41*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

4.8 USB2.0 ports

i.MX8M Mini SoC is equipped with two dual-role USB2.0 controllers and PHYs. One port supports OTG functionality, while the second port is configured permanently for host mode.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the USB2.0 interface signals.

Table 16 USB OTG port #1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB1_DN	P1-14	IO	USB2.0 negative data	Always available
USB1_DP	P1-12	IO	USB2.0 positive data	Always available
USB1_ID	P1-22	I	USB1 OTG ID signal	Always available
USB1_VBUS_DET	P1-24	I	USB1 VBUS detect	Always available

Table 17 USB host port #2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB2_DN	P1-5	IO	USB2.0 negative data	Always available
USB2_DP	P1-3	IO	USB2.0 positive data	Always available
USB2_VBUS_DET	P1-1	I	USB2 VBUS detect	Always available

4.9 MMC / SD /SDIO

UCM-iMX8M-Mini features one MMC/SD/SDIO port. The port is derived from the i.MX8M Mini on-chip MMC/SD/SDIO controller (uSDHC2). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to 25 MB/s
- 1-bit or 4-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes
- Dedicated card detection, write protection and Reset signals.

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 18 MMC/SD/SDIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD2_nCD	P2-92*	I	Card detection pin	Always available
EXT_SD2_CLK	P2-96*	O	Clock for MMC/SD/SDIO card	Always available
EXT_SD2_CMD	P2-100*	IO	CMD line connect to card	Always available
EXT_SD2_DATA0	P2-97*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
EXT_SD2_DATA1	P2-99*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always available
EXT_SD2_DATA2	P2-94*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
EXT_SD2_DATA3	P2-98*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
SD2_RESET_B	P2-51*	O	Card hardware reset signal, active LOW	Always available
	P1-58*			Always available
SD2_WP	P2-49*	I	Card write protect detection	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.10 UART

UCM-iMX8M-Mini enables access to up-to four i.MX8M Mini universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Mini UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: UART4 is used for the on-board Bluetooth module. Using UART4 interface signals available through the carrier board interface precludes on-board Bluetooth operation.

NOTE: By default UART3 is assigned to be used as the main debug console port.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the UART interface signals.

Table 19 UART1 Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	P1-76*	O	UART-1 clear to send	Always available
	P1-38*			Always available
UART1_RTS_B	P1-74*	I	UART-1 request to send	Always available
	P1-28*			Always available
UART1_RXD	P1-70*	I	UART-1 serial data receive	Always available
	P1-32*			Always available
UART1_TXD	P1-72*	O	UART-1 serial data transmit	Always available
	P1-34*			Always available

Table 20 UART2 Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS_B	P1-84*	O	UART-2 clear to send	Always available
	P1-21*			Always available
UART2_RTS_B	P1-86*	I	UART-2 request to send	Always available
	P1-19*			Always available
UART2_RXD	P1-80*	I	UART-2 serial data receive	Always available
	P1-23*			Always available
UART2_TXD	P1-82*	O	UART-2 serial data transmit	Always available
	P1-15*			Always available

Table 21 UART3 Signals

Signal Name	Pin #	Type	Description	Availability
UART3_RXD (DBG)	P1-76*	I	UART-3 serial data receive	Always available

Signal Name	Pin #	Type	Description	Availability
UART3_RXD	P1-48*			Always available
UART3_TXD (DBG)	P1-74*	O	UART-3 serial data transmit	Always available
UART3_TXD	P1-42*			Always available
UART3_CTS_B	P1-44*	O	UART-3 clear to send	Always available
UART3_RTS_B	P1-46*	I	UART-3 request to send	Always available

Table 22 UART4 Signals

Signal Name	Pin #	Type	Description	Availability
UART4_RXD	P1-84*	I	UART-4 serial data receive	Always available, precludes Bluetooth
	P2-93*	I	UART-4 serial data receive	Only w/o "WB" option
UART4_TXD	P1-86*	O	UART-4 serial data transmit	Always available, precludes Bluetooth
	P2-95*	O	UART-4 serial data transmit	Only w/o "WB" option
UART4_CTS_B	P2-89*	O	UART-4 clear to send	Only w/o "WB" option
UART4_RTS_B	P2-91*	I	UART-4 request to send	Only w/o "WB" option

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 I2C

UCM-iMX8M-Mini features up-to three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the I2C interface signals.

Table 23 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_SCL	P1-100*	O	I2C serial clock line	Always available
I2C1_SDA	P1-96*	IO	I2C serial data line	Always available

Table 24 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	P1-94*	O	I2C serial clock line	Always available
I2C3_SDA	P1-91*	IO	I2C serial data line	Always available

Table 25 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	P1-87*	O	I2C serial clock line	Always available
I2C4_SDA	P1-89*	IO	Always available	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 ECSPI

Up-to three SPI interfaces are accessible through the UCM-iMX8M-Mini carrier board interface. The SPI interfaces are derived from i.MX8M Mini integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

Table 26 ECSPI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI1_MISO	P1-44*	I	SPI-1 Master data in; slave data out	Always available
ECSPI1_MOSI	P1-42*	O	SPI-1 Master data out; slave data in	Always available
ECSPI1_SCLK	P1-48*	O	SPI-1 Master clock out; slave clock in	Always available
ECSPI1_SS0	P1-46*	O	SPI-1 Chip select 0	Always available

Table 27 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2_MISO	P2-89*	I	SPI-2 Master data in; slave data out	Only w/o "WB" option
ECSPI2_MOSI	P2-95*	O	SPI-2 Master data out; slave data in	Only w/o "WB" option
ECSPI2_SCLK	P2-93*	O	SPI-2 Master clock out; slave clock in	Only w/o "WB" option
ECSPI2_SS0	P2-91*	O	SPI-2 Chip select 0	Only w/o "WB" option

Table 28 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3_MISO	P1-80*	I	SPI-3 Master data in; slave data out	Always available
ECSPI3_MOSI	P1-72*	O	SPI-3 Master data out; slave data in	Always available
ECSPI3_SCLK	P1-70*	O	SPI-3 Master clock out; slave clock in	Always available
ECSPI3_SS0	P1-82*	O	SPI-3 Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 QSPI

UCM-iMX8M-Mini features one Quad SPI interface. The interface is implemented with the iMX8M Mini integrated QSPI controller. The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Parallel Flash mode.
- Direct Memory Access (DMA) support.

- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the QSPI interface signals.

Table 29 QSPI Interface Signals

Signal Name	Pin #	Type	Description	Availability
QSPI_A_DATA0	P2-61*	IO	Data IO 0	Always available
QSPI_A_DATA1	P2-56*	IO	Data IO 1	Always available
QSPI_A_DATA2	P2-43*	IO	Data IO 2	Always available
QSPI_A_DATA3	P2-58*	IO	Data IO 3	Always available
QSPI_A_SCLK	P2-55*	O	Serial clock	Always available
QSPI_A_SS0_B	P2-65*	O	Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 PWM

UCM-iMX8M-Mini features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 30 PWM Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	P1-77*	O	PWM1 functional output	Always available
	P1-89*			Always available
	P1-56*			Always available
PWM2_OUT	P1-79*	O	PWM2 functional output	Always available
	P1-87*			Always available
	P1-60*			Always available
PWM3_OUT	P1-81*	O	PWM3 functional output	Always available
	P1-91*			Always available
PWM4_OUT	P1-17*	O	PWM4 functional output	Always available
	P1-94*			Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 JTAG

UCM-iMX8M-Mini enables access to the i.MX8M Mini JTAG port through the carrier board interface.

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 31 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_MOD	P1-75	I	JTAG MODE	Always available
JTAG_nTRST	P1-63	I	Test Reset	Always available
JTAG_TCK	P1-73	I	Test Clock	Always available
JTAG_TDI	P1-71	I	Test Data In	Always available
JTAG_TDO	P1-67	O	Test Data Out	Always available
JTAG_TMS	P1-65	I	Test Mode Select	Always available

4.16 GPIO

Up-to 85 of the i.MX8M Mini general purpose input/output (GPIO) signals are available through the UCM-iMX8M-Mini carrier board interface. When configured as an output, it is possible to write to an i.MX8M Mini register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Mini register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Mini Reference manual for additional details.

NOTE: Internal IO pull up/down is not supported due to errata of the i.MX8M Mini SoC. Use external pull up/down resistors and disable the internal pull up/down in software. For additional details refer to i.MX8M Mini errata e50080.

The table below summarizes the GPIO interface signals.

Table 32 GPIO Signals

Signal Name	Pin #	Type	Description	Always available
GPIO1_IO[1]	P1-56*	IO	GPIO	Always available
GPIO1_IO[5]	P1-95*	IO	GPIO	Always available
GPIO1_IO[6]	P1-85*	IO	GPIO	Always available
GPIO1_IO[7]	P2-90*	IO	GPIO	Always available
GPIO1_IO[8]	P1-58*	IO	GPIO	Always available
GPIO1_IO[10]	P1-22*	IO	GPIO	Always available
GPIO1_IO[13]	P1-60*	IO	GPIO	Always available
GPIO2_IO[12]	P2-92*	IO	GPIO	Always available
GPIO2_IO[13]	P2-96*	IO	GPIO	Always available
GPIO2_IO[14]	P2-100*	IO	GPIO	Always available
GPIO2_IO[15]	P2-97*	IO	GPIO	Always available
GPIO2_IO[16]	P2-99*	IO	GPIO	Always available
GPIO2_IO[17]	P2-94*	IO	GPIO	Always available
GPIO2_IO[18]	P2-98*	IO	GPIO	Always available
GPIO2_IO[19]	P2-51*	IO	GPIO	Always available
GPIO2_IO[20]	P2-49*	IO	GPIO	Always available
GPIO3_IO[0]	P2-55*	IO	GPIO	Always available
GPIO3_IO[1]	P2-65*	O	GPIO	Always available
GPIO3_IO[6]	P2-61*	O	GPIO	Always available
GPIO3_IO[7]	P2-56*	IO	GPIO	Always available
GPIO3_IO[8]	P2-43*	IO	GPIO	Always available
GPIO3_IO[9]	P2-58*	IO	GPIO	Always available
GPIO3_IO[19]	P1-39*	IO	GPIO	Always available
GPIO3_IO[20]	P1-31*	IO	GPIO	Always available
GPIO3_IO[21]	P1-35*	IO	GPIO	Always available
GPIO3_IO[22]	P1-33*	IO	GPIO	Always available
GPIO3_IO[23]	P1-37*	IO	GPIO	Always available
GPIO3_IO[24]	P1-29*	IO	GPIO	Always available
GPIO3_IO[25]	P1-41*	IO	GPIO	Always available
GPIO4_IO[0]	P2-47*	IO	GPIO	Always available
GPIO4_IO[1]	P2-69*	IO	GPIO	Always available
GPIO4_IO[2]	P2-48*^	IO	GPIO	Always available
GPIO4_IO[3]	P2-50*^	IO	GPIO	Always available
GPIO4_IO[4]	P2-52*^	IO	GPIO	Always available
GPIO4_IO[5]	P2-60*^	IO	GPIO	Always available
GPIO4_IO[10]	P2-41*	IO	GPIO	Always available

Signal Name	Pin #	Type	Description	Always available
GPIO4_IO[11]	P2-45*	IO	GPIO	Always available
GPIO4_IO[12]	P2-53*^	IO	GPIO	Always available
GPIO4_IO[13]	P2-59*^	IO	GPIO	Always available
GPIO4_IO[14]	P2-63*^	IO	GPIO	Always available
GPIO4_IO[15]	P2-67*^	IO	GPIO	Always available
GPIO4_IO[20]	P2-62*	IO	GPIO	Always available
GPIO4_IO[21]	P1-34*	IO	GPIO	Always available
GPIO4_IO[22]	P1-32*	IO	GPIO	Always available
GPIO4_IO[23]	P1-28*	IO	GPIO	Always available
GPIO4_IO[24]	P1-38*	IO	GPIO	Always available
GPIO4_IO[25]	P1-36*	IO	GPIO	Always available
GPIO4_IO[26]	P1-26*	IO	GPIO	Always available
GPIO4_IO[27]	P1-30*	IO	GPIO	Always available
GPIO4_IO[28]	P1-25*	IO	GPIO	Always available
GPIO4_IO[29]	P1-21*	IO	GPIO	Always available
GPIO4_IO[30]	P1-19*	IO	GPIO	Always available
GPIO4_IO[31]	P1-23*	IO	GPIO	Always available
GPIO5_IO[0]	P1-15*	IO	GPIO	Always available
GPIO5_IO[1]	P1-13*	IO	GPIO	Always available
GPIO5_IO[2]	P1-17*	IO	GPIO	Always available
GPIO5_IO[3]	P1-81*	IO	GPIO	Always available
GPIO5_IO[4]	P1-79*	IO	GPIO	Always available
GPIO5_IO[5]	P1-77*	IO	GPIO	Always available
GPIO5_IO[6]	P1-48*	IO	GPIO	Always available
GPIO5_IO[7]	P1-42*	IO	GPIO	Always available
GPIO5_IO[8]	P1-44*	IO	GPIO	Always available
GPIO5_IO[9]	P1-46*	IO	GPIO	Always available
GPIO5_IO[10]	P2-93*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[11]	P2-95*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[12]	P2-89*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[13]	P2-91*	IO	GPIO	Only w/o "WB" option
GPIO5_IO[14]	P1-100*	IO	GPIO	Always available
GPIO5_IO[15]	P1-96*	IO	GPIO	Always available
GPIO5_IO[18]	P1-94*	IO	GPIO	Always available
GPIO5_IO[19]	P1-91*	IO	GPIO	Always available
GPIO5_IO[20]	P1-87*	IO	GPIO	Always available
GPIO5_IO[21]	P1-89*	IO	GPIO	Always available
GPIO5_IO[22]	P1-70*	IO	GPIO	Always available
GPIO5_IO[23]	P1-72*	IO	GPIO	Always available
GPIO5_IO[24]	P1-80*	IO	GPIO	Always available
GPIO5_IO[25]	P1-82*	IO	GPIO	Always available
GPIO5_IO[26]	P1-76*	IO	GPIO	Always available
GPIO5_IO[27]	P1-74*	IO	GPIO	Always available
GPIO5_IO[28]	P1-84*	IO	GPIO	Always available
GPIO5_IO[29]	P1-86*	IO	GPIO	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

5 SYSTEM LOGIC

5.1 Power Supply

Table 33 Power signals

Signal Name	Connector #	Pin#	Type	Description
V_SOM	P1	11, 27, 43, 57, 69, 83	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
	P2	9, 19, 29, 39, 57, 71, 87		
VCC_RTC	P1	93	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
GND	P1	10, 20, 40, 54, 64, 78, 88	P	Common ground
	P2	10, 16, 22, 28, 34, 40, 46, 54, 72, 82		
RGMII_VIO	P1	55	P	RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

UCM-iMX8M-Mini supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Mini SoC. The logic that controls both signals is supplied by the i.MX8M Mini SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that UCM-iMX8M-Mini is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 34 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	P1-66	O, 1.8V	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	P1-68	O, 1.8V	Active high power-up request output from i.MX8M Mini SoC.	Always available
PWRBTN	P2-64	I, 1.8V	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

NOTE: PMIC_STBY_REQ, PMIC_ON_REQ, PWRBTN signal operate at 1.8V voltage level.

5.3 Reset

The POR_B signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX8M-Mini. Please refer to the i.MX8M Mini Reference manual for additional details.

Table 35 Reset signals

Signal Name	Pin #	Type	Description	Availability
POR_B	P2-66	I	Active Low cold reset input signal. Should be used as main system reset Maximum rise/fall time is 5.0nS. Open-drain signal with a 10k onboard pull-up resistor to 3.3V	Always available

5.4 Boot Sequence

UCM-iMX8M-Mini boot sequence defines which interface/media is used by UCM-iMX8M-Mini to load and execute the initial software (such as SPL or/and U-boot). UCM-iMX8M-Mini can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD/MMC card using the MMC/SD/SDIO 2 interface

UCM-iMX8M-Mini will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by UCM-iMX8M-Mini:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows UCM-iMX8M-Mini to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 36 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P1-90	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 37 UCM-iMX8M-Mini Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on MMC/SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 98 of the UCM-iMX8M-Mini carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX8M-Mini CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX8M-Mini pins are derived from the i.MX8M Mini SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

NOTE: Internal IO pull up/down is not supported due to errata of the i.MX8M Mini SoC. Use external pull up/down resistors and disable the internal pull up/down in software. For additional details refer to i.MX8M Mini errata e50080.

Table 38 Multifunctional Signals

Pin #	SoC signal / ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
P1-13*	SAI3_TXD0	GPT1_COMPARE3	SAI5_RXD3			GPIO5_IO[1]	Always available
P1-15*	SAI3_TXC	GPT1_COMPARE2	SAI5_RXD2		UART2_TXD	GPIO5_IO[0]	Always available
P1-17*	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO[2]	Always available
P1-19*	SAI3_RXD	GPT1_COMPARE1	SAI5_RXD0		UART2_RTS_B	GPIO4_IO[30]	Always available
P1-21*	SAI3_RXC	GPT1_CLK	SAI5_RX_BCLK		UART2_CTS_B	GPIO4_IO[29]	Always available
P1-22*	GPIO1_IO[10]	USB1_OTG_ID					Always available
P1-23*	SAI3_TXFS	GPT1_CAPTURE2	SAI5_RXD1	SAI3_TXD1	UART2_RXD	GPIO4_IO[31]	Always available
P1-25*	SAI3_RXFS	GPT1_CAPTURE1	SAI5_RX_SYNC	SAI3_RX_DATA1		GPIO4_IO[28]	Always available
P1-26*	SAI2_TXD	SAI5_TXD3				GPIO4_IO[26]	Always available
P1-28*	SAI2_RXD	SAI5_TXD0			UART1_RTS_B	GPIO4_IO[23]	Always available
P1-29*	SAI5_RXD3	SAI1_TXD5	SAI1_TX_SYNC	SAI5_TXD0		GPIO3_IO[24]	Always available
P1-30*	SAI2_MCLK	SAI5_MCLK				GPIO4_IO[27]	Always available
P1-31*	SAI5_RXC	SAI1_TXD1				GPIO3_IO[20]	Always available
P1-32*	SAI2_RXC	SAI5_TXC			UART1_RXD	GPIO4_IO[22]	Always available
P1-33*	SAI5_RXD1	SAI1_TXD3	SAI1TX_SYNC	SAI5_TX_SYNC		GPIO3_IO[22]	Always available
P1-34*	SAI2_RXFS	SAI5_TX_SYNC	SAI5_TXD1		UART1_TXD	GPIO4_IO[21]	Always available
P1-35*	SAI5_RXD0	SAI1_TXD2				GPIO3_IO[21]	Always available
P1-36*	SAI2_TXC	SAI5_TXD2				GPIO4_IO[25]	Always available
P1-37*	SAI5_RXD2	SAI1_TXD4	SAI1_TX_SYNC	SAI5_TX_BCLK		GPIO3_IO[23]	Always available
P1-38*	SAI2_TXFS	SAI5_TXD1			UART1_CTS_B	GPIO4_IO[24]	Always available
P1-39*	SAI5_RXFS	SAI1_TXD0				GPIO3_IO[19]	Always available
P1-41*	SAI5_MCLK	SAI1_TXC				GPIO3_IO[25]	Always available
P1-42*	ECSPI1_MOSI	UART3_TXD				GPIO5_IO[7]	Always available
P1-44*	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]	Always available
P1-46*	ECSPI1_SS0	UART3_.RTS_B				GPIO5_IO[9]	Always available
P1-48*	ECSPI1_SCLK	UART3_RXD				GPIO5_IO[6]	Always available
P1-56*	GPIO1_IO[1]	PWM1_OUT					Always available
P1-58*	GPIO1_IO[8]					SD2_RESET_B	Always available
P1-60*	GPIO1_IO[13]					PWM2_OUT	Always available
P1-70*	UART1_RXD	ECSPI3_SCLK				GPIO5_IO[22]	Always available
P1-72*	UART1_TXD	ECSPI3_MOSI				GPIO5_IO[23]	Always available
P1-74*	UART3_TXD (DBG)	UART1_RTS_B				GPIO5_IO[27]	Always available
P1-76*	UART3_RXD (DBG)	UART1_CTS_B				GPIO5_IO[26]	Always available
P1-77*	SPDIF_EXT_CLK	PWM1_OUT				GPIO5_IO[5]	Always available
P1-79*	SPDIF_RX	PWM2_OUT				GPIO5_IO[4]	Always available
P1-80*	UART2_RXD	ECSPI3_MISO				GPIO5_IO[24]	Always available
P1-81*	SPDIF_TX	PWM3_OUT				GPIO5_IO[3]	Always available
P1-82*	UART2_TXD	ECSPI3_SS0				GPIO5_IO[25]	Always available
P1-84*	UART4_RXD	UART2_CTS_B				GPIO5_IO[28]	Always available
P1-85	GPIO1_IO[6]	ENET_MDC					Always available
P1-86*	UART4_TXD	UART2_RTS_B				GPIO5_IO[29]	Always available
P1-87*	I2C4_SCL	PWM2_OUT				GPIO5_IO[20]	Always available

Pin #	SoC signal / ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	Availability
P1-89*	I2C4_SDA	PWM1_OUT				GPIO5_IO[21]	Always available
P1-91*	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]	Always available
P1-94*	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]	Always available
P1-95	GPIO1_IO[5]						Always available
P1-96*	I2C1_SDA	ENET_MDIO				GPIO5_IO[15]	Always available
P1-100*	I2C1_SCL	ENET_MDC				GPIO5_IO[14]	Always available
P2-41*	SAI1_TXFS	SAI5_TXFS				GPIO4_IO[10]	Always available
P2-43*		QSPI_A_DATA2				GPIO3_IO[8]	Always available
P2-45*	SAI1_TXC	SAI5_TXC				GPIO4_IO[11]	Always available
P2-47*	SAI1_RXFS	SAI5_RXFS				GPIO4_IO[0]	Always available
P2-48*	SAI1_RXD0	SAI5_RXD0	SAI1_TXD1			GPIO4_IO[2]	Always available
P2-49*	SD2_WP					GPIO2_IO[20]	Always available
P2-50*	SAI1_RXD1	SAI5_RXD1				GPIO4_IO[3]	Always available
P2-51*	SD2_nRST					GPIO2_IO[19]	Always available
P2-52*	SAI1_RXD2	SAI5_RXD2				GPIO4_IO[4]	Always available
P2-53*	SAI1_TXD0	SAI5_TXD0				GPIO4_IO[12]	Always available
P2-55*	NAND_ALE	QSPI_A_SCLK				GPIO3_IO[0]	Always available
P2-56*	NAND_DATA1	QSPI_A_DATA1				GPIO3_IO[7]	Always available
P2-58*	NAND_DATA3	QSPI_A_DATA3				GPIO3_IO[9]	Always available
P2-59*	SAI1_TXD1	SAI5_TXD1				GPIO4_IO[13]	Always available
P2-60*	SAI1_RXD3	SAI5_RXD3				GPIO4_IO[5]	Always available
P2-61*	NAND_DATA0	QSPI_A_DATA0				GPIO3_IO[6]	Always available
P2-62*	SAI1_MCLK	SAI5_MCLK	SAI1_TXC			GPIO4_IO[20]	Always available
P2-63*	SAI1_TXD2	SAI5_TXD2				GPIO4_IO[14]	Always available
P2-65*	NAND_nCE0	QSPI_A_SS0_B				GPIO3_IO[1]	Always available
P2-67*	SAI1_TXD3	SAI5_TXD3				GPIO4_IO[15]	Always available
P2-68	GPIO1_IO[9]						Only w/o "E" option
P2-69*	SAI1_RXC	SAI5_RX_BCLK				GPIO4_IO[1]	Always available
P2-70	GPIO1_IO[11]						Only w/o "E" option
P2-73*	ENET_TD3						Only w/o "E" option
P2-74*	ENET_TX_CTL						Only w/o "E" option
P2-75*	ENET_TD0						Only w/o "E" option
P2-76*	ENET_MDC						Only w/o "E" option
P2-77*	ENET_TD2						Only w/o "E" option
P2-78*	ENET_TD1						Only w/o "E" option
P2-79*	ENET_RX_CTL						Only w/o "E" option
P2-80*	ENET_RXC						Only w/o "E" option
P2-81*	ENET_TXC						Only w/o "E" option
P2-83*	ENET_RD1						Only w/o "E" option
P2-84*	ENET_RD2						Only w/o "E" option
P2-85*	ENET_RD3						Only w/o "E" option
P2-86*	ENET_RD0						Only w/o "E" option
P2-88*	ENET_MDIO						Only w/o "E" option
P2-89*	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO[12]	Only w/o "WB" option
P2-90	GPIO1_IO[7]	ENET_MDIO					Always available
P2-91*	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO[13]	Only w/o "WB" option
P2-92*	SD2_nCD					GPIO2_IO[12]	Always available
P2-93*	ECSPI2_SCLK	UART4_RXD				GPIO5_IO[10]	Only w/o "WB" option
P2-94*	EXT_SD2_DATA2					GPIO2_IO[17]	Always available
P2-95*	ECSPI2_MOSI	UART4_TXD				GPIO5_IO[11]	Only w/o "WB" option
P2-96*	EXT_SD2_CLK					GPIO2_IO[13]	Always available
P2-97*	EXT_SD2_DATA0					GPIO2_IO[15]	Always available
P2-98*	EXT_SD2_DATA3					GPIO2_IO[18]	Always available
P2-99*	EXT_SD2_DATA1					GPIO2_IO[16]	Always available
P2-100*	EXT_SD2_CMD					GPIO2_IO[14]	Always available

5.6 RTC

UCM-iMX8M-Mini features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about UCM-iMX8M-Mini RTC please refer to the AM1805 datasheet.

5.7 LED

UCM-iMX8M-Mini features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Mini. The LED is ON when GPIO1_IO[12] is logic LOW.

5.8 Reserved Signals

The following UCM-iMX8M-Mini signals are reserved and must be left unconnected.

Table 39 Reserved Signals

Signal Name	Connector #	Pin#
RESERVED	P1	59, 97, 99
	P2	24, 26

5.9 Boot Strap Signals

The following UCM-iMX8M-Mini signals must not be pulled or driven by carrier board during SoM power-up or reset.

Table 40 Boot Strap Signals

Connector #	Pin#
P1	-
P2	48, 50, 52, 53, 59, 60, 63, 67, 75, 83

6 CARRIER BOARD INTERFACE

The UCM-iMX8M-Mini CoM/SoM carrier board interface uses 2 x 100 Pin carrier board connectors. The SoM pinout is detailed in the table below.

6.1 Connectors Pinout

Table 41 Connector P1

Pin #	UCM-iMX8M-Mini Signal Name	Ref.		Pin #	UCM-iMX8M-Mini Signal Name	Ref.
2	NC	-		1	USB2_VBUS_DET	4.8
4	NC	-		3	USB2_DP	4.8
6	NC	-		5	USB2_DN	4.8
8	NC	-		7	NC	-
10	GND	5.1		9	NC	-
12	USB1_DP	4.8		11	V_SOM	5.1
14	USB1_DN	4.8		13	SAI3_TXD0 GPT1_COMPARE3 SAI5_RXD3 GPIO5_IO[1]	4.7 - 4.7 4.16
16	NC	-		15	SAI3_TXC GPT1_COMPARE2 SAI5_RXD2 UART2_TXD GPIO5_IO[0]	4.7 - 4.7 4.10 4.16
18	NC	-		17	SAI3_MCLK PWM4_OUT SAI5_MCLK GPIO5_IO[2]	4.7 4.14 4.7 4.16
20	GND	5.1		19	SAI3_RXD GPT1_COMPARE1 SAI5_RXD0 UART2_RTS_B GPIO4_IO[30]	4.7 - 4.7 4.10 4.16
22	USB1_ID GPIO1_IO[10]	4.8 4.16		21	SAI3_RXC GPT1_CAPTURE1 SAI5_RX_BCLK UART2_CTS_B GPIO4_IO[29]	4.7 - 4.7 4.10 4.16
24	USB1_VBUS_DET	4.8		23	SAI3_TXFS GPT1_CLK SAI5_RXD1 UART2_RXD GPIO4_IO[31]	4.7 - 4.7 4.10 4.16
26	SAI2_TXD SAI5_TXD3 GPIO4_IO[26]	4.7 4.7 4.16		25	SAI3_RXFS GPT1_CAPTURE1 SAI5_RX_SYNC GPIO4_IO[28]	4.7 - 4.7 4.16
28	SAI2_RXD SAI5_TXD0 UART1_RTS_B GPIO4_IO[23]	4.7 4.7 4.10 4.16		27	V_SOM	5.1
30	SAI2_MCLK SAI5_MCLK GPIO4_IO[27]	4.7 4.7 4.16		29	SAI1_TXD5 SAI1_TX_SYNC SAI5_RXD3 SAI5_TXD0 GPIO3_IO[24]	4.7 4.7 4.7 4.7 4.16
32	SAI2_RXC SAI5_TX_BCLK UART1_RXD GPIO4_IO[22]	4.7 4.7 4.10 4.16		31	SAI1_TXD1 SAI5_RXC GPIO3_IO[20]	4.7 4.7 4.16
34	SAI2_RXFS SAI5_TX_SYNC SAI5_TXD1 UART1_TXD GPIO4_IO[21]	4.7 4.7 4.7 4.10 4.16		33	SAI1_TXD3 SAI1_TX_SYNC SAI5_RXD1 SAI5_TX_SYNC GPIO3_IO[22]	4.7 4.7 4.7 4.7 4.16
36	SAI2_TXC SAI5_TXD2 GPIO4_IO[25]	4.7 4.7 4.16		35	SAI1_TXD2 SAI5_RXD0 GPIO3_IO[21]	4.7 4.7 4.16

38	SAI2_TXFS SAI5_TXD1 UART1_CTS_B GPIO4_IO[24]	4.7 4.7 4.10 4.16		37	SAI1_TXD4 SAI1_TX_SYNC SAI5_RXD2 GPIO3_IO[23]	4.7 4.7 4.7 4.16
40	GND	5.1		39	SAI1_TXD0 SAI5_RXFS GPIO3_IO[19]	4.7 4.7 4.16
42	ECSPI1_MOSI UART3_TXD GPIO5_IO[7]	4.12 4.10 4.16		41	SAI1_TXC SAI5_MCLK GPIO3_IO[25]	4.7 4.7 4.16
44	ECSPI1_MISO UART3_CTS_B GPIO5_IO[8]	4.12 4.10 4.16		43	V_SOM	5.1
46	ECSPI1_SS0 UART3_RTS_B GPIO5_IO[9]	4.12 4.10 4.16		45	NC	-
48	ECSPI1_SCLK UART3_RXD GPIO5_IO[6]	4.12 4.10 4.16		47	NC	-
50	NC	-		49	NC	-
52	NC	-		51	NC	-
54	GND	5.1		53	NC	-
56	PWM1_OUT GPIO1_IO[1]	4.14 4.16		55	RGMII_VIO	4.3.2
58	SD2_RESET_B GPIO1_IO[8]	4.9 4.16		57	V_SOM	5.1
60	PWM2_OUT GPIO1_IO[13]	4.14 4.16		59	RESERVED	5.8
62	AVDD33_ETH	4.3		61	NC	-
64	GND	5.1		63	JTAG_nTRST	4.15
66	PMIC_STBY_REQ	5.2.1		65	JTAG_TMS	4.15
68	PMIC_ON_REQ	5.2.1		67	JTAG_TDO	4.15
70	UART1_RXD ECSPI3_SCLK GPIO5_IO[22]	4.10 4.12 4.16		69	V_SOM	5.1
72	UART1_TXD ECSPI3_MOSI GPIO5_IO[23]	4.10 4.12 4.16		71	JTAG_TDI	4.15
74	UART3_TXD (DBG) UART1_RTS_B GPIO5_IO[27]	4.10 4.10 4.16		73	JTAG_TCK	4.15
76	UART3_RXD (DBG) UART1_CTS_B GPIO5_IO[26]	4.10 4.10 4.16		75	JTAG_MOD	4.15
78	GND	5.1		77	SPDIF_EXT_CLK PWM1_OUT GPIO5_IO[5]	4.6 4.14 4.16
80	UART2_RXD ECSPI3_MISO GPIO5_IO[24]	4.10 4.12 4.16		79	SPDIF_RX PWM2_OUT GPIO5_IO[4]	4.6 4.14 4.16
82	UART2_TXD ECSPI3_SS0 GPIO5_IO[25]	4.10 4.12 4.16		81	SPDIF_TX PWM3_OUT GPIO5_IO[3]	4.6 4.14 4.16
84	UART4_RXD UART2_CTS_B GPIO5_IO[28]	4.10 4.10 4.16		83	V_SOM	5.1
86	UART4_TXD UART2_RTS_B GPIO5_IO[29]	4.10 4.10 4.16		85	ENET_MDC GPIO1_IO[6]	4.3.2 4.16
88	GND	5.1		87	I2C4_SCL PWM2_OUT GPIO5_IO[20]	4.11 4.14 4.16
90	ALT_BOOT	5.4		89	I2C4_SDA PWM1_OUT GPIO5_IO[21]	4.11 4.14 4.16
92	NC	-		91	I2C3_SDA PWM3_OUT GPT3_CLK GPIO5_IO[19]	4.11 4.14 - 4.16
94	I2C3_ SCL PWM4_OUT GPT2_CLK GPIO5_IO[18]	4.11 4.14 - 4.16		93	VCC_RTC	5.1

96	I2C1_SDA ENET_MDIO GPIO5_IO[15]	4.11 4.3.2 4.16		95	GPIO1_IO[5]	4.16
98	NC	-		97	RESERVED	5.8
100	I2C1_SCL ENET_MDC GPIO5_IO[14]	4.11 4.3.2 4.16		99	RESERVED	5.8

Table 42 Connector P2

Pin #	UCM-iMX8M-Mini Signal Name	Ref.		Pin #	UCM-iMX8M-Mini Signal Name	Ref.
2	CSI_P1_CKN	4.2		1	DSI_DN0	4.1
4	CSI_P1_CKP	4.2		3	DSI_DP0	4.1
6	CSI_P1_DN0	4.2		5	DSI_DN2	4.1
8	CSI_P1_DP0	4.2		7	DSI_DP2	4.1
10	GND	5.1		9	V_SOM	5.1
12	NC	-		11	DSI_DN3	4.1
14	NC	-		13	DSI_DP3	4.1
16	GND	5.1		15	DSI_DN1	4.1
18	NC	-		17	DSI_DP1	4.1
20	NC	-		19	V_SOM	5.1
22	GND	5.1		21	DSI_CKN	4.1
24	RESERVED	5.8		23	DSI_CKP	4.1
26	RESERVED	5.8		25	CSI_P1_DN2	4.2
28	GND	5.1		27	CSI_P1_DP2	4.2
30	PCIE1_RXN_N	4.5		29	V_SOM	5.1
32	PCIE1_RXN_P	4.5		31	CSI_P1_DN1	4.2
34	GND	5.1		33	CSI_P1_DP1	4.2
36	PCIE1_TXN_N	4.5		35	CSI_P1_DN3	4.2
38	PCIE1_TXN_P	4.5		37	CSI_P1_DP3	4.2
40	GND	5.1		39	V_SOM	5.1
42	PCIE1_REF_CLKP	4.5		41	SAI1_TXFS SAI5_TXFS GPIO4_IO[10]	4.7 4.7 4.16
44	PCIE1_REF_CLKN	4.5		43	QSPI_A_DATA2 GPIO3_IO[8]	4.13 4.16
46	GND	5.1		45	SAI1_TXC SAI5_TXC GPIO4_IO[11]	4.7 4.7 4.16
48	SAI1_RXD0 SAI5_RXD0 SAI1_TXD1 GPIO4_IO[2]	4.7 4.7 4.7 4.16		47	SAI1_RXFS SAI5_RXFS GPIO4_IO[0]	4.7 4.7 4.16
50	SAI1_RXD1 SAI5_RXD1 GPIO4_IO[3]	4.7 4.7 4.16		49	SD2_WP GPIO2_IO[20]	4.9 4.16
52	SAI1_RXD2 SAI5_RXD2 GPIO4_IO[4]	4.7 4.7 4.16		51	SD2_nRST GPIO2_IO[19]	4.9 4.16
54	GND	5.1		53	SAI1_TXD0 SAI5_TXD0 GPIO4_IO[12]	4.7 4.7 4.16
56	QSPI_A_DATA1 GPIO3_IO[7]	4.13 4.16		55	QSPI_A_SCLK GPIO3_IO[0]	4.13 4.16
58	QSPI_A_DATA3 GPIO3_IO[9]	4.13 4.16		57	V_SOM	5.1
60	SAI1_RXD3 SAI5_RXD3 GPIO4_IO[5]	4.7 4.7 4.16		59	SAI1_TXD1 SAI5_TXD1 GPIO4_IO[13]	4.7 4.7 4.16
62	SAI1_MCLK SAI5_MCLK SAI1_TXC GPIO4_IO[20]	4.7 4.7 4.7 4.16		61	QSPI_A_DATA0 GPIO3_IO[6]	4.13 4.16
64	PWRBTN	5.2.1		63	SAI1_TXD2 SAI5_TXD2 GPIO4_IO[14]	4.7 4.7 4.16
66	POR_B	5.3		65	QSPI_A_SS0_B GPIO3_IO[1]	4.13 4.16
68	GPIO1_IO[9]	4.16		67	SAI1_TXD3 SAI5_TXD3 GPIO4_IO[15]	4.7 4.7 4.16

70	GPIO1_IO[11]	4.16		69	SAI1_RXC SAI5_RX_BCLK GPIO4_IO[1]	4.7 4.7 4.16
72	GND	5.1		71	V_SOM	5.1
74	ETH1_MDI0P ENET_TX_CTL	4.3.1 4.3.2		73	ETH1_MDI0N ENET_TD3	4.3.1 4.3.2
76	ENET_MDC	4.3.2		75	ETH1_LINK-LED_1000 ENET_TD0	4.3.1 4.3.2
78	ETH1_MDI1P ENET_TD1	4.3.1 4.3.2		77	ENET_TD2	4.3.2
80	ETH1_MDI1N ENET_RXC	4.3.1 4.3.2		79	ETH1_MDI2P ENET_RX_CTL	4.3.1 4.3.2
82	GND	5.1		81	ETH1_MDI2N ENET_TXC	4.3.1 4.3.2
84	ETH1_MDI3P ENET_RD2	4.3.1 4.3.2		83	ETH1_LED_ACT ENET_RD1	4.3.1 4.3.2
86	ETH1_LINK-LED_10_100 ENET_RD0	4.3.1 4.3.2		85	ETH1_MDI3N ENET_RD3	4.3.1 4.3.2
88	ENET_MDIO	4.3.2		87	V_SOM	5.1
90	ENET_MDIO GPIO1_IO[7]	4.3.2 4.16		89	ECSPI2_MISO UART4_CTS_B GPIO5_IO[12]	4.12 4.10 4.16
92	SD2_nCD GPIO2_IO[12]	4.9 4.16		91	ECSPI2_SS0 UART4_RTS_B GPIO5_IO[13]	4.12 4.10 4.16
94	EXT_SD2_DATA2 GPIO2_IO[17]	4.9 4.16		93	ECSPI2_SCLK UART4_RXD GPIO5_IO[10]	4.12 4.10 4.16
96	EXT_SD2_CLK GPIO2_IO[13]	4.9 4.16		95	ECSPI2_MOSI UART4_TXD GPIO5_IO[11]	4.12 4.10 4.16
98	EXT_SD2_DATA3 GPIO2_IO[18]	4.9 4.16		97	EXT_SD2_DATA0 GPIO2_IO[15]	4.9 4.16
100	EXT_SD2_CMD GPIO2_IO[14]	4.9 4.16		99	EXT_SD2_DATA1 GPIO2_IO[16]	4.9 4.16

6.2 Mating Connectors

Table 43 Connector type

UCM-iMX8M-Mini connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1, P2	Hirose DF40C-100DP-0.4V51	Hirose	DF40HC(3.0)-100DS-0.4V(51)

6.3 Mechanical Drawings

Figure 3 UCM-iMX8M-Mini top

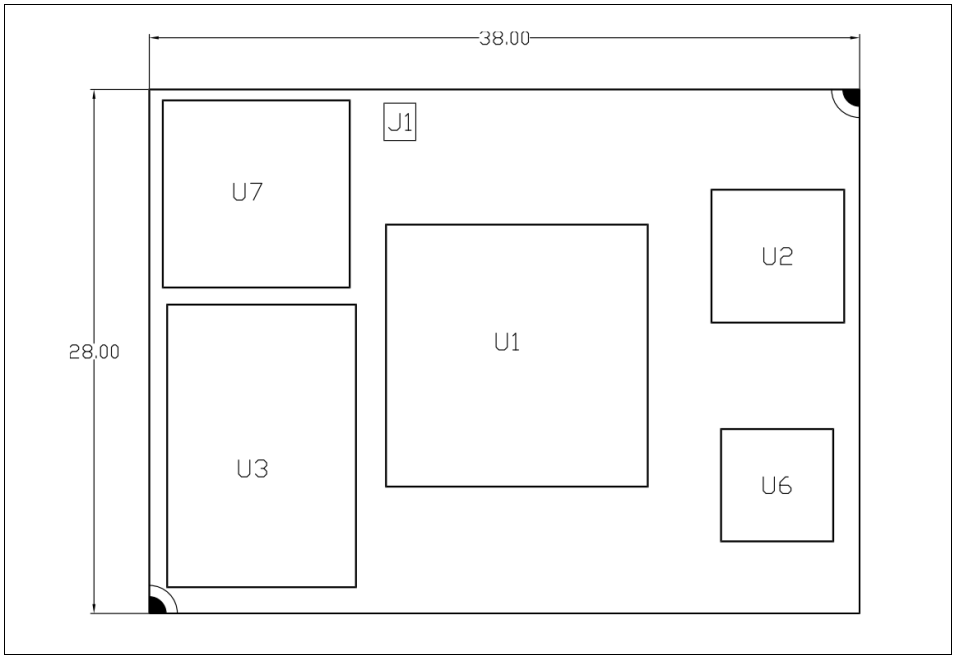
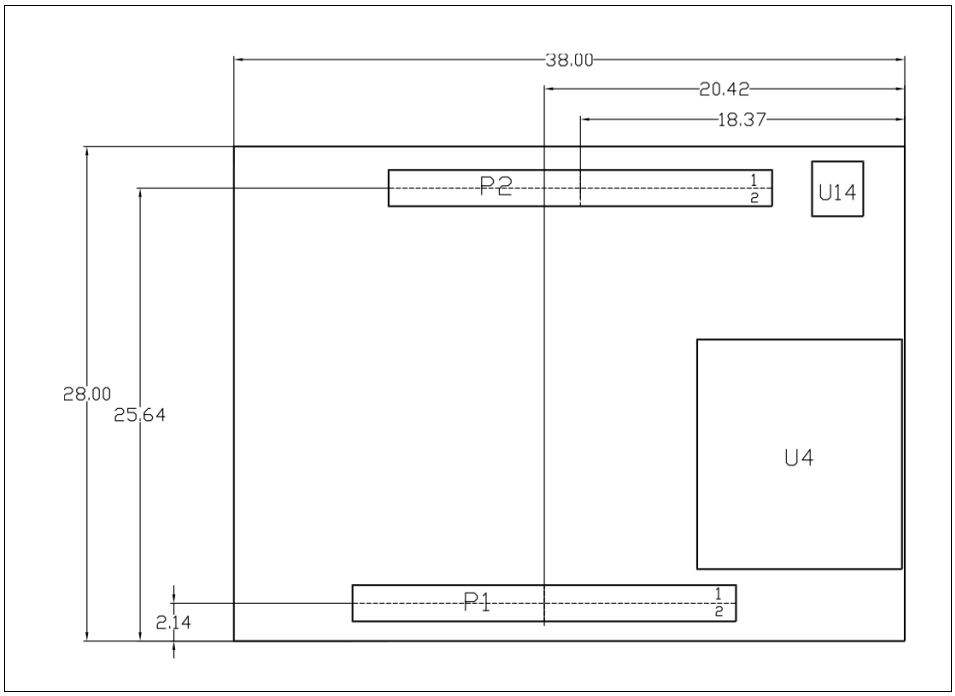


Figure 4 UCM-iMX8M-Mini bottom



1. All dimensions are in millimeters.
2. The height of all components is < 2.0mm.
3. Baseboard connectors provide 3 ± 0.15mm board-to-board clearance.
4. Board thickness is 1.6mm.

3D model and mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/ucm-imx8m-mini-nxp-i-mx-8m-mini-som-system-on-module-computer/#devres

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 44 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 45 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 Typical Power Consumption

Table 46 SOM Typical Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
Linux up – low-power	Linux up, Ethernet down, display output off	97mA	340mW
Linux up – typical	Linux up, Ethernet link up, display output on	301mA	1055mW
Video playback	Video playback with GStreamer in Linux	370mA	1295mW
Camera input to LCD	Video capture from camera to LCD with GStreamer	460mA	1610mW
GPU load	GLMark on 1280x720 @60Hz	500mA	1750mW
WiFi load	WiFi running iPerf3, display output off	480mA	1680mW
Heavy mixed load	GLMark + video playback + CPU load + Ethernet activity	840mA	2940mW

Power consumption has been measured with the following setup:

1. Stock module configuration - UCM-iMX8M-C1800QM-D2-N16-E-WB
2. SB-UCMIMX8 carrier-board, V_SOM = 3.5V
3. 5" WXGA LCD panel
4. LI-OV5640 camera module
5. Software stack - stock Yocto build r1.2.

Table 47 Deep Sleep Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
Deep sleep mode	CPU in deep sleep. DRAM in self-refresh.	5mA	18mW

Table 48 RTC timekeeping current

Use case	Use case description	I_{VCC_RTC}
RTC only	VCC_RTC (3.0V) is supplied from external coin-cell battery V_SOM is not present	70nA

7.4 ESD Performance

Table 49 ESD Performance

Interface	ESD Performance
i.MX8M Mini pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX8M-Mini operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX8M-Mini.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation. For details please refer to section 5.9.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- The carrier board interface connectors provide 3mm mating height. Bear in mind that there are components on the bottom side of UCM-iMX8M-Mini. It is not recommended to place any components underneath the UCM-iMX8M-Mini module.
- Refer to the SB-UCMIMX8 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX8M-Mini, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX8 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.