MCM-iMX8M-Mini

Reference Guide

Compulab Ltd.
P.O. Box 687 Yokneam Illit
20692 ISRAEL
Tel: +972 (4) 8290100
https://www.compulab.com
Fax: +972 (4) 8325251

Table of Contents

Table 1 Revision Notes

Date	Description
July 2020	• First release
July 2020	• Fixed PWM2_OUT pin-out in tables 39 and 28 • Fixed UART4_TXD pin-out in tables 39 and 20 • Fixed I2C1_SDA pin-out in table 39 • Fixed alternative function of pin 91 in table 36 • Fixed minor signal naming typos in table 36
October 2020	• Added SOM typical power consumption table 42 in section 7.3 • Added recommended footprint drawing in section 8.2
February 2021	• Added deep sleep power consumption in section 7.3 • Updated reset description in table 33 in section 5.3 • Added voltage level information in table 32 in section 5.2.1

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab MCM-iMX8M-Mini System-on-Module.

1.2 MCM-iMX8M-Mini Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the MCM-iMX8M-Mini part number: https://www.compulab.com/products/computer-on-modules/mcm-imx8m-mini-nxp-i-mx-8m-mini-solder-down-som-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
MCM-iMX8M-Mini Developer Resources	https://www.compulab.com/products/computer-on-modules/mcm-imx8m-mini-nxp-i-mx-8m-mini-solder-down-som-system-on-module//#devres
i.MX8M Mini Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-mini-family-arm-cortex-a53-cortex-m4-audio-voice-video:i.MX8MMINI?tab=Documentation_Tab
i.MX8M Mini Datasheet	

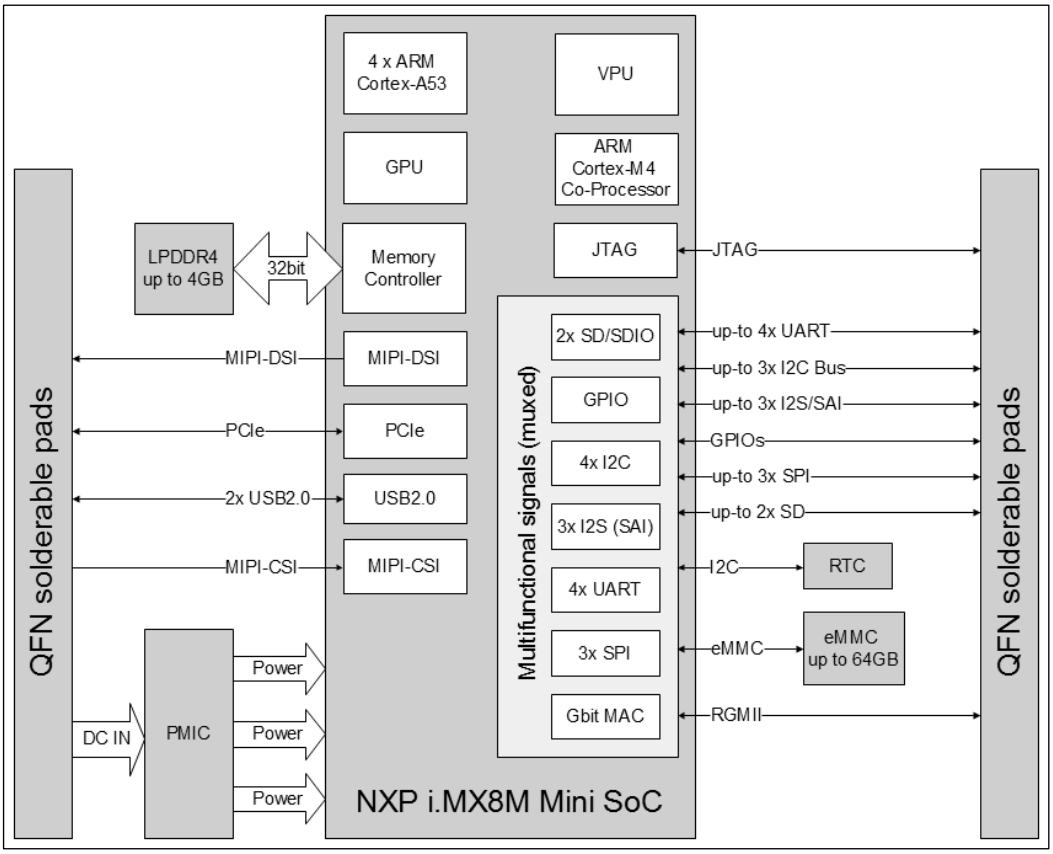
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Mini Processor, up-to 1.8GHz
- Up to 4GB LPDDR4 and 64GB eMMC
- Integrated 2D/3D GPU and 1080p VPU
- MIPI-DSI, up to 1080p60, MIPI-CSI camera input
- PCIe, RGMII, 2x USB, 4x UART, 73x GPIO
- Tiny size and weight - 30 x 30 mm, 5 gram

2.2 Block Diagram

Figure 1 MCM-iMX8M-Mini Block Diagram



2.3 MCM-iMX8M-Mini Features

The "Option" column specifies the SOM configuration option required to have the particular feature. When a SOM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a SOM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Mini DualLite, dual-core ARM Cortex-A53, 1.8GHz	C1800D
	NXP i.MX8M Mini Dual, dual-core ARM Cortex-A53, 1.8GHz	C1800DM
	NXP i.MX8M Mini Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
Video Decode	1080p60 H.265, H.264, VP8, VP9	C1800DM or 1800QM
Video Encode	1080p60 H.264, VP8	C1800DM or 1800QM
GPU	GC NanoUltra GPU OpenGL ES 2.0, Open VG 1.1	+
Real-Time Co-processor	ARM Cortex-M4	+
Memory and Storage		
RAM	1GB – 4GB, LPDDR4	D
Storage	eMMC flash, 4GB - 64GB	N
Display, Camera and Audio		
Display	MIPI-DSI, 4 data lanes, up to 1080p60	+
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	MIPI-CSI, 4 lanes	+
Digital Audio	Up-to 2x I2S / SAI	+
	S/PDIF input/output	+
Network		
Ethernet	1000Mbps Ethernet port, RGMII interface	+
I/O		
PCI Express	PCIe x1 Gen. 2.1	+
USB	2x USB2.0 dual-role ports	+
Serial Ports (UARTs)	Up to 4x UART	+
MMC/SD/SDIO	Up to 2x MMC/SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 86x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

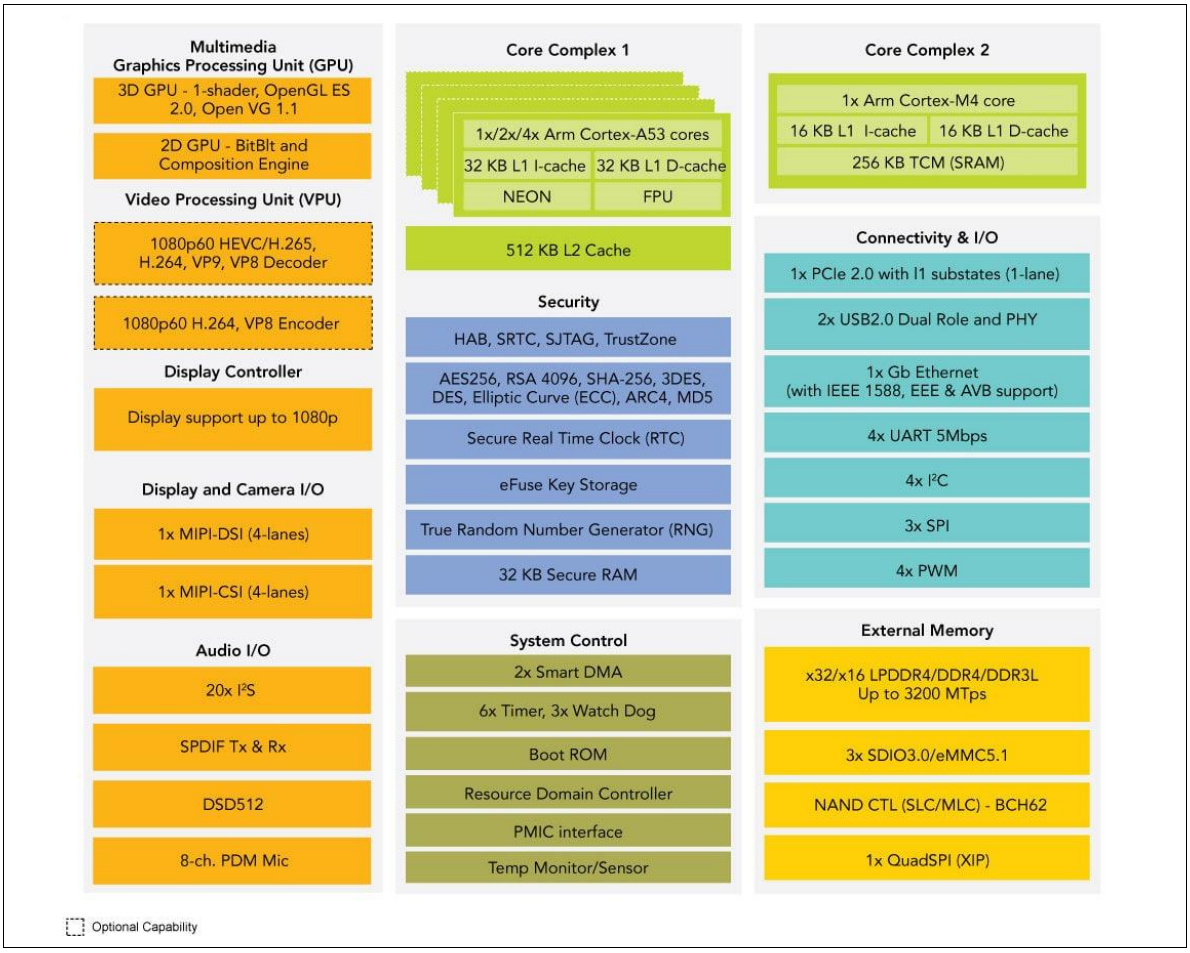
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	30 x 30 x 3 mm
Weight	5 gram
Package	140-pin, 0.8mm pitch QFN
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Mini SoC

The i.MX8M Mini family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M4 core processor enables low-power processing.

Figure 2 i.MX8M Mini Block Diagram



3.2 Memory

3.2.1 DRAM

MCM-iMX8M-Mini is equipped with up to 4GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide and operates at 1600 MHz clock frequency (LPDDR4-3200).

3.2.2 Bootloader and General Purpose Storage

MCM-iMX8M-Mini uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

MCM-iMX8M-Mini implements a variety of peripheral interfaces through the 140-pin carrier board interface pads. The following notes apply to interfaces available through the carrier-board pads:

- Some interfaces/signals are available only with/without certain configuration options of the MCM-iMX8M-Mini SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the MCM-iMX8M-Mini carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5.
- All of the MCM-iMX8M-Mini digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on MCM-iMX8M-Mini configuration options, certain carrier board interface pins are physically disconnected (floating). The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD" -** Always pulled down onboard MCM-iMX8M-Mini, followed by pull value.
- **"PU" -** Always pulled up onboard MCM-iMX8M-Mini, followed by pull value.
- **"LVDS" -** Low-voltage differential signaling.

4.1 MIPI-DSI Interface

The MCM-iMX8M-Mini MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Mini SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals

Table 5 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description
DSI_CKN	39	AO	Negative part of MIPI-DSI clock diff-pair
DSI_CKP	38	AO	Positive part of MIPI-DSI clock diff-pair
DSI_DN0	43	AO	Negative part of MIPI-DSI data diff-pair 0
DSI_DP0	42	AO	Positive part of MIPI-DSI data diff-pair 0
DSI_DN1	41	AO	Negative part of MIPI-DSI data diff-pair 1
DSI_DP1	40	AO	Positive part of MIPI-DSI data diff-pair 1
DSI_DN2	37	AO	Negative part of MIPI-DSI data diff-pair 2
DSI_DP2	36	AO	Positive part of MIPI-DSI data diff-pair 2
DSI_DN3	35	AO	Negative part of MIPI-DSI data diff-pair 3
DSI_DP3	34	AO	Positive part of MIPI-DSI data diff-pair 3

4.2 MIPI-CSI Interface

MCM-iMX8M-Mini MIPI-CSI interface is derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Mini SoC. The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the MIPI-CSI interface signals

Table 6 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description
CSI_P1_CKN	29	AI	Negative part of MIPI-CSI clock diff-pair
CSI_P1_CKP	28	AI	Positive part of MIPI-CSI clock diff-pair
CSI_P1_DN0	33	AI	Negative part of MIPI-CSI data diff-pair 0
CSI_P1_DP0	32	AI	Positive part of MIPI-CSI data diff-pair 0
CSI_P1_DN1	31	AI	Negative part of MIPI-CSI data diff-pair 1
CSI_P1_DP1	30	AI	Positive part of MIPI-CSI data diff-pair 1
CSI_P1_DN2	27	AI	Negative part of MIPI-CSI data diff-pair 2
CSI_P1_DP2	26	AI	Positive part of MIPI-CSI data diff-pair 2
CSI_P1_DN3	25	AI	Negative part of MIPI-CSI data diff-pair 3
CSI_P1_DP3	24	AI	Positive part of MIPI-CSI data diff-pair 3

4.3 RGMII Ethernet

MCM-iMX8M-Mini RGMII interface is derived directly from the i.MX8M Mini Ethernet MAC RGMII and MDIO signals. Please refer to the i.MX8M Mini Reference manual for additional details.

The following table summarizes the Ethernet RGMII interface signals.

Table 7 RGMII Interface Signals

Signal Name	Pin #	Type	Description
ENET_MDC	53* 88* 115*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal
ENET_MDIO	54* 86* 116*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset
ENET_RD0	109*	I	Ethernet input data from the PHY
ENET_RD1	110*	I	Ethernet input data from the PHY
ENET_RD2	113*	I	Ethernet input data from the PHY
ENET_RD3	114*	I	Ethernet input data from the PHY
ENET_RX_CTL	111*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)
ENET_RXC	112*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE
ENET_TD0	106*	O	Ethernet output data to PHY
ENET_TD1	108*	O	Ethernet output data to PHY
ENET_TD2	104*	O	Ethernet output data to PHY
ENET_TD3	107*	O	Ethernet output data to PHY
ENET_TXC	103*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE
ENET_TX_CTL	105*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)
RGMII_VIO	117	P	RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements

NOTE: 2.5V or 3.3V power must be supplied via the RGMII_VIO pin if any of the RGMII signals are used on the carrier-board

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.4 PCI-Express

MCM-iMX8M-Mini provides one PCI Express port. The port requires an external PCIe reference clock to be supplied from the carrier-board.

Table 8 PCIE Interface Signals

Signal Name	Pin #	Type	Description
PCIE1_REF_CLKN	16	AI	100 MHz PCIe reference clock differential input negative
PCIE1_REF_CLKP	17	AI	100 MHz PCIe reference clock differential input positive
PCIE1_RXN_N	19	I	PCI Express receive data negative
PCIE1_RXN_P	18	I	PCI Express receive data positive
PCIE1_TXN_N	20	O	PCI Express transmit data negative
PCIE1_TXN_P	21	O	PCI Express transmit data positive

4.5 Sony/Philips Digital Interface (S/PDIF)

MCM-iMX8M-Mini provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 9 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description
SPDIF_EXT_CLK	81*	I	External clock signal
SPDIF_RX	84*	I	SPDIF input data line signal
SPDIF_TX	82*	O	SPDIF output data line signal

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 Digital Audio (SAI)

MCM-iMX8M-Mini enables access to 3 of the i.MX8M Mini integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Mini Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 10 SAI1 Interface Signals

Signal Name	Pin #	Type	Description
SAI1_MCLK	95*	IO	Audio master clock. An input when generated externally and an output when generated internally.
SAI1_RXC	92*	I	Receive bit clock. An input when generated externally and an output when generated internally.
SAI1_RXD0	91*^	I	Receive data, sampled synchronously by the bit clock

Signal Name	Pin #	Type	Description
SAI1_RXFS	93*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally
SAI1_TXC	90* 95*	O	Transmit bit clock. An input when generated externally and an output when generated internally
SAI1_TXD0	P2-89*^	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI1_TXFS	94*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.

Table 11 SAI2 Interface Signals

Signal Name	Pin #	Type	Description
SAI2_MCLK	99*	IO	Audio master clock. An input when generated externally and an output when generated internally.
SAI2_RXD	102*	I	Receive data, sampled synchronously by the bit clock
SAI2_RXC	97*	I	Receive bit clock. An input when generated externally and an output when generated internally.
SAI2_RXFS	96*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.
SAI2_TXD	98*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI2_TXC	100*	O	Transmit bit clock. An input when generated externally and an output when generated internally.
SAI2_TXFS	101*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.

Table 12 SAI5 Interface Signals

Signal Name	Pin #	Type	Description
SAI5_MCLK	95* 99*	IO	Audio master clock. An input when generated externally and an output when generated internally
SAI5_RX_BCLK	92*	I	Receive bit clock. An input when generated externally and an output when generated internally.
SAI5_RXD0	91*	I	Receive data, sampled synchronously by the bit clock
SAI5_RXFS	93*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally
SAI5_TXD0	89* 102*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI5_TXC	90* 97*	O	Transmit bit clock. An input when generated externally and an output when generated internally.
SAI5_TXD1	96* 101*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI5_TXD2	100*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI5_TXD3	98*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word
SAI5_TX_SYNC	96*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally
SAI5_TXFS	94*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

4.7 USB2.0 ports

i.MX8M Mini SoC is equipped with two dual-role USB2.0 controllers and PHYs. One port supports OTG functionality, while the second port is configured permanently for host mode.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the USB2.0 interface signals.

Table 13 USB OTG port #1 Signals

Signal Name	Pin #	Type	Description
USB1_DN	140	IO	USB2.0 negative data
USB1_DP	139	IO	USB2.0 positive data
USB1_ID	1 79*	I	USB1 OTG ID signal
USB1_VBUS_DET	2	I	USB1 VBUS detect

Table 14 USB host port #2 Signals

Signal Name	Pin #	Type	Description
USB2_DN	137	IO	USB2.0 negative data
USB2_DP	136	IO	USB2.0 positive data
USB2_VBUS_DET	138	I	USB2 VBUS detect

4.8 MMC / SD /SDIO

MCM-iMX8M-Mini features two MMC/SD/SDIO ports derived from the i.MX8M Mini MMC/SD/SDIO controllers (uSDHC1 and uSDHC2). uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to 25 MB/s
- 1-bit, 4-bit or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes
- Dedicated card detection, write protection and Reset signals.

Please refer to the i.MX8M Mini Reference manual for additional details.

The following tables summarize the MMC/SD/SDIO interface signals.

Table 15 MMC/SD/SDIO Port #1 Interface Signals

Signal Name	Pin #	Type	Description
SD1_CLK	118*	O	Clock for MMC/SD/SDIO card
SD1_CMD	126*	IO	CMD line connect to card
SD1_DATA0	122*	IO	DATA0 line in all modes. Also used to detect busy state
SD1_DATA1	123*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode
SD1_DATA2	129*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode

Signal Name	Pin #	Type	Description
SD1_DATA3	119*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD1_DATA4	128*	IO	DATA4 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD1_DATA5	127*	IO	DATA5 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD1_DATA6	124*	IO	DATA6 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD1_DATA7	125*	IO	DATA7 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD1_RESET_B	121*	O	Card hardware reset signal, active LOW

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 16 MMC/SD/SDIO Port #2 Interface Signals

Signal Name	Pin #	Type	Description
SD2_nCD	74*	I	Card detection pin
EXT_SD2_CLK	70*	O	Clock for MMC/SD/SDIO card
EXT_SD2_CMD	69*	IO	CMD line connect to card
EXT_SD2_DATA0	72*	IO	DATA0 line in all modes. Also used to detect busy state
EXT_SD2_DATA1	73*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode
EXT_SD2_DATA2	68*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode
EXT_SD2_DATA3	67*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.
SD2_RESET_B	75* 85*	O	Card hardware reset signal, active LOW
SD2_WP	71*	I	Card write protect detection

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.9 UART

MCM-iMX8M-Mini enables access to up-to four i.MX8M Mini universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Mini UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: By default UART3 is assigned to be used as the main debug console port.

Please refer to the i.MX8M Mini Reference manual for additional details.

The following tables summarize the UART interface signals.

Table 17 UART1 Signals

Signal Name	Pin #	Type	Description
UART1_CTS_B	64* 101*	O	UART-1 clear to send
UART1_RTS_B	63* 102*	I	UART-1 request to send
UART1_RXD	60* 97*	I	UART-1 serial data receive
UART1_TXD	59* 96*	O	UART-1 serial data transmit

Table 18 UART2 Signals

Signal Name	Pin #	Type	Description
UART2_CTS_B	66*	O	UART-2 clear to send
UART2_RTS_B	65*	I	UART-2 request to send
UART2_RXD	61*	I	UART-2 serial data receive
UART2_TXD	62*	O	UART-2 serial data transmit

Table 19 UART3 Signals

Signal Name	Pin #	Type	Description
UART3_RXD (DBG)	64*	I	UART-3 serial data receive
UART3_RXD	48*		
UART3_TXD (DBG)	63*	O	UART-3 serial data transmit
UART3_TXD	45*		
UART3_CTS_B	47*	O	UART-3 clear to send
UART3_RTS_B	46*	I	UART-3 request to send

Table 20 UART4 Signals

Signal Name	Pin #	Type	Description
UART4_RXD	52*	I	UART-4 serial data receive
	66*	I	UART-4 serial data receive
UART4_TXD	51*	O	UART-4 serial data transmit
	65*	O	UART-4 serial data transmit
UART4_CTS_B	50*	O	UART-4 clear to send
UART4_RTS_B	49*	I	UART-4 request to send

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.10 I2C

MCM-iMX8M-Mini features up-to three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the I2C interface signals.

Table 21 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_SCL	53*	O	I2C serial clock line	Always available
I2C1_SDA	54*	IO	I2C serial data line	Always available

Table 22 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	58*	O	I2C serial clock line	Always available
I2C3_SDA	57*	IO	I2C serial data line	Always available

Table 23 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	56*	O	I2C serial clock line	Always available
I2C4_SDA	55*	IO	Always available	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 ECSPI

Up-to three SPI interfaces are accessible through the MCM-iMX8M-Mini carrier board interface. The SPI interfaces are derived from i.MX8M Mini integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX8M Mini Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

Table 24 ECSPI1 Interface Signals

Signal Name	Pin #	Type	Description
ECSPI1_MISO	47*	I	SPI-1 Master data in; slave data out
ECSPI1_MOSI	45*	O	SPI-1 Master data out; slave data in
ECSPI1_SCLK	48*	O	SPI-1 Master clock out; slave clock in
ECSPI1_SS0	46*	O	SPI-1 Chip select 0

Table 25 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description
ECSPI2_MISO	50*	I	SPI-2 Master data in; slave data out
ECSPI2_MOSI	51*	O	SPI-2 Master data out; slave data in
ECSPI2_SCLK	52*	O	SPI-2 Master clock out; slave clock in
ECSPI2_SS0	49*	O	SPI-2 Chip select 0

Table 26 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description
ECSPI3_MISO	61*	I	SPI-3 Master data in; slave data out
ECSPI3_MOSI	59*	O	SPI-3 Master data out; slave data in
ECSPI3_SCLK	60*	O	SPI-3 Master clock out; slave clock in
ECSPI3_SS0	62*	O	SPI-3 Chip select 0

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 QSPI

MCM-iMX8M-Mini features one quad SPI interface. The interface is implemented with the iMX8M Mini integrated QSPI controller. The following features are supported by the QSPI controller:

- Flexible sequence engine to support various flash vendor devices.
- Single pad, dual pad or quad pad mode of operation.
- Single data rate/double data rate mode of operation.
- Parallel Flash mode.
- Direct Memory Access (DMA) support.
- Memory mapped read access to connected flash devices.
- Multi-master access with priority and flexible and configurable buffer for each master.

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the QSPI interface signals.

Table 27 QSPI Interface Signals

Signal Name	Pin #	Type	Description
QSPI_A_DATA0	9*	IO	Data IO 0
QSPI_A_DATA1	5*	IO	Data IO 1
QSPI_A_DATA2	6*	IO	Data IO 2
QSPI_A_DATA3	8*	IO	Data IO 3
QSPI_A_SCLK	10*	O	Serial clock
QSPI_A_SS0_B	7*	O	Chip select 0

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 PWM

MCM-iMX8M-Mini features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 28 PWM Interface Signals

Signal Name	Pin #	Type	Description
PWM1_OUT	55* 81* 87*	O	PWM1 functional output
PWM2_OUT	56* 79* 84*	O	PWM2 functional output
PWM3_OUT	57* 82*	O	PWM3 functional output
PWM4_OUT	58*	O	PWM4 functional output

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 JTAG

MCM-iMX8M-Mini enables access to the i.MX8M Mini JTAG port through the carrier board interface.

Please refer to the i.MX8M Mini Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 29 JTAG Interface Signals

Signal Name	Pin #	Type	Description
JTAG_MOD	134	I	JTAG MODE
JTAG_nTRST	135	I	Test Reset
JTAG_TCK	133	I	Test Clock
JTAG_TDI	131	I	Test Data In
JTAG_TDO	132	O	Test Data Out
JTAG_TMS	130	I	Test Mode Select

4.15 GPIO

Up-to 86 of the i.MX8M Mini general purpose input/output (GPIO) signals are available through the MCM-iMX8M-Mini carrier board interface. When configured as an output, it is possible to write to an i.MX8M Mini register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Mini register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Mini Reference manual for additional details.

NOTE: Internal IO pull up/down is not supported due to errata of the i.MX8M Mini SoC. Use external pull up/down resistors and disable the internal pull up/down in software. For additional details refer to i.MX8M Mini errata e50080.

The table below summarizes the GPIO interface signals.

Table 30 GPIO Signals

Signal Name	Pin #	Type	Description
GPIO1_IO[1]	87*	IO	GPIO
GPIO1_IO[5]	80	IO	GPIO
GPIO1_IO[6]	88*	IO	GPIO
GPIO1_IO[7]	86*	IO	GPIO
GPIO1_IO[8]	85	IO	GPIO
GPIO1_IO[9]	83	IO	GPIO
GPIO1_IO[10]	79*	IO	GPIO
GPIO1_IO[11]	78	IO	GPIO
GPIO1_IO[13]	77	IO	GPIO
GPIO1_IO[16]	115*	IO	GPIO
GPIO1_IO[17]	116*	IO	GPIO
GPIO1_IO[18]	107*	IO	GPIO
GPIO1_IO[19]	104*	IO	GPIO
GPIO1_IO[20]	108*	IO	GPIO
GPIO1_IO[21]	106*	IO	GPIO
GPIO1_IO[22]	105*	IO	GPIO
GPIO1_IO[23]	103*	IO	GPIO
GPIO1_IO[24]	111*	IO	GPIO
GPIO1_IO[26]	109*	IO	GPIO
GPIO1_IO[27]	110*	IO	GPIO
GPIO1_IO[28]	113*	IO	GPIO
GPIO1_IO[29]	114*	IO	GPIO
GPIO2_IO[0]	118*	IO	GPIO
GPIO2_IO[1]	126*	IO	GPIO
GPIO2_IO[2]	122*	IO	GPIO
GPIO2_IO[3]	123*	IO	GPIO
GPIO2_IO[4]	129*	IO	GPIO
GPIO2_IO[5]	119*	IO	GPIO
GPIO2_IO[6]	128*	IO	GPIO
GPIO2_IO[7]	127*	IO	GPIO
GPIO2_IO[8]	124*	IO	GPIO
GPIO2_IO[9]	125*	IO	GPIO
GPIO2_IO[10]	121*	IO	GPIO
GPIO2_IO[11]	120	IO	GPIO
GPIO2_IO[12]	74*	IO	GPIO
GPIO2_IO[13]	70*	IO	GPIO
GPIO2_IO[14]	69*	IO	GPIO
GPIO2_IO[15]	72*	IO	GPIO
GPIO2_IO[16]	73*	IO	GPIO
GPIO2_IO[17]	68*	IO	GPIO
GPIO2_IO[18]	67*	IO	GPIO
GPIO2_IO[19]	75*	IO	GPIO
GPIO2_IO[20]	71*	IO	GPIO
GPIO3_IO[0]	10*	IO	GPIO
GPIO3_IO[1]	7*	O	GPIO
GPIO3_IO[6]	9*	O	GPIO
GPIO3_IO[7]	5*	IO	GPIO
GPIO3_IO[8]	6*	IO	GPIO
GPIO3_IO[9]	8*	IO	GPIO

Signal Name	Pin #	Type	Description
GPIO4_IO[0]	93*	IO	GPIO
GPIO4_IO[1]	92*	IO	GPIO
GPIO4_IO[2]	91*^	IO	GPIO
GPIO4_IO[10]	94*	IO	GPIO
GPIO4_IO[11]	90*	IO	GPIO
GPIO4_IO[12]	89*^	IO	GPIO
GPIO4_IO[20]	95*	IO	GPIO
GPIO4_IO[21]	96*	IO	GPIO
GPIO4_IO[22]	97*	IO	GPIO
GPIO4_IO[23]	102*	IO	GPIO
GPIO4_IO[24]	101*	IO	GPIO
GPIO4_IO[25]	100*	IO	GPIO
GPIO4_IO[26]	98*	IO	GPIO
GPIO4_IO[27]	99*	IO	GPIO
GPIO5_IO[3]	82*	IO	GPIO
GPIO5_IO[4]	84*	IO	GPIO
GPIO5_IO[5]	81*	IO	GPIO
GPIO5_IO[6]	48*	IO	GPIO
GPIO5_IO[7]	45*	IO	GPIO
GPIO5_IO[8]	47*	IO	GPIO
GPIO5_IO[9]	46*	IO	GPIO
GPIO5_IO[10]	52*	IO	GPIO
GPIO5_IO[11]	51*	IO	GPIO
GPIO5_IO[12]	50*	IO	GPIO
GPIO5_IO[13]	49*	IO	GPIO
GPIO5_IO[14]	53*	IO	GPIO
GPIO5_IO[15]	54*	IO	GPIO
GPIO5_IO[18]	58*	IO	GPIO
GPIO5_IO[19]	57*	IO	GPIO
GPIO5_IO[20]	56*	IO	GPIO
GPIO5_IO[21]	55*	IO	GPIO
GPIO5_IO[22]	60*	IO	GPIO
GPIO5_IO[23]	59*	IO	GPIO
GPIO5_IO[24]	61*	IO	GPIO
GPIO5_IO[25]	62*	IO	GPIO
GPIO5_IO[26]	64*	IO	GPIO
GPIO5_IO[27]	63*	IO	GPIO
GPIO5_IO[28]	66*	IO	GPIO
GPIO5_IO[29]	65*	IO	GPIO

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

5 SYSTEM LOGIC

5.1 Power Supply

Table 31 Power signals

Signal Name	Pin#	Type	Description
V_SOM	4,15,141	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
VCC_RTC	13	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
GND	142	P	Common ground
RGMII_VIO	117	P	RGMII interface power supply input. This pin must be connected to 2.5V or 3.3V power rail depending on the PHY requirements

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

MCM-iMX8M-Mini supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Mini SoC. The logic that controls both signals is supplied by the i.MX8M Mini SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that MCM-iMX8M-Mini is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Mini Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 32 External regulator control signals

Signal Name	Pin #	Type	Description
PMIC_STBY_REQ	23	O, 1.8V	When the processor enters SUSPEND mode, it will assert this signal.
PMIC_ON_REQ	44	O, 1.8V	Active high power-up request output from i.MX8M Mini SoC.
PWRBTN	3	I, 1.8V	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).

NOTE: PMIC_STBY_REQ, PMIC_ON_REQ, PWRBTN signals operate at 1.8V voltage level.

5.3 Reset

The POR_B signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on MCM-iMX8M-Mini. Please refer to the i.MX8M Mini Reference manual for additional details.

Table 33 Reset signals

Signal Name	Pin #	Type	Description
POR_B	14	I	Active Low cold reset input signal. Should be used as main system reset. Maximum rise/fall time is 5.0nS. Open-drain signal with a 10konboard pull-up resistor to 3.3V

5.4 Boot Sequence

MCM-iMX8M-Mini boot sequence defines which interface/media is used by MCM-iMX8M-Mini to load and execute the initial software (such as SPL or/and U-boot). MCM-iMX8M-Mini can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD/MMC card using the MMC/SD/SDIO 2 interface

MCM-iMX8M-Mini will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by MCM-iMX8M-Mini:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows MCM-iMX8M-Mini to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 34 Alternative Boot selection signal

Signal Name	Pin #	Type	Description
ALT_BOOT	76	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence

Table 35 MCM-iMX8M-Mini Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on MMC/SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 89 of the MCM-iMX8M-Mini carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the MCM-iMX8M-Mini CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of MCM-iMX8M-Mini pins are derived from the i.MX8M Mini SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

NOTE: Internal IO pull up/down is not supported due to errata of the i.MX8M Mini SoC. Use external pull up/down resistors and disable the internal pull up/down in software. For additional details refer to i.MX8M Mini errata e50080.

Table 36 Multifunctional Signals

Pin #	SoC signal / ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
5	NAND_DATA1	QSPI_A_DATA1				GPIO3_IO[7]
6	NAND_DATA2	QSPI_A_DATA2				GPIO3_IO[8]
7	NAND_nCE0	QSPI_A_SS0_B				GPIO3_IO[1]
8	NAND_DATA3	QSPI_A_DATA3				GPIO3_IO[9]
9	NAND_DATA0	QSPI_A_DATA0				GPIO3_IO[6]
10	NAND_ALE	QSPI_A_SCLK				GPIO3_IO[0]
45	ECSPI1_MOSI	UART3_TXD				GPIO5_IO[7]
46	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO[9]
47	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO[8]
48	ECSPI1_SCLK	UART3_RXD				GPIO5_IO[6]
49	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO[13]
50	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO[12]
51	ECSPI2_MOSI	UART4_TXD				GPIO5_IO[11]
52	ECSPI2_SCLK	UART4_RXD				GPIO5_IO[10]
53	I2C1_SCL	ENET_MDC				GPIO5_IO[14]
54	I2C1_SDA	ENET_MDIO				GPIO5_IO[15]
55	I2C4_SDA	PWM1_OUT				GPIO5_IO[21]
56	I2C4_SCL	PWM2_OUT				GPIO5_IO[20]
57	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO[19]
58	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO[18]
59	UART1_TXD	ECSPI3_MOSI				GPIO5_IO[23]
60	UART1_RXD	ECSPI3_SCLK				GPIO5_IO[22]
61	UART2_RXD	ECSPI3_MISO				GPIO5_IO[24]
62	UART2_TXD	ECSPI3_SS0				GPIO5_IO[25]
63	UART3_TXD (DBG)	UART1_RTS_B				GPIO5_IO[27]
64	UART3_RXD (DBG)	UART1_CTS_B				GPIO5_IO[26]
65	UART4_TXD	UART2_RTS_B				GPIO5_IO[29]
66	UART4_RXD	UART2_CTS_B				GPIO5_IO[28]
67	EXT_SD2_DATA3					GPIO2_IO[18]
68	EXT_SD2_DATA2					GPIO2_IO[17]
69	EXT_SD2_CMD					GPIO2_IO[14]
70	EXT_SD2_CLK					GPIO2_IO[13]
71	SD2_WP					GPIO2_IO[20]
72	EXT_SD2_DATA0					GPIO2_IO[15]
73	EXT_SD2_DATA1					GPIO2_IO[16]
74	SD2_nCD					GPIO2_IO[12]
75	SD2_RESET_B					GPIO2_IO[19]
77	GPIO1_IO[13]					PWM2_OUT
78	GPIO1_IO[11]					
79	GPIO1_IO[10]	USB1 OTG ID				
80	GPIO1_IO[5]					
81	SPDIF_EXT_CLK	PWM1_OUT				GPIO5_IO[5]

Pin #	SoC signal / ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
82	SPDIF_TX	PWM3_OUT				GPIO5_IO[3]
83	GPIO1_IO[9]					
84	SPDIF_RX	PWM2_OUT				GPIO5_IO[4]
85	GPIO1_IO[8]					SD2_RESET_B
86	GPIO1_IO[7]	ENET_MDIO				
87	GPIO1_IO[1]	PWM1_OUT				
88	GPIO1_IO[6]	ENET_MDC				
89	SAI1_TXD0	SAI5_TXD0				GPIO4_IO[12]
90	SAI1_TXC	SAI5_TXC				GPIO4_IO[11]
91	SAI1_RXD0	SAI5_RXD0				GPIO4_IO[2]
92	SAI1_RXC	SAI5_RX_BCLK				GPIO4_IO[1]
93	SAI1_RXFS	SAI5_RXFS				GPIO4_IO[0]
94	SAI1_TXFS	SAI5_TXFS				GPIO4_IO[10]
95	SAI1_MCLK	SAI5_MCLK	SAI1_TXC			GPIO4_IO[20]
96	SAI2_RXFS	SAI5_TX_SYNC	SAI5_TXD1		UART1_TXD	GPIO4_IO[21]
97	SAI2_RXC	SAI5_TXC			UART1_RXD	GPIO4_IO[22]
98	SAI2_TXD	SAI5_TXD3				GPIO4_IO[26]
99	SAI2_MCLK	SAI5_MCLK				GPIO4_IO[27]
100	SAI2_TXC	SAI5_TXD2				GPIO4_IO[25]
101	SAI2_TXFS	SAI5_TXD1			UART1_CTS_B	GPIO4_IO[24]
102	SAI2_RXD	SAI5_TXD0			UART1_RTS_B	GPIO4_IO[23]
103	ENET_TXC					GPIO1_IO[23]
104	ENET_TD2					GPIO1_IO[19]
105	ENET_TX_CTL					GPIO1_IO[22]
106	ENET_TD0					GPIO1_IO[21]
107	ENET_TD3					GPIO1_IO[18]
108	ENET_TD1					GPIO1_IO[20]
109	ENET_RD0					GPIO1_IO[26]
110	ENET_RD1					GPIO1_IO[27]
111	ENET_RX_CTL					GPIO1_IO[24]
112	ENET_RXC					GPIO1_IO[25]
113	ENET_RD2					GPIO1_IO[28]
114	ENET_RD3					GPIO1_IO[29]
115	ENET_MDC					GPIO1_IO[16]
116	ENET_MDIO					GPIO1_IO[17]
118	SD1_CLK					GPIO2_IO[0]
119	SD1_DATA3					GPIO2_IO[5]
120	SD1_STROBE					GPIO2_IO[11]
121	SD1_RESET_B					GPIO2_IO[10]
122	SD1_DATA0					GPIO2_IO[2]
123	SD1_DATA1					GPIO2_IO[3]
124	SD1_DATA6					GPIO2_IO[8]
125	SD1_DATA7					GPIO2_IO[9]
126	SD1_CMD					GPIO2_IO[1]
127	SD1_DATA5					GPIO2_IO[7]
128	SD1_DATA4					GPIO2_IO[6]
129	SD1_DATA2					GPIO2_IO[4]

5.6 RTC

MCM-iMX8M-Mini features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about MCM-iMX8M-Mini RTC please refer to the AM1805 datasheet.

5.7 LED

MCM-iMX8M-Mini features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Mini. The LED is ON when GPIO1_IO[12] is logic LOW.

5.8 Reserved Signals

The following MCM-iMX8M-Mini signals are reserved and must be left unconnected.

Table 37 Reserved Signals

Signal Name	Pin#
RESERVED	11, 12, 22

5.9 Boot Strap Signals

The following MCM-iMX8M-Mini signals must not be pulled or driven by carrier board during SoM power-up or reset.

Table 38 Boot Strap Signals

Pin#
89, 91

6 CARRIER BOARD INTERFACE

The MCM-iMX8M-Mini SOM carrier board interface uses 140-pin QFN package. SOM pinout is detailed in the following table.

6.1 Package Pinout

Table 39 Package Pinout

Pin #	MCM-iMX8M-Mini Signal Name	Ref.	Pin #	MCM-iMX8M-Mini Signal Name	Ref.
1	USB1_ID	4.7	71	SD2_WP GPIO2_IO[20]	4.8 4.15
2	USB1_VBUS_DET	4.7	72	EXT_SD2_DATA0 GPIO2_IO[15]	4.8 4.15
3	PWRBTN	5.2	73	EXT_SD2_DATA1 GPIO2_IO[16]	4.8 4.15
4	V_SOM	5.1	74	SD2_nCD GPIO2_IO[12]	4.8 4.15
5	QSPI_A_DATA1 GPIO3_IO[7]	4.12 4.15	75	SD2_RESET_B GPIO2_IO[19]	4.8 4.15
6	QSPI_A_DATA2 GPIO3_IO[8]	4.12 4.15	76	ALT_BOOT	5.4
7	QSPI_A_SS0_B GPIO3_IO[1]	4.12 4.15	77	GPIO1_IO[13]	4.15
8	QSPI_A_DATA3 GPIO3_IO[9]	4.12 4.15	78	GPIO1_IO[11] PWM2_OUT	4.15 4.13
9	QSPI_A_DATA0 GPIO3_IO[6]	4.12 4.15	79	USB1_ID GPIO1_IO[10]	4.7 4.13 4.15
10	QSPI_A_SCLK GPIO3_IO[0]	4.12 4.15	80	GPIO1_IO[5]	4.15
11	RESERVED	5.8	81	SPDIF_EXT_CLK PWM1_OUT GPIO5_IO[5]	4.5 4.5 4.15
12	RESERVED	5.8	82	SPDIF_TX PWM3_OUT	4.5 4.5
13	VCC_RTC	5.1	83	GPIO1_IO[9]	4.15
14	POR_B	0	84	SPDIF_RX PWM2_OUT	4.5 4.5
15	V_SOM	5.1	85	SD2_RESET_B	4.8
16	PCIE1_REF_CLKN	4.4	86	ENET_MDIO GPIO1_IO[7]	4.3 4.15
17	PCIE1_REF_CLKP	4.4	87	PWM1_OUT GPIO1_IO[1]	4.13 4.15
18	PCIE1_RXN_P	4.4	88	ENET_MDC GPIO1_IO[6]	4.3 4.15
19	PCIE1_RXN_N	4.4	89	SAI1_TXD0 SAI5_TXD0 GPIO4_IO[12]	4.6
20	PCIE1_TXN_N	4.4	90	SAI1_TXC SAI5_TXC GPIO4_IO[11]	4.6 4.6 4.15
21	PCIE1_TXN_P	4.4	91	SAI1_RXD0 SAI5_RXD0 GPIO4_IO[2]	4.6 4.6 4.15
22	RESERVED	5.8	92	SAI1_RXC SAI5_RX_BCLK GPIO4_IO[1]	4.6 4.6 4.15
23	PMIC_STBY_REQ	5.2	93	SAI1_RXFS SAI5_RXFS GPIO4_IO[0]	4.6 4.6 4.15
24	CSI_P1_DP3	4.2	94	SAI1_TXFS SAI5_TXFS GPIO4_IO[10]	4.6 4.6 4.15
25	CSI_P1_DN3	4.2	95	SAI1_MCLK SAI1_TXC SAI5_MCLK GPIO4_IO[20]	4.6 4.6 4.6 4.15
26	CSI_P1_DP2	4.2	96	SAI2_RXFS SAI5_TXD1	4.6 4.6

					SAI5_TX_SYNC UART1_TXD GPIO4_IO[21]	4.6 4.9 4.15
27	CSI_P1_DN2	4.2		97	SAI2_RXC SAI5_TXC UART1_RXD GPIO4_IO[22]	4.6 4.6 4.9 4.15
28	CSI_P1_CKP	4.2		98	SAI2_TXD SAI5_TXD3 GPIO4_IO[26]	4.6 4.6 4.64. 94.1 5
29	CSI_P1_CKN	4.2		99	SAI2_MCLK SAI5_MCLK GPIO4_IO[27]	4.6 4.6 4.64. 94.1 5
30	CSI_P1_DP1	4.2		100	SAI2_TXC SAI5_TXD2 GPIO4_IO[25]	4.6 4.6 4.64. 94.1 5
31	CSI_P1_DN1	4.2		101	SAI2_TXFS SAI5_TXD1 UART1_CTS_B GPIO4_IO[24]	4.6 4.6 4.9 4.15
32	CSI_P1_DP0	4.2		102	SAI2_RXD SAI5_TXD0 UART1_RTS_B GPIO4_IO[23]	4.6 4.6 4.9 4.15
33	CSI_P1_DN0	4.2		103	ENET_TXC GPIO1_IO[23]	4.3 4.15
34	DSI_DP3	4.1		104	ENET_TD2 GPIO1_IO[19]	4.3 4.15
35	DSI_DN3	4.2		105	ENET_TX_CTL GPIO1_IO[22]	4.3 4.15
36	DSI_DP2	4.1		106	ENET_TD0 GPIO1_IO[21]	4.3 4.15
37	DSI_DN2	4.1		107	ENET_TD3 GPIO1_IO[18]	4.3 4.15
38	DSI_CKP	4.1		108	ENET_TD1 GPIO1_IO[20]	4.3 4.15
39	DSI_CKN	4.1		109	ENET_RD0 GPIO1_IO[26]	4.3 4.15
40	DSI_DP1	4.1		110	ENET_RD1 GPIO1_IO[27]	4.3 4.15
41	DSI_DN1	4.1		111	ENET_RX_CTL GPIO1_IO[24]	4.3 4.15
42	DSI_DP0	4.1		112	ENET_RXC	43
43	DSI_DN0	4.1		113	ENET_RD2 GPIO1_IO[28]	4.3 4.15
44	PMIC_ON_REQ	5.2		114	ENET_RD3 GPIO1_IO[29]	4.3 4.15
45	UART3_TXD ECSPI1_MOSI GPIO5_IO[7]	4.9 4.11 4.15		115	ENET_MDC GPIO1_IO[16]	4.3 4.15
46	UART3_RTS_B ECSPI1_SS0 GPIO5_IO[9]	4.9 4.11 4.15		116	ENET_MDIO GPIO1_IO[17]	4.3 4.15
47	UART3_CTS_B ECSPI1_MISO GPIO5_IO[8]	4.9 4.11 4.15		117	RGMII_VIO	4.3
48	UART3_RXD ECSPI1_SCLK GPIO5_IO[6]	4.9 4.11 4.15		118	SD1_CLK GPIO2_IO[0]	4.8 4.15
49	UART4_RTS_B ECSPI2_SS0 GPIO5_IO[13]	4.9 4.11 4.15		119	SD1_DATA3 GPIO2_IO[5]	4.8 4.15
50	UART4_CTS_B ECSPI2_MISO GPIO5_IO[12]	4.9 4.11 4.15		120	GPIO2_IO[11]	4.15
51	UART4_TXD ECSPI2_MOSI GPIO5_IO[11]	4.9 4.11 4.15		121	SD1_RESET_B GPIO2_IO[10]	4.8 4.15

52	UART4_RXD ECSPI2_SCLK GPIO5_IO[10]	4.9 4.11 4.15		122	SD1_DATA0 GPIO2_IO[2]	4.8 4.15
53	ENET_MDC I2C1_SCL GPIO5_IO[14]	4.3 4.10 4.15		123	SD1_DATA1 GPIO2_IO[3]	4.8 4.15
54	ENET_MDIO I2C1_SDA GPIO5_IO[15]	4.3 4.10 4.15		124	SD1_DATA6 GPIO2_IO[8]	4.8 4.15
55	I2C4_SDA PWM1_OUT GPIO5_IO[21]	4.10 4.13 4.15		125	SD1_DATA7 GPIO2_IO[9]	4.8 4.15
56	I2C4_SCL PWM2_OUT GPIO5_IO[20]	4.10 4.13 4.15		126	SD1_CMD GPIO2_IO[1]	4.8 4.15
57	I2C3_SDA PWM3_OUT GPIO5_IO[19]	4.10 4.13 4.15		127	SD1_DATA5 GPIO2_IO[7]	4.8 4.15
58	I2C3_SCL PWM4_OUT GPIO5_IO[18]	4.10 4.13 4.15		128	SD1_DATA4 GPIO2_IO[6]	4.8 4.15
59	UART1_TXD ECSPI3_MOSI GPIO5_IO[23]	4.9 4.11 4.15		129	SD1_DATA2 GPIO2_IO[4]	4.8 4.15
60	UART1_RXD ECSPI3_SCLK GPIO5_IO[22]	4.9 4.11 4.15		130	JTAG_TMS	4.14
61	UART2_RXD ECSPI3_MISO GPIO5_IO[24]	4.9 4.11 4.15 4.11		131	JTAG_TDI	4.14
62	UART2_TXD ECSPI3_SS0 GPIO5_IO[25]	4.9 4.11 4.15		132	JTAG_TDO	4.14
63	UART1_RTS_B UART3_TXD (DBG) GPIO5_IO[27]	4.9 4.9 4.15		133	JTAG_TCK	4.14
64	UART1_CTS_B UART3_RXD (DBG) GPIO5_IO[26]	4.9 4.9 4.15		134	JTAG_MOD	4.14
65	UART2_RTS_B UART4_TXD GPIO5_IO[29]	4.9 4.94. 9 4.15		135	JTAG_nTRST	4.14
66	UART2_CTS_B UART4_RXD GPIO5_IO[28]	4.9 4.9 4.15		136	USB2_DP	4.7
67	EXT_SD2_DATA3 GPIO2_IO[18]	4.8 4.15		137	USB2_DN	4.7
68	EXT_SD2_DATA2 GPIO2_IO[17]	4.8 4.15		138	USB2_VBUS_DET	4.7
69	EXT_SD2_CMD GPIO2_IO[14]	4.8 4.15		139	USB1_DP	4.7
70	EXT_SD2_CLK GPIO2_IO[13]	4.8 4.15		140	USB1_DN	4.7
				141	V_SOM corner pad	5.1
				142	GND center pads	5.1

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 40 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 41 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 Typical Power Consumption

Table 42 SOM Typical Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
OFF mode	System shut down	1mA	4mW
Suspend mode	Linux suspend to RAM	4mA	15mW
Linux up – low-power	Linux up, Ethernet down, display output off	65mA	240mW
Linux up – typical	Linux up, Ethernet link up, display output on	301mA	1110mW
Video playback	Video playback with GStreamer in Linux	380mA	1406mW
Camera input to LCD	Video capture from camera to LCD with GStreamer	480mA	1776mW
GPU load	GLMark on 1280x720 @60Hz	465mA	1720mW
Heavy mixed load	GLMark + video playback + CPU load + Ethernet activity	780mA	2886mW

Power consumption has been measured with the following setup:

1. Stock module configuration - MCM-iMX8M-C1800QM-D2-N16
2. SB-MCMIMX8M carrier-board, V_SOM = 3.7V
3. 5" WXGA LCD panel
4. LI-OV5640 camera module
5. Software stack - stock Yocto build r1.0.

Table 43 Deep Sleep Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
Deep sleep mode	CPU in deep sleep. DRAM in self-refresh.	4mA	15mW

Table 44 RTC timekeeping current

Use case	Use case description	I_{VCC_RTC}
RTC only	VCC_RTC (3.0V) is supplied from external coin-cell battery V_SOM is not present	70nA

7.4 ESD Performance

Table 45 ESD Performance

Interface	ESD Performance
i.MX8M Mini pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 MECHANICAL SPECIFICATIONS

8.1 Mechanical Drawings

Figure 3 MCM-iMX8M-Mini top

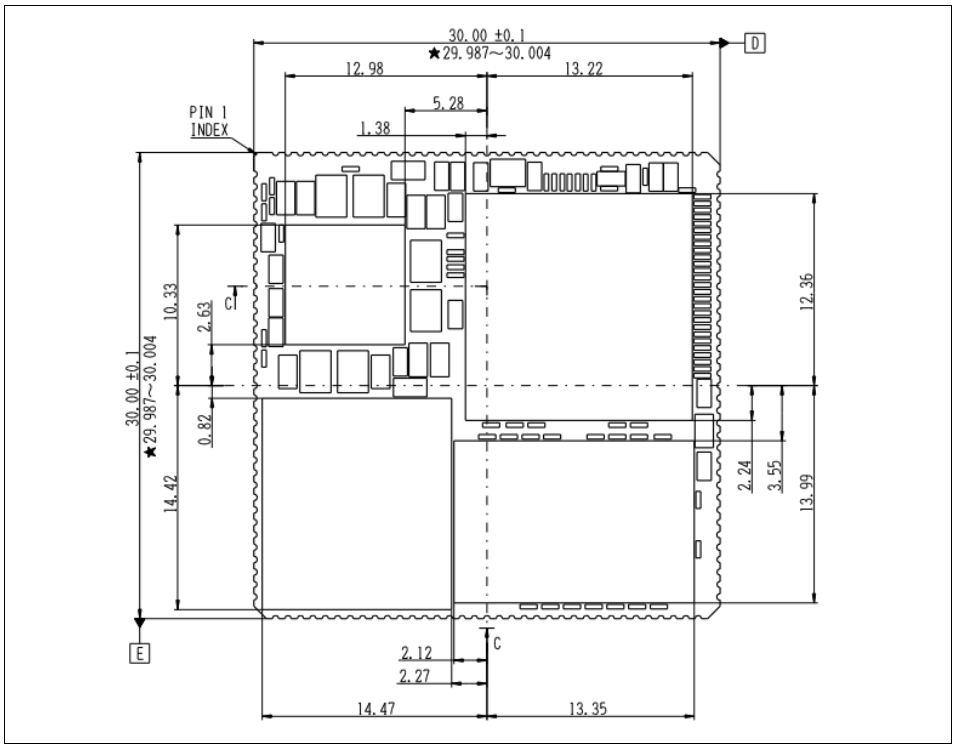
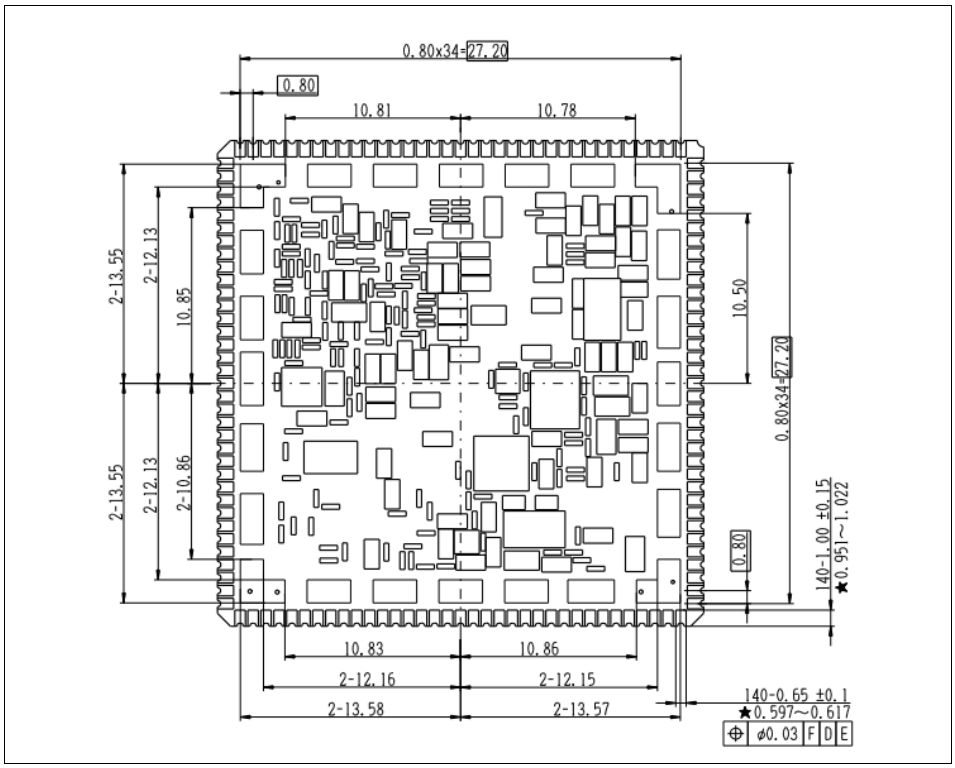


Figure 4 MCM-iMX8M-Mini bottom

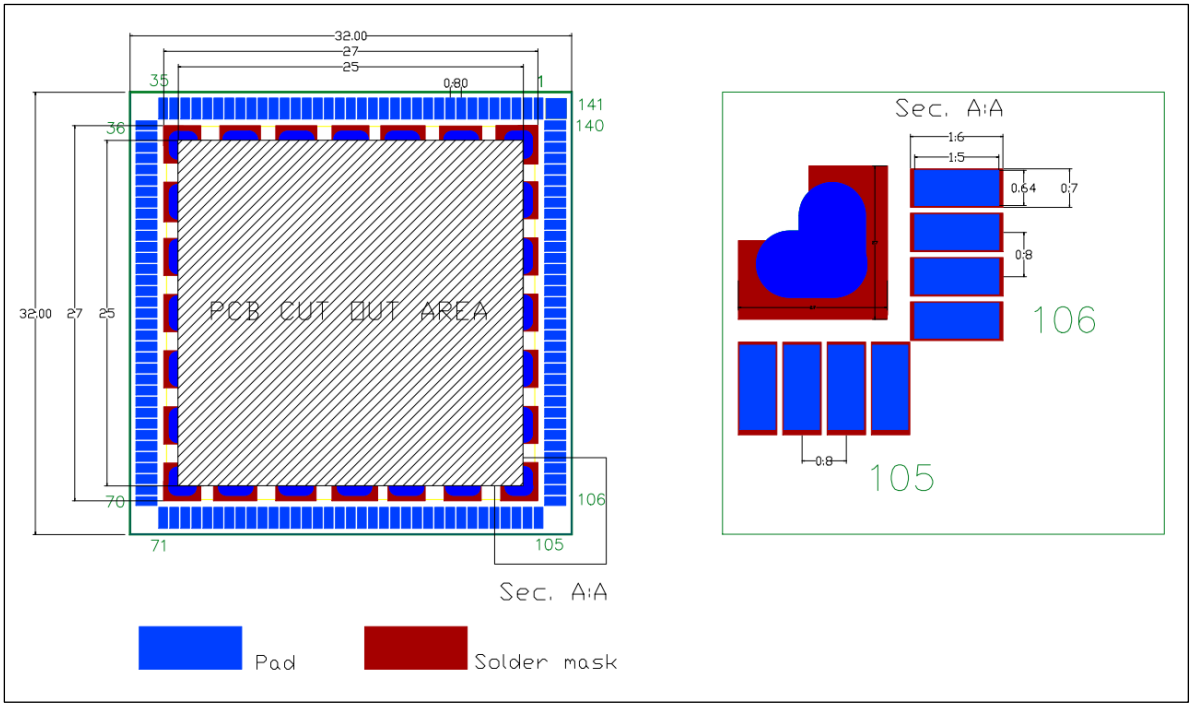


1. All dimensions are in millimeters.
2. Board thickness is 1.2mm.

3D model and mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/mcm-imx8m-mini-nxp-i-mx-8m-mini-solder-down-som-system-on-module/#devres

8.2 Recommended Footprint

Figure 5 MCM-iMX8M-Mini footprint



MCM-iMX8M-Mini footprint in DXF and HKP formats is available at https://www.compulab.com/products/computer-on-modules/mcm-imx8m-mini-nxp-i-mx-8m-mini-solder-down-som-system-on-module/#devres

9 APPLICATION NOTES

9.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for MCM-iMX8M-Mini operation. All power-up circuitry and all required pullups/pulldowns are available onboard MCM-iMX8M-Mini.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation. For details please refer to section 5.9.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Refer to the SB-MCMIMX8M carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

9.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

  - Devices improperly driving the local bus
  - External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
  - Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between the SOM pads. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is recommended to check using an X-ray. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from MCM-iMX8M-Mini, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-MCMIMX8M carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.