

CL-SOM-iMX8MAX

Reference Guide



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Table 1 **Revision Notes**

Date	Description
March 2021	First release

Please check for a newer revision of this manual at the CompuLab website <http://www.compulab.com/>. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX8MAX Computer-on-Module.

1.2 CL-SOM-iMX8MAX Part Number Legend

Please refer to the CompuLab website ‘Ordering information’ section to decode the CL-SOM-iMX8MAX part number: <https://www.compulab.com/products/computer-on-modules/cl-som-imx8max-nxp-i-mx-8-som-system-on-module-computer/#ordering>

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX8MAX Developer Resources	http://www.compulab.com/products/computer-on-modules/cl-som-imx8max-nxp-i-mx-8-som-system-on-module-computer/#devres
iMX 8QuadMax/iMX 8QuadXPlus Hardware Developer’s Guide	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8?tab=Documentation_Tab
iMX 8QuadMax Datasheet	
iMX 8QuadPlus Datasheet	

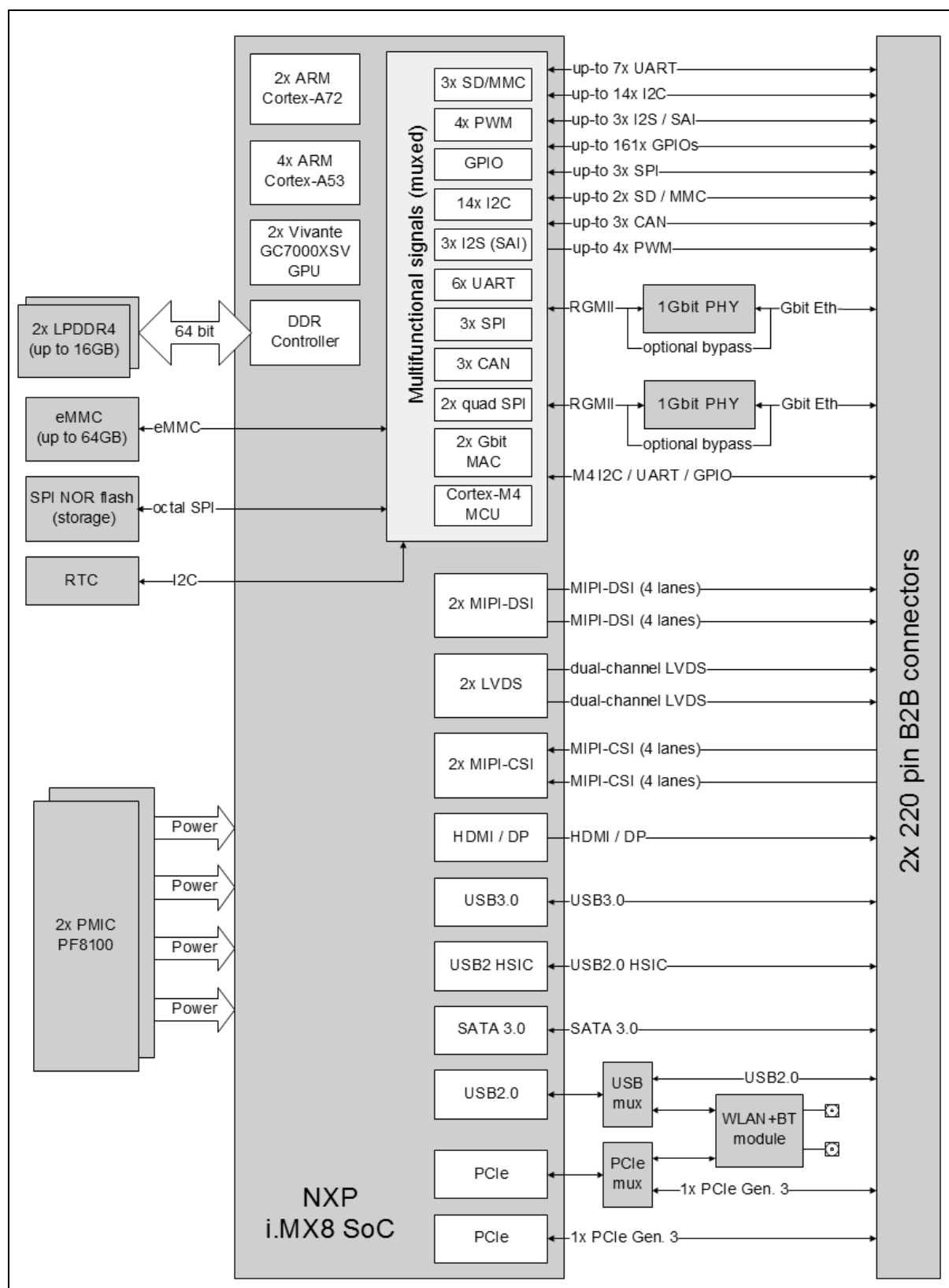
2 OVERVIEW

2.1 Highlights

- NXP i.MX 8QuadMax or NXP i.MX 8QuadPlus processors. Dual/single-core ARM Cortex-A72 @ 1.6GHz, quad-core ARM Cortex-A53 @ 1.2GHz
- Real-time 2x ARM Cortex-M4F co-processor
- Dual 32-bit GPU subsystems, 4K H.265 capable VPU
- Up to 16GB of LPDDR4
- Up to 64GB on-board eMMC storage
- Up to 2Gb on-board octal SPI flash
- Single UltraHD 4Kp60 display or up to 4 independent FullHD 1080p60 displays
- HDMI 2.0a / eDP 1.4 / DP 1.3, 2x MIPI-DSI, 2x dual-channel LVDS, up to 1080p60
- 2x Gbit Ethernet, WiFi 802.11ac, BT 4.2 BLE
- SATA 3, up to 3x PCIe Gen. 3.0, USB 3.0, up to 2x USB 2.0 dual-role port, USB 2.0 HSIC, 2x MIPI-CSI
- Up to 7x UART, 2x USDHC, 3x CAN / CAN-FD, 4-channel ADC converter, up to 161x GPIO
- Miniature size: 70 x 45 x 7.3 mm

2.2 Block Diagram

Figure 1 CL-SOM-iMX8MAX Block Diagram



2.3 CL-SOM-iMX8MAX Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by "NOT", the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the "Option" column. "+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX 8QuadMax, dual-core ARM Cortex-A72, 1.6GHz, quad-core ARM Cortex-A53, 1.2GHz	C1600QM
	NXP i.MX 8QuadPlus, single-core ARM Cortex-A72, 1.6GHz, quad-core ARM Cortex-A53, 1.26GHz	C1600QP
Video Decode	4k H.265, 4K H.264, VP8, MPEG4.2 ASP, RealVideo	+
Video Encode	2x1080p H.264	C1600QM
	2x1080p H.264	C1600QP
GPU	2× GC7000XSVX GPUs OpenGL 3.0, OpenGL ES 3.2, OpenCL 1.2 FP, OpenVG 1.1, Vulkan	+
DSP	Tensilica® HiFi 4 DSP	+
Real-Time Coprocessor	2x ARM Cortex-M4F, 264 MHz	+
Memory and Storage		
RAM	LPDDR4 (64bit), 2GB – 16GB	D
Storage	eMMC flash, 4GB - 64GB	N
	Octal SPI flash, up to 2Gb	NOR
	Quad / Dual SPI flash, 16Mb	+
Display and Camera		
Display	Single UltraHD 4Kp60 display or up to 4 independent FullHD 1080p60 displays	+
	HDMI 2.0a / eDP 1.4 / DP 1.3	
	2x MIPI-DSI, 4 data lanes, up to 1080p60	
	2x dual-channel LVDS, up to 1080p60	
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Network		
Ethernet	1x Gigabit Ethernet port (MAC+PHY)	E1
	2x Gigabit Ethernet ports (MAC+PHY)	E2
	Up-to 2x RGMII / RMII	NOT E1 and NOT E2
WiFi	Certified 802.11ac WiFi interface Intel 8265 chipset * mutually exclusive with PCIe port	WB
Bluetooth	Bluetooth 4.2 BLE	
Audio		
Digital Audio	Up-to 3x I2S / SAI	+
	1x ESAI	+
	S/PDIF input/output	+
I/O		
PCI Express	1x PCIe Gen. 3.0	+
	additional 1x PCIe Gen. 3.0 * mutually exclusive with WiFi	+
PCI Express / SATA	1x PCIe Gen. 3.0 * mutually exclusive with SATA	+
	1x SATA 3 * mutually exclusive with PCIe	C1600QM
	USB	1× USB 3.0

Feature	Description	Option
	1x USB 2.0 dual-role port	+
	1x USB 2.0 dual-role port * mutually exclusive with BT	+
	USB 2.0 HSIC	+
UART	Up to 7x UART	+
SD / MMC	2x USDHC	+
CAN bus	Up to 3x CAN / CAN-FD	+
SPI	Up to 3x SPI	+
I2C	Up to 14x I2C	+
PWM	Up to 4x general purpose PWM signals	+
ADC	1× 4-channel ADC converter	+
GPIO	Up to 161x GPIO (multifunctional signals shared with other functions)	+
System Logic and Debug		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

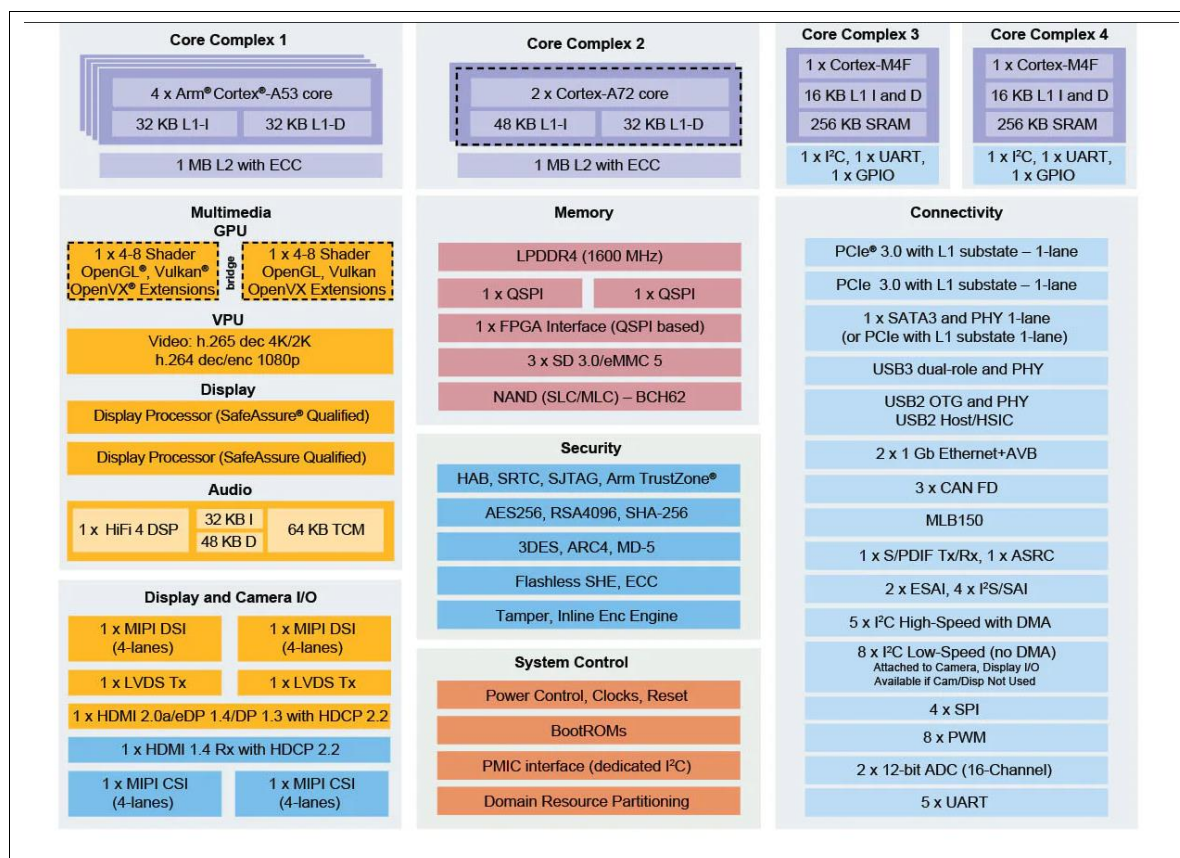
Electrical Specifications	
Supply Voltage	4.0V to 5.5V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	70 x 45 x 7 mm
Weight	26 gram
Connectors	2x AMP 3-6318490-6: 220 contacts, Pitch:0.5mm
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 iMX 8 SoC

The i.MX 8 family of processors features advanced implementation of up to dual-core ARM® Cortex®-A72, which operates at speeds of up to 1.6 GHz and a quad-core ARM® Cortex®-A53, which operates at speeds of up to 1.2 GHz. A general purpose Cortex®-M4F core processor enables low-power processing.

Figure 2 i.MX 8 Block Diagram



3.2 Memory

3.2.1 DRAM

CL-SOM-iMX8MAX is equipped with up to 16GB of on-board, 64-bit LPDDR4 memory.

3.2.2 Additional Storage

CL-SOM-iMX8MAX can be assembled with an up to 256MB of SPI flash for general use.

3.2.3 Bootloader and General Purpose Storage

The CL-SOM-iMX8MAX uses on-board non-volatile memory (eMMC) storage as its bootloader host. The remaining eMMC space is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

CL-SOM-iMX8MAX implements a variety of peripheral interfaces through the carrier board connectors. The following notes apply to interfaces available through the two AMP 3-6318490-6, 220 contacts (each) connectors:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-iMX8MAX SoM. The availability restrictions of each signal are described in the “Signals description” table for each interface.
- Some of the CL-SOM-iMX8MAX carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the CL-SOM-iMX8 digital interfaces operate at 3.3V voltage levels unless otherwise noted.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#”** – The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **“Type”** – Signal type, see the definition of different signal types below
- **“Description”** – Signal description with regards to the interface in question.
- **“Availability”** – Depending on CL-SOM-iMX8AX Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-SOM-iMX8MAX. The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **“O”** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **“PD”** - Always pulled down onboard CL-SOM-IMX8, followed by pull value.
- **“PU”** - Always pulled up onboard CL-SOM-IMX8, followed by pull value.
- **“LVDS”** - Low-voltage differential signaling.

4.1 HDMI / DP

CL-SOM-iMX8MAX HDMI-TX / DisplayPort interface is derived from the i.MX 8 HD Display Transmitter Controller IP. It supports up to 4K resolution.

The controller supports the following protocols:

- HDMI 2.0a Specification
- HDMI 1.4b Specification
- eDP 1.4
- DP 1.3
- High-bandwidth Digital Content Protection system, Mapping HDCP to HDMI, Revision 2.2
- High-bandwidth Digital Content Protection system, Mapping HDCP to DisplayPort, Revision 2.2
- CEA-861-F
- IEC60958

The table below summarizes the HDMI interface signals:

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_AUXN	P2-B104	IO	HEAC -	Always available
HDMI_AUXP	P2-B105	IO	HEAC +	Always available
HDMI_CEC	P2-B93	O	Consumer Electronics Control	Always available
HDMI_CLKN	P2-B102	O	TMDS Clock-	Always available
HDMI_CLKP	P2-B101	O	TMDS Clock+	Always available
HDMI_DDC_SCL	P2-B92	O	VESA Data Display Channel clock	Always available
HDMI_DDC_SDA	P2-B91	IO	VESA Data Display Channel data signal	Always available
HDMI_HPD	P2-B107	O	Hot Plug Detect	Always available
HDMI_TXN0	P2-B99	O	TMDS Data0-	Always available
HDMI_TXN1	P2-B96	O	TMDS Data1-	Always available
HDMI_TXN2	P2-B89	O	TMDS Data2-	Always available
HDMI_TXP0	P2-B98	O	TMDS Data0+	Always available
HDMI_TXP1	P2-B95	O	TMDS Data1+	Always available
HDMI_TXP2	P2-B88	O	TMDS Data2+	Always available

4.2 MIPI-DSI Interface

The MIPI-DSI interface available with CL-SOM-iMX8MAX is based on the two four-lane MIPI-DSI display interface available with the iMX 8 SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 Data Lanes
- Supports MIPI Standard for D-PHY
- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Supports up to 4K resolution at 30Hz
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

The table below summarizes the MIPI-DSI interface signals:

Table 6 MIPI-DSI0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI0_CLKN	P2-B58	O	Negative part of MIPI-DSI0 clock diff-pair	Always available
DSI0_CLKP	P2-B59	O	Positive part of MIPI-DSI0 clock diff-pair	Always available
DSI0_DN0	P2-B55	O	Negative part of MIPI-DSI0 data diff-pair 0	Always available
DSI0_DN1	P2-B62	O	Negative part of MIPI-DSI0 data diff-pair 1	Always available
DSI0_DN2	P2-B52	O	Negative part of MIPI-DSI0 data diff-pair 2	Always available
DSI0_DN3	P2-B65	O	Negative part of MIPI-DSI0 data diff-pair 3	Always available
DSI0_DP0	P2-B56	O	Positive part of MIPI-DSI0 data diff-pair 0	Always available

Signal Name	Pin #	Type	Description	Availability
DSI0_DP1	P2-B63	O	Positive part of MIPI-DSI0 data diff-pair 1	Always available
DSI0_DP2	P2-B53	O	Positive part of MIPI-DSI0 data diff-pair 2	Always available
DSI0_DP3	P2-B66	O	Positive part of MIPI-DSI0 data diff-pair 3	Always available
DSI0_GPIO0_00	P2-A67*	IO	Dedicated GPIO signal for MIPI-DSI0	Always available
DSI0_GPIO0_01	P2-A68*	IO	Dedicated GPIO signal for MIPI-DSI0	Always available
DSI0_I2C0_SCL	P2-A66*	O	Dedicated I2C clock for MIPI-DSI0	Always available
DSI0_I2C0_SDA	P2-A65*	IO	Dedicated I2C data for MIPI-DSI0	Always available

Table 7 MIPI-DSI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI1_CLKN	P2-A53	O	Negative part of MIPI-DSI1 clock diff-pair	Always available
DSI1_CLKP	P2-A52	O	Positive part of MIPI-DSI1 clock diff-pair	Always available
DSI1_DN0	P2-A50	O	Negative part of MIPI-DSI1 data diff-pair 0	Always available
DSI1_DN1	P2-A56	O	Negative part of MIPI-DSI1 data diff-pair 1	Always available
DSI1_DN2	P2-A47	O	Negative part of MIPI-DSI1 data diff-pair 2	Always available
DSI1_DN3	P2-A59	O	Negative part of MIPI-DSI1 data diff-pair 3	Always available
DSI1_DP0	P2-A49	O	Positive part of MIPI-DSI1 data diff-pair 0	Always available
DSI1_DP1	P2-A55	O	Positive part of MIPI-DSI1 data diff-pair 1	Always available
DSI1_DP2	P2-A46	O	Positive part of MIPI-DSI1 data diff-pair 2	Always available
DSI1_DP3	P2-A58	O	Positive part of MIPI-DSI1 data diff-pair 3	Always available
DSI1_GPIO0_00	P2-A64*	IO	Dedicated GPIO signal for MIPI-DSI1	Always available
DSI1_GPIO0_01	P2-A63*	IO	Dedicated GPIO signal for MIPI-DSI1	Always available
DSI1_I2C0_SCL	P2-A61*	O	Dedicated I2C clock for MIPI-DSI1	Always available
DSI1_I2C0_SDA	P2-A62*	IO	Dedicated I2C data for MIPI-DSI1	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.3 LVDS Display interface

The LVDS interface available with CL-SOM-iMX8MAX is based on the two two-lane LVDS display interface available with the iMX 8 SoC. The following main features are supported:

- Two LVDS interfaces supporting:
 - 1080p60 on a single interface
 - 4k30 when aggregating the two interfaces

The tables below summarize the LVDS interface signals

Table 8 LVDS 0 display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CH0_CLK_N	P2-B15	O	Negative part of differential clock of LVDS0 channel 0	Always available
LVDS0_CH0_CLK_P	P2-B16	O	Positive part of differential clock of LVDS0 channel 0	Always available
LVDS0_CH0_TX0_N	P2-B12	O	Negative part of differential data 0 of LVDS0 channel 0	Always available
LVDS0_CH0_TX0_P	P2-B13	O	Positive part of differential data 0 of LVDS0 channel 0	Always available
LVDS0_CH0_TX1_N	P2-B9	O	Negative part of differential data 1 of LVDS0 channel 0	Always available
LVDS0_CH0_TX1_P	P2-B10	O	Positive part of differential data 1 of LVDS0 channel 0	Always available
LVDS0_CH0_TX2_N	P2-B6	O	Negative part of differential data 2 of LVDS0 channel 0	Always available
LVDS0_CH0_TX2_P	P2-B7	O	Positive part of differential data 2 of LVDS0 channel 0	Always available
LVDS0_CH0_TX3_N	P2-B3	O	Negative part of differential data 3 of LVDS0 channel 0	Always available
LVDS0_CH0_TX3_P	P2-B4	O	Positive part of differential data 3 of LVDS0 channel 0	Always available
LVDS0_CH1_CLK_N	P2-A30	O	Negative part of differential clock of LVDS0 channel 1	Always available
LVDS0_CH1_CLK_P	P2-A29	O	Positive part of differential clock of LVDS0 channel 1	Always available
LVDS0_CH1_TX0_N	P2-A33	O	Negative part of differential data 0 of LVDS0 channel 1	Always available
LVDS0_CH1_TX0_P	P2-A32	O	Positive part of differential data 0 of LVDS0 channel 1	Always available
LVDS0_CH1_TX1_N	P2-A36	O	Negative part of differential data 1 of LVDS0 channel 1	Always available
LVDS0_CH1_TX1_P	P2-A35	O	Positive part of differential data 1 of LVDS0 channel 1	Always available
LVDS0_CH1_TX2_N	P2-A39	O	Negative part of differential data 2 of LVDS0 channel 1	Always available
LVDS0_CH1_TX2_P	P2-A38	O	Positive part of differential data 2 of LVDS0 channel 1	Always available
LVDS0_CH1_TX3_N	P2-A43	O	Negative part of differential data 3 of LVDS0 channel 1	Always available
LVDS0_CH1_TX3_P	P2-A42	O	Positive part of differential data 3 of LVDS0 channel 1	Always available
LVDS0_GPIO00	P2-A25*	IO	Dedicated GPIO signal for LVDS0	Always available
LVDS0_GPIO01	P2-A24*	IO	Dedicated GPIO signal for LVDS0	Always available

Signal Name	Pin #	Type	Description	Availability
LVDS0_I2C0_SCL	P2-A44*	O	Dedicated I2C clock for LVDS0 channel 0	Always available
LVDS0_I2C1_SCL	P2-A26*	O	Dedicated I2C clock for LVDS0 channel 1	Always available
LVDS0_I2C1_SDA	P2-A27*	IO	Dedicated I2C data for LVDS0 channel 1	Always available

Table 9 LVDS 1 Display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS1_CH0_CLK_N	P2-B15	O	Negative part of differential clock of LVDS1 channel 0	Always available
LVDS1_CH0_CLK_P	P2-B16	O	Positive part of differential clock of LVDS1 channel 0	Always available
LVDS1_CH0_TX0_N	P2-B12	O	Negative part of differential data 0 of LVDS1 channel 0	Always available
LVDS1_CH0_TX0_P	P2-B13	O	Positive part of differential data 0 of LVDS1 channel 0	Always available
LVDS1_CH0_TX1_N	P2-B26	O	Negative part of differential data 1 of LVDS1 channel 0	Always available
LVDS1_CH0_TX1_P	P2-B27	O	Positive part of differential data 1 of LVDS1 channel 0	Always available
LVDS1_CH0_TX2_N	P2-B23	O	Negative part of differential data 2 of LVDS1 channel 0	Always available
LVDS1_CH0_TX2_P	P2-B24	O	Positive part of differential data 2 of LVDS1 channel 0	Always available
LVDS1_CH0_TX3_N	P2-B18	O	Negative part of differential data 3 of LVDS1 channel 0	Always available
LVDS1_CH0_TX3_P	P2-B19	O	Positive part of differential data 3 of LVDS1 channel 0	Always available
LVDS1_CH1_CLK_N	P2-B35	O	Negative part of differential clock of LVDS1 channel 1	Always available
LVDS1_CH1_CLK_P	P2-B36	O	Positive part of differential clock of LVDS1 channel 1	Always available
LVDS1_CH1_TX0_N	P2-B38	O	Negative part of differential data 0 of LVDS1 channel 1	Always available
LVDS1_CH1_TX0_P	P2-B39	O	Positive part of differential data 0 of LVDS1 channel 1	Always available
LVDS1_CH1_TX1_N	P2-B43	O	Negative part of differential data 1 of LVDS1 channel 1	Always available
LVDS1_CH1_TX1_P	P2-B44	O	Positive part of differential data 1 of LVDS1 channel 1	Always available
LVDS1_CH1_TX2_N	P2-B46	O	Negative part of differential data 2 of LVDS1 channel 1	Always available
LVDS1_CH1_TX2_P	P2-B47	O	Positive part of differential data 2 of LVDS1 channel 1	Always available
LVDS1_CH1_TX3_N	P2-B49	O	Negative part of differential data 3 of LVDS1 channel 1	Always available
LVDS1_CH1_TX3_P	P2-B50	O	Positive part of differential data 3 of LVDS1 channel 1	Always available
LVDS1_GPIO00	P2-B61*	IO	Dedicated GPIO signal for LVDS1	Always available
LVDS1_GPIO01	P2-B20*	IO	Dedicated GPIO signal for LVDS1	Always available
LVDS1_I2C0_SCL	P2-B22*	O	Dedicated I2C clock for LVDS1 channel 0	Always available
LVDS1_I2C1_SCL	P2-B42*	O	Dedicated I2C clock for LVDS1 channel 1	Always available
LVDS1_I2C1_SDA	P2-B40*	IO	Dedicated I2C data for LVDS1 channel 1	Always available

4.4 Camera Serial Interface

CL-SOM-iMX8MAX MIPI-CSI interface is derived from the four-lane MIPI CSI2 host controller integrated into the iMX 8 SoC. The following main features are supported:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol, Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode (80Mbps - 1.5Gbps) per lane
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs

The table below summarizes the MIPI-CSI interface signals:

Table 10 MIPI-CSI0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI0_CLKN	P2-A78	O	Negative part of MIPI-CSI0 clock diff-pair	Always available
CSI0_CLKP	P2-A79	O	Positive part of MIPI-CSI0 clock diff-pair	Always available
CSI0_DN0	P2-A75	I	Negative part of MIPI-CSI0 data diff-pair 0	Always available
CSI0_DN1	P2-A81	I	Negative part of MIPI-CSI0 data diff-pair 1	Always available
CSI0_DN2	P2-A72	I	Negative part of MIPI-CSI0 data diff-pair 2	Always available
CSI0_DN3	P2-A84	I	Negative part of MIPI-CSI0 data diff-pair 3	Always available
CSI0_DP0	P2-A76	I	Positive part of MIPI-CSI0 data diff-pair 0	Always available
CSI0_DP1	P2-A82	I	Positive part of MIPI-CSI0 data diff-pair 1	Always available
CSI0_DP2	P2-A73	I	Positive part of MIPI-CSI0 data diff-pair 2	Always available
CSI0_DP3	P2-A85	I	Positive part of MIPI-CSI0 data diff-pair 3	Always available
CSI0_MCLK_OUT	P2-A87*	O	Clock output	Always available
CSI0_GPIO0_00	P2-A69*	IO	Dedicated GPIO signal for MIPI-CSI0	Always available
CSI0_GPIO0_01	P2-A71*	IO	Dedicated GPIO signal for MIPI-CSI0	Always available

Signal Name	Pin #	Type	Description	Availability
CS10_I2C0_SCL	P2-A91*	O	Dedicated I2C clock for MIPI-CS10	Always available
CS10_I2C0_SDA	P2-A92*	IO	Dedicated I2C data for MIPI-CS10	Always available

Table 11 MIPI-CS11 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CS11_CLKN	P2-A102	O	Negative part of MIPI-CS11 clock diff-pair	Always available
CS11_CLKP	P2-A101	O	Positive part of MIPI-CS11 clock diff-pair	Always available
CS11_DN0	P2-A99	I	Negative part of MIPI-CS11 data diff-pair 0	Always available
CS11_DN1	P2-A106	I	Negative part of MIPI-CS11 data diff-pair 1	Always available
CS11_DN2	P2-A89	I	Negative part of MIPI-CS11 data diff-pair 2	Always available
CS11_DN3	P2-A109	I	Negative part of MIPI-CS11 data diff-pair 3	Always available
CS11_DP0	P2-A98	I	Positive part of MIPI-CS11 data diff-pair 0	Always available
CS11_DP1	P2-A105	I	Positive part of MIPI-CS11 data diff-pair 1	Always available
CS11_DP2	P2-A88	I	Positive part of MIPI-CS11 data diff-pair 2	Always available
CS11_DP3	P2-A108	I	Positive part of MIPI-CS11 data diff-pair 3	Always available
CS11_MCLK_OUT	P2-A93*	O	Clock output	Always available
CS11_GPIO0_00	P2-A96*	IO	Dedicated GPIO signal for MIPI-CS11	Always available
CS11_GPIO0_01	P2-A104*	IO	Dedicated GPIO signal for MIPI-CS11	Always available
CS11_I2C0_SCL	P2-A94*	O	Dedicated I2C clock for MIPI-CS11	Always available
CS11_I2C0_SDA	P2-A95*	IO	Dedicated I2C data for MIPI-CS11	Always available

4.5 Ethernet

CL-SOM-iMX8MAX incorporates two optional full-featured 10/100/1000 Ethernet interfaces, implemented with the i.MX 8 MAC.

4.5.1 Gigabit Ethernet

CL-SOM-iMX8MAX features one (“E1” configuration option) or two (“E2” configuration option) onboard AR8033 PHYs which support the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports all IEEE 1588 frames - inside the MAC
- Automatic channel swap (ACS) Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The table below summarizes the GbE interface signals:

Table 12 GbE 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EPHY0_TRXN0	P1-B33*	O	Negative part of GbE 0 100ohm diff-pair 0	E1 or E2
EPHY0_TRXP0	P1-B34*	I	Positive part of GbE 0 100ohm diff-pair 0	E1 or E2
EPHY0_TRXN1	P1-B36*	O	Negative part of GbE 0 100ohm diff-pair 1	E1 or E2
EPHY0_TRXP1	P1-B37*	I	Positive part of GbE 0 100ohm diff-pair 1	E1 or E2
EPHY0_TRXN2	P1-B39*	O	Negative part of GbE 0 100ohm diff-pair 2	E1 or E2
EPHY0_TRXP2	P1-B40*	I	Positive part of GbE 0 100ohm diff-pair 2	E1 or E2
EPHY0_TRXN3	P1-B29*	O	Negative part of GbE 0 100ohm diff-pair 3	E1 or E2
EPHY0_TRXP3	P1-B30*	I	Positive part of GbE 0 100ohm diff-pair 3	E1 or E2
EPHY0_LED_10_100	P1-B32*	PU/PD	Activity LED driver	E1 or E2
EPHY0_LED_1000	P1-B27*	PU/PD	Activity LED driver	E1 or E2
EPHY0_LED_ACT	P1-B26*	PU/PD	Activity LED driver	E1 or E2

Table 13 GbE 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
EPHY1_TRXN0	P1-B18*	O	Negative part of GbE 1 100ohm diff-pair 0	E2
EPHY1_TRXP0	P1-B19*	I	Positive part of GbE 1 100ohm diff-pair 0	E2
EPHY1_TRXN1	P1-B15*	O	Negative part of GbE 1 100ohm diff-pair 1	E2
EPHY1_TRXP1	P1-B16*	I	Positive part of GbE 1 100ohm diff-pair 1	E2

Signal Name	Pin #	Type	Description	Availability
EPHY1_TRXN2	P1-B12*	O	Negative part of GbE 1 100ohm diff-pair 2	E2
EPHY1_TRXP2	P1-B13*	I	Positive part of GbE 1 100ohm diff-pair 2	E2
EPHY1_TRXN3	P1-B10*	O	Negative part of GbE 1 100ohm diff-pair 3	E2
EPHY1_TRXP3	P1-B9*	I	Positive part of 100ohm diff-pair 3	E2
EPHY1_LED_10_100	P1-B5*	PU/PD	Activity LED driver	E2
EPHY1_LED_1000	P1-B7*	PU/PD	Activity LED driver	E2
EPHY1_LED_ACT	P1-B6*	PU/PD	Activity LED driver	E2

4.5.2 RGMII

When CL-SOM-iMX8MAX is assembled without the “E1” or “E2” configuration options, the i.MX 8 RGMII and MDIO signals are routed to the carrier board interface.

The tables below summarize the RGMII interface signals

Table 14 MDIO Signals

Signal Name	Pin #	Type	Description	Availability
ETH0_MDC	P1-B3*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	NOT E2
ETH0_MDIO	P1-B2*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	NOT E2
ETH0_REFCLK	P1-B24*	O	Clock (25MHz, 50MHz, 62.5MHz or 125MHz)	Always available
ETH1_MDC	P1-A17*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Always available
ETH1_MDIO	P1-A18*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Always available
ETH1_REFCLK	P1-B4*	O	Clock (25MHz, 50MHz, 62.5MHz or 125MHz)	Always available

Table 15 RGMII 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET0_RGMII_RXD0	P1-B30*	I	Ethernet input data from the PHY	Not E1 and not E2
ENET0_RGMII_RXD1	P1-B29*	I	Ethernet input data from the PHY	Not E1 and not E2
ENET0_RGMII_RXD2	P1-B26*	I	Ethernet input data from the PHY	Not E1 and not E2
ENET0_RGMII_RXD3	P1-B32*	I	Ethernet input data from the PHY	Not E1 and not E2
ENET0_RGMII_RX_CTL	P1-B39*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode).	Not E1 and not E2
ENET0_RGMII_RXC	P1-B27*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Not E1 and not E2
ENET0_RGMII_TD0	P1-B36*	O	Serial output Ethernet data to PHY	Not E1 and not E2
ENET0_RGMII_TD1	P1-B37*	O	Serial output Ethernet data to PHY	Not E1 and not E2
ENET0_RGMII_TD2	P1-B33*	O	Serial output Ethernet data to PHY	Not E1 and not E2
ENET0_RGMII_TD3	P1-B34*	O	Serial output Ethernet data to PHY	Not E1 and not E2
ENET0.RGMII_TXC	P1-B25*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Not E1 and not E2
ENET0.RGMII_TX_CTL	P1-B40*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Not E1 and not E2
VCC_ENET0	P1-B23	P	RGMII interface power supply input. This pin must be connected to 1.8V, 2.5V or 3.3V power rail for external PHY usage depending on the PHY requirements or for using the ENET interface as GPIO	Not E1 and not E2

Table 16 RGMII 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET1_RGMII_RXD0	P1-B9*	I	Ethernet input data from the PHY	Not E2
ENET1_RGMII_RXD1	P1-B10*	I	Ethernet input data from the PHY	Not E2

Signal Name	Pin #	Type	Description	Availability
ENET1_RGMII_RXD2	P1-B6*	I	Ethernet input data from the PHY	Not E2
ENET1_RGMII_RXD3	P1-B5*	I	Ethernet input data from the PHY	Not E2
ENET1_RGMII_RX_CTL	P1-B12*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode).	Not E2
ENET1_RGMII_RXC	P1-B7*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Not E2
ENET1_RGMII_TD0	P1-B15*	O	Serial output Ethernet data to PHY	Not E2
ENET1_RGMII_TD1	P1-B16*	O	Serial output Ethernet data to PHY	Not E2
ENET1_RGMII_TD2	P1-B18*	O	Serial output Ethernet data to PHY	Not E2
ENET1_RGMII_TD3	P1-B19*	O	Serial output Ethernet data to PHY	Not E2
ENET1.RGMII_TXC	P1-B25*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Not E2
ENET1.RGMII_TX_CTL	P1-B13*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Not E2
VCC_ENET1	P1-B22	P	RGMII interface power supply input. This pin must be connected to 1.8V, 2.5V or 3.3V power rail for external PHY usage depending on the PHY requirements or for using the ENET interface as GPIO	Not E2

NOTE1: 1.8V, 2.5V or 3.3V power must be supplied via the EPHY_RGMII_VDDH pins if any of the RGMII signals are used on the carrier-board

NOTE2: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 Wireless Interface

CL-SOM-iMX8MAX optional 802.11ac WLAN and Bluetooth 4.2 functions (configuration “WB”) are implemented with Intel Dual Band Wireless-AC 8265 chipset (M.2 1216 module). The WLAN sub-system is interfaced with the i.MX 8 SoC through a multiplexed PCIe interface. On-board multiplexing allows to route the PCIe0 interface either to the WLAN module or to the carrier board interface. Multiplexing is controlled by signal PCIe0_MUX_SEL (carrier board connector P1 pin B81).

Table 17 WiFi and PCIe multiplexing logic

PCIe0_MUX_SEL	PCIe routing	Operation mode
High	WLAN	Utilize on-board WLAN module
Low	Carrier board interface	Utilize PCIe0 interface for an external device

The Bluetooth sub-system is interfaced with the i.MX 8 SoC through a multiplexed USB interface. On-board multiplexing allows to route the USB_OTG1 interface either to the BT module (only in “WB” configuration) or to the carrier board interface. Multiplexing is controlled by signal USB_OTG1_MUX_SEL (SOC GPIO2.IO13).

Table 18 Bluetooth and USB multiplexing logic

USB_OTG1_MUX_SEL	USB routing	Operation mode
High	BT	Utilize on-board BT module
Low	Carrier board interface	Utilize USB_OTG1 interface for an external device

CL-SOM-iMX8MAX is equipped with two MHF4 high-frequency connectors allowing easy integration with external antennas:

- Primary (MAIN) WLAN/BT antenna connector ANT2. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality.
- Secondary (AUX) WLAN antenna connector ANT1. Can be used with any type of 2.4GHz/5.0GHz antenna for dual-band WLAN functionality.

Table 19 ANT1 & ANT2 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	W.FL2-R-MT(60)	Hirose W.FL2-LP-062HF

4.6.1 Wireless certification

Intel 8265 M.2 1216 module is certified for usage in most world regions. For Intel 8265 certification documentation:

- Follow <https://www.intel.com/content/www/us/en/support/articles/000007443/network-and-i-o/wireless-networking.html>
- Expand the “Current Adapter” section
- Expand the “Intel® Dual Band Wireless-AC 8265” sub-section
- Download 8265D2W documents

NOTE1: CL-SOM-iMX8MAX WiFi 802.11ac and Bluetooth functions are available only with the 'WB' ordering option.

NOTE2: CL-SOM-iMX8MAX WiFi and PCIe0 are mutually exclusive.

NOTE3: CL-SOM-iMX8MAX BT and USB_OTG1 are mutually exclusive.

4.7 PCI-Express

The i.MX 8 SoC is equipped with three single lane PCI Express ports (PCIe) Gen. 3.0. PCIe0 is mutually exclusive with wifi, PCIe1 is always available and PCIe_SATA is mutually exclusive with SATA interface. Both SATA and PCIe_SATA are routed directly to the carrier board interface. All PCIe ports requires an external PCIe clock to be supplied in order to utilize the interface. The CL-SOM-iMX8MAX is equipped with an on board PCIe clock generator.

PCIe0 is routed to the carrier board interface via on-board multiplexer. On CL-SOM-iMX8MAX assembled with on-board WiFi/Bluetooth module ("WB" option) PCIe0 interface can be routed either to the WLAN module or to the carrier board interface. Multiplexing is controlled by signal PCIE0_MUX_SEL (carrier board connector P1 pin B81). On CL-SOM-iMX8MAX assembled without on-board WiFi/Bluetooth, PCIe0 interface is always available on the carrier board interface.

The PCI Express port supports the following main features:

- Compliant with PCI Express base specification Gen3
- PCIe 1.0 and 2.0 compliant
- Dual mode operation to function as root complex or endpoint
- Automatic Integration with Most PHY types
- Supports Separate Refclk with Independent Spread Spectrum Clocking

The tables below summarize the PCIe interface signals

Table 20 PCIe 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE0_TX0_P	P1-B69	O	PCI Express transmit data positive	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_TX0_N	P1-B68	O	PCI Express transmit data negative	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_RX0_P	P1-B66	I	PCI Express receive data positive	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_RX0_N	P1-B65	I	PCI Express receive data negative	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_PERST#	P1-B71*	O	PCI Express reset signal	Always available
PCIE0_REFCLK0_P	P1-B76	I	100 MHz positive-side reference clock differential input for PCIe	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_REFCLK0_N	P1-B75	I	100 MHz negative-side reference clock differential input for PCIe	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_WAKE#	P1-B73*	I	PCI Express wake signal	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_CLKREQ#	P1-B72*	I	PCIe clock request signal	NOT WB or WB@ PCIE0_MUX_SEL = '0'
PCIE0_MUX_SEL	P1-B81	I	PCIe multiplexing select signal	Always available

Table 21 PCIe 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE1_TX0_P	P1-B79	O	PCI Express transmit data positive	Always available
PCIE1_TX0_N	P1-B78	O	PCI Express transmit data negative	Always available
PCIE1_RX0_P	P1-B86	I	PCI Express receive data positive	Always available
PCIE1_RX0_N	P1-B85	I	PCI Express receive data negative	Always available
PCIE1_PERST#	P1-B83*	O	PCI Express reset signal	Always available
PCIE1_CLKGEN1_P	P1-B89	I	100 MHz positive-side reference clock differential input for PCIe	Always available

Signal Name	Pin #	Type	Description	Availability
PCIE1_CLKGEN1_N	P1-B88	I	100 MHz negative-side reference clock differential input for PCIe	Always available
PCIE1_WAKE#	P1-B82*	I	PCI Express wake signal	Always available
PCIE1_CLKREQ#	P1-B91*	I	PCIe clock request signal	Always available

Table 22 PCIe_SATA Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_SATA_TX0_P	P1-B102	O	PCI Express transmit data positive	Always available
PCIE_SATA_TX0_N	P1-B101	O	PCI Express transmit data negative	Always available
PCIE_SATA_RX0_P	P1-B99	I	PCI Express receive data positive	Always available
PCIE_SATA_RX0_N	P1-B98	I	PCI Express receive data negative	Always available
PCIE_SATA_CLKGEN0_P	P1-B96	I	100 MHz positive-side reference clock differential input for PCIe	Always available
PCIE_SATA_CLKGEN0_N	P1-B95	I	100 MHz negative-side reference clock differential input for PCIe	Always available
PCIE_SATA_CLKREQ#	P1-B93	I	PCIe clock request signal	Always available

NOTE1: CL-SOM-iMX8MAX PCIe0 and WiFi are mutually exclusive.

NOTE2: CL-SOM-iMX8MAX PCIe_SATA and SATA are mutually exclusive.

NOTE3: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 SATA

The i.MX 8 SoC is equipped with SATA 3.0. The SATA interface can be used as PCIe one-lane. It is routed directly to the carrier board interface.

The SATA port supports the following main features:

- Supports a line rate of 1.5 - 6.0 Gbps
- Supports the SATA specification 3.0
- Supports AHCI specification 1.3

The table below summarize the SATA interface signals:

Signal Name	Pin #	Type	Description	Availability
PCIE_SATA_TX0_P	P1-B102	O	SATA transmit data positive	Always available
PCIE_SATA_TX0_N	P1-B101	O	SATA transmit data negative	Always available
PCIE_SATA_RX0_P	P1-B99	I	SATA receive data positive	Always available
PCIE_SATA_RX0_N	P1-B98	I	SATA receive data negative	Always available

NOTE1: CL-SOM-iMX8MAX SATA and PCIe_SATA are mutually exclusive.

4.9 Sony/Philips Digital Interface (SPDIF)

CL-SOM-iMX8MAX provides one SPDIF transmitter with one output and one SPDIF receiver with one input.

The table below summarizes the SPDIF interface signals:

Table 23 SPDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	P1-A93*	I	External clock signal	Always available
SPDIF_RX	P1-A92*	I	SPDIF input data line signal	Always available
SPDIF_TX	P1-A91*	O	SPDIF output data line signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.10 Digital Audio (SAI)

CL-SOM-iMX8MAX enables access to 3 of the i.MX 8 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Maximum Frame Size of 32 words
- Word size of between 8-bits and 32-bits
- Asynchronous 64 × 32-bit FIFO for each transmit and receive data line

The tables below summarize the SAI interface signals

Table 24 SAI0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI0_TXC	P1-A86*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P1-A95*			
SAI0_TXD	P1-A89*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
	P1-A98*			
SAI0_RXD	P1-A87*	I	Receive data, sampled synchronously by the bit clock	Always available
	P1-A97*			
SAI0_RXFS	P1-A96*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI0_RXC	P1-A99*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI0_TXFS	P1-A88*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P1-A65*			

Table 25 SAI1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1_TXC	P1-A86*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI1_TXD	P1-A85*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Always available
SAI1_RXD	P1-A88*	I	Receive data, sampled synchronously by the bit clock	Always available
SAI1_RXFS	P1-A87*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P1-A84*			
SAI1_RXC	P1-A89*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
	P1-A85*			
SAI1_TXFS	P1-A84*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available

Table 26 SAI 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2_RXD	P1-A102*	I	Receive data, sampled synchronously by the bit clock	Always available

Signal Name	Pin #	Type	Description	Availability
SAI2_RXFS	P1-A101*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available
SAI2_RXC	P1-A103*	O	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 Enhanced Serial Audio Interface (ESAI)

CL-SOM-iMX8MAX enables access to 1 of the i.MX 8 integrated enhanced serial audio interface (ESAI) modules. The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers, and other DSPs. The following main features are supported:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode One
- 128-word Transmit FIFO shared by six transmitters
- 128-word Receive FIFO shared by four receivers

The tables below summarize the ESAI interface signals

Table 27 ESAI0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ESAI0_FSR	P1-A81*	IO	The receive framesync clock is utilized to clock in each audio sample received by the DSP	Always available
ESAI0_FST	P1-A79*	IO	The transmit framesync clock is utilized to clock out each audio sample transmitted by the DSP	Always available
ESAI0_SCKR	P1-A78*	IO	The receive bit clock is utilized to clock in each bit of audio data received by the DSP	Always available
ESAI0_SCKT	P1-A77*	IO	The transmit bit clock is utilized to clock out each bit of audio data transmitted by the DSP	Always available
ESAI0_TX0	P1-A76*	O	The ESAI0_TX0 data pin operates only as a transmitter pin in conjunction with the transmitter clocks	Always available
ESAI0_TX1	P1-A75*	O	The ESAI0_TX1 data pin operates only as a transmitter pin in conjunction with the transmitter clocks	Always available
ESAI0_TX2_RX3	P1-A74*	IO	The ESAI0_TX2_RX3 data pin can be programmed as either a transmitter (TX2) or as a receiver (RX3). When operating as a transmitter this pin operates in conjunction with the transmit clocks. When operating as a receiver this pin operates in conjunction with the receiver clocks	Always available
ESAI0_TX3_RX2	P1-A73*	IO	The ESAI0_TX3_RX2 data pin can be programmed as either a transmitter (TX3) or as a receiver (RX2). When operating as a transmitter this pin operates in conjunction with the transmit clocks. When operating as a receiver this pin operates in conjunction with the receiver clocks	Always available

Signal Name	Pin #	Type	Description	Availability
ESAI0_TX4_RX1	P1-A72*	IO	The ESAI0_TX4_RX1 data pin can be programmed as either a transmitter (TX4) or as a receiver (RX1). When operating as a transmitter this pin operates in conjunction with the transmit clocks. When operating as a receiver this pin operates in conjunction with the receiver clocks	Always available
ESAI0_TX5_RX0	P1-A71*	IO	The ESAI0_TX5_RX0 data pin can be programmed as either a transmitter (TX5) or as a receiver (RX0). When operating as a transmitter this pin operates in conjunction with the transmit clocks. When operating as a receiver this pin operates in conjunction with the receiver clocks	Always available
MCLK_IN0	P1-A83*	IO	The receive over sample clock is convenient for generating the bit clock (SCKR) and framesync clock (FSR)	Always available
MCLK_OUT0	P1-A82*	IO	The transmit over sample clock is convenient for generating the bit clock (SCKT) and framesync clock (FST)	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 USB

CL-SOM-iMX8MAX is equipped with a single USB 3.0 port and two USB 2.0 dual-role ports, one of them is mutually exclusive with BT and one USB 2.0 as HSIC.

USB_SS3, USB_OTG2 and USB_HSIC are always available and USB_OTG1 is mutually exclusive with BT.

USB_OTG1 is routed to the carrier board interface via on-board multiplexer. On CL-SOM-iMX8MAX assembled with on-board WiFi/Bluetooth module ("WB" option) USB_OTG1 interface can be routed either to the BT module or to the carrier board interface. Multiplexing is controlled by signal USB_OTG1_MUX_SEL (SOC GPIO2.IO13). On CL-SOM-iMX8MAX assembled without on-board WiFi/Bluetooth, USB_OTG1 interface is always available on the carrier board interface.

USB ports support the following main features:

- SuperSpeed, Hi Speed and Full Speed support
- USB3 U1/U2/U3 support
- USB2 L1/L2 support

The tables below summarize the USB interface signals

Table 28 USB_SS3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_SS3_RX_N	P1-B56	I	USB3.0 receive negative lane	Always available
USB_SS3_RX_P	P1-B55	I	USB3.0 receive positive lane	Always available
USB_SS3_TX_N	P1-B59	O	USB3.0 transmit negative lane	Always available
USB_SS3_TX_P	P1-B58	O	USB3.0 transmit positive lane	Always available
USB_SS3_TC0	P1-B46*	IO	USB3.0 control 0	Always available
USB_SS3_TC1	P1-B49*	IO	USB3.0 control 1	Always available
USB_SS3_TC2	P1-B47*	IO	USB3.0 control 2	Always available
USB_SS3_TC3	P1-B50*	IO	USB3.0 control 3	Always available

Table 29 USB_UTG1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_OTG1_DN	P1-B43	IO	USB2.0 negative data	NOT WB or WB@ USB_OTG1_MUX_SEL = '0'
USB_OTG1_DP	P1-B42	IO	USB2.0 positive data	NOT WB or WB@

Signal Name	Pin #	Type	Description	Availability
				USB_OTG1_MUX_SEL = '0'
USB_OTG1_VBUS	P1-A3	AI	USB2.0 VBUS detect	Always available
USB_OTG1_ID	P1-B45	I	USB2.0 ID signal	Always available

Table 30 USB_UTG2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_OTG2_DN	P1-B53	IO	USB2.0 negative data	Always available
USB_OTG2_DP	P1-B52	IO	USB2.0 positive data	Always available
USB_OTG2_VBUS	P1-A4	AI	USB2.0 VBUS detect	Always available
USB_OTG2_ID	P1-B48	I	USB2.0 ID signal	Always available

Table 31 USB_HSIC Interface Signals

Signal Name	Pin #	Type	Description	Availability
USB_HSIC0_STROBE	P1-B62*	IO	HSIC strobe pin of the USB Interface	Always available
USB_HSIC0_DATA	P1-B63*	IO	HSIC data pin of the USB Interface	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 MMC / SD /SDIO

Two MMC/SD/SDIO ports are available through the CL-SOM-iMX8MAX carrier board interface. The ports derived from the i.MX 8 on-chip Ultra Secured Digital Host Controller (uSDHC). uSDHC module supports the following main features:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/5.0/5.1
- Compatible with the SD Memory Card Specification version 3.0 and supports the extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0/3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes
- Dedicated card detection, write protection and reset signals

The tables below summarize the MMC/SD/SDIO interface signals

Table 32 USDHC1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC1_CLK	P1-A63	O	Clock for MMC/SD/SDIO card	Always available
USDHC1_CMD	P1-A62*	IO	CMD line connect to card	Always available
USDHC1_DATA0	P1-A59*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
USDHC1_DATA1	P1-A58*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	Always available
USDHC1_DATA2	P1-A57*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
USDHC1_DATA3	P1-A56*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
USDHC1_DATA4	P1-A55*	IO	DATA4 line in 8-bit mode	Always available
USDHC1_DATA5	P1-A54*	IO	DATA5 line in 8-bit mode	Always available
USDHC1_DATA6	P1-A53*	*IO	DATA6 line in 8-bit mode or card write protect detection	Always available
USDHC1_DATA7	P1-A52*	IO	DATA7 line in 8-bit mode or card detection pin	Always available

Signal Name	Pin #	Type	Description	Availability
USDHC1_STROBE	P1-A61*	O	STROBE for MMC/SD/SDIO card	Always available
USDHC1_RESET_B	P1-A64*	O	Card hardware reset signal, active LOW	Always available

Table 33 USDHC2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
USDHC2_CLK	P1-A43*	O	Clock for MMC/SD/SDIO card	Always available
USDHC2_CMD	P1-A42*	IO	CMD line connect to card	Always available
USDHC2_DATA0	P1-A39*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
USDHC2_DATA1	P1-A38*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	Always available
USDHC2_DATA2	P1-A37*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
USDHC2_DATA3	P1-A36*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
USDHC2_RESET_B	P1-A40*	O	Card hardware reset signal, active LOW	Always available
USDHC2_WP	P1-A45*	I	Card write protect detection	Always available
USDHC2_CD_B	P1-A44*	I	Card detection pin	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 UART

CL-SOM-iMX8MAX enables access to up to 7 of the i.MX 8 universal asynchronous receiver/transmitter (UART) interfaces. The UART module supports the following features:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Programmable 7-bit, 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals

The tables below summarize the UART interface signals

Table 34 UART 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART0_CTS_B	P1-A30*	O	UART-0 clear to send	Always available
UART0_RTS_B	P1-A29*	I	UART-0 request to send	Always available
UART0_RX	P1-A27*	I	UART-0 serial data receive	Always available
UART0_TX	P1-A28*	O	UART-0 serial data transmit	Always available

Table 35 UART 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	P1-A32*	O	UART-1 clear to send	Always available
	P1-A33*			
UART1_RTS_B	P1-A33*	I	UART-1 request to send	Always available
	P1-A32*			
UART1_RX	P1-A34*	I	UART-1 serial data receive	Always available
UART1_TX	P1-A35*	O	UART-1 serial data transmit	Always available

Table 36 UART 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2_RX	P1-A29*	I	UART-2 serial data receive	Always available
	P2-A27*			
UART2_TX	P1-A30*	O	UART-2 serial data transmit	Always available

Signal Name	Pin #	Type	Description	Availability
	P2-A26*			

Table 37 UART 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3_CTS_B	P1-B7*	O	UART-3 clear to send	Always available
UART3_RTS_B	P1-B19*	I	UART-3 request to send	Always available
UART3_RX	P1-A19*	I	UART-3 serial data receive	Always available
	P1-B5*			
	P2-B40*			
UART3_TX	P1-A20*	O	UART-3 serial data transmit	Always available
	P1-B18*			
	P2-B42*			

Table 38 UART 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4_CTS_B	P1-A37*	O	UART-4 clear to send	Always available
UART4_RTS_B	P1-A36*	I	UART-4 request to send	Always available
UART4_RX	P2-A96*	I	UART-4 serial data receive	Always available
	P1-A39*			
UART4_TX	P2-A104*	O	UART-4 serial data transmit	Always available
	P1-A38*			

Table 39 M40 UART 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
M40_UART0_RX	P1-A25*	I	UART tightly coupled with M4F 0 core- serial data receive	Always available
M40_UART0_TX	P1-A24*	O	UART tightly coupled with M4F 0 core- serial data transmit	Always available

Table 40 M41 UART 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
M41_UART0_RX	P1-A23*	I	UART tightly coupled with M4F 1 core- serial data receive	Always available
M41_UART0_TX	P1-A22*	O	UART tightly coupled with M4F 1 core- serial data receive	Always available

Table 41 SCU UART 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SCU_UART0_RX	P1-A5*	I	UART tightly coupled with SCU-serial data receive	Always available
SCU_UART0_TX	P1-A6*	O	UART tightly coupled with SCU-serial data receive	Always available

NOTE1: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE2: By default, UART0 is assigned to be used as the main debug console port

4.15 CAN Bus

CL-SOM-iMX8MAX provides up to three CAN bus interfaces implemented with the i.MX 8 integrated FlexCAN module. The following features are supported by the FlexCAN module:

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B
- Flexible mailboxes of zero to eight bytes data length
- Compliant with the ISO 11898-1 standard

The tables below summarize the CAN Bus interface signals

Table 42 CAN 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN0_TX	P1-B104*	O	FLEXCAN transmit pin	Always available
CAN0_RX	P1-B105*	I	FLEXCAN receive pin	Always available

Table 43 CAN 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN1_TX	P1-B106*	O	FLEXCAN transmit pin	Always available
CAN1_RX	P1-B107*	I	FLEXCAN receive pin	Always available

Table 44 CAN 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN2_TX	P1-B108*	O	FLEXCAN transmit pin	Always available
CAN2_RX	P1-B109*	I	FLEXCAN receive pin	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 I2C

CL-SOM-iMX8MAX features up to 14 I2C bus interfaces. The following general features are supported by the I2C bus interfaces:

- Standard, Fast, Fast+ and Ultra Fast modes
- High speed mode (HS) in slave mode
- High speed mode (HS) in master mode, if SCL pin implements current source pull-up (device specific)
- Multi-master support, including synchronization and arbitration

The tables below summarize the I2C interface signals

Table 45 I2C 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C0_SCL	P2-A69*	O	I2C serial clock line	Always available
I2C0_SDA	P2-A71*	IO	I2C serial data line	Always available

Table 46 I2C 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_3V3_SCL	P1-A15*	O	I2C serial clock line	Always available
	P1-B62*			
I2C1_3V3_SDA	P1-A16*	IO	I2C serial data line	Always available
	P1-B63*			

Table 47 I2C 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_3V3_SCL	P1-A13*	O	I2C serial clock line	Always available
I2C2_3V3_SDA	P1-A14*	IO	I2C serial data line	Always available

Table 48 I2C 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	P1-B3*	O	I2C serial clock line	NOT E2
	P1-A17*			Always available
I2C4_SDA	P1-B2*	IO	I2C serial data line	NOT E2
	P1-A18*			Always available

Table 49 MIPI-CSIO_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSIO_I2C0_SCL	P2-A91*	O	Dedicated I2C clock for MIPI-CSIO	Always available
CSIO_I2C0_SDA	P2-A92*	IO	Dedicated I2C data for MIPI-CSIO	Always available

Table 50 MIPI-CSI1_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI1_I2C0_SCL	P2-A94*	O	Dedicated I2C clock for MIPI-CSI1	Always available
CSI1_I2C0_SDA	P2-A95*	IO	Dedicated I2C data for MIPI-CSI1	Always available

Table 51 MIPI-DSIO_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSIO_I2C0_SCL	P2-A66*	O	Dedicated I2C clock for MIPI-DSIO	Always available
DSIO_I2C0_SDA	P2-A65*	IO	Dedicated I2C data for MIPI-DSIO	Always available

Table 52 MIPI-DSI1_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI1_I2C0_SCL	P2-A61*	O	Dedicated I2C clock for MIPI-DSI1	Always available
DSI1_I2C0_SDA	P2-A62*	IO	Dedicated I2C data for MIPI-DSI1	Always available

Table 53 LVDS0_I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_I2C1_SCL	P2-A26*	O	Dedicated I2C clock for LVDS0 channel 1	Always available
LVDS0_I2C1_SDA	P2-A27*	IO	Dedicated I2C data for LVDS0 channel 1	Always available

Table 54 LVDS1_I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS1_I2C1_SCL	P2-B42*	O	Dedicated I2C clock for LVDS1 channel 1	Always available
LVDS1_I2C1_SDA	P2-B40*	IO	Dedicated I2C data for LVDS1 channel 1	Always available

Table 55 HDMI_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_DDC_SCL	P2-B92	O	Dedicated I2C clock for HDMI	Always available
HDMI_DDC_SDA	P2-B91	IO	Dedicated I2C data for HDMI	Always available

Table 56 HDMI_RX_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_RX_DDC_SCL	P2-B71	O	Dedicated I2C clock for HDMI-RX	Always available
HDMI_RX_DDC_SDA	P2-B72	IO	Dedicated I2C data for HDMI-RX	Always available

Table 57 M40_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
M40_I2C_SCL	P1-A25*	O	Dedicated I2C clock for M4F 0 core	Always available
M40_I2C_SDA	P1-A24*	IO	Dedicated I2C data for M4F 0 core	Always available

Table 58 M41_I2C Interface Signals

Signal Name	Pin #	Type	Description	Availability
M41_I2C_SCL	P1-A23*	O	Dedicated I2C clock for M4F 1 core	Always available
M41_I2C_SDA	P1-A22*	IO	Dedicated I2C data for M4F 1 core	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.17 SPI

Up-to three SPI interfaces are accessible through the CL-SOM-iMX8MAX carrier board interface. The SPI interfaces are derived from iMX8M integrated full-duplex enhanced Synchronous Serial Interface. Each is configurable to support Master/Slave modes. The following features are supported:

- Master operation supporting up to 4 peripheral chip select
- Slave operation
- Command/transmit FIFO of 64 words
- Receive FIFO of 64 words
- Support for full and half duplex transfers supporting 1-bit transmit and receive on each clock edge
- Support for half duplex transfers supporting 2-bit or 4-bit transmit or receive on each clock edge (master only)

The tables below summarize the SPI interface signals

Table 59 SPI 0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI0_SCK	P1-A99*	O	SPI0 clock	Always available
SPI0_MOSI	P1-A98*	O	SPI0 data out	Always available
SPI0_MISO	P1-A97*	I	SPI0 data in	Always available
SPI0_CSO	P1-A96*	O	SPI0 chip select 0	Always available
SPI0_CS1	P1-A95*	O	SPI0 chip select 1	Always available

Table 60 SPI 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI2_SCK	P1-A69*	O	SPI2 clock	Always available
SPI2_MOSI	P1-A68*	O	SPI2 data out	Always available
SPI2_MISO	P1-A67*	I	SPI2 data in	Always available
SPI2_CSO	P1-A66*	O	SPI2 chip select 0	Always available
SPI2_CS1	P1-A65*	O	SPI2 chip select 1	Always available

Table 61 SPI 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI3_SCK	P1-A109*	O	SPI3 clock	Always available
	P1-A35*			
SPI3_MOSI	P1-A108*	O	SPI3 data out	Always available
	P1-A34*			
SPI3_MISO	P1-A107*	I	SPI3 data in	Always available
	P1-A33*			
SPI3_CSO	P1-A106*	O	SPI3 chip select 0	Always available
	P1-A32*			
SPI3_CS1	P1-A105*	O	SPI3 chip select 1	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.18 PWM

CL-SOM-iMX8MAX features up to four independent PWM channels. Additional dedicated PWM interfaces are available as part of LVDS and MIPI-DSI interfaces

The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead

- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

The table below summarize the PWM interface signals:

Table 62 PWM Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM0	P1-A29*	O	PWM functional output	Always available
PWM1	P1-A30*	O	PWM functional output	Always available
PWM2	P1-A12*	O	PWM functional output	Always available
PWM3	P1-A104*	O	PWM functional output	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.19 ADC

CL-SOM-iMX8MAX enables access to one 4-channel Analog-to-digital Converter. The following main features are supported:

- Linear successive approximation algorithm
- Channel support for up to 64 analog input channels for conversion of external pins and from internal sources
- Channel scaling allows input voltage levels higher than the ADC reference voltage
- Configurable analog input sample time
- Trigger detect with up to 8 trigger sources with priority level configuration. Software or hardware trigger option for each
- Automatic compare for less-than, greater-than, within range, or out-of-range with "store on true" and "repeat until true" options
- 16-entry conversion result data FIFO with configurable watermark and overflow detection
- Interrupt, DMA or polled operation

The table below summarize the ADC interface signals:

Table 63 ADC Interface Signals

Signal Name	Pin #	Type	Description	Availability
ADC_IN0	P1-A50*	AI	ADC interface input	Always available
ADC_IN1	P1-A49*	AI	ADC interface input	Always available
ADC_IN2	P1-A48*	AI	ADC interface input	Always available
ADC_IN3	P1-A47*	AI	ADC interface input	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.20 JTAG

CL-SOM-iMX8MAX enables access to the i.MX 8 JTAG port through the carrier board interface.

The table below summarizes the JTAG interface signals:

Table 64 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_TCK	P1-A9	I	Test Clock	Always available
JTAG_TDI	P1-A7	I	Test Data In	Always available
JTAG_TDO	P1-A8	O	Test Data Out	Always available
JTAG_TMS	P1-A10	I	Test Mode Select	Always available

4.21 GPIO

Up-to 161 of the iMX8M general purpose input/output (GPIO) signals are available through the carrier board interface.

The table below summarizes the GPIO interface signals:

Table 65 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Voltage domain	Availability
GPIO0.IO06	P1-A25*	IO	GPIO	3.3V	Always available
GPIO0.IO07	P1-A24*	IO	GPIO	3.3V	Always available
GPIO0.IO10	P1-A23*	IO	GPIO	3.3V	Always available
GPIO0.IO11	P1-A22*	IO	GPIO	3.3V	Always available
GPIO0.IO12	P1-A19*	IO	GPIO	3.3V	Always available
GPIO0.IO13	P1-A20*	IO	GPIO	3.3V	Always available
GPIO0.IO14	P1-A15*	IO	GPIO	3.3V	Always available
GPIO0.IO15	P1-A16*	IO	GPIO	3.3V	Always available
GPIO0.IO16	P1-A104*	IO	GPIO	3.3V	Always available
GPIO0.IO17	P1-A13*	IO	GPIO	3.3V	Always available
GPIO0.IO18	P1-A14*	IO	GPIO	3.3V	Always available
GPIO0.IO19	P1-A12*	IO	GPIO	3.3V	Always available
GPIO0.IO20	P1-A27*	IO	GPIO	3.3V	Always available
GPIO0.IO21	P1-A28*	IO	GPIO	3.3V	Always available
GPIO0.IO22	P1-A29*	IO	GPIO	3.3V	Always available
GPIO0.IO23	P1-A30*	IO	GPIO	3.3V	Always available
GPIO0.IO24	P1-A35*	IO	GPIO	3.3V	Always available
GPIO0.IO25	P1-A34*	IO	GPIO	3.3V	Always available
GPIO0.IO26	P1-A33*	IO	GPIO	3.3V	Always available
GPIO0.IO27	P1-A32*	IO	GPIO	3.3V	Always available
GPIO0.IO28	P1-A5*	IO	GPIO	1.8V	Always available
GPIO0.IO29	P1-A6*	IO	GPIO	1.8V	Always available
GPIO1.IO04	P2-A25*	IO	GPIO	3.3V	Always available
GPIO1.IO05	P2-A24*	IO	GPIO	3.3V	Always available
GPIO1.IO06	P2-A44*	IO	GPIO	3.3V	Always available
GPIO1.IO08	P2-A26*	IO	GPIO	3.3V	Always available
GPIO1.IO09	P2-A27*	IO	GPIO	3.3V	Always available
GPIO1.IO10	P2-B61*	IO	GPIO	3.3V	Always available
GPIO1.IO11	P2-B20*	IO	GPIO	3.3V	Always available
GPIO1.IO12	P2-B22*	IO	GPIO	3.3V	Always available
GPIO1.IO14	P2-B42*	IO	GPIO	3.3V	Always available
GPIO1.IO15	P2-B40*	IO	GPIO	3.3V	Always available
GPIO1.IO16	P2-A66*	IO	GPIO	3.3V	Always available
GPIO1.IO17	P2-A65*	IO	GPIO	3.3V	Always available
GPIO1.IO18	P2-A67*	IO	GPIO	3.3V	Always available
GPIO1.IO19	P2-A68*	IO	GPIO	3.3V	Always available
GPIO1.IO20	P2-A61*	IO	GPIO	3.3V	Always available
GPIO1.IO21	P2-A62*	IO	GPIO	3.3V	Always available
GPIO1.IO22	P2-A64*	IO	GPIO	3.3V	Always available
GPIO1.IO23	P2-A63*	IO	GPIO	3.3V	Always available
GPIO1.IO24	P2-A87*	IO	GPIO	1.8V	Always available
GPIO1.IO25	P2-A91*	IO	GPIO	1.8V	Always available
GPIO1.IO26	P2-A92*	IO	GPIO	1.8V	Always available
GPIO1.IO27	P2-A69*	IO	GPIO	1.8V	Always available
GPIO1.IO28	P2-A71*	IO	GPIO	1.8V	Always available
GPIO1.IO29	P2-A93*	IO	GPIO	1.8V	Always available
GPIO1.IO30	P2-A96*	IO	GPIO	1.8V	Always available
GPIO1.IO31	P2-A104*	IO	GPIO	1.8V	Always available
GPIO2.IO00	P2-A94*	IO	GPIO	1.8V	Always available
GPIO2.IO01	P2-A95*	IO	GPIO	1.8V	Always available
GPIO2.IO07	P1-A103*	IO	GPIO	3.3V	Always available
GPIO2.IO08	P1-A102*	IO	GPIO	3.3V	Always available

Signal Name	Pin #	Type	Description	Voltage domain	Availability
GPIO2.IO09	P1-A101*	IO	GPIO	3.3V	Always available
GPIO2.IO14	P1-A92*	IO	GPIO	3.3V	Always available
GPIO2.IO15	P1-A91*	IO	GPIO	3.3V	Always available
GPIO2.IO16	P1-A93*	IO	GPIO	3.3V	Always available
GPIO2.IO17	P1-A109*	IO	GPIO	3.3V	Always available
GPIO2.IO18	P1-A108*	IO	GPIO	3.3V	Always available
GPIO2.IO19	P1-A107*	IO	GPIO	3.3V	Always available
GPIO2.IO20	P1-A106*	IO	GPIO	3.3V	Always available
GPIO2.IO21	P1-A105*	IO	GPIO	3.3V	Always available
GPIO2.IO22	P1-A81*	IO	GPIO	3.3V	Always available
GPIO2.IO23	P1-A79*	IO	GPIO	3.3V	Always available
GPIO2.IO24	P1-A78*	IO	GPIO	3.3V	Always available
GPIO2.IO25	P1-A77*	IO	GPIO	3.3V	Always available
GPIO2.IO26	P1-A76*	IO	GPIO	3.3V	Always available
GPIO2.IO27	P1-A75*	IO	GPIO	3.3V	Always available
GPIO2.IO28	P1-A74*	IO	GPIO	3.3V	Always available
GPIO2.IO29	P1-A73*	IO	GPIO	3.3V	Always available
GPIO2.IO30	P1-A72*	IO	GPIO	3.3V	Always available
GPIO2.IO31	P1-A71*	IO	GPIO	3.3V	Always available
GPIO3.IO00	P1-A83*	IO	GPIO	3.3V	Always available
GPIO3.IO01	P1-A82*	IO	GPIO	3.3V	Always available
GPIO3.IO02	P1-A99*	IO	GPIO	3.3V	Always available
GPIO3.IO03	P1-A98*	IO	GPIO	3.3V	Always available
GPIO3.IO04	P1-A97*	IO	GPIO	3.3V	Always available
GPIO3.IO05	P1-A96*	IO	GPIO	3.3V	Always available
GPIO3.IO06	P1-A95*	IO	GPIO	3.3V	Always available
GPIO3.IO07	P1-A69*	IO	GPIO	3.3V	Always available
GPIO3.IO08	P1-A68*	IO	GPIO	3.3V	Always available
GPIO3.IO09	P1-A67*	IO	GPIO	3.3V	Always available
GPIO3.IO10	P1-A66*	IO	GPIO	3.3V	Always available
GPIO3.IO11	P1-A65*	IO	GPIO	3.3V	Always available
GPIO3.IO12	P1-A89*	IO	GPIO	3.3V	Always available
GPIO3.IO13	P1-A88*	IO	GPIO	3.3V	Always available
GPIO3.IO14	P1-A87*	IO	GPIO	3.3V	Always available
GPIO3.IO15	P1-A86*	IO	GPIO	3.3V	Always available
GPIO3.IO16	P1-A85*	IO	GPIO	3.3V	Always available
GPIO3.IO17	P1-A84*	IO	GPIO	3.3V	Always available
GPIO3.IO18	P1-A50*	IO	GPIO	1.8V	Always available
GPIO3.IO19	P1-A49*	IO	GPIO	1.8V	Always available
GPIO3.IO20	P1-A48*	IO	GPIO	1.8V	Always available
GPIO3.IO21	P1-A47*	IO	GPIO	1.8V	Always available
GPIO3.IO29	P1-B105*	IO	GPIO	3.3V	Always available
GPIO3.IO30	P1-B104*	IO	GPIO	3.3V	Always available
GPIO3.IO31	P1-B107*	IO	GPIO	3.3V	Always available
GPIO4.IO00	P1-B106*	IO	GPIO	3.3V	Always available
GPIO4.IO01	P1-B109*	IO	GPIO	3.3V	Always available
GPIO4.IO02	P1-B108*	IO	GPIO	3.3V	Always available
GPIO4.IO03	P1-B46*	IO	GPIO	3.3V	Always available
GPIO4.IO04	P1-B49*	IO	GPIO	3.3V	Always available
GPIO4.IO05	P1-B47*	IO	GPIO	3.3V	Always available
GPIO4.IO06	P1-B50*	IO	GPIO	3.3V	Always available
GPIO4.IO07	P1-A64*	IO	GPIO	3.3V	Always available
GPIO4.IO09	P1-A40*	IO	GPIO	3.3V	Always available
GPIO4.IO11	P1-A45*	IO	GPIO	3.3V	Always available
GPIO4.IO12	P1-A44*	IO	GPIO	3.3V	Always available
GPIO4.IO13	P1-B2*	IO	GPIO	3.3V	NOT E2
GPIO4.IO14	P1-B3*	IO	GPIO	3.3V	NOT E2
GPIO4.IO15	P1-B24*	IO	GPIO	3.3V	Always available
GPIO4.IO16	P1-B4*	IO	GPIO	3.3V	Always available
GPIO4.IO17	P1-A18*	IO	GPIO	3.3V	Always available
GPIO4.IO18	P1-A17*	IO	GPIO	3.3V	Always available
GPIO4.IO27	P1-B72*	IO	GPIO	3.3V	NOT WB or WB@PCIe0_MUX_SEL = '0'
GPIO4.IO28	P1-B73*	IO	GPIO	3.3V	NOT WB or WB@PCIe0_MUX_SEL = '0'
GPIO4.IO29	P1-B71*	IO	GPIO	3.3V	Always available
GPIO4.IO30	P1-B91*	IO	GPIO	3.3V	Always available
GPIO4.IO31	P1-B82*	IO	GPIO	3.3V	Always available

Signal Name	Pin #	Type	Description	Voltage domain	Availability
GPIO5.IO00	P1-B83*	IO	GPIO	3.3V	Always available
GPIO5.IO01	P1-B63*	IO	GPIO	3.3V	Always available
GPIO5.IO02	P1-B62*	IO	GPIO	3.3V	Always available
GPIO5.IO14	P1-A62*	IO	GPIO	3.3V	Always available
GPIO5.IO15	P1-A59*	IO	GPIO	3.3V	Always available
GPIO5.IO16	P1-A58*	IO	GPIO	3.3V	Always available
GPIO5.IO17	P1-A57*	IO	GPIO	3.3V	Always available
GPIO5.IO18	P1-A56*	IO	GPIO	3.3V	Always available
GPIO5.IO19	P1-A55*	IO	GPIO	3.3V	Always available
GPIO5.IO20	P1-A54*	IO	GPIO	3.3V	Always available
GPIO5.IO21	P1-A53*	IO	GPIO	3.3V	Always available
GPIO5.IO22	P1-A52*	IO	GPIO	3.3V	Always available
GPIO5.IO23	P1-A61*	IO	GPIO	3.3V	Always available
GPIO5.IO24	P1-A43*	IO	GPIO	3.3V	Always available
GPIO5.IO25	P1-A42*	IO	GPIO	3.3V	Always available
GPIO5.IO26	P1-A39*	IO	GPIO	3.3V	Always available
GPIO5.IO27	P1-A38*	IO	GPIO	3.3V	Always available
GPIO5.IO28	P1-A37*	IO	GPIO	3.3V	Always available
GPIO5.IO29	P1-A36*	IO	GPIO	3.3V	Always available
GPIO5.IO30	P1-B25*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO5.IO31	P1-B40*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO00	P1-B36*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO01	P1-B37*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO02	P1-B33*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO03	P1-B34*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO04	P1-B27*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO05	P1-B39*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO06	P1-B30*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO07	P1-B29*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO08	P1-B26*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO09	P1-B32*	IO	GPIO	3.3V/2.5V/1.8V	Not E1 and not E2
GPIO6.IO10	P1-B25*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO11	P1-B13*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO12	P1-B15*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO13	P1-B16*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO14	P1-B18*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO15	P1-B19*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO16	P1-B7*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO17	P1-B12*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO18	P1-B9*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO19	P1-B10*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO20	P1-B6*	IO	GPIO	3.3V/2.5V/1.8V	Not E2
GPIO6.IO21	P1-B5*	IO	GPIO	3.3V/2.5V/1.8V	Not E2

NOTE1: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE2: 1.8V, 2.5V or 3.3V power must be supplied via the EPHY_RGMII_VDDH pins if any of the RGMII signals are used as GPIOs on the carrier-board

5 SYSTEM LOGIC

5.1 Power Supply

Table 66 Power signals

Signal Name	Pin#	Type	Description
V_SOM	P2-A2, P2-A3, P2-A4, P2-A5, P2-A6, P2-A7, P2-A8, P2-A9, P2-A10, P2-A12, P2-A13, P2-A14, P2-A15, P2-A16, P2-A17, P2-A18	P	Main power supply. Connect to a regulated DC supply
VCC_RTC	P1-B92	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery.
GND	P1-B1, P1-B8, P1-B11, P1-B14, P1-B17, P1-B21, P1-B28, P1-B31, P1-B35, P1-B38, P1-B41, P1-B44, P1-B51, P1-B54, P1-B57, P1-B60, P1-B64, P1-B67, P1-B70, P1-B74, P1-B77, P1-B80, P1-B84, P1-B87, P1-B90, P1-B94, P1-B97, P1-B100, P1-B103, P1-B110, P1-A1, P1-A11, P1-A21, P1-A26, P1-A31, P1-A41, P1-A46, P1-A51, P1-A60, P1-A70, P1-A80, P1-A90, P1-A94, P1-A100, P1-A110, P2-B1, P2-B5, P2-B8, P2-B11, P2-B14, P2-B17, P2-B21, P2-B25, P2-B28, P2-B31, P2-B34, P2-B37, P2-B41, P2-B45, P2-B48, P2-B51, P2-B54, P2-B57, P2-B60, P2-B64, P2-B67, P2-B70, P2-B74, P2-B77, P2-B80, P2-B83, P2-B87, P2-B90, P2-B94, P2-B97, P2-B100, P2-B103, P2-B106, P2-B110, P2-A1, P2-A11, P2-A19, P2-A21, P2-A28, P2-A31, P2-A34, P2-A37, P2-A41, P2-A45, P2-A48, P2-A51, P2-A54, P2-A57, P2-A60, P2-A70, P2-A74, P2-A77, P2-A80, P2-A83, P2-A86, P2-A90, P2-A97, P2-A100, P2-A103, P2-A107, P2-A110	P	Common ground.
VCC_ENET0	P1-B23	P	RGMII interface power supply input. This pin must be connected to 1.8V, 2.5V or 3.3V power rail for external PHY usage depending on the PHY requirements or for using the ENET interface as GPIO
VCC_ENET1	P1-B22	P	RGMII interface power supply input. This pin must be connected to 1.8V, 2.5V or 3.3V power rail for external PHY usage depending on the PHY requirements or for using the ENET interface as GPIO

5.2 System and Miscellaneous Signals

5.2.1 Control and power management

Control and power management signals are available through the carrier board interface.

The table below summarizes the control and power management signals:

Table 67 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
SEQUENCE 2 ON	P2-B109	O	An indication that VCC_3V3 is ON	Always available
PMIC_ON_REQ	P2-B108	O	Active high power-up request output from iMX8M SoC.	Always available
PWRBTN	P2-A20	I	Active low ON/OFF signal (designed for an ON/OFF switch).	Always available

5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX8MAX.

The POR_B_1V8 is controlled by the PMICs.

Table 68 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	P2-A40	I	Active Low cold reset input signal. A valid pulse is low for at least 1us	Always available
POR_B_1V8	P1-B61	O	Open-drain reset output from the PMICs	Always available

5.4 Boot Sequence

CL-SOM-iMX8MAX boot sequence defines which interface/media is used by CL-SOM-iMX8MAX to load and execute the initial software (such as SPL or/and U-boot). CL-SOM-iMX8MAX can load initial software from the following interfaces/media:

- On-board primary boot device (eMMC with pre-flashed boot-loader)
- External SD card using the USDHC1 interface

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 69 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P1-A2	I	Active low alternate boot sequence select input. Leave floating for standard boot sequence	Always available

Table 70 CL-SOM-iMX8MAX Boot sequences

Sequence	ALT_BOOT	Boot device
Standard	Floating	Onboard eMMC (Primary boot storage)
Alternate	Low	SD card on USDHC1 interface

5.5 Signal Multiplexing Characteristics

Up to 161 of the CL-SOM-iMX8MAX carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX8MAX CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 4 functions (ALT MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX8MAX pins are derived from the iMX8M SoC control module

NOTE1: Pin function selection is controlled by software.

NOTE2: Each pin can be used for a single function at a time.

NOTE3: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE4: An empty MUX mode is a “RESERVED” function and must not be used.

Table 71 Multifunctional Signals

Pin #	i.MX 8 signal / ALT0	ALT1	ALT2	ALT3	Availability
P1-A5	SCU_GPIO0_00	SCU_UART0_RX		GPIO0.IO28	Always available
P1-A6	SCU_GPIO0_01	SCU_UART0_TX		GPIO0.IO29	Always available
P1-A12	GPT1_COMPARE	PWM2	KPP0_ROW5	GPIO0.IO19	Always available
P1-A13	GPT1_CLK	I2C2_SCL	KPP0_COL7	GPIO0.IO17	Always available
P1-A14	GPT1_CAPTURE	I2C2_SDA	KPP0_ROW4	GPIO0.IO18	Always available
P1-A15	GPT0_CLK	I2C1_SCL	KPP0_COL4	GPIO0.IO14	Always available
P1-A16	GPT0_CAPTURE	I2C1_SDA	KPP0_COL5	GPIO0.IO15	Always available
P1-A17	ENET1_MDC	I2C4_SCL		GPIO4.IO18	Always available
P1-A18	ENET1_MDIO	I2C4_SDA		GPIO4.IO17	Always available
P1-A19	M41_GPIO0_00	M41_TPM0_CH0	UART3_RX	GPIO0.IO12	Always available
P1-A20	M41_GPIO0_01	M41_TPM0_CH1	UART3_TX	GPIO0.IO13	Always available
P1-A22	M41_I2C0_SDA	M41_UART0_TX	M41_GPIO0_IO03	GPIO0.IO11	Always available
P1-A23	M41_I2C0_SCL	M41_UART0_RX	M41_GPIO0_IO02	GPIO0.IO10	Always available
P1-A24	M40_I2C0_SDA	M40_UART0_TX	M40_GPIO0_IO03	GPIO0.IO07	Always available
P1-A25	M40_I2C0_SCL	M40_UART0_RX	M40_GPIO0_IO02	GPIO0.IO06	Always available
P1-A27	UART0_RX			GPIO0.IO20	Always available
P1-A28	UART0_TX			GPIO0.IO21	Always available
P1-A29	UART0_RTS_B	PWM0	UART2_RX	GPIO0.IO22	Always available
P1-A30	UART0_CTS_B	PWM1	UART2_TX	GPIO0.IO23	Always available
P1-A32	UART1_CTS_B	SPI3_CSO	UART1_RTS_B	GPIO0.IO27	Always available
P1-A33	UART1_RTS_B	SPI3_SDI	UART1_CTS_B	GPIO0.IO26	Always available
P1-A34	UART1_RX	SPI3_SDO		GPIO0.IO25	Always available
P1-A35	UART1_TX	SPI3_SCK		GPIO0.IO24	Always available
P1-A36	USDHC2_DATA3	UART4_RTS_B		GPIO5.IO29	Always available
P1-A37	USDHC2_DATA2	UART4_CTS_B		GPIO5.IO28	Always available
P1-A38	USDHC2_DATA1	UART4_TX		GPIO5.IO27	Always available
P1-A39	USDHC2_DATA0	UART4_RX		GPIO5.IO26	Always available
P1-A40	USDHC2_RESET_B			GPIO4.IO09	Always available
P1-A42	USDHC2_CMD	AUD_MQS_L		GPIO5.IO25	Always available
P1-A43	USDHC2_CLK	AUD_MQS_R		GPIO5.IO24	Always available
P1-A44	USDHC2_CD_B			GPIO4.IO12	Always available
P1-A45	USDHC2_WP			GPIO4.IO11	Always available
P1-A47	ADC_IN3	DMA_SPI1_SCK	KPP0_COL3	GPIO3.IO21	Always available
P1-A48	ADC_IN2		KPP0_COL2	GPIO3.IO20	Always available
P1-A49	ADC_IN1		KPP0_COL1	GPIO3.IO19	Always available
P1-A50	ADC_IN0		KPP0_COL0	GPIO3.IO18	Always available
P1-A52	USDHC1_DATA7	NAND_ALE	USDHC1_CD_B	GPIO5.IO22	Always available
P1-A53	USDHC1_DATA6	NAND_WE_B	USDHC1_WP	GPIO5.IO21	Always available
P1-A54	USDHC1_DATA5	NAND_RE_B		GPIO5.IO20	Always available
P1-A55	USDHC1_DATA4	NAND_CE0_B		GPIO5.IO19	Always available
P1-A56	USDHC1_DATA3	NAND_DQS_P		GPIO5.IO18	Always available
P1-A57	USDHC1_DATA2	NAND_DQS_N		GPIO5.IO17	Always available
P1-A58	USDHC1_DATA1	NAND_RE_P		GPIO5.IO16	Always available
P1-A59	USDHC1_DATA0	NAND_RE_N		GPIO5.IO15	Always available
P1-A61	USDHC1_STROBE	NAND_CE1_B		GPIO5.IO23	Always available
P1-A62	USDHC1_CMD			GPIO5.IO14	Always available
P1-A64	USDHC1_RESET_B			GPIO4.IO07	Always available

Pin #	i.MX 8 signal / ALT0	ALT1	ALT2	ALT3	Availability
P1-A65	SPI2_CS1	AUD_SAI0_TXFS		GPIO3.IO11	Always available
P1-A66	SPI2_CS0			GPIO3.IO10	Always available
P1-A67	SPI2_MISO			GPIO3.IO09	Always available
P1-A68	SPI2_MOSI			GPIO3.IO08	Always available
P1-A69	SPI2_SCK			GPIO3.IO07	Always available
P1-A71	ESAI0_TX5_RX0			GPIO2.IO31	Always available
P1-A72	ESAI0_TX4_RX1			GPIO2.IO30	Always available
P1-A73	ESAI0_TX3_RX2			GPIO2.IO29	Always available
P1-A74	ESAI0_TX2_RX3			GPIO2.IO28	Always available
P1-A75	ESAI0_TX1			GPIO2.IO27	Always available
P1-A76	ESAI0_TX0			GPIO2.IO26	Always available
P1-A77	ESAI0_SCKT			GPIO2.IO25	Always available
P1-A78	ESAI0_SCKR			GPIO2.IO24	Always available
P1-A79	ESAI0_FST			GPIO2.IO23	Always available
P1-A81	ESAI0_FSR			GPIO2.IO22	Always available
P1-A82	MCLK_OUT0	AUD_ESAI0_TX_HF_CLK		GPIO3.IO01	Always available
P1-A83	MCLK_IN0	AUD_ESAI0_RX_HF_CLK		GPIO3.IO00	Always available
P1-A84	SAI1_TXFS	AUD_SAI1_RXFS		GPIO3.IO17	Always available
P1-A85	SAI1_TXD	AUD_SAI1_RXC		GPIO3.IO16	Always available
P1-A86	SAI1_TXC	AUD_SAI0_TXC		GPIO3.IO15	Always available
P1-A87	SAI1_RXFS	AUD_SAI0_RXD		GPIO3.IO14	Always available
P1-A88	SAI1_RXD	AUD_SAI0_TXFS		GPIO3.IO13	Always available
P1-A89	SAI1_RXC	AUD_SAI0_TXD		GPIO3.IO12	Always available
P1-A91	SPDIF_TX	AUD_MQS_L	AUD_ACM_MCLK_OUT1	GPIO2.IO15	Always available
P1-A92	SPDIF_RX	AUD_MQS_R	AUD_ACM_MCLK_IN1	GPIO2.IO14	Always available
P1-A93	SPDIF_EXT_CLK	DMA0_REQ_IN0		GPIO2.IO16	Always available
P1-A95	SPI0_CS1	AUD_SAI0_TXC		GPIO3.IO06	Always available
P1-A96	SPI0_CS0	AUD_SAI0_RXFS		GPIO3.IO05	Always available
P1-A97	SPI0_MISO	AUD_SAI0_RXD		GPIO3.IO04	Always available
P1-A98	SPI0_MOSI	AUD_SAI0_TXD		GPIO3.IO03	Always available
P1-A99	SPI0_SCK	AUD_SAI0_RXC		GPIO3.IO02	Always available
P1-A101	ESAI1_TX1	AUD_SAI2_RXFS		GPIO2.IO09	Always available
P1-A102	ESAI1_TX0	AUD_SAI2_RXD		GPIO2.IO08	Always available
P1-A103	ESAI1_SCKT	AUD_SAI2_RXC		GPIO2.IO07	Always available
P1-A104	GPT0_COMPARE	PWM3	KPP0_COL6	GPIO0.IO16	Always available
P1-A105	SPI3_CS1			GPIO2.IO21	Always available
P1-A106	SPI3_CS0	FTM_CH2		GPIO2.IO20	Always available
P1-A107	SPI3_MISO	FTM_CH1		GPIO2.IO19	Always available
P1-A108	SPI3_MOSI	FTM_CH0		GPIO2.IO18	Always available
P1-A109	SPI3_SCK			GPIO2.IO17	Always available
P1-B2	ENET0_MDIO	I2C4_SDA		GPIO4.IO13	NOT E2
P1-B3	ENET0_MDC	I2C4_SCL		GPIO4.IO14	NOT E2
P1-B4	ETH1_REFCLK	CONN_ENET1_PPS		GPIO4.IO16	Always available
P1-B5	ETH1_RGMII_RXD3	UART3_RX	VPU_TSI_S1_CLK	GPIO6.IO21	NOT E2
P1-B6	ETH1_RGMII_RXD2	CONN_ENET1_RMII_RX_ER	VPU_TSI_S0_CLK	GPIO6.IO20	NOT E2
P1-B7	ETH1_RGMII_RXC	UART3_CTS_B	VPU_TSI_S1_DATA	GPIO6.IO16	NOT E2
P1-B9	ETH1_RGMII_RXD0		VPU_TSI_S0_SYNC	GPIO6.IO18	NOT E2
P1-B10	ETH1_RGMII_RXD1		VPU_TSI_S0_DATA	GPIO6.IO19	NOT E2
P1-B12	ETH1_RGMII_RX_CTL		VPU_TSI_S0_VID	GPIO6.IO17	NOT E2
P1-B13	ETH1_RGMII_TX_CTL			GPIO6.IO11	NOT E2
P1-B15	ETH1_RGMII_TXD0			GPIO6.IO12	NOT E2
P1-B16	ETH1_RGMII_TXD1			GPIO6.IO13	NOT E2
P1-B18	ETH1_RGMII_TXD2	UART3_TX	VPU_TSI_S1_VID	GPIO6.IO14	NOT E2
P1-B19	ETH1_RGMII_TXD3	UART3_RTS_B	VPU_TSI_S1_SYNC	GPIO6.IO15	NOT E2
P1-B20	ETH1_RGMII_TXC	CONN_ENET1_RCLK50M_OUT	CONN_ENET1_RCLK50M_IN	GPIO6.IO10	NOT E2
P1-B24	ETH0_REFCLK	CONN_ENET0_PPS		GPIO4.IO15	Always available
P1-B25	ETH0_RGMII_TXC		CONN_ENET0_RCLK50M_IN	GPIO5.IO30	Not E1 and not E2
P1-B26	ETH0_RGMII_RXD2	CONN_ENET0_RMII_RX_ER		GPIO6.IO08	Not E1 and not E2
P1-B27	ETH0_RGMII_RXC			GPIO6.IO04	Not E1 and not E2
P1-B29	ETH0_RGMII_RXD1			GPIO6.IO07	Not E1 and not E2
P1-B30	ETH0_RGMII_RXD0			GPIO6.IO06	Not E1 and not E2
P1-B32	ETH0_RGMII_RXD3			GPIO6.IO09	Not E1 and not E2
P1-B33	ETH0_RGMII_TXD2			GPIO6.IO03	Not E1 and not E2
P1-B34	ETH0_RGMII_TXD3			GPIO6.IO02	Not E1 and not E2
P1-B36	ETH0_RGMII_TXD0			GPIO6.IO00	Not E1 and not E2
P1-B37	ETH0_RGMII_TXD1			GPIO6.IO01	Not E1 and not E2
P1-B39	ETH0_RGMII_RX_CTL			GPIO6.IO05	Not E1 and not E2
P1-B40	ETH0_RGMII_TX_CTL			GPIO5.IO31	Not E1 and not E2
P1-B46	USB_SS3_TC0	CONN_USB_OTG1_PWR		GPIO4.IO03	Always available
P1-B47	USB_SS3_TC2	CONN_USB_OTG2_PWR		GPIO4.IO04	Always available
P1-B49	USB_SS3_TC1	CONN_USB_OTG1_OC		GPIO4.IO05	Always available
P1-B50	USB_SS3_TC3	CONN_USB_OTG2_OC		GPIO4.IO06	Always available
P1-B62	USB_HSIC0_STROBE	I2C1_SCL		GPIO5.IO02	Always available
P1-B63	USB_HSIC0_DATA	I2C1_SDA		GPIO5.IO01	Always available

Pin #	i.MX 8 signal / ALT0	ALT1	ALT2	ALT3	Availability
P1-B71	PCIE0_PERST_B			GPIO4.IO29	Always available
P1-B72	PCIE0_CLKREQ_B			GPIO4.IO27	NOT WB or WB@PCIE0_MUX_SEL = '0'
P1-B73	PCIE0_WAKE_B			GPIO4.IO28	NOT WB or WB@PCIE0_MUX_SEL = '0'
P1-B82	PCIE1_WAKE_B			GPIO4.IO31	Always available
P1-B83	PCIE1_PERST_B			GPIO5.IO00	Always available
P1-B91	PCIE1_CLKREQ_B			GPIO4.IO30	Always available
P1-B104	CAN0_TX			GPIO3.IO30	Always available
P1-B105	CAN0_RX			GPIO3.IO29	Always available
P1-B106	CAN1_TX			GPIO4.IO00	Always available
P1-B107	CAN1_RX			GPIO3.IO31	Always available
P1-B108	CAN2_TX			GPIO4.IO02	Always available
P1-B109	CAN2_RX			GPIO4.IO01	Always available
P2-A24	LVDS0_GPIO01			GPIO1.IO05	Always available
P2-A25	LVDS0_GPIO00	LVDS_PWM0		GPIO1.IO04	Always available
P2-A26	LVDS0_I2C1_SCL	UART2_TX		GPIO1.IO08	Always available
P2-A27	LVDS0_I2C1_SDA	UART2_RX		GPIO1.IO09	Always available
P2-A44	LVDS0_I2C0_SCL	LVDS0_GPIO0_IO02		GPIO1.IO06	Always available
P2-A61	MIPI_DS11_I2C_SCL			GPIO1.IO20	Always available
P2-A62	MIPI_DS11_I2C_SDA			GPIO1.IO21	Always available
P2-A63	MIPI_DS11_GPIO0_01			GPIO1.IO23	Always available
P2-A64	MIPI_DS11_GPIO0_00	MIPI_DS11_PWM0		GPIO1.IO22	Always available
P2-A65	MIPI_DS10_I2C_SDA			GPIO1.IO17	Always available
P2-A66	MIPI_DS10_I2C_SCL			GPIO1.IO16	Always available
P2-A67	MIPI_DS10_GPIO0_00	MIPI_DS10_PWM0		GPIO1.IO18	Always available
P2-A68	MIPI_DS10_GPIO0_01			GPIO1.IO19	Always available
P2-A69	MIPI_CSI0_GPIO0_00	I2C0_SCL		GPIO1.IO27	Always available
P2-A71	MIPI_CSI0_GPIO0_01	I2C0_SDA		GPIO1.IO28	Always available
P2-A87	MIPI_CSI0_MCLK_OUT			GPIO1.IO24	Always available
P2-A91	MIPI_CSI0_I2C0_SCL			GPIO1.IO25	Always available
P2-A92	MIPI_CSI0_I2C0_SDA			GPIO1.IO26	Always available
P2-A93	MIPI_CSI1_MCLK_OUT			GPIO1.IO29	Always available
P2-A94	MIPI_CSI1_I2C0_SCL			GPIO2.IO00	Always available
P2-A95	MIPI_CSI1_I2C0_SDA			GPIO2.IO01	Always available
P2-A96	MIPI_CSI1_GPIO0_00	UART4_RX		GPIO1.IO30	Always available
P2-A104	MIPI_CSI1_GPIO0_01	UART4_TX		GPIO1.IO31	Always available
P2-B20	LVDS1_GPIO01			GPIO1.IO11	Always available
P2-B22	LVDS1_I2C0_SCL	LVDS1_GPIO0_IO02		GPIO1.IO12	Always available
P2-B40	LVDS1_I2C1_SDA	UART3_RX		GPIO1.IO15	Always available
P2-B42	LVDS1_I2C1_SCL	UART3_TX		GPIO1.IO14	Always available
P2-B61	LVDS1_GPIO00	LVDS1_PWM0		GPIO1.IO10	Always available

5.6 RTC

CL-SOM-iMX8MAX features an on-board ultra-low-power EM3027 real time clock (RTC). The RTC connected to the i.MX 8 SoC using I2C1_3V3 interface at address 56h.

Back-up power supply should be connected to VCC_RTC power rail in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about CL-SOM-iMX8MAX RTC please refer to the EM3027 datasheet.

5.7 LED

CL-SOM-iMX8MAX features a single general purpose green LED controlled by GPIO1_12IO23 signal of iMX 8. The LED is ON when GPIO1_12IO23 is logic High.

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX8MAX CoM/SoM carrier board interface uses 2x 220 Pins carrier board connectors. The SoM pinout is detailed in the table below.

6.1 Connectors Pinout

Table 72 Connector P1

Pin #	CL-SOM-iMX8MAX Signal Name	Ref.	Pin #	CL-SOM-iMX8MAX Signal Name	Ref.
B1	GND	5.1	A1	GND	5.1
B2	ETH0_MDIO	4.7	A2	ALT_BOOT#	5.4
	I2C4_SDA	4.16			
	GPIO4.IO13	4.21			
B3	ETH0_MDC	4.7	A3	USB_OTG1_VBUS	4.12
	I2C4_SCL	4.16			
	GPIO4.IO14	4.21			
B4	ETH1_REFCLK	4.7	A4	USB_OTG2_VBUS	4.12
	CONN_ENET1_PPS	N/A			
	GPIO4.IO16	4.21			
B5	EPHY1_LED_10_100	4.5.1	A5	SCU_GPIO0_02	4.74.21
	GPIO6.IO21	4.21		SCU_UART0_RX	N/A
				GPIO0.IO28	4.14
B6	EPHY1_LED_ACT	4.5.1	A6	SCU_GPIO0_01	4.74.21
	GPIO6.IO20	4.21		SCU_UART0_TX	N/A
				GPIO0.IO29	4.14
B7	EPHY1_LED_1000	4.5.1	A7	JTAG_TDI	4.20
B8	GPIO6.IO16	4.21	A8	JTAG_TDO	4.20
B9	EPHY1_TRXP3	4.5.1	A9	JTAG_TCK	4.20
	VPU_TSI_S0_SYNC	N/A			
	GPIO6.IO18	4.21			
B10	EPHY1_TRXN3	4.5.1	A10	JTAG_TMS	4.20
	VPU_TSI_S0_DATA	N/A			
	GPIO6.IO19	4.21			
B11	GND	5.1	A11	GND	5.1
B12	EPHY1_TRXN2	4.5.1	A12	PWM2 or GPIO_BA51	4.18
	VPU_TSI_S0_VID	N/A		GPT1_COMPARE	N/A
	GPIO6.IO17	4.21		KPP0_ROW5	N/A
B13	EPHY1_TRXP2	4.5.1	A13	I2C2_3V3_SCL	4.16
	GPIO6.IO11	4.21		GPT1_CLK	N/A
				KPP0_COL7	N/A
B14	GND	5.1	A14	GPIO0.IO17	4.21
				I2C2_3V3_SDA	4.16
				GPT1_CAPTURE	N/A
B15	EPHY1_TRXN1	4.5.1	A15	KPP0_ROW4	N/A
	GPIO6.IO12	4.21		GPIO0.IO18	4.21
				I2C1_3V3_SCL	4.16
B16	EPHY1_TRXP1	4.5.1	A16	GPT0_CLK	N/A
	GPIO6.IO13	4.21		KPP0_COL4	N/A
				GPIO0.IO14	4.21
B17	GND	5.1	A17	I2C1_3V3_SDA	4.16
				GPT0_CAPTURE	N/A
				KPP0_COL5	N/A
B18	EPHY1_TRXN0	4.5.1	A18	GPIO0.IO15	4.21
	UART3_TX	4.14		ETH1_MDC	4.5.2
	VPU_TSI_S1_VID	N/A		I2C4_SCL	4.16
B19	GPIO6.IO14	4.21	A19	GPIO4.IO18	4.21
	EPHY1_TRXP0	4.5.1		ETH1_MDIO	4.5.2
	UART3_RTS_B	4.14		I2C4_SDA	4.16
	VPU_TSI_S1_SYNC	N/A		GPIO4.IO17	4.21
	GPIO6.IO15	4.21		UART3_RX	4.14
				M41_GPIO0_00	N/A
				M41_TPM0_CH0	N/A
				GPIO0.IO12	4.21

B20	EPHY1_TXC_BYP CONN_ENET1_RCLK50M_OUT CONN_ENET1_RCLK50M_IN GPIO6.IO10	4.5.1 N/A N/A 4.21	A20	UART3_TX M41_GPIO0_01 M41_TPM0_CH1 GPIO0.IO13	4.14 N/A N/A 4.21
B21	GND	5.1	A21	GND	5.1
B22	VCC_ENET1	5.1	A22	M41_UART0_TX M41_I2C0_SDA M41_GPIO0_IO03 GPIO0.IO11	4.14 4.16 N/A 4.21
B23	VCC_ENET0	5.1	A23	M41_UART0_RX M41_I2C0_SCL M41_GPIO0_IO02 GPIO0.IO10	4.14 4.16 N/A 4.21
B24	ETH0_REFCLK CONN_ENET0_PPS GPIO4.IO15	4.7 N/A 4.21	A24	M40_UART0_TX M40_I2C0_SDA M40_GPIO0_IO03 GPIO0.IO07	4.14 4.16 N/A 4.21
B25	EPHY0_TXC_BYP CONN_ENET0_RCLK50M_IN GPIO5.IO30	4.7 N/A 4.21	A25	M40_UART0_RX M40_I2C0_SCL M40_GPIO0_IO02 GPIO0.IO06	4.14 4.16 N/A 4.21
B26	EPHY0_LED_ACT CONN_ENET0_RMII_RX_ER GPIO6.IO08	4.5.1 N/A 4.21	A26	GND	5.1
B27	EPHY0_LED_1000 GPIO6.IO04	4.5.1 4.21	A27	DBG_UART_RX GPIO0.IO20	4.14 4.21
B28	GND	5.1	A28	DBG_UART_TX GPIO0.IO21	4.14 4.21
B29	EPHY0_TRXN3 GPIO6.IO07	4.5.1 4.21	A29	UART2_RX UART0_RTS_B PWM0 GPIO0.IO22	4.14 4.14 4.18 4.21
B30	EPHY0_TRXP3 GPIO6.IO06	4.5.1 4.21	A30	UART2_TX UART0_CTS_B PWM1 GPIO0.IO23	4.14 4.14 4.18 4.21
B31	GND	5.1	A31	GND	5.1
B32	EPHY0_LED_10_100 GPIO6.IO09	4.5.1 4.21	A32	UART1_CTS SPI3_CSO UART1_RTS_B GPIO0.IO27	4.14 4.17 4.14 4.21
B33	EPHY0_TRXN0 GPIO6.IO03	4.5.1 4.21	A33	UART1_RTS SPI3_SDI UART1_CTS_B GPIO0.IO26	4.14 4.17 4.14 4.21
B34	EPHY0_TRXP0 GPIO6.IO02	4.5.1 4.21	A34	UART1_RX SPI3_SDO GPIO0.IO25	4.14 4.17 4.21
B35	GND	5.1	A35	UART1_TX SPI3_SCK GPIO0.IO24	4.14 4.17 4.21
B36	EPHY0_TRXN1 GPIO6.IO00	4.5.1 4.21	A36	USDHC2_DATA3 UART4_RTS_B GPIO5.IO29	4.13 4.14 4.21
B37	EPHY0_TRXP1 GPIO6.IO01	4.5.1 4.21	A37	USDHC2_DATA2 UART4_CTS_B GPIO5.IO28	4.13 4.14 4.21
B38	GND	5.1	A38	USDHC2_DATA1 UART4_TX GPIO5.IO27	4.13 4.14 4.21
B39	EPHY0_TRXN2 GPIO6.IO05	4.5.1 4.21	A39	USDHC2_DATA0 UART4_RX GPIO5.IO26	4.13 4.14 4.21
B40	EPHY0_TRXP2 GPIO5.IO31	4.5.1 4.21	A40	USDHC2_RESET_B GPIO4.IO09	4.13 4.21
B41	GND	5.1	A41	GND	5.1
B42	MUX_USB_OTG1_DP	4.12	A42	USDHC2_CMD AUD_MQS_L GPIO5.IO25	4.13 N/A 4.21
B43	MUX_USB_OTG1_DN	4.12	A43	USDHC2_CLK AUD_MQS_R GPIO5.IO24	4.13 N/A 4.21
B44	GND	5.1	A44	USDHC2_CD_B GPIO4.IO12	4.13 4.21

B45	USB_OTG1_ID	4.12	A45	USDHC2_WP GPIO4.IO11	4.13 4.21
B46	USB_OTG1_PWREN USB_SS3_TC0 GPIO4.IO03	4.12 4.12 4.21	A46	GND	5.1
B47	USB_OTG1_OC USB_SS3_TC2 GPIO4.IO05	4.12 4.12 4.21	A47	ADC_IN3 DMA_SPI1_SCK KPP0_COL3 GPIO3.IO21	4.19 N/A N/A 4.21
B48	USB_OTG2_ID	4.12	A48	ADC_IN2 KPP0_COL2 GPIO3.IO20	4.19 N/A 4.21
B49	USB_OTG2_PWREN USB_SS3_TC1 GPIO4.IO04	4.12 4.12 4.21	A49	ADC_IN1 KPP0_COL1 GPIO3.IO19	4.19 N/A 4.21
B50	USB_OTG2_OC USB_SS3_TC3 GPIO4.IO06	4.12 4.12 4.21	A50	ADC_IN0 KPP0_COL0 GPIO3.IO18	4.19 N/A 4.21
B51	GND	5.1	A51	GND	5.1
B52	USB_OTG2_DP	4.12	A52	USDHC1_DATA7 NAND_ALE USDHC1_CD_B GPIO5.IO22	4.13 N/A 4.13 4.21
B53	USB_OTG2_DN	4.12	A53	USDHC1_DATA6 NAND_WE_B USDHC1_WP GPIO5.IO21	4.13 N/A 4.13 4.21
B54	GND	5.1	A54	USDHC1_DATA5 NAND_RE_B GPIO5.IO20	4.13 N/A 4.21
B55	USB_SS3_RX_P	4.12	A55	USDHC1_DATA4 NAND_CE0_B GPIO5.IO19	4.13 N/A 4.21
B56	USB_SS3_RX_N	4.12	A56	USDHC1_DATA3 NAND_DQS_P GPIO5.IO18	4.13 N/A 4.21
B57	GND	5.1	A57	USDHC1_DATA2 NAND_DQS_N GPIO5.IO17	4.13 N/A 4.21
B58	USB_SS3_TX_P	4.12	A58	USDHC1_DATA1 NAND_RE_P GPIO5.IO16	4.13 N/A 4.21
B59	USB_SS3_TX_N	4.12	A59	USDHC1_DATA0 NAND_RE_N GPIO5.IO15	4.13 N/A 4.21
B60	GND	5.1	A60	GND	5.1
B61	POR_B_1V8	5.3	A61	USDHC1_STROBE NAND_CE1_B GPIO5.IO23	4.13 N/A 4.21
B62	USB_HSIC0_STROBE I2C1_3V3_SCL GPIO5.IO02	4.12 4.16 4.21	A62	USDHC1_CMD GPIO5.IO14	4.13 4.21
B63	USB_HSIC0_DATA I2C1_3V3_SDA GPIO5.IO01	4.12 4.16 4.21	A63	USDHC1_CLK	4.13
B64	GND	5.1	A64	USDHC1_RESET_B GPIO4.IO07	4.13 4.21
B65	PCIE0_RX0_N_SB	4.7	A65	SPI2_CS1 AUD_SAI0_TXFS GPIO3.IO11	4.17 4.10 4.21
B66	PCIE0_RX0_P_SB	4.7	A66	SPI2_CS0 GPIO3.IO10	4.17 4.21
B67	GND	5.1	A67	SPI2_MISO GPIO3.IO09	4.17 4.21
B68	PCIE0_TX0_N_SB	4.7	A68	SPI2_MOSI GPIO3.IO08	4.17 4.21
B69	PCIE0_TX0_P_SB	4.7	A69	SPI2_SCK GPIO3.IO07	4.17 4.21
B70	GND	5.1	A70	GND	5.1
B71	PCIE0_PERST# GPIO4.IO29	4.7 4.21	A71	ESAI0_TX5_RX0 GPIO2.IO31	4.11 4.21
B72	PCIE0_CLKREQ#_SB GPIO4.IO27	4.7 4.21	A72	ESAI0_TX4_RX1 GPIO2.IO30	4.11 4.21

B73	PCIE0_WAKE#_SB GPIO4.IO28	4.7 4.21		A73	ESAI0_TX3_RX2 GPIO2.IO29	4.11 4.21
B74	GND	5.1		A74	ESAI0_TX2_RX3 GPIO2.IO28	4.11 4.21
B75	PCIE0_REFCLK0_N_SB	4.7		A75	ESAI0_TX1 GPIO2.IO27	4.11 4.21
B76	PCIE0_REFCLK0_P_SB	4.7		A76	ESAI0_TX0 GPIO2.IO26	4.11 4.21
B77	GND	5.1		A77	ESAI0_SCKT GPIO2.IO25	4.11 4.21
B78	PCIE1_TX0_N	4.7		A78	ESAI0_SCKR GPIO2.IO24	4.11 4.21
B79	PCIE1_TX0_P	4.7		A79	ESAI0_FST GPIO2.IO23	4.11 4.21
B80	GND	5.1		A80	GND	5.1
B81	PCIE0_MUX_SEL	4.7		A81	ESAI0_FSR GPIO2.IO22	4.11 4.21
B82	PCIE1_WAKE# GPIO4.IO31	4.7 4.21		A82	MCLK_OUT0 AUD_ESAI0_TX_HF_CLK GPIO3.IO01	4.11 N/A 4.21
B83	PCIE1_PERST# GPIO5.IO00	4.7 4.21		A83	MCLK_IN0 AUD_ESAI0_RX_HF_CLK GPIO3.IO00	4.11 N/A 4.21
B84	GND	5.1		A84	SAI1_TXFS AUD_SAI1_RXFS GPIO3.IO17	4.10 4.10 4.21
B85	PCIE1_RX0_N	4.7		A85	SAI1_TXD AUD_SAI1_RXC GPIO3.IO16	4.10 4.10 4.21
B86	PCIE1_RX0_P	4.7		A86	SAI1_TXC AUD_SAI0_TXC GPIO3.IO15	4.10 4.10 4.21
B87	GND	5.1		A87	SAI1_RXFS AUD_SAI0_RXD GPIO3.IO14	4.10 4.10 4.21
B88	PCIE1_CLKGEN1_N	4.7		A88	SAI1_RXD AUD_SAI0_TXFS GPIO3.IO13	4.10 4.10 4.21
B89	PCIE1_CLKGEN1_P	4.7		A89	SAI1_RXC AUD_SAI0_TXD GPIO3.IO12	4.10 4.10 4.21
B90	GND	5.1		A90	GND	5.1
B91	PCIE1_CLKREQ# GPIO4.IO30	4.7 4.21		A91	SPDIF_TX AUD_MQS_L AUD_ACM_MCLK_OUT1 GPIO2.IO15	4.9 N/A N/A 4.21
B92	VCC_RTC	5.1		A92	SPDIF_RX AUD_MQS_R AUD_ACM_MCLK_IN1 GPIO2.IO14	4.9 N/A N/A 4.21
B93	PCIE_SATA_CLKREQ#	4.7		A93	SPDIF_EXT_CLK DMA0_REQ_IN0 GPIO2.IO16	4.9 N/A 4.21
B94	GND	5.1		A94	GND	5.1
B95	PCIE_SATA_CLKGEN0_N	4.7		A95	SPI0_CS1 AUD_SAI0_TXC GPIO3.IO06	4.10 4.17 4.21
B96	PCIE_SATA_CLKGEN0_P	4.7		A96	SPI0_CS0 AUD_SAI0_RXFS GPIO3.IO05	4.10 4.17 4.21
B97	GND	5.1		A97	SPI0_MISO AUD_SAI0_RXD GPIO3.IO04	4.10 4.17 4.21
B98	PCIE_SATA_RX0_N	4.7		A98	SPI0_MOSI AUD_SAI0_TXD GPIO3.IO03	4.10 4.17 4.21
B99	PCIE_SATA_RX0_P	4.7		A99	SPI0_SCK AUD_SAI0_RXC GPIO3.IO02	4.10 4.17 4.21
B100	GND	5.1		A100	GND	5.1
B101	PCIE_SATA_TX0_N	4.7		A101	SAI2_RXFS ESAI1_TX1 GPIO2.IO09	4.10 N/A 4.21

B102	PCIE_SATA_TX0_P	4.7		A102	SAI2_RXD ESAI1_TX0 GPIO2.IO08	4.10 N/A 4.21
B103	GND	5.1		A103	SAI2_RXC ESAI1_SCKT GPIO2.IO07	4.10 N/A 4.21
B104	CAN0_TX GPIO3.IO30	4.15 4.21		A104	PWM3 or GPIO_AW53 GPT0_COMPARE KPP0_COL6 GPIO0.IO16	4.18 N/A N/A 4.21
B105	CAN0_RX GPIO3.IO29	4.15 4.21		A105	SPI3_CS1 GPIO2.IO21	4.17 4.21
B106	CAN1_TX GPIO4.IO00	4.15 4.21		A106	SPI3_CS0 FTM_CH2 GPIO2.IO20	4.17 N/A 4.21
B107	CAN1_RX GPIO3.IO31	4.15 4.21		A107	SPI3_MISO FTM_CH1 GPIO2.IO19	4.17 N/A 4.21
B108	CAN2_TX GPIO4.IO02	4.15 4.21		A108	SPI3_MOSI FTM_CH0 GPIO2.IO18	4.17 N/A 4.21
B109	CAN2_RX GPIO4.IO01	4.15 4.21		A109	SPI3_SCK GPIO2.IO17	4.17 4.21
B110	GND	5.1		A110	GND	5.1

Table 73 Connector P2

Pin #	CL-SOM-iMX8MAX Signal Name	Ref.		Pin #	CL-SOM-iMX8MAX Signal Name	Ref.
B1	GND	5.1		A1	GND	5.1
B2	JTAG_nRST	N/A		A2	V_SOM	5.1
B3	LVDS0_CH0_TX3_N	4.3		A3	V_SOM	5.1
B4	LVDS0_CH0_TX3_P	4.3		A4	V_SOM	5.1
B5	GND	5.1		A5	V_SOM	5.1
B6	LVDS0_CH0_TX2_N	4.3		A6	V_SOM	5.1
B7	LVDS0_CH0_TX2_P	4.3		A7	V_SOM	5.1
B8	GND	5.1		A8	V_SOM	5.1
B9	LVDS0_CH0_TX1_N	4.3		A9	V_SOM	5.1
B10	LVDS0_CH0_TX1_P	4.3		A10	V_SOM	5.1
B11	GND	5.1		A11	GND	5.1
B12	LVDS0_CH0_TX0_N	4.3		A12	V_SOM	5.1
B13	LVDS0_CH0_TX0_P	4.3		A13	V_SOM	5.1
B14	GND	5.1		A14	V_SOM	5.1
B15	LVDS0_CH0_CLK_N	4.3		A15	V_SOM	5.1
B16	LVDS0_CH0_CLK_P	4.3		A16	V_SOM	5.1
B17	GND	5.1		A17	V_SOM	5.1
B18	LVDS1_CH0_TX3_N	4.3		A18	V_SOM	5.1
B19	LVDS1_CH0_TX3_P	4.3		A19	GND	5.1
B20	LVDS1_TS_INT LVDS1_GPIO01 GPIO1.IO11	4.3 4.3 4.21		A20	PWRBTN	5.2.1
B21	GND	5.1		A21	GND	5.1
B22	LVDS1_GPIO02 LVDS1_I2C0_SCL GPIO1.IO12	4.3 4.3 4.21		A22	TAMPER_IN	N/A
B23	LVDS1_CH0_TX2_N	4.3		A23	TAMPER_OUT	N/A
B24	LVDS1_CH0_TX2_P	4.3		A24	LVDS0_TS_INT LVDS0_GPIO01 GPIO1.IO05	4.3 4.3 4.21
B25	GND	5.1		A25	LVDS0_BL_PWM LVDS0_GPIO00 GPIO1.IO04	4.3 4.3 4.21
B26	LVDS1_CH0_TX1_N	4.3		A26	LVDS0_TS_SCL UART2_TX GPIO1.IO08	4.3/4.16 4.14 4.21
B27	LVDS1_CH0_TX1_P	4.3		A27	LVDS0_TS_SDA UART2_RX GPIO1.IO09	4.3/4.16 4.14 4.21
B28	GND	5.1		A28	GND	5.1
B29	LVDS1_CH0_TX0_N	4.3		A29	LVDS0_CH1_CLK_P	4.3
B30	LVDS1_CH0_TX0_P	4.3		A30	LVDS0_CH1_CLK_N	4.3
B31	GND	5.1		A31	GND	5.1
B32	LVDS1_CH0_CLK_N	4.3		A32	LVDS0_CH1_TX0_P	4.3

B33	LVDS1_CH0_CLK_P	4.3	A33	LVDS0_CH1_TX0_N	4.3
B34	GND	5.1	A34	GND	5.1
B35	LVDS1_CH1_CLK_N	4.3	A35	LVDS0_CH1_TX1_P	4.3
B36	LVDS1_CH1_CLK_P	4.3	A36	LVDS0_CH1_TX1_N	4.3
B37	GND	5.1	A37	GND	5.1
B38	LVDS1_CH1_TX0_N	4.3	A38	LVDS0_CH1_TX2_P	4.3
B39	LVDS1_CH1_TX0_P	4.3	A39	LVDS0_CH1_TX2_N	4.3
B40	LVDS1_TS_SDA UART3_RX GPIO1.IO15	4.3/4.16 4.14 4.21	A40	COLD_RESET_IN	5.3
B41	GND	5.1	A41	GND	5.1
B42	LVDS1_TS_SCL UART3_TX GPIO1.IO14	4.3/4.16 4.14 4.21	A42	LVDS0_CH1_TX3_P	4.3
B43	LVDS1_CH1_TX1_N	4.3	A43	LVDS0_CH1_TX3_N	4.3
B44	LVDS1_CH1_TX1_P	4.3	A44	LVDS0_GPIO02 LVDS0_I2C0_SCL GPIO1.IO06	4.3 4.3 4.21
B45	GND	5.1	A45	GND	5.1
B46	LVDS1_CH1_TX2_N	4.3	A46	MIPI_DSI1_DATA2_P	4.2
B47	LVDS1_CH1_TX2_P	4.3	A47	MIPI_DSI1_DATA2_N	4.2
B48	GND	5.1	A48	GND	5.1
B49	LVDS1_CH1_TX3_N	4.3	A49	MIPI_DSI1_DATA0_P	4.2
B50	LVDS1_CH1_TX3_P	4.3	A50	MIPI_DSI1_DATA0_N	4.2
B51	GND	5.1	A51	GND	5.1
B52	MIPI_DSI0_DATA2_N	4.2	A52	MIPI_DSI1_CLK_P	4.2
B53	MIPI_DSI0_DATA2_P	4.2	A53	MIPI_DSI1_CLK_N	4.2
B54	GND	5.1	A54	GND	5.1
B55	MIPI_DSI0_DATA0_N	4.2	A55	MIPI_DSI1_DATA1_P	4.2
B56	MIPI_DSI0_DATA0_P	4.2	A56	MIPI_DSI1_DATA1_N	4.2
B57	GND	5.1	A57	GND	5.1
B58	MIPI_DSI0_CLK_N	4.2	A58	MIPI_DSI1_DATA3_P	4.2
B59	MIPI_DSI0_CLK_P	4.2	A59	MIPI_DSI1_DATA3_N	4.2
B60	GND	5.1	A60	GND	5.1
B61	LVDS1_BL_PWM LVDS1_GPIO00 GPIO1.IO10	4.3 4.3 4.21	A61	MIPI_DSI1_I2C_SCL GPIO1.IO20	4.2/4.16 4.21
B62	MIPI_DSI0_DATA1_N	4.2	A62	MIPI_DSI1_I2C_SDA GPIO1.IO21	4.2/4.16 4.21
B63	MIPI_DSI0_DATA1_P	4.2	A63	MIPI_DSI1_INT MIPI_DSI1_GPIO0_01 GPIO1.IO23	4.2 4.2 4.21
B64	GND	5.1	A64	MIPI_DSI1_PWM MIPI_DSI1_GPIO0_00 GPIO1.IO22	4.2 4.2 4.21
B65	MIPI_DSI0_DATA3_N	4.2	A65	MIPI_DSI0_I2C_SDA GPIO1.IO17	4.2/4.16 4.21
B66	MIPI_DSI0_DATA3_P	4.2	A66	MIPI_DSI0_I2C_SCL GPIO1.IO16	4.2/4.16 4.21
B67	GND	5.1	A67	MIPI_DSI0_PWM MIPI_DSI0_GPIO0_00 GPIO1.IO18	4.2 4.2 4.21
B68	HDMI_RX_DAT2_P	-	A68	MIPI_DSI0_INT MIPI_DSI0_GPIO0_01 GPIO1.IO19	4.2 4.2 4.21
B69	HDMI_RX_DAT2_N	-	A69	MIPI_CSI0_GPIO_RST# I2C0_SCL GPIO1.IO27	4.4 4.16 4.21
B70	GND	5.1	A70	GND	5.1
B71	HDMI_RX_DDC_SCL	-	A71	MIPI_CSI0_GPIO_PWRDN I2C0_SDA GPIO1.IO28	4.4 4.16 4.21
B72	HDMI_RX_DDC_SDA	-	A72	MIPI_CSI0_DATA2_N	4.4
B73	HDMI_RX_HPD	-	A73	MIPI_CSI0_DATA2_P	4.4
B74	GND	5.1	A74	GND	5.1
B75	HDMI_RX_DAT1_P	-	A75	MIPI_CSI0_DATA0_N	4.4
B76	HDMI_RX_DAT1_N	-	A76	MIPI_CSI0_DATA0_P	4.4
B77	GND	5.1	A77	GND	5.1
B78	HDMI_RX_DAT0_P	-	A78	MIPI_CSI0_CLK_N	4.4
B79	HDMI_RX_DAT0_N	-	A79	MIPI_CSI0_CLK_P	4.4
B80	GND	5.1	A80	GND	5.1
B81	HDMI_RX_CLK_P	-	A81	MIPI_CSI0_DATA1_N	4.4
B82	HDMI_RX_CLK_N	-	A82	MIPI_CSI0_DATA1_P	4.4

B83	GND	5.1		A83	GND	5.1
B84	HDMI_RX_ARC_P	-		A84	MIPI_CSI0_DATA3_N	4.4
B85	HDMI_RX_MON_5V	-		A85	MIPI_CSI0_DATA3_P	4.4
B86	HDMI_RX_CEC	-		A86	GND	5.1
B87	GND	5.1		A87	MIPI_CSI0_MCLK_OUT GPIO1.IO24	4.4 4.21
B88	HDMI_TX_DAT2_DP0_P	4.1		A88	MIPI_CSI1_DATA2_P	4.4
B89	HDMI_TX_DAT2_DP0_N	4.1		A89	MIPI_CSI1_DATA2_N	4.4
B90	GND	5.1		A90	GND	5.1
B91	HDMI_TX_DDC_SDA	4.1/4.16		A91	MIPI_CSI0_I2C0_SCL GPIO1.IO25	4.4 4.21
B92	HDMI_TX_DDC_SCL	4.1/4.16		A92	MIPI_CSI0_I2C0_SDA GPIO1.IO26	4.4 4.21
B93	HDMI_TX_CEC	4.1		A93	MIPI_CSI1_MCLK_OUT GPIO1.IO29	4.4 4.21
B94	GND	5.1		A94	MIPI_CSI1_I2C0_SCL GPIO2.IO00	4.4 4.21
B95	HDMI_TX_DAT1_DP1_P	4.1		A95	MIPI_CSI1_I2C0_SDA GPIO2.IO01	4.4 4.21
B96	HDMI_TX_DAT1_DP1_N	4.1		A96	MIPI_CSI1_GPIO_RST# UART4_RX GPIO1.IO30	4.4 4.14 4.21
B97	GND	5.1		A97	GND	5.1
B98	HDMI_TX_DAT0_DP2_P	4.1		A98	MIPI_CSI1_DATA0_P	4.4
B99	HDMI_TX_DAT0_DP2_N	4.1		A99	MIPI_CSI1_DATA0_N	4.4
B100	GND	5.1		A100	GND	5.1
B101	HDMI_TX_CLK_DP3_P	4.1		A101	MIPI_CSI1_CLK_P	4.4
B102	HDMI_TX_CLK_DP3_N	4.1		A102	MIPI_CSI1_CLK_N	4.4
B103	GND	5.1		A103	GND	5.1
B104	HDMI_TX_AUX_N	4.1		A104	MIPI_CSI1_GPIO_PWRDN UART4_TX GPIO1.IO31	4.4 4.14 4.21
B105	HDMI_TX_AUX_P	4.1		A105	MIPI_CSI1_DATA1_P	4.4
B106	GND	5.1		A106	MIPI_CSI1_DATA1_N	4.4
B107	HDMI_TX_HPD	4.1		A107	GND	5.1
B108	SCU_PMIC_ON_REQ	5.2.1		A108	MIPI_CSI1_DATA3_P	4.4
B109	SEQUENCE 2 ON	5.2.1		A109	MIPI_CSI1_DATA3_N	4.4
B110	GND	5.1		A110	GND	5.1

6.2 Mating Connectors

Table 74 Connector type

CL-SOM-iMX8MAX connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	AMP 3-6318490-6: 220 contacts	AMP	3-1827253-6
P2	AMP 3-6318490-6: 220 contacts	AMP	3-1827253-6

6.3 Mechanical Drawings

Figure 3 CL-SOM-iMX8MAX top

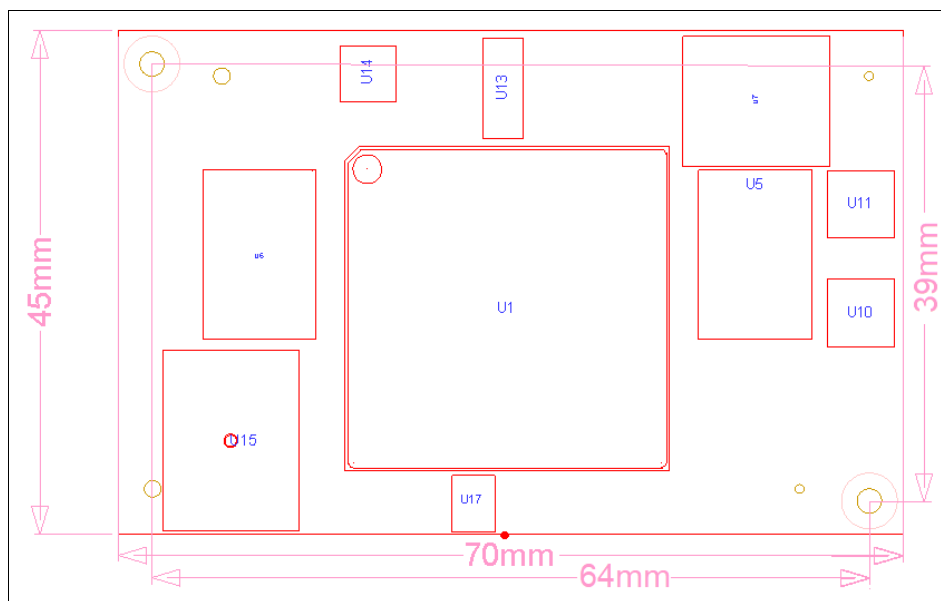
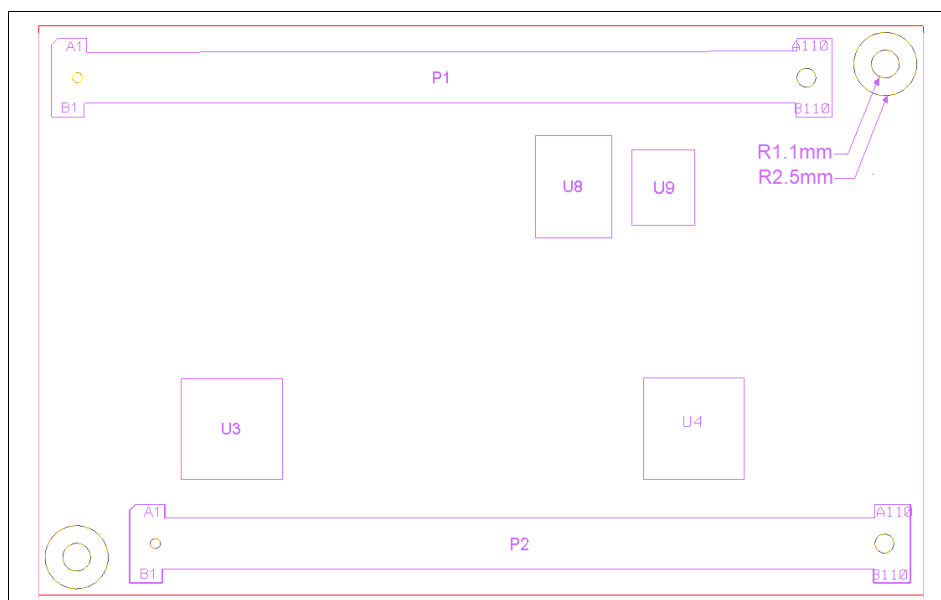


Figure 4 CL-SOM-iMX8MAX bottom



1. All dimensions are in millimeters.
2. The height of all components on top is < 2.52mm.
3. The height of all components on bottom is < 3.25mm.
4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format at
<https://www.compulab.com/products/computer-on-modules/cl-som-imx8max-nxp-i-mx-8-system-on-module-computer/#devres>

6.4 Heat Spreader and Cooling Solutions

CompuLab provides CL-SOM-iMX8MAX with an optional heat-spreader assembly. The CL-SOM-iMX8MAX heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the CL-SOM-iMX8MAX temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 75 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	6	V
USB OTG1 VBUS	-0.3	5.5	V
USB OTG2 VBUS	-0.3	5.5	V
ADC signals	-0.1	2.1	V
Voltage on any 3.3V I/O pins	-0.3	3.6	V
Voltage on any 1.8V I/O pins	-0.3	2.1	V
Backup battery supply voltage (VCC_RTC)	-0.3	6	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 76 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.95	4	5.5	V
Backup battery supply voltage (VCC_RTC)	1.4	3.3	5.5	V

7.3 ESD Performance

Table 77 ESD Performance

Interface	ESD Performance
iMX8M pins	1kV Human Body Model (HBM), 250V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails – V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10uF and 100uF capacitors between V_SOM and GND near the carrier-board connector (P2).
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
 - PCIe, SATA, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
 - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
 - PCIe TX/RX data pairs require 85 ohm differential impedance.
 - USB 3.0, USB 2.0: DP/DM and SS_TX/SS_RX signals require 90 ohm differential impedance.
 - Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI) and LVDS signals require 100 ohm differential impedance.
 - All single-ended signals require 50 ohm impedance.
- Refer to the SB-iMX8MAX carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to the Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, check the following potential issues:
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.

- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.