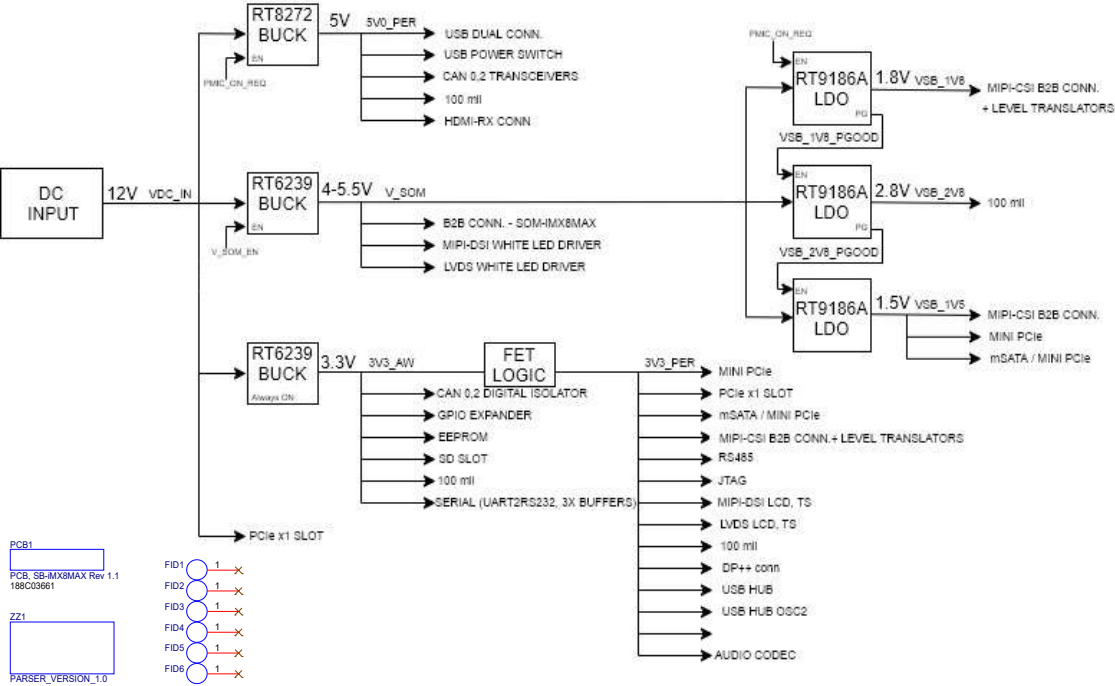


SB-iMX8MAX

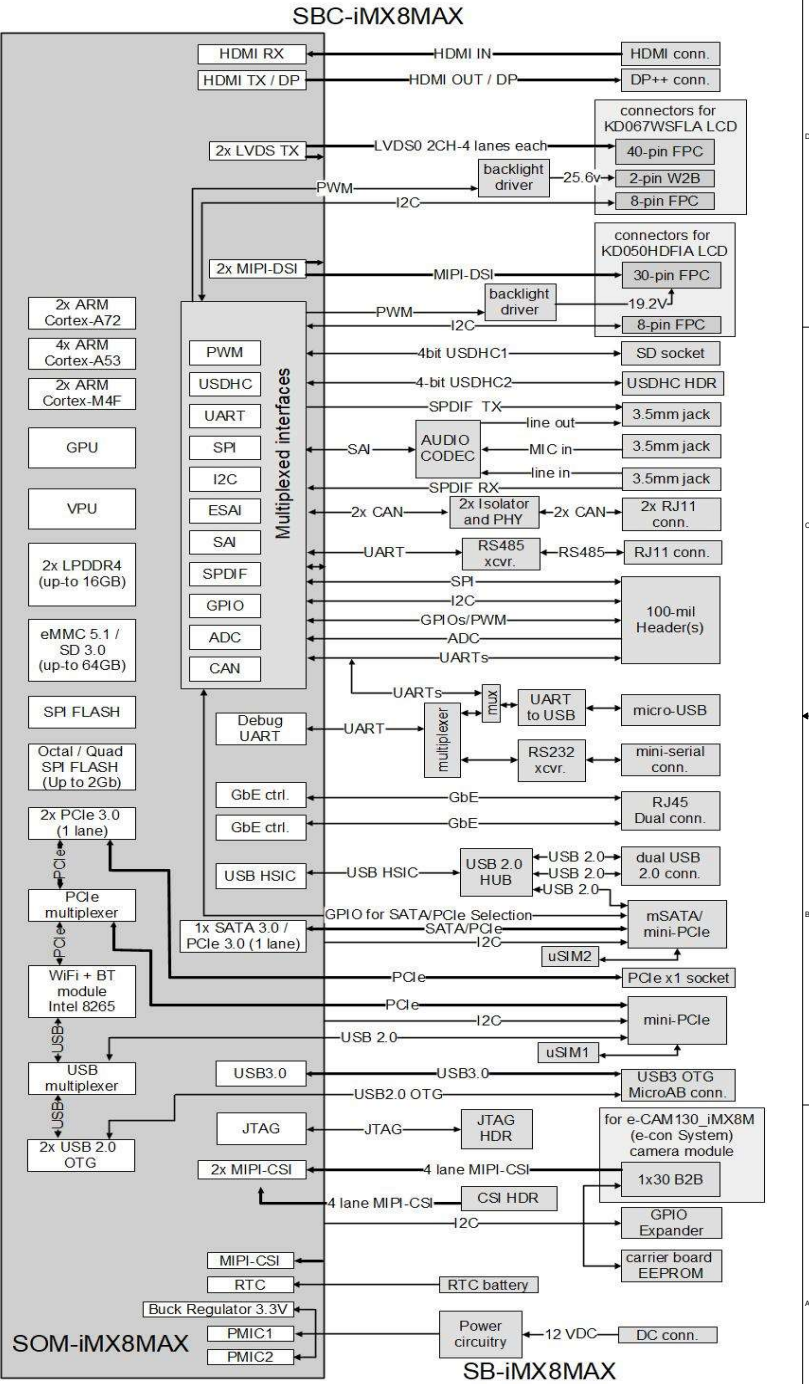
BOARD REVISION: 1.1

| PAGE | FUNCTION |
|------|--------------------------------|
| 01 | BLOCK & POWER DIAGRAM |
| 02 | CARRIER BOARD INTERFACE |
| 03 | ETHERNET |
| 04 | USB |
| 05 | PCIe , SATA |
| 06 | JTAG, 100 MIL CONN |
| 07 | CSI, CAN, GPIO EXP |
| 08 | UART, RS232, RS485, EEPROM, SD |
| 09 | POWER |
| 10 | MIPI-DSI |
| 11 | DISPLAYPORT DUAL MODE |
| 12 | LVDS 2CH DISPLAY |
| 13 | AUDIO |
| 14 | HDMI_RX |
| 15 | MECHANICS |

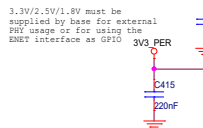
Power Diagram



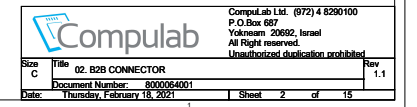
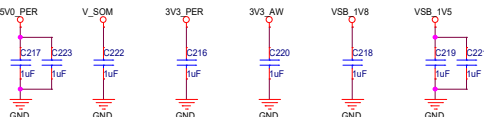
Block Diagram



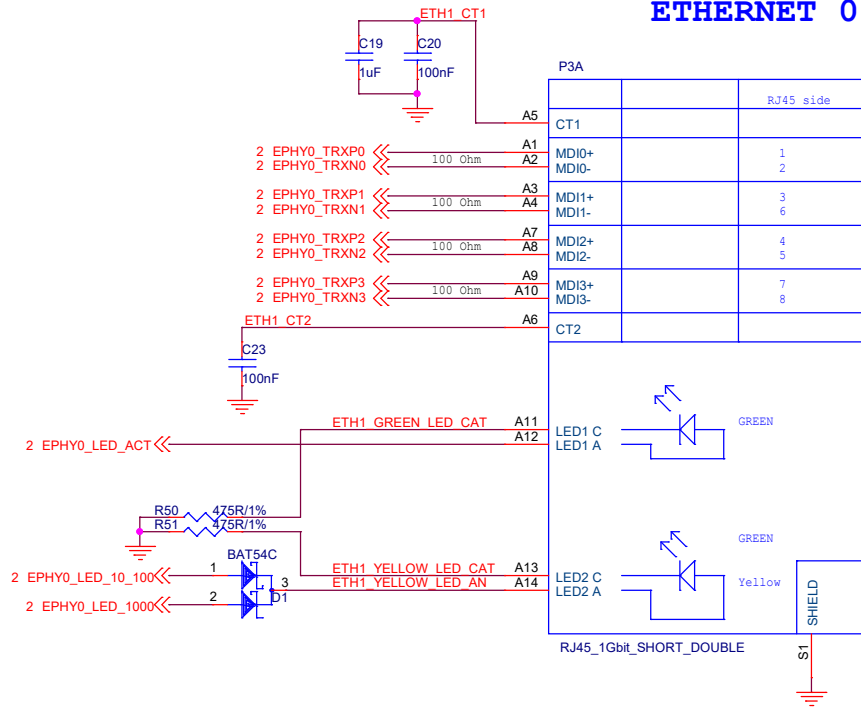
CARRIER BOARD INTERFACE



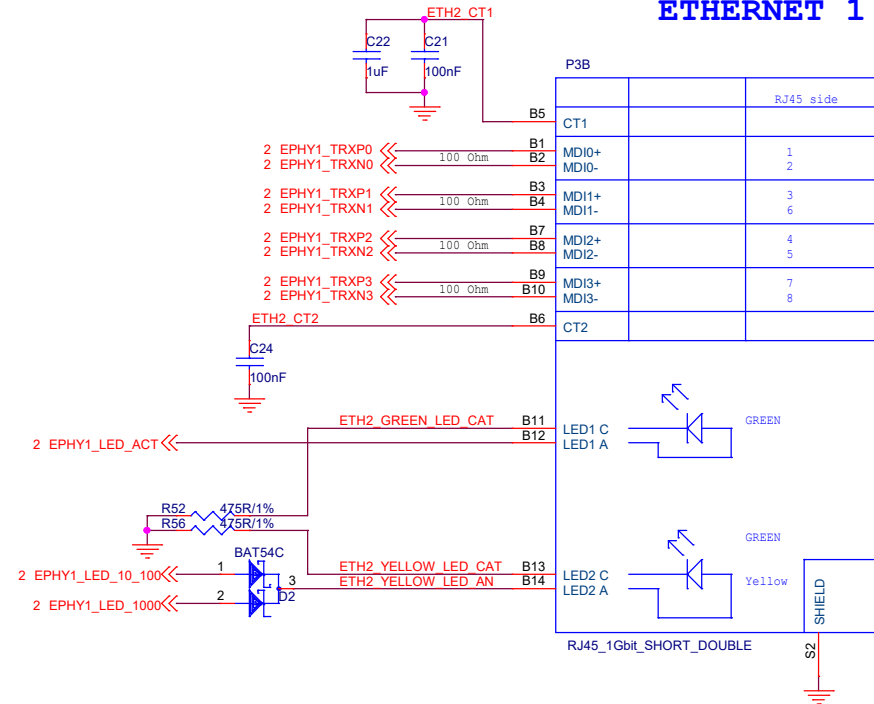
PLANE STITCHING CAPACITORS



ETHERNET 0



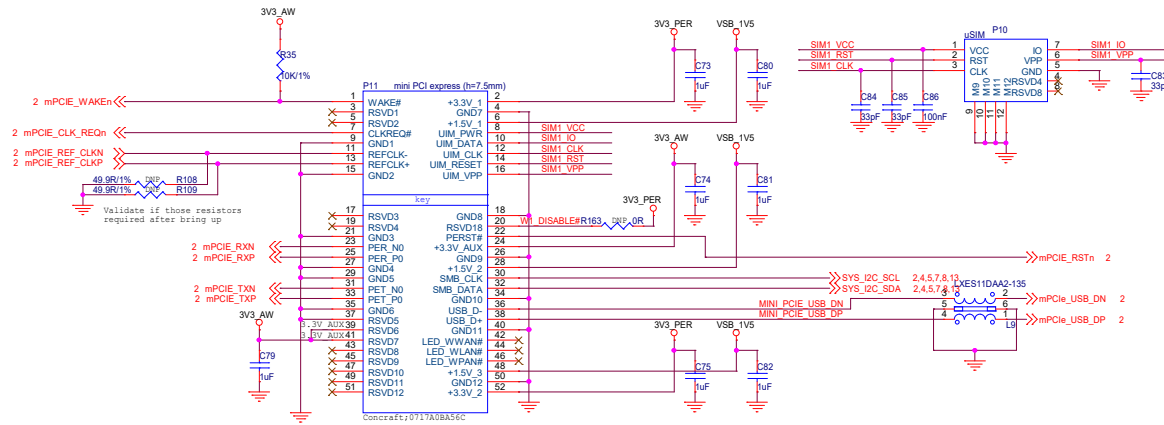
ETHERNET 1



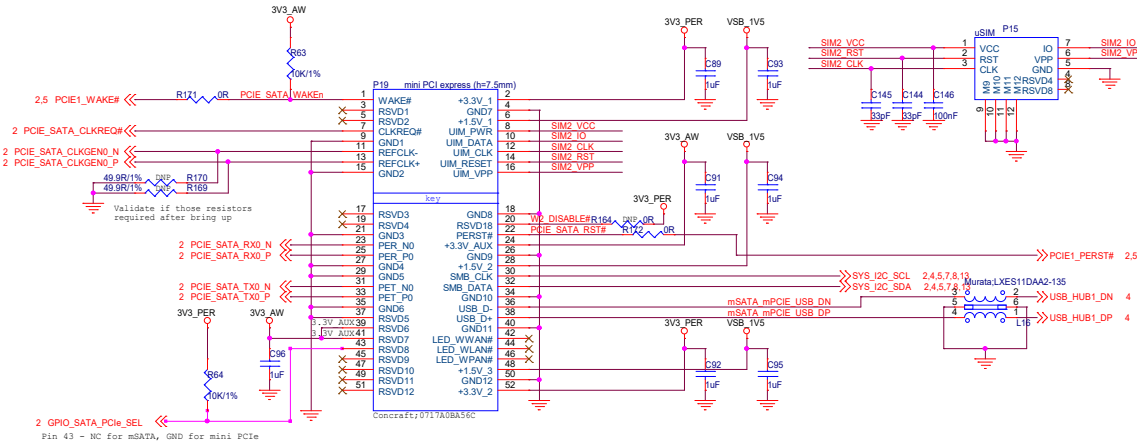
Layout notes

- 1: 100ohm differential impedance control.
- 2: Match each differential signals pair ± 5 mils.
- 3: Not more than two vias on each differential trace
- 4: GND stitching VIA near every signal VIA
- 5: The spacing between differential pair signals and other signals should be at least three times the trace width.

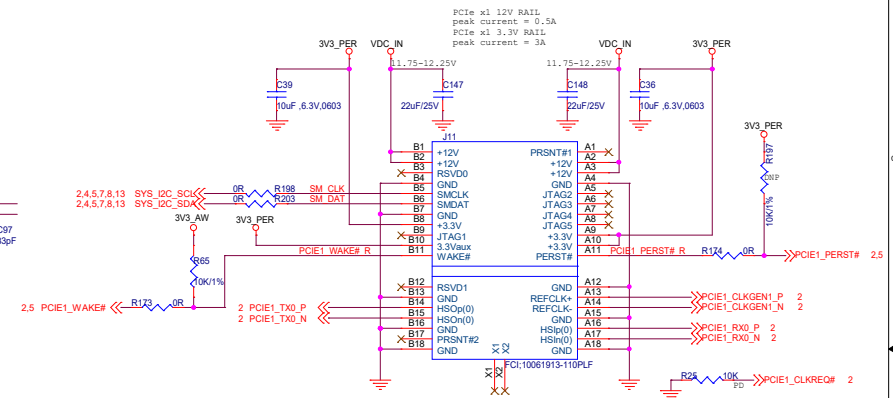
mini PCIe & SIM



mSATA / mini PCIe & SIM

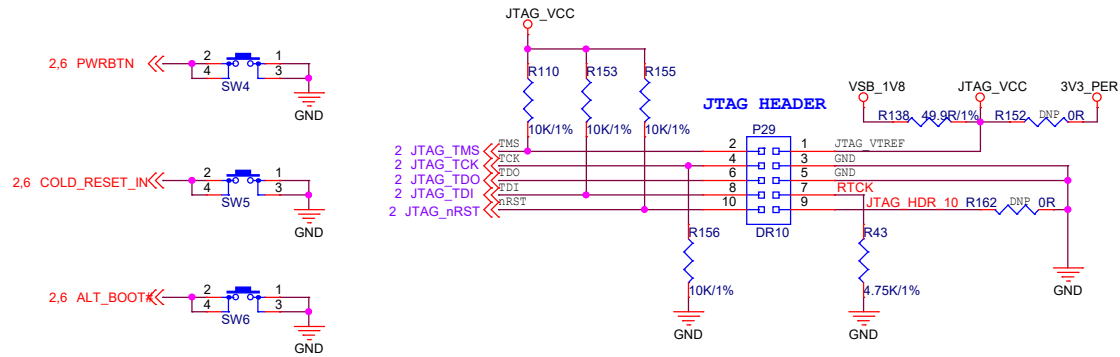


PCIe X1 SLOT



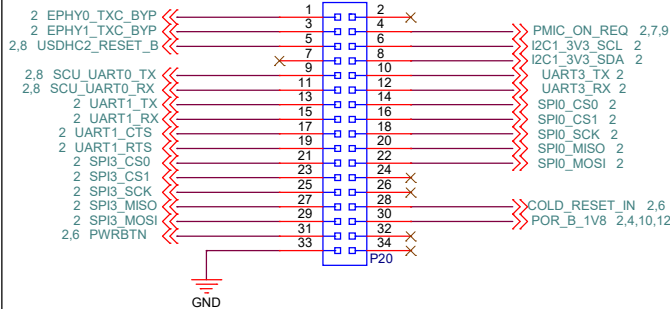
| | | |
|-----------------|-----------------------------|---------------|
| Title | | |
| 05. PCIe , SATA | | |
| Size | Document Number | Rev |
| C | <Doc> | 1.1 |
| Date: | Thursday, February 18, 2021 | Sheet 5 of 15 |

POWER/RESET/BOOT SWITCHES & JTAG



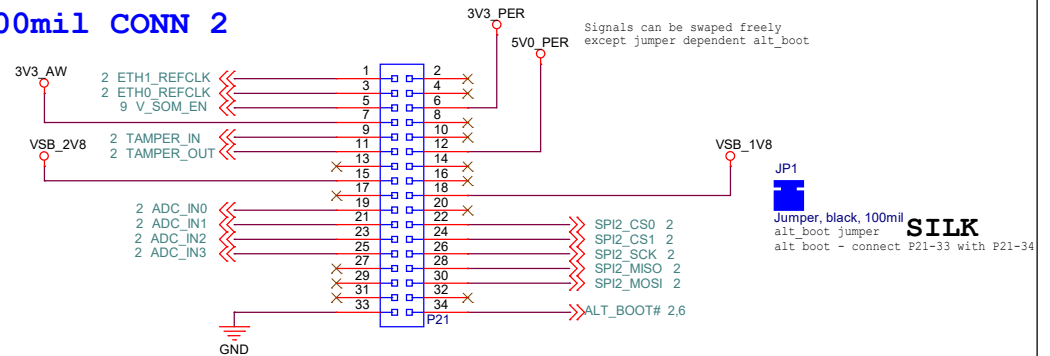
100mil CONN 1

Signals can be swapped freely



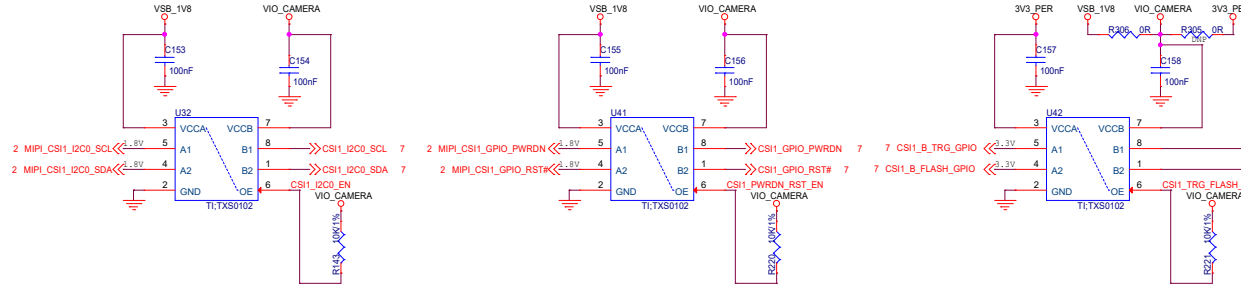
100mil CONN 2

Signals can be swapped freely except jumper dependent alt_boot

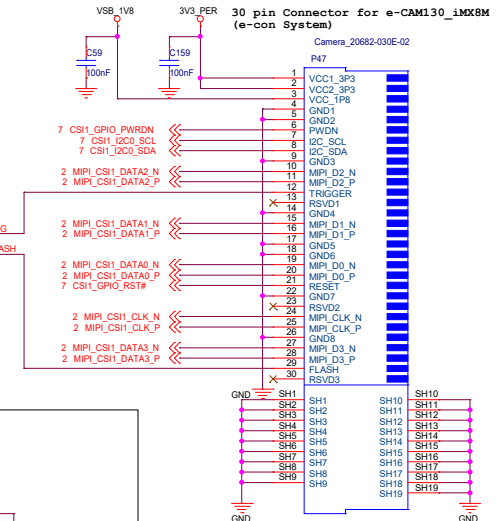
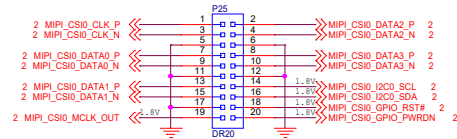


- Layout notes for PCIe and LVDS signals
- 1: 100ohm differential impedance control for LVDS, 85ohm for PCIe.
 - 2: Match each differential signals pair ± 5 mils.
 - 3: Not more than two vias on each differential trace
 - 4: GND stitching VIA near every signal VIA
 - 5: The spacing between differential pair signal and other signals should at least three times the trace width.

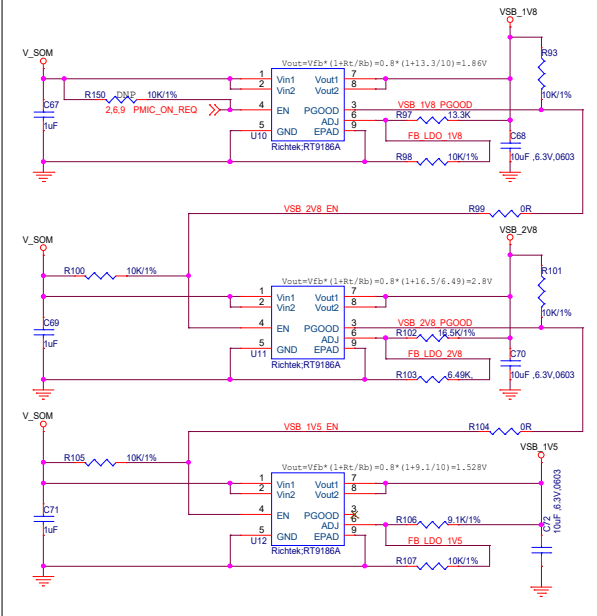
MIPI-CSI MODULE



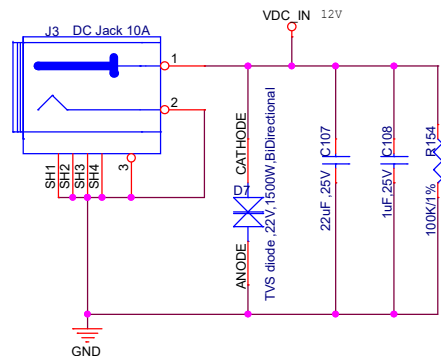
MIPI-CSI HEADER



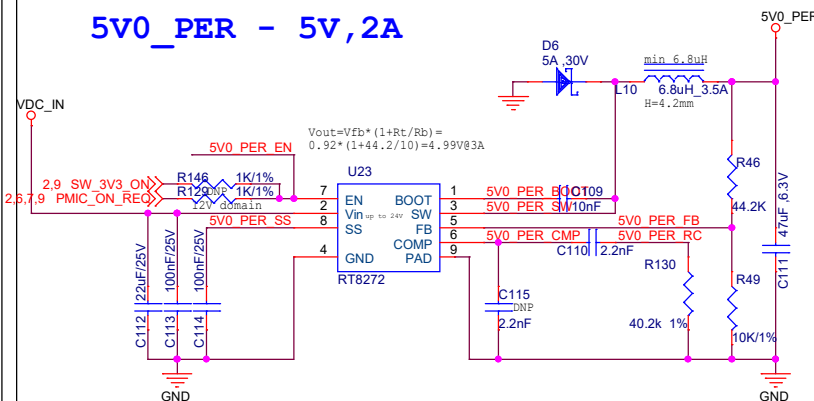
VSB_1V5, VSB_1V8 & VCC_2V8 CSI sources



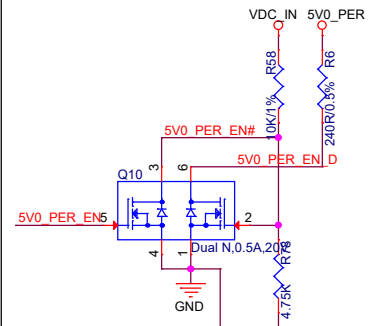
DC INPUT



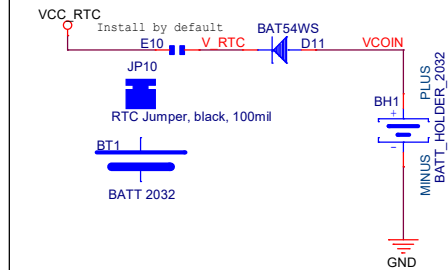
5V0_PER - 5V, 2A



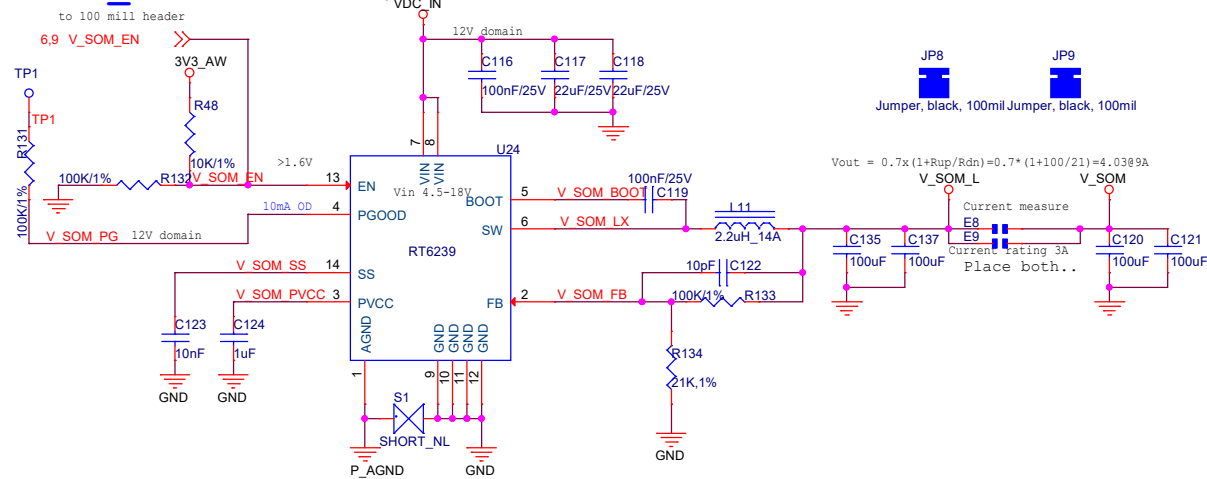
5V0_PER DISCHARGE



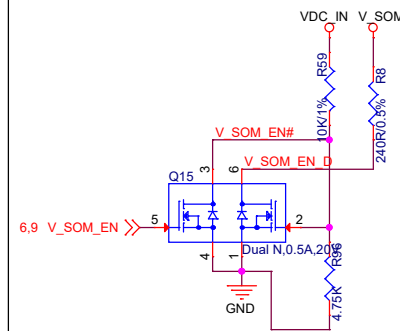
RTC BATTERY



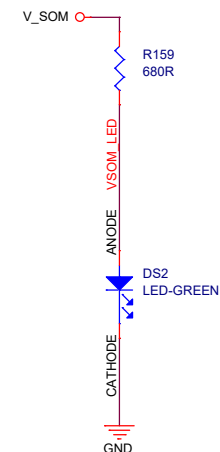
V_SOM - 4-5.5V, 8A



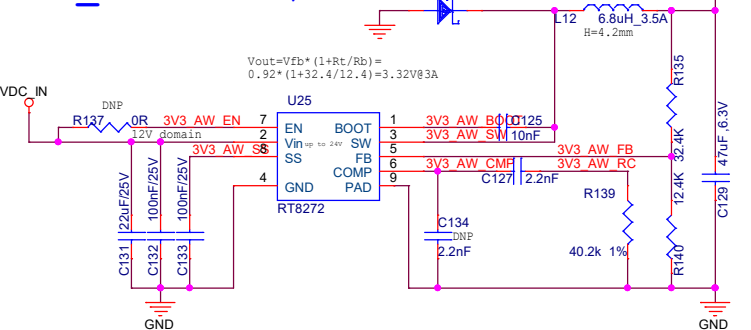
V_SOM DISCHARGE



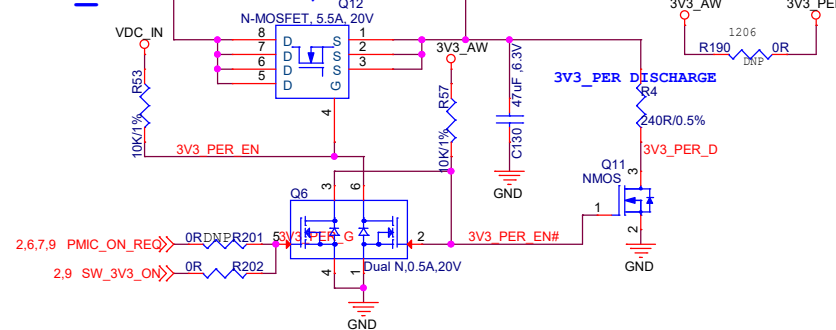
V_SOM LED



3V3_AW - 3.3V, 2.75A



3V3_PER - 3.3V, 2.75A

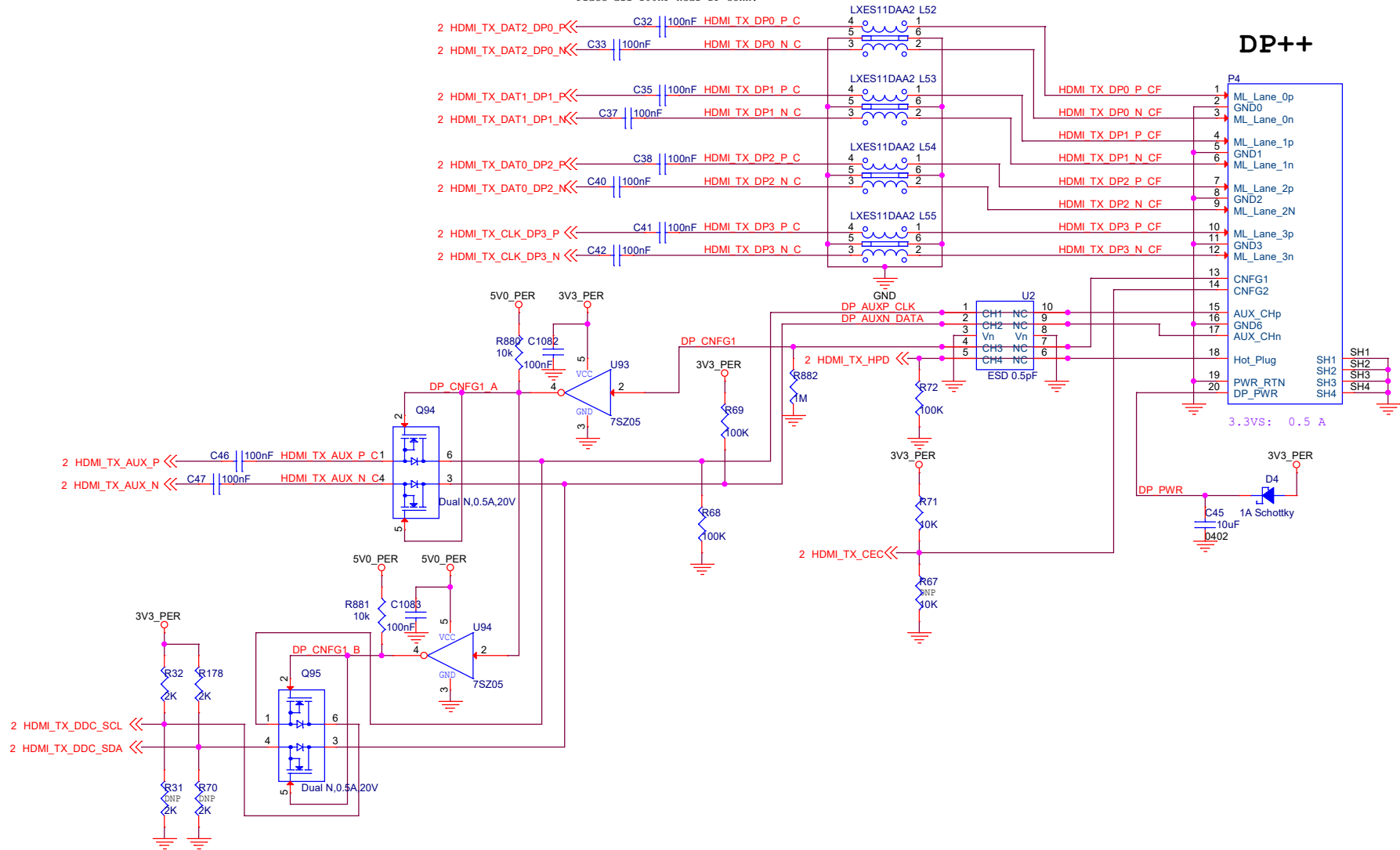


TFT

[illegible]

DISPLAYPORT DUAL MODE (DP++)

Place all 100nF near DP conn.



| | | | |
|------------------------------------|-----------------------------|-------|------------|
| | | | |
| Title 11. DISPLAYPORT DUAL MODE | | | |
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[illegible]

Touchscreen

I2C address: 0xBA/0xBB or 0x28/0x29

I2C for touchscreen

2 LVDS0_TS_SCL
2 LVDS0_TS_SDA

3V3_PER

R66 4.75K/1%

3V3_PER

R184 4.75K/1%

2 LVDS0_TS_INT
7 LVDS0_TS_INT_GPIO

7 LVDS0_TS_RESET
2,4,6,10 POR_B_1V8

3V3V

R251 0R LVDS0_FPC_GND
R256 0R LVDS0_FPC_VDDIO
R230 0R LVDS0_FPC_VDD
R246 0R LVDS0_FPC_SCL
R248 0R LVDS0_FPC_SDA
R247 0R LVDS0_FPC_INT
R252 0R

R249 0R LVDS0_FPC_RES#
R253 0R

GND

R250 0R LVDS0_FPC8_GND

P48

1
2
3
4
5
6
7
8

FPC_Connector_8

LVDS0_FPC_SDA
LVDS0_FPC_SCL
LVDS0_FPC_INT
LVDS0_FPC_RES#

6
4
3
2

LVDS0_FPC_VDD
VBUS GND

2 LVDS0_FPC_GND

IP4220CZ6 U36

Typical LED configuration: Two parallel chains of 6 serially connected LEDs

2 LVDS0_BL_PWM << R213 0R

7 LVDS0_LED_GPI << R255 0R

LVDS0_LED EN 4

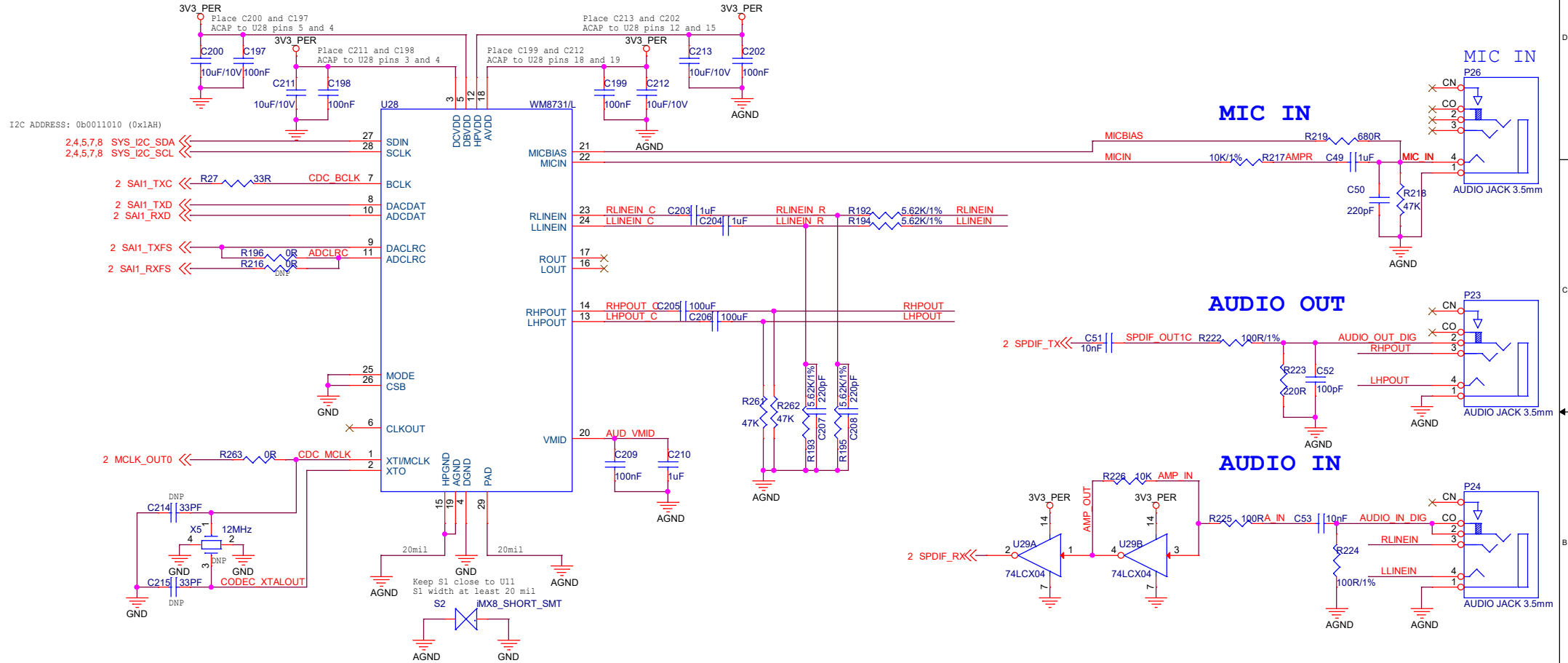
LVDS0_LED A

LVDS0_LED K

Conn., W2B, 2x1

| | | | |
|----------------------|-----------------------------|-------|------------|
| Title | | | |
| 12. LVDS 2CH DISPLAY | | | |
| Size B | Document Number <Doc> | | Rev 1.1 |
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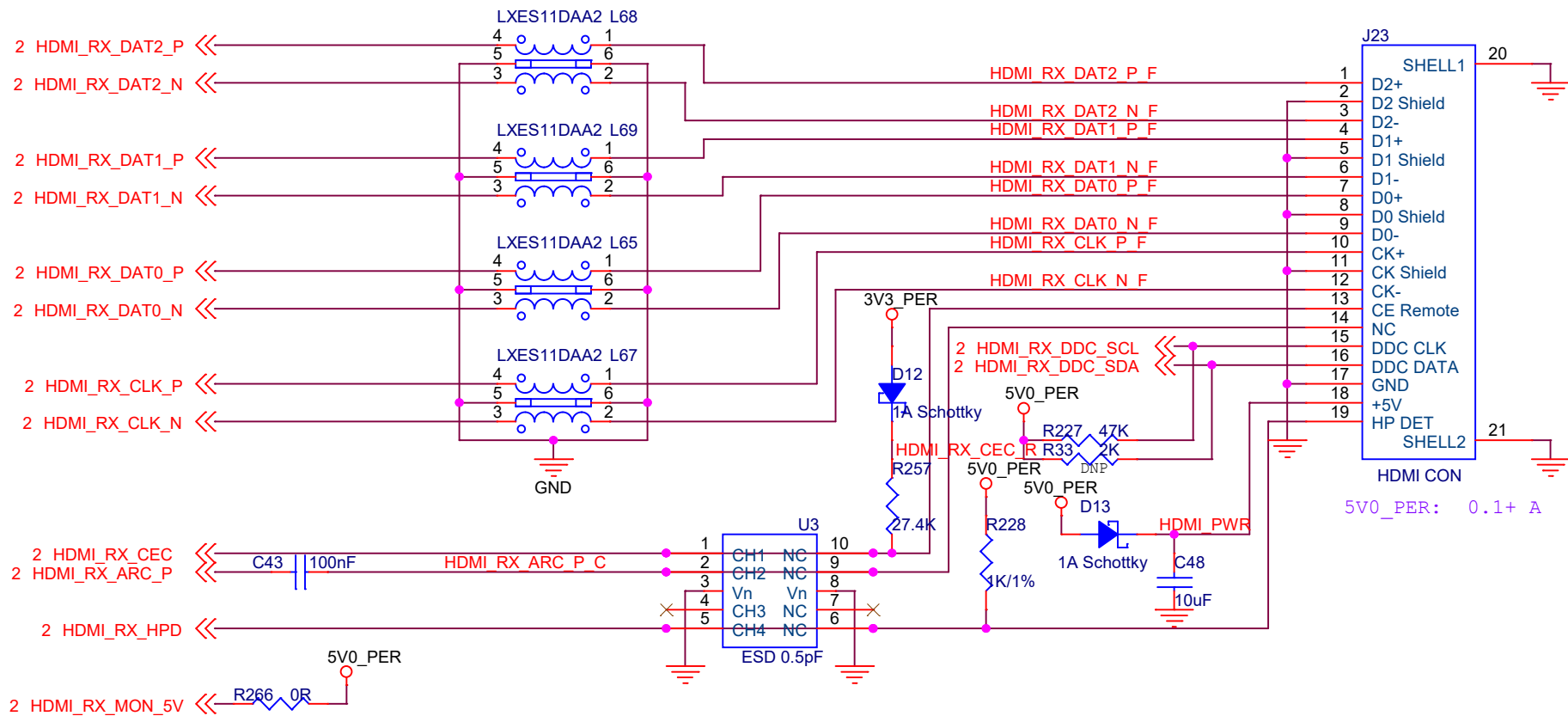
CODEC



| | | |
|-----------|-----------------------------|----------------|
| Title | | |
| 13. AUDIO | | |
| Size | Document Number | Rev |
| B | <Doc> | 1.1 |
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HDMI RX

HDMI

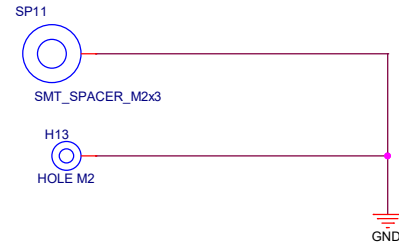


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|-------------|-----------------------------|----------------|
| Title | | |
| 14. HDMI_RX | | |
| Size | Document Number | Rev |
| A | <Doc> | 1.1 |
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mPCIe SPACER



mSATA/mPCIe SPACER



SB-iMX8MAX SPACERS

