CL-SOM-iMX8Plus

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
April 2022	• Initial release
June 2022	• Fixed USB signal naming in table #19 • Fixed UART3_RX, UART3_TX pin-out availability on pin #95 in table #24
March 2023	• Fixed function names of pins 80, 167, 193 in table #43
April 2023	• Fixed pin functions of pins 26 and 30 in table #43 • Fixed UART channel number of pin 65 in table #43 • Fixed I2C channel of pin 72 in table #43 • SAI5 port has been removed from list of available interfaces Tables #41 and #43 have been updated accordingly
October 2023	• Updated function description of pins 3 and 5 • Updated chapter 4.15 – removed SPI1 • Updated chapter 4.18 0 removed GPIO5_IO16 and GPIO5_IO17
January 2024	• Fixed pin numbering of LVDS1_D0_P in table #8 • Fixed LVDS pin naming in table #41
January 2026	• Fixed SoC pin names for pins 81, 93, 95, 99 • Corrected availability of I2C1

Please check for a newer revision of this manual at the CompuLab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX8Plus System-on-Module.

1.2 CL-SOM-iMX8Plus Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-iMX8Plus part number: https://www.compulab.com/products/computer-on-modules/cl-som-imx8plus-nxp-i-mx-8m-plus-system-on-module-computer/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX8Plus Developer Resources	https://www.compulab.com/products/computer-on-modules/cl-som-imx8plus-nxp-i-mx-8m-plus-system-on-module-computer/#devres
i.MX8M Plus Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation_Tab
i.MX8M Plus Datasheet	

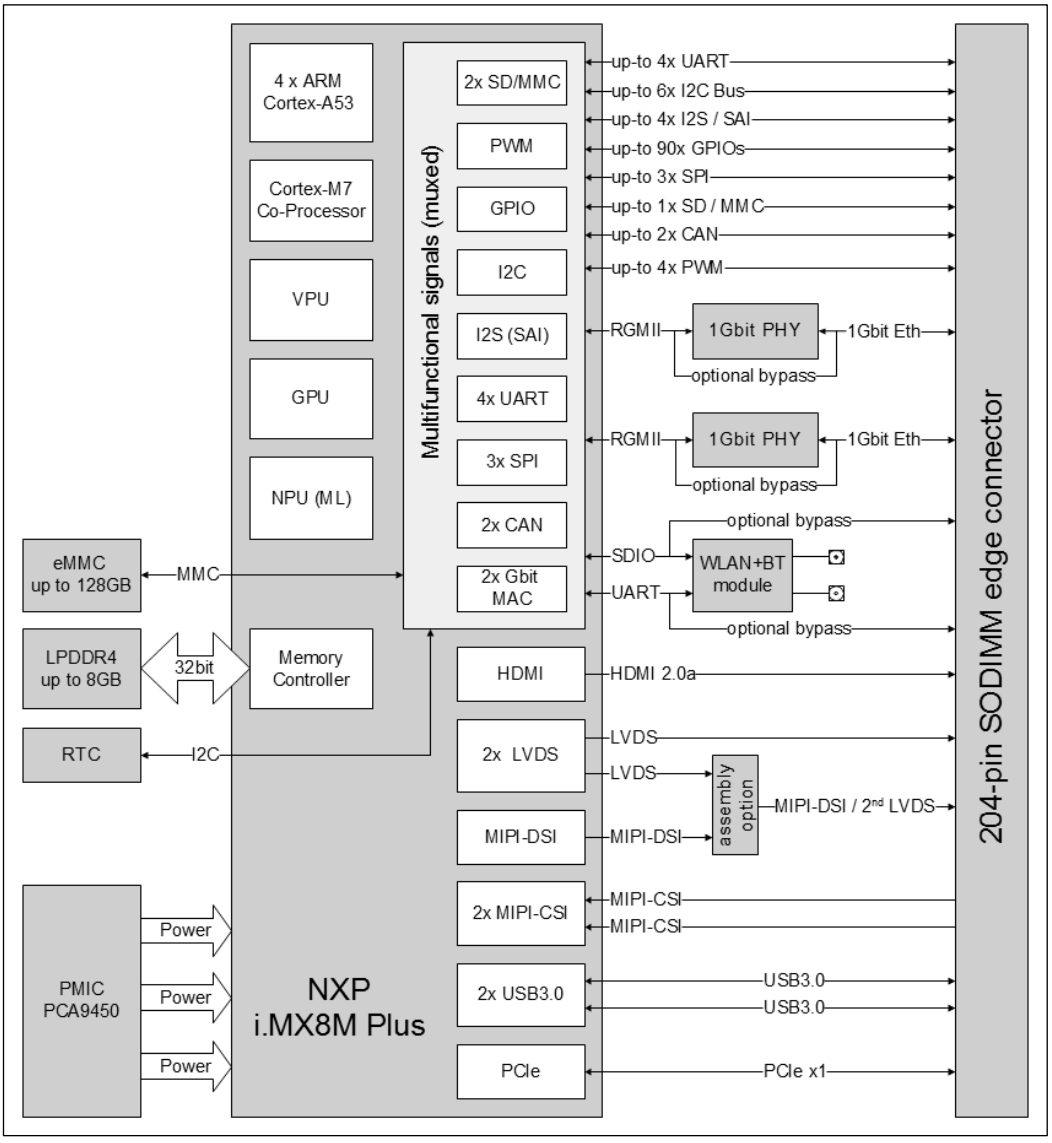
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Plus Processor, up-to 1.8GHz
- Up to 8GB LPDDR4 and 128GB eMMC
- 2D/3D GPU, 1080p VPU and audio DSP
- Integrated AI/ML Neural Processing Unit
- HDMI, LVDS, MIPI-DSI
- 2x MIPI-CSI camera inputs with dedicated ISP
- PCIe, 2x GbE / RGMII, 2x USB3.0
- 2x CAN, 4x UART, 3x SPI, 90x GPIO

2.2 Block Diagram

Figure 1 CL-SOM-iMX8Plus Block Diagram



2.3 CL-SOM-iMX8Plus Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.6GHz, industrial temp. grade	C1600QM
	NXP i.MX8M Plus QuadLite, quad-core ARM Cortex-A53, 1.8GHz	C1800Q
Video Decode	1080p60 HEVC/H.265, AVC/H.264, VP9, VP8	C1800QM or C1600QM
Video Encode	1080p60 HEVC/H.265, AVC/H.264	
GPU	GC7000UL (3D): OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.1/1.2; GC520L (2D): DirectFB, GDI/DirectDraw	+
NPU	AI/ML Neural Processing Unit, up to 2.3 TOPS	C1800QM or C1600QM
DSP	Tensilica® HiFi 4 DSP	
Real-Time Co-processor	ARM Cortex-M7, 800Mhz	+
Memory and Storage		
RAM	1GB – 8GB, LPDDR4	D
Storage	eMMC flash, 16GB - 128GB	N
Display, Audio and Camera		
Display	HDMI 2.0a, up to 1080p60	+
	Single-channel LVDS, up to 1366x768	+
	Dual-channel LVDS, up to 1080p60	L2
	MIPI-DSI, 4 data lanes, up to 1080p60	not L2
Touchscreen	Capacitive touch-screen support through eSPI and I2C interfaces	+
Digital Audio	Up-to 4x I2S / SAI	+
	S/PDIF input/output	+
Camera	2x MIPI-CSI, 4 data lanes	+
Network		
Ethernet	1x Gigabit Ethernet port (MAC+PHY)	E1
	2x Gigabit Ethernet ports (MAC+PHY)	E2
	Up-to 2x RGMII	not E1/E2
WiFi	Certified 802.11ac WiFi NXP 88W8997 chipset	WB
Bluetooth	Bluetooth 5.0 BLE	
I/O		
PCI Express	PCIe Gen. 3.0 x1	+
USB	2x USB3.0 (one host, one dual-role)	+
UART	Up to 4x UART	+
CAN bus	Up-to 2x CAN	+
MMC/SD/SDIO	Up to 2x SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 5x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 90x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

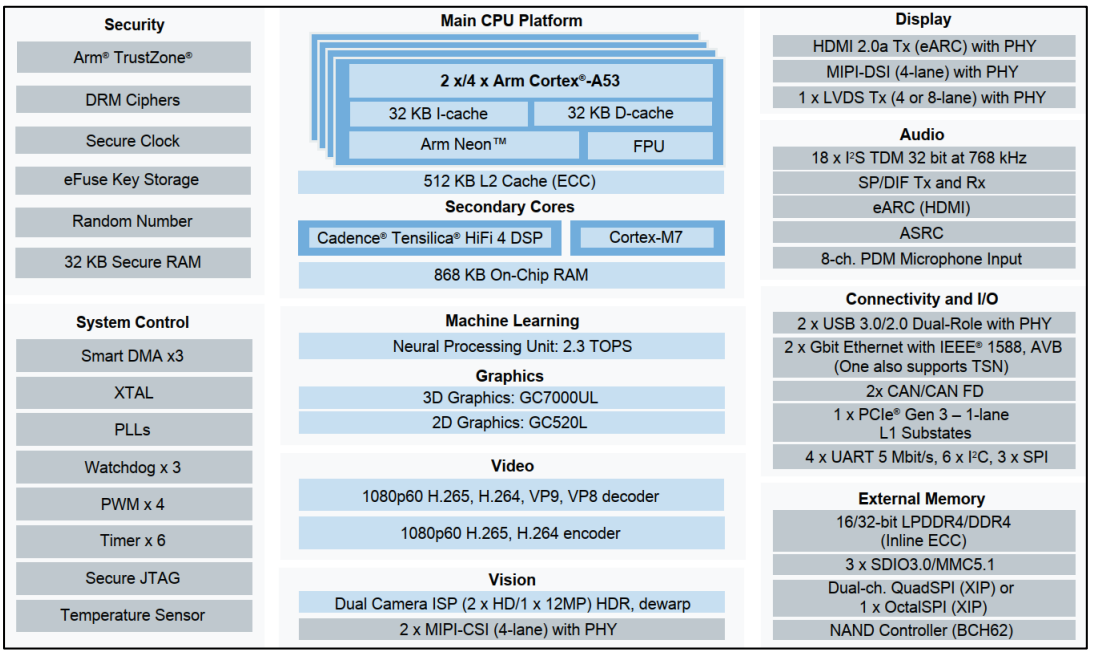
Electrical Specifications	
Supply Voltage	3.45V to 4.4V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	36 x 68 x 5 mm
Weight	12 gram
Connectors	204-pin SO-DIMM edge connector
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C - only with C1600QM
	Industrial: -40° to 85° C - only with C1600QM
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Plus SoC

The i.MX8M Plus family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M7 core processor enables low-power processing.

Figure 2 i.MX8M Plus Block Diagram



3.2 Memory

3.2.1 DRAM

CL-SOM-iMX8Plus is equipped with up to 8GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

CL-SOM-iMX8Plus uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

CL-SOM-iMX8Plus implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the carrier-board connector:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-iMX8Plus SoM. The availability restrictions of each signal are described in the “Signals description” table for each interface.
- Some of the CL-SOM-iMX8Plus carrier board interface pins are multifunctional. Up to 6 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.5.
- All of the CL-SOM-iMX8Plus digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#” –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **“Type” –** Signal type, see the definition of different signal types below
- **“Description” –** Signal description with regards to the interface in question.
- **“Availability” –** Depending on CL-SOM-iMX8Plus configuration options, certain carrier board interface pins are physically disconnected (floating). The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **"O"** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **"PD" -** Always pulled down onboard CL-SOM-iMX8Plus, followed by pull value
- **"PU" -** Always pulled up onboard CL-SOM-iMX8Plus, followed by pull value
- **“LVDS” -** Low-voltage differential signaling

4.1 HDMI

The CL-SOM-iMX8Plus HDMI interface is implemented with the HDMI interface of the i.MX8M Plus SoC. It supports the following main features:

- Compliant with HDMI 2.0a
- HDMI 2.1 eARC
- Supports display resolutions of up-to 1080p60

The following table summarizes the HDMI interface signals.

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description	Availability
HDMI_TXCN	155	AO	Negative part of HDMI clock diff-pair	Always available
HDMI_TXCP	157	AO	Positive part of HDMI clock diff-pair	Always available
HDMI_TX0N	137	AO	Negative part of HDMI data diff-pair 0	Always available
HDMI_TX0P	139	AO	Positive part of HDMI data diff-pair 0	Always available
HDMI_TX1N	143	AO	Negative part of HDMI data diff-pair 1	Always available
HDMI_TX1P	145	AO	Positive part of HDMI data diff-pair 1	Always available
HDMI_TX2N	161	AO	Negative part of HDMI data diff-pair 2	Always available
HDMI_TX2P	163	AO	Positive part of HDMI data diff-pair 2	Always available
HDMI_DDC_SCL	147*	O	VESA Data Display Channel clock	Always available
HDMI_DDC_SDA	149*	IO	VESA Data Display Channel data signal	Always available
HDMI_HPD	151*	AO	Hot Plug Detect	Always available
HDMI_CEC	153*	O	Consumer Electronics Control signal	Always available
EARC_N_HPD	129	AO		Always available
EARC_P_UTIL	135	AO		Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.2 MIPI-DSI Interface

The CL-SOM-iMX8Plus MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Plus SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals

Table 6 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
DSI_CKN	35	AO	Negative part of MIPI-DSI clock diff-pair	Only without ‘L2' option
DSI_CKP	33	AO	Positive part of MIPI-DSI clock diff-pair	Only without ‘L2' option
DSI_DN0	41	AO	Negative part of MIPI-DSI data diff-pair 0	Only without ‘L2' option
DSI_DP0	49	AO	Positive part of MIPI-DSI data diff-pair 0	Only without ‘L2' option
DSI_DN1	47	AO	Negative part of MIPI-DSI data diff-pair 1	Only without ‘L2' option
DSI_DP1	45	AO	Positive part of MIPI-DSI data diff-pair 1	Only without ‘L2' option
DSI_DN2	53	AO	Negative part of MIPI-DSI data diff-pair 2	Only without ‘L2' option

Signal Name	Pin #	Type	Description	Availability
DSI_DP2	51	AO	Positive part of MIPI-DSI data diff-pair 2	Only without ‘L2' option
DSI_DN3	59	AO	Negative part of MIPI-DSI data diff-pair 3	Only without ‘L2' option
DSI_DP3	57	AO	Positive part of MIPI-DSI data diff-pair 3	Only without ‘L2' option

NOTE: MIPI-DSI interface is available only without “L2” configuration option.

4.3 LVDS Interface

The CL-SOM-iMX8Plus provides up-to two LVDS interface derived from the i.MX8M Plus LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366x768p60

The following tables summarize the LVDS interface signals.

Table 7 LVDS0 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS0_CLK_N	104	AO	Negative part of LVDS clock diff-pair	Always available
LVDS0_CLK_P	106	AO	Positive part of LVDS clock diff-pair	Always available
LVDS0_D0_N	110	AO	Negative part of LVDS data diff-pair 0	Always available
LVDS0_D0_P	112	AO	Positive part of LVDS data diff-pair 0	Always available
LVDS0_D1_N	92	AO	Negative part of LVDS data diff-pair 1	Always available
LVDS0_D1_P	94	AO	Positive part of LVDS data diff-pair 1	Always available
LVDS0_D2_N	98	AO	Negative part of LVDS data diff-pair 2	Always available
LVDS0_D2_P	100	AO	Positive part of LVDS data diff-pair 2	Always available
LVDS0_D3_N	116	AO	Negative part of LVDS data diff-pair 3	Always available
LVDS0_D3_P	118	AO	Positive part of LVDS data diff-pair 3	Always available

Table 8 LVDS1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
LVDS1_CLK_N	35	AO	Negative part of LVDS clock diff-pair	Only with 'L2' option
LVDS1_CLK_P	33	AO	Positive part of LVDS clock diff-pair	Only with 'L2' option
LVDS1_D0_N	41	AO	Negative part of LVDS data diff-pair 0	Only with 'L2' option
LVDS1_D0_P	39	AO	Positive part of LVDS data diff-pair 0	Only with 'L2' option
LVDS1_D1_N	47	AO	Negative part of LVDS data diff-pair 1	Only with 'L2' option
LVDS1_D1_P	45	AO	Positive part of LVDS data diff-pair 1	Only with 'L2' option
LVDS1_D2_N	53	AO	Negative part of LVDS data diff-pair 2	Only with 'L2' option
LVDS1_D2_P	51	AO	Positive part of LVDS data diff-pair 2	Only with 'L2' option
LVDS1_D3_N	59	AO	Negative part of LVDS data diff-pair 3	Only with 'L2' option
LVDS1_D3_P	57	AO	Positive part of LVDS data diff-pair 3	Only with 'L2' option

NOTE: LVDS1 interface is available only with “L2” configuration option.

4.4 Camera Serial Interface

CL-SOM-iMX8Plus provides two MIPI-CSI interfaces, both derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Plus SoC with dedicated Image Signal Processor (ISP). The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Image Signal Processor (ISP):
  - Input formats: YCbCr420, YCbCr422, RAW8/10/12/14, RGB444/555/565/666/888
  - Image cropping, de-noising, LS and CA lens correction, AWB

Please refer to the i.MX8M Plus Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 8 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description	Availability
MIPI_CSI1 _CLK_N	184	AI	Negative part of MIPI-CSI1 clock diff-pair	Always available
MIPI_CSI1 _CLK_P	182	AI	Positive part of MIPI-CSI1 clock diff-pair	Always available
MIPI_CSI1_D0_N	23	AI	Negative part of MIPI-CSI1 data diff-pair 0	Always available
MIPI_CSI1_D0_P	21	AI	Positive part of MIPI-CSI1 data diff-pair 0	Always available
MIPI_CSI1_D1_N	29	AI	Negative part of MIPI-CSI11 data diff-pair 1	Always available
MIPI_CSI1_D1_P	27	AI	Positive part of MIPI-CSI1 data diff-pair 1	Always available
MIPI_CSI1_D2_N	17	AI	Negative part of MIPI-CSI1 data diff-pair 2	Always available
MIPI_CSI1_D2_P	15	AI	Positive part of MIPI-CSI1 data diff-pair 2	Always available
MIPI_CSI1_D3_N	9	AI	Negative part of MIPI-CSI1 data diff-pair 3	Always available
MIPI_CSI1_D3_P	7	AI	Positive part of MIPI-CSI1 data diff-pair 3	Always available
MIPI_CSI2 _CLK_N	83	AI	Negative part of MIPI-CSI2 clock diff-pair	Always available
MIPI_CSI2 _CLK_P	85	AI	Positive part of MIPI-CSI2 clock diff-pair	Always available
MIPI_CSI2_D0_N	89	AI	Negative part of MIPI-CSI2 data diff-pair 0	Always available
MIPI_CSI2_D0_P	91	AI	Positive part of MIPI-CSI2 data diff-pair 0	Always available
MIPI_CSI2_D1_N	107	AI	Negative part of MIPI-CSI21 data diff-pair 1	Always available
MIPI_CSI2_D1_P	109	AI	Positive part of MIPI-CSI2 data diff-pair 1	Always available
MIPI_CSI2_D2_N	113	AI	Negative part of MIPI-CSI2 data diff-pair 2	Always available
MIPI_CSI2_D2_P	115	AI	Positive part of MIPI-CSI2 data diff-pair 2	Always available
MIPI_CSI2_D3_N	119	AI	Negative part of MIPI-CSI2 data diff-pair 3	Always available
MIPI_CSI2_D3_P	121	AI	Positive part of MIPI-CSI2 data diff-pair 3	Always available

4.5 Ethernet

CL-SOM-iMX8Plus incorporates up-to two optional 10/100/1000 Ethernet interfaces, implemented with the i.MX8M Plus MACs coupled with two optional onboard GbE PHYs.

4.5.1 Gigabit Ethernet

CL-SOM-iMX8Plus with onboard AR8033 PHY(s) ("E1" and "E2" configuration options) supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant.
- IEEE 802.3u compliant Auto-Negotiation.
- Supports all IEEE 1588 frames - inside the MAC.
- Automatic channel swap (ACS).
- Automatic MDI/MDIX crossover.
- Automatic polarity correction.
- Activity and speed indicator LED controls.

The following tables summarize the GbE interface signals.

Table 9 Ethernet 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH1_LED_ACT	4^	IO;PD8K2	Active High, activity LED driver. 2.5V signal, PHY strap	Only with 'E1' or 'E2' option
ETH1_LINK-LED_10_100	22	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	Only with 'E1' or 'E2' option
ETH1_LINK-LED_1000	16^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal, PHY strap	Only with 'E1' or 'E2' option
ETH1_MDI0N	6	AIO	Negative part of 100ohm diff-pair 0	Only with 'E1' or 'E2' option
ETH1_MDI0P	8	AIO	Positive part of 100ohm diff-pair 0	Only with 'E1' or 'E2' option
ETH1_MDI1N	12	AIO	Negative part of 100ohm diff-pair 1	Only with 'E1' or 'E2' option
ETH1_MDI1P	14	AIO	Positive part of 100ohm diff-pair 1	Only with 'E1' or 'E2' option
ETH1_MDI2N	18	AIO	Negative part of 100ohm diff-pair 2	Only with 'E1' or 'E2' option
ETH1_MDI2P	20	AIO	Positive part of 100ohm diff-pair 2	Only with 'E1' or 'E2' option
ETH1_MDI3N	24	AIO	Negative part of 100ohm diff-pair 3	Only with 'E1' or 'E2' option
ETH1_MDI3P	26	AIO	Positive part of 100ohm diff-pair 3	Only with 'E1' or 'E2' option

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.

Table 10 Ethernet 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ETH2_LED_ACT	25^	IO;PD8K2	Active High, activity LED driver. 2.5V signal, PHY strap	Only with 'E2' option
ETH2_LINK-LED_10_100	34	IO	Active High, 10/100Mbps link LED driver. 2.5V signal	Only with 'E2' option
ETH2_LINK-LED_1000	40^	IO; PD	Active High, 1Gbps link LED driver. 2.5V signal, PHY strap	Only with 'E2' option
ETH2_MDI0N	30	AIO	Negative part of 100ohm diff-pair 0	Only with 'E2' option
ETH2_MDI0P	32	AIO	Positive part of 100ohm diff-pair 0	Only with 'E2' option
ETH2_MDI1N	36	AIO	Negative part of 100ohm diff-pair 1	Only with 'E2' option

Signal Name	Pin #	Type	Description	Availability
ETH2_MDI1P	38	AIO	Positive part of 100ohm diff-pair 1	Only with 'E2' option
ETH2_MDI2N	42	AIO	Negative part of 100ohm diff-pair 2	Only with 'E2' option
ETH2_MDI2P	44	AIO	Positive part of 100ohm diff-pair 2	Only with 'E2' option
ETH2_MDI3N	48	AIO	Negative part of 100ohm diff-pair 3	Only with 'E2' option
ETH2_MDI3P	50	AIO	Positive part of 100ohm diff-pair 3	Only with 'E2' option

NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM

4.5.2 RGMII

When assembled without on-board PHY(s) (“E1” and “E2” configuration options) CL-SOM-iMX8Plus provides up-to two RMGII interfaces.

Primary RGMII interface ENET1 is available only when CL-SOM-iMX8Plus is assembled without “E1” and E2” configuration options.

Secondary RGMII interface ENET2 is available only when CL-SOM-iMX8Plus is assembled without E2” configuration option.

The following tables summarize the Ethernet RGMII interface signals.

Table 11 Primary RGMII ENET1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET_MDC	52*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Only w/o 'E1' and ‘E2’options
ENET_MDIO	97*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Only w/o 'E1' and ‘E2’options
ENET1_RD0	22*	I	Ethernet input data from the PHY	Only w/o 'E1' and ‘E2’options
ENET1_RD1	4*	I	Ethernet input data from the PHY	Only w/o 'E1' and‘E2’options
ENET1_RD2	26*	I	Ethernet input data from the PHY	Only w/o 'E1' and ‘E2’options
ENET1_RD3	24*	I	Ethernet input data from the PHY	Only w/o 'E1' and ‘E2’options
ENET1_RX_CTL	18*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	Only w/o 'E1' and ‘E2’options
ENET1_RXC	14*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Only w/o 'E1' and ‘E2’option
ENET1_TD0	16*	O	Ethernet output data to PHY	Only w/o 'E1' and ‘E2’option
ENET1_TD1	12*	O	Ethernet output data to PHY	Only w/o 'E1' and ‘E2’option
ENET1_TD2	62*	O	Ethernet output data to PHY	Only w/o 'E1' and ‘E2’option
ENET1_TD3	8*	O	Ethernet output data to PHY	Only w/o 'E1' and ‘E2’option
ENET1_TXC	20*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Only w/o 'E1' and‘E2’option
ENET1_TX_CTL	6*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Only w/o 'E1' and ‘E2’option
RGMII0_VIO1	102*	P	Power supply input for RGMII ENET1. This pin must be connected to external 1.8V power rail	Only w/o 'E1' and ‘E2’option

NOTE: 1.8V power must be supplied via pin RGMII_VIO1 if any of the RGMII ENET1 signals are used on the carrier-board

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 12 Secondary RGMII ENET2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET2_ MDC	54	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	Only w/o 'WB' and 'E2' options
ENET2_MDIO	56	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	Only w/o 'WB' and 'E2' options
ENET2_RD0	34*	I	Ethernet input data from the PHY	Only w/o 'E2'option
ENET2_RD1	25*	I	Ethernet input data from the PHY	Only w/o 'E2'option
ENET2_RD2	48*	I	Ethernet input data from the PHY	Only w/o 'E2'option
ENET2_RD3	50*	I	Ethernet input data from the PHY	Only w/o 'E2'option
ENET2_RX_CTL	42*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	Only w/o 'E2'option
ENET2_RXC	38*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	Only w/o 'E2'option
ENET2_TD0	40*	O	Ethernet output data to PHY	Only w/o 'E2'option
ENET2_TD1	36*	O	Ethernet output data to PHY	Only w/o 'E2'option
ENET2_TD2	128*	O	Ethernet output data to PHY	Only w/o 'E2'option
ENET2_TD3	32*	O	Ethernet output data to PHY	Only w/o 'E2'option
ENET2_TXC	44*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	Only w/o 'E2'option
ENET2_TX_CTL	30*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	Only w/o 'E2'option
RGMII0_VIO2	138	P	RGMII interface power supply input. This pin must be connected to 1.8V power rail	Only w/o 'E2'option

NOTE: 1.8V power must be supplied via pin RGMII_VIO2 if any of the RGMII ENET2 signals are used on the carrier-board

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 WiFi and Bluetooth Interfaces

CL-SOM-iMX8Plus provides optional 802.11ac WiFi and Bluetooth functions implemented with AzureWave AW-CM276NF certified WiFi module (NXP 88W8997 chipset).

AzureWave AW-CM276NF provides the following key features:

- IEEE 802.11 ac/a/b/g/n, Wi-Fi compliant
- IEEE 802.11i for advanced security
- Multiple power saving modes for low power consumption
- Quality of Service (QoS) support
- Bluetooth 5.0 complaint

The wireless module is interfaced with i.MX8M Plus SoC through the following interfaces:

- i.MX8M Plus SDIO1 is used for WiFi data
- i.MX8M Plus UART1 is used for Bluetooth data

The wireless module provides two on-board MHF4 antenna connectors:

- ANT_A – main WiFi antenna
- ANT_B – auxiliary WiFi / Bluetooth antenna

NOTE: WiFi and Bluetooth functions are available only with "WB" configuration option.

4.7 PCI-Express

SOM-iMX8M-Plus provides one PCI Express port.

Table 13 PCIE Interface Signals

Signal Name	Pin #	Type	Description	Availability
PCIE_REF_CLKN	101	AO	100 MHz PCIe reference clock differential output negative	Always available
PCIE_REF_CLKP	103	AO	100 MHz PCIe reference clock differential output positive	Always available
PCIE_RXN_N	133	I	PCI Express receive data negative	Always available
PCIE_RXN_P	131	I	PCI Express receive data positive	Always available
PCIE_TXN_N	127	O	PCI Express transmit data negative	Always available
PCIE_TXN_P	125	O	PCI Express transmit data positive	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Sony/Philips Digital Interface (S/PDIF)

CL-SOM-iMX8Plus provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 14 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_EXT_CLK	49* 193*	I	External clock signal	Always available
SPDIF_RX	24*	I	SPDIF input data line signal	Only w/o 'E1' and 'E2'options

Signal Name	Pin #	Type	Description	Availability
	90*			Always available
	197*			Always available
SPDIF_RX	43*	I	SPDIF input data line signal	Always available
SPDIF_TX	6*	O	SPDIF output data line signal	Only w/o 'E1' and 'E2'options
SPDIF_TX	31*	O	SPDIF output data line signal	Always available
	88*			
	187*			

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.9 Digital Audio (SAI)

CL-SOM-iMX8Plus enables access to three of the i.MX8M Plus integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Plus Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 15 SAI3 Interface Signals

Signal Name		Type	Description	Availability
SAI3_MCLK	187*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Always available
	192*			
SAI3_RXD0	201*	I	Receive data 0, sampled synchronously by the bit clock	Always available
SAI3_RXD1	197*	I	Receive data 1, sampled synchronously by the bit clock	Always available
SAI3_RXC	199*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_RXFS	197*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available
SAI3_TXD0	193*	O	Transmit data signal 0.Synchronous to bit clock.	Always available
SAI3_TXC	191*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Always available
SAI3_TXFS	189*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Always available

Table 16 SAI6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI6_MCLK	6*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o 'E1' and 'E2'options
	50*			Only w/o 'E2' option
SAI6_RXD0	25*	I		

Signal Name	Pin #	Type	Description	Availability
	26*		Receive data 0, sampled synchronously by the bit clock	Only w/o 'E1' and 'E2'options
	44*			Only w/o 'E2' option
	62*			Only w/o 'E1' and 'E2'option
SAI6_RXC	12*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Only w/o 'E1' and 'E2'options
	16*			Only w/o 'E1' and 'E2'options
SAI6_RXFS	30*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E2'option
	34*			Only w/o 'E2'option
	48*			Only w/o 'E2' option
SAI6_TXD0	25*	O	Transmit data signal 0.Synchronous to bit clock.	Always available
	26*			Only w/o 'E1' and 'E2'options
	44*			Always available
SAI6_TXC	8*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o 'E1' and 'E2'options
SAI6_TXFS	30*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E2'option
	97*			Only w/o 'E1' and 'E2'options
	36*			Only w/o 'E2'option
	48*			Always available

Table 18 SAI7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI7_MCLK	24*	IO	Audio master clock. An input when generated externally and an output when generated internally.	Only w/o 'E1' and 'E2'options
	152*			Always available
SAI7_RXD0	22*	I	Receive data, sampled synchronously by the bit clock	Only w/o 'E1' and 'E2'options
	99*			Always available
SAI7_RXC	95*	I	Receive bit clock. An input when generated externally and an output when generated internally.	Always available
SAI7_RXFS	4*	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E1' and 'E2'options
	93*			Always available
SAI7_TXD0	20*	O	Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word	Only w/o 'E1' and 'E2'options
	148*			Always available
SAI7_TXC	14*	O	Transmit bit clock. An input when generated externally and an output when generated internally.	Only w/o 'E1' and 'E2'options
	154*			Always available
SAI7_TXFS	18*	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	Only w/o 'E1' and 'E2'options
	81*			Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.10 USB

i.MX8M Plus SoC is equipped with two dual-role USB3.0 controllers and PHYs. One port supports dual-role functionality, while the second port is configured permanently for host mode.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the USB3.0 interface signals.

Table 17 USB (dual-role) port #1 Signals

Signal Name	Pin #	Type	Description	Availability
USB1_DN	178	IO	USB2.0 negative data	Always available
USB1_DP	176	IO	USB2.0 positive data	Always available
USB1_ID	174	I	USB1 OTG ID signal	Always available
USB1_VBUS_DET	180	I	USB1 VBUS detect	Always available
USB1_TX_N	198	AO	USB3.0 transmit negative lane	Always available
USB1_TX_P	200	AO	USB3.0 transmit positive lane	Always available
USB1_RX_N	188	AI	USB3.0 receive negative lane	Always available
USB1_RX_P	190	AI	USB3.0 receive positive lane	Always available

Table 18 USB (host) port #2 Signals

Signal Name	Pin #	Type	Description	Availability
USB2_DN	170	IO	USB2.0 negative data	Always available
USB2_DP	172	IO	USB2.0 positive data	Always available
USB2_VBUS_DET	196	I	USB2 VBUS detect	Always available
USB2_TX_N	158	AO	USB3.0 transmit negative lane	Always available
USB2_TX_P	160	AO	USB3.0 transmit positive lane	Always available
USB2_RX_N	164	AI	USB3.0 receive negative lane	Always available
USB2_RX_P	166	AI	USB3.0 receive positive lane	Always available

4.11 MMC / SD /SDIO

SOM-iMX8M-Plus features up-to two SD/SDIO ports. These ports are derived from the i.MX8M Plus SD/SDIO controllers uSDHC1 and uSDHC2. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.01 command/response sets and physical layer

Please refer to the i.MX8M Plus Reference manual for additional details.

The following tables summarize the MMC/SD/SDIO interface signals.

Table 19 SD/SDIO port #1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD1_CLK	54*	O	Clock for MMC/SD/SDIO card	Only w/o 'WB' option
SD1_CMD	56*	IO	CMD line connect to card	Only w/o 'WB' option
SD1_DATA0	58*	IO	DATA0 line in all modes. Also used to detect busy state	Only w/o 'WB' option
SD1_DATA1	60*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Only w/o 'WB' option
SD1_DATA2	69*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Only w/o 'WB' option
SD1_DATA3	66*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Only w/o 'WB' option
SD1_DATA4	68*	IO	DATA4 line in 8-bit mode	Always available
SD1_DATA5	70*	IO	DATA5 line in 8-bit mode	Always available
SD1_DATA6	72*	IO	DATA6 line in 8-bit mode	Always available
SD1_DATA7	62* 76*	IO	DATA7 line in 8-bit mode	Always available
SD1_WP	67*	I	Card write protect detection	Always available
SD1_RESET_B	130*	O	Card hardware reset signal, active LOW	Always available
SD1_STRB	74*	O	Input clock for eMMC HS400 mode	Always available

NOTE: SD/SDIO port #1 is only available without 'WB' configuration option

NOTE: SD/SDIO port #1 is pre-configured to operate only at 3.3V voltage levels

Table 20 SD/SDIO port #2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD2_CLK	80*	O	Clock for MMC/SD/SDIO card	Always available
SD2_CMD	82*	IO	CMD line connect to card	Always available
SD2_DATA0	84*	IO	DATA0 line in all modes. Also used to detect busy state	Always available
SD2_DATA1	86*	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	Always available
SD2_DATA2	88*	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	Always available
SD2_DATA3	90*	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	Always available
SD2_WP	67*	I	Card write protect detection	Always available
SD2_RESET_B	179*	O	Card hardware reset signal, active LOW	Always available
SD2_nCD	148*	I	Card detection pin	Always available

NOTE: SD/SDIO port #2 can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin GPIO1_IO04.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 UART

CL-SOM-iMX8Plus provides up-to four i.MX8M Plus universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Plus UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: By default UART2 is assigned to be used as the main system console port.

NOTE: By default UART4 is assigned to be used as the M7 core debug port.

Please refer to the i.MX8M Plus Reference manual for additional details.

The following tables summarize the UART interface signals.

Table 21 UART1 Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS_B	58*	O	UART-2 clear to send	Only w/o 'WB' option
	75*			Only w/o 'WB' option
	60*			Only w/o 'WB' option
	77*			Only w/o 'WB' option
	79*			Only w/o 'WB' option
UART1_RTS_B	58*	I	UART-2 request to send	Always available
	60*			Always available
	77*			Only w/o 'WB' option
	75*			Only w/o 'WB' option
UART1_RXD	54*	I	UART-2 serial data receive	Only w/o 'WB' option
	56*			Only w/o 'WB' option
	73*			Only w/o 'WB' option
	65*			Always available
	136*			Only w/o 'E2' option
UART1_TXD	54*	O	UART-2 serial data transmit	Only w/o 'WB' option
	56*			Only w/o 'WB' option
	73*			Only w/o 'WB' option
	65*			Always available
	136*			Only w/o 'E2' option

Table 22 UART2 Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS_B	11*	O	UART-2 clear to send	Always available
	68*			
	199*			
	13*			
	70*			
	201*			
UART2_RTS_B	11*	I	UART-2 request to send	Always available
	68*			
	199*			
	13*			
	70*			
	201*			
UART2_RXD	66*	I	UART-2 serial data receive	Only w/o 'WB' option
	69*			Only w/o 'WB' option
	111*			Always available
	117*			Always available
	84*			Always available
	189*			Always available
	86*			Always available
	91*			Always available
UART2_TXD	66*	O	UART-2 serial data transmit	Only w/o 'WB' option
	69*			Only w/o 'WB' option
	111*			Always available
	117*			Always available
	84*			Always available
	189*			Always available
	86*			Always available
	91*			Always available

Table 23 UART3 Signals

Signal Name	Pin #	Type	Description	Availability
UART3_CTS_B	74*	O	UART-3 clear to send	Always available
	99*			
	81*			
	130*			
UART3_RTS_B	74*	I	UART-3 request to send	Always available
	99*			
	81*			
	130*			
UART3_RXD	76*	I	UART-3 serial data receive	Always available
	77*			Only w/o 'WB' option
	79*			
	93*			Always available
	95*			Always available
UART3_TXD	76*	O	UART-3 serial data transmit	Always available
	77*			Only w/o 'WB' option
	79*			
	93*			Always available
	95*			Always available

Table 24 UART4 Signals

Signal Name	Pin #	Type	Description	Availability
UART4_CTS_B	146*	O	UART-2 clear to send	Always available
	152*			
UART4_RTS_B	146*	I	UART-2 request to send	Always available
	152*			
UART4_RXD	11*	I	UART-2 serial data receive	Always available
	148*			
	13*			
	154*			
	80*			
	82*			
UART4_TXD	11*	O	UART-2 serial data transmit	Always available
	148*			
	13*			
	154*			

Signal Name	Pin #	Type	Description	Availability
	80*			
	82*			

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 CAN Bus

CL-SOM-iMX8Plus features up-to two CAN bus interfaces. These interfaces support the following key features:

- Full implementation of the CAN version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8M Plus Reference manual for additional details.

The following tables summarize the CAN interface signals.

Table 25 CAN1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN1_TX	31*	O	CAN transmit pin	Always available
	65*			
	147*			
CAN1_RX	43*	I	CAN receive pin	Always available
	63*			
	149*			

Table 26 CAN2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN2_TX	77*	O	CAN transmit pin	Only w/o 'WB' option
	194*			Always available
	153*			Always available
CAN2_RX	79*	I	CAN receive pin	Only w/o 'WB' option
	192*			Always available
	151*			Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 I2C

CL-SOM-iMX8Plus features up-to five I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multi-master operation
- Master or Slave operation mode

Please refer to the i.MX8M Plus Reference manual for additional details.

NOTE: I2C2 is the system I2C channel utilized for the following on-board functions: RTC, EEPROM.

The tables below summarize the I2C interface signals.

Table 27 I2C2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_SCL	3*	O	I2C serial clock line	Always available
	99*			
I2C2_SDA	5*	IO	I2C serial data line	Always available

Table 28 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C3_SCL	130*	O	I2C serial clock line	Always available
	154*			
	167*			
I2C3_SDA	74*	IO	I2C serial data line	Always available
	169*			
	148*			

Table 29 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	69*	O	I2C serial clock line	Only w/o 'WB' option
	86*			Always available
	152*			Always available
	173*			Always available
I2C4_SDA	66*	IO	I2C serial data line	Only w/o 'WB' option
	76*			Always available
	146*			
	81*			
	84*			
	175*			

Table 30 I2C5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C5_SCL	31*	O	I2C serial clock line	Always available
	54*			Only w/o 'WB' option
	147*			Always available
I2C5_SDA	43*	IO	I2C serial data line	Always available
	56*			Only w/o 'WB' option
	149*			Always available

Table 31 I2C6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C6_SCL	11*	O	I2C serial clock line	Always available
	58*			Only w/o 'WB' option
	153*			Always available
I2C6_SDA	13*	IO	I2C serial data line	Always available
	60*			Only w/o 'WB' option
	151*			Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 ECSPI

Up-to two SPI interfaces are accessible through the CL-SOM-iMX8Plus carrier board interface. The SPI interfaces are derived from i.MX8M Plus integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the i.MX8M Plus Reference manual for additional details.

The following tables summarize the ECSPI interface signals.

Table 32 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI2_MISO	90* 152* 173*	I	SPI-2 Master data in; slave data out	Always available
ECSPI2_MOSI	82* 148* 169*	O	SPI-2 Master data out; slave data in	Always available
ECSPI2_SCLK	80* 154* 167*	O	SPI-2 Master clock out; slave clock in	Always available
ECSPI2_SS0	88* 175* 146*	O	SPI-2 Chip select 0	Always available

Table 33 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ECSPI3_MISO	117*	I	SPI-3 Master data in; slave data out	Always available
ECSPI3_MOSI	75*	O	SPI-3 Master data out; slave data in	Only w/o 'WB' option
ECSPI3_SCLK	73*	O	SPI-3 Master clock out; slave clock in	Only w/o 'WB' option
ECSPI3_SS0	111*	O	SPI-3 Chip select 0	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 PWM

SOM-iMX8M-Plus features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 34 PWM Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	49*	O	PWM1 functional output	Always available
	175*			
PWM2_OUT	2*	O	PWM2 functional output	Only w/o “E1”and ‘E2” options
	173*			Always available
	43*			
	134			Only w/o “E1”and ‘E2” options
PWM3_OUT	169*	O	PWM3 functional output	Always available
PWM4_OUT	167*	O	PWM4 functional output	Always available
	184*			

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.17 JTAG

CL-SOM-iMX8Plus enables access to the i.MX8M Plus JTAG port through the carrier board interface.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 35 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Availability
JTAG_MOD	108	I	JTAG MODE	Always available
JTAG_TCK	122	I	Test Clock	Always available
JTAG_TDI	120	I	Test Data In	Always available
JTAG_TDO	126	O	Test Data Out	Always available
JTAG_TMS	124	I	Test Mode Select	Always available

4.18 GPIO

Up-to 90 of the i.MX8M Plus general purpose input/output (GPIO) signals are available through the CL-SOM-iMX8Plus carrier board interface. When configured as an output, it is possible to write to an i.MX8M Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Plus register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Plus Reference manual for additional details.
The following table summarizes the GPIO interface signals.

Table 40 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
GPIO1_IO05*	140	IO	GPIO	3.3V	Only w/o ‘E2” option
GPIO1_IO09*	2	IO	GPIO	3.3V	Only w/o “E1”and ‘E2” options
GPIO1_IO11*	134	IO	GPIO	3.3V	Only w/o “E1”and ‘E2” options
GPIO1_IO16*	52	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” options
GPIO1_IO17*	97	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” options
GPIO1_IO18*	8	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO19*	62	IO	GPIO	RGMII_VIO2	Only w/o “E1”and ‘E2” options
GPIO1_IO20*	12	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” options
GPIO1_IO21*	16	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO22*	6	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO23*	20	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO24*	18	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO25*	14	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO26*	22	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO27*	4	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO28*	26	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO1_IO29*	24	IO	GPIO	RGMII_VIO1	Only w/o “E1”and ‘E2” option
GPIO2_IO0*	54	IO	GPIO	3.3V	Only w/o “WB” option
GPIO2_IO1*	56	IO	GPIO	3.3V	Only w/o “WB” option
GPIO2_IO6*	68	IO	GPIO	3.3V	Always available
GPIO2_IO7*	70	IO	GPIO	3.3V	Always available
GPIO2_IO8*	72	IO	GPIO	3.3V	Always available
GPIO2_IO9*	76	IO	GPIO	3.3V	Always available
GPIO2_IO10*	130	IO	GPIO	3.3V	Always available
GPIO2_IO11*	74	O	GPIO	3.3V	Always available
GPIO2_IO12*	61	O	GPIO	3.3V	Always available
GPIO2_IO13*	80	O	GPIO	3.3V	Always available
GPIO2_IO14*	82	IO	GPIO	3.3V	Always available
GPIO2_IO15*	84	IO	GPIO	3.3V	Always available
GPIO2_IO16*	86	IO	GPIO	3.3V	Always available
GPIO2_IO17*	88	IO	GPIO	3.3V	Always available
GPIO2_IO18*	90	IO	GPIO	3.3V	Always available
GPIO2_IO19*	179	IO	GPIO	3.3V	Always available
GPIO2_IO2*	58	IO	GPIO	3.3V	Only w/o “WB” option
GPIO2_IO20*	67	IO	GPIO	3.3V	Always available
GPIO2_IO3*	60	IO	GPIO	3.3V	Only w/o “WB” option
GPIO3_IO26*	147	IO	GPIO	3.3V	Always available
GPIO3_IO27*	149	IO	GPIO	3.3V	Always available
GPIO3_IO28*	153	IO	GPIO	3.3V	Always available
GPIO3_IO29*	151	IO	GPIO	3.3V	Always available
GPIO4_IO2*	69	IO	GPIO	3.3V	Only w/o “WB” option
GPIO4_IO6*	34	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO7*	25	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO8*	48	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO9*	81	IO	GPIO	3.3V	Always available
GPIO4_IO10*	42	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO11*	38	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO12*	40	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO13*	36	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO14*	128	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO15*	32	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO16*	30	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO17*	44	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO21*	136	IO	GPIO	RGMII_VIO2	Only w/o “E2” option
GPIO4_IO22*	65	IO	GPIO	3.3V	Always available

Signal Name	Pin #	Type	Description	Voltage Domain	Availability
GPIO4_IO25*	63	IO	GPIO	3.3V	Always available
GPIO4_IO26*	194	IO	GPIO	3.3V	Always available
GPIO4_IO27*	192	IO	GPIO	3.3V	Always available
GPIO4_IO28*	197	IO	GPIO	3.3V	Always available
GPIO4_IO29*	199	IO	GPIO	3.3V	Always available
GPIO4_IO30*	201	IO	GPIO	3.3V	Always available
GPIO4_IO31*	189	IO	GPIO	3.3V	Always available
GPIO5_IO0*	191	IO	GPIO	3.3V	Always available
GPIO5_IO1*	193	IO	GPIO	3.3V	Always available
GPIO5_IO2*	187	IO	GPIO	3.3V	Always available
GPIO5_IO3*	31	IO	GPIO	3.3V	Always available
GPIO5_IO4*	43	IO	GPIO	3.3V	Always available
GPIO5_IO5*	49	IO	GPIO	3.3V	Always available
GPIO5_IO6*	93	IO	GPIO	3.3V	Always available
GPIO5_IO7*	95	IO	GPIO	3.3V	Always available
GPIO5_IO8*	99	IO	GPIO	3.3V	Always available
GPIO5_IO9*	81	IO	GPIO	3.3V	Always available
GPIO5_IO10*	154	IO	GPIO	3.3V	Always available
GPIO5_IO11*	148	IO	GPIO	3.3V	Always available
GPIO5_IO12*	152	IO	GPIO	3.3V	Always available
GPIO5_IO13*	146	IO	GPIO	3.3V	Always available
GPIO5_IO18*	167	IO	GPIO	3.3V	Always available
GPIO5_IO19*	169	IO	GPIO	3.3V	Always available
GPIO5_IO20*	173	IO	GPIO	3.3V	Always available
GPIO5_IO21*	175	IO	GPIO	3.3V	Always available
GPIO5_IO22*	73	IO	GPIO	3.3V	Only w/o “WB” option
GPIO5_IO23*	75	IO	GPIO	3.3V	Only w/o “WB” option
GPIO5_IO24*	117	IO	GPIO	3.3V	Always available
GPIO5_IO25*	111	IO	GPIO	3.3V	Always available
GPIO5_IO26*	77	IO	GPIO	3.3V	Only w/o “WB” option
GPIO5_IO27*	79	IO	GPIO	3.3V	Only w/o “WB” option
GPIO5_IO28*	11	IO	GPIO	3.3V	Always available
GPIO5_IO29*	13	IO	GPIO	3.3V	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: 1.8V or 3.3V power must be supplied via pin RGMII_VIO1 and RGMII_VIO2 if any of the RGMII_VIO domain signals are used on the carrier-board

5 SYSTEM LOGIC

5.1 Power Supply

Table 41 Power signals

Signal Name	Pin#	Type	Description
V_SOM	10,28,46,64,78,96,114 132,150,168,186,204	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
VCC_RTC	183	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND.
GND	1,19,37,55,71,87,105,123 141,159,177,195	P	Common ground
RGMII_VIO1	102	P	RGMII_VIO1 domain power supply input. If RGMII ENET1 pins are used, this pin must be supplied from external 1.8V power. If RGMII_VIO1 domain signals are used for other functions (such as GPIO), this pin must be supplied from external 3.3V or 1.8V power – depending on I/O voltage requirements.
RGMII_VIO2	138	P	RGMII_VIO2 domain power supply input. If RGMII ENET2 pins are used, this pin must be supplied from external 1.8V power. If RGMII_VIO2 domain signals are used for other functions (such as GPIO), this pin must be supplied from external 3.3V or 1.8V power – depending on I/O voltage requirements.

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

CL-SOM-iMX8Plus supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Plus SoC. The logic that controls both signals is supplied by the i.MX8M Plus SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that CL-SOM-iMX8Plus is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 42 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	181	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	202	O	Active high power-up request output from i.MX8M Plus SoC.	Always available
PWRBTN	165	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).	Always available

5.3 Reset

POR_B signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX8Plus. Please refer to the i.MX8M Plus Reference manual for additional details.

Table 43 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset	Always available

5.4 Boot Sequence

CL-SOM-iMX8Plus boot sequence defines which interface/media is used by CL-SOM-iMX8Plus to load and execute the initial software (such as SPL or/and U-boot). CL-SOM-iMX8Plus can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD/SDIO 2 interface

CL-SOM-iMX8Plus will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CL-SOM-iMX8Plus:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows CL-SOM-iMX8Plus to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 36 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 37 CL-SOM-iMX8Plus Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on SD/SDIO2 interface

5.5 Signal Multiplexing Characteristics

Up to 90 of the CL-SOM-iMX8Plus carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX8Plus CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX8Plus pins are derived from the i.MX8M Plus SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a “RESERVED” function and must not be used.

Table 38 Multifunctional Signals

Pin #	SoC Pin Name	GPIO	SAI	ENET1(QOS)	ENET2	SDIO	I2C	UART	SPI	PWM	CAN	SPDIF	Availability
2	GPIO1_IO09	GPIO1_IO09								PWM2_OUT			NOT E1 AND NOT E2
4	ENET_RD1	GPIO1_IO27	SAI7_RX_SYNC	ENET1_RD1									NOT E1 AND NOT E2
6	ENET_TX_CTL	GPIO1_IO22	SAI6_MCLK	ENET1_TX_CTL								SPDIF1_OUT	NOT E1 AND NOT E2
8	ENET_TD3	GPIO1_IO18	SAI6-TX_BCLK	ENET1_TD3									NOT E1 AND NOT E2
11	UART4_RXD	GPIO5_IO28					I2C6_SCL	UART2_CTS/RTS UART4_RX/TX					Always
12	ENET_TD1	GPIO1_IO20	SAI6_RX_SYNC	ENET1_TD1									NOT E1 AND NOT E2
13	UART4_TXD	GPIO5_IO29					I2C6_SDA	UART2_RTS/CTS					Always

								UART4_RX/TX					
Pin #	SoC Pin Name	GPIO	SAI	ENET1(QOS)	ENET2	SDIO	I2C	UART	SPI	PWM	CAN	SPDIF	Availability
14	ENET_RXC	GPIO1_IO25	SAI7_TX_BCLK	ENET1_RXC									NOT E1 AND NOT E2
16	ENET_TD0	GPIO1_IO21	SAI6_RX_BCLK	ENET1_TD0									NOT E1 AND NOT E2
18	ENET_RX_CTL	GPIO1_IO24	SAI7_TX_SYNC	ENET1_RX_CTL									NOT E1 AND NOT E2
20	ENET_TXC	GPIO1_IO23	SAI7_TXD0	ENET1_TXC									NOT E1 AND NOT E2
22	ENET_RD0	GPIO1_IO26	SAI7_RXD0	ENET1_RD0									NOT E1 AND NOT E2
24	ENET_RD3	GPIO1_29	SAI7_MCLK	ENET1_RD3								SPDIF1_IN	NOT E1 AND NOT E2
25	SAI1_RXD5	GPIO4_IO7	SAI6_RXD0/TXD0		ENET2_RD1								NOT E2
26	ENET_RD2	GPIO1_IO28		ENET1_RD2									NOT E1 AND NOT E2
30	SAI1_TXD4	GPIO4_IO16	SAI6_RX_BCLK/TX_BCLK		ENET2_TX_CTL								NOT E2
31	SPDIF_TX	GPIO5_IO3					I2C5_SCL			PWM3_OUT	CAN1_TX	SPDIF1_OUT	Always
32	SAI1_TXD3	GPIO4_IO15			ENET2_TD3								NOT E2
34	SAI1_RXD4	GPIO4_IO6	SAI6_RX_BCLK/TX_BCLK		ENET2_RXD0								NOT E2
36	SAI1_TXD1	GPIO4_IO13			ENET2_TXD1								NOT E2
38	SAI1_TXC	GPIO4_IO11			ENET2_RXC								NOT E2
40	SAI1_TXD0	GPIO4_IO12			ENET2_TD0								NOT E2
42	SAI1_TXFS	GPIO4_IO10			ENET2_RX_CTL								NOT E2
43	SPDIF_RX	GPIO5_IO4					I2C5_SDA			PWM2_OUT	CAN1_RX	SPDIF1_IN	Always
44	SAI1_TXD5	GPIO4_IO17	SAI6_TXD0/RXD0		ENET2_TXC								NOT E2
48	SAI1_RXD6	GPIO4_IO8	SAI6_RX_SYNC/TX_SYNC		ENET2_RD2								NOT E2

49	SPDIF_EXT_CLK	GPIO5_IO5								PWM1_OUT		SPDIF1_EXT_CLK	Always
50	SAI1_RXD7		SAI6_MCLK		ENET2_RD3								NOT E2
52	ENET_MDC	GPIO1_IO16		ENET1_MDC									NOT E1 AND NOT E2
54	SD1_CLK	GPIO2_IO0			ENET2_ MDC	SD1_CLK	I2C5_SCL	UART1_TX/RX					NOT WB
56	SD1_CMD	GPIO2_IO1			ENET2_MDIO	SD1_CMD	I2C5_SDA	UART1_TX/RX					NOT WB
58	SD1_DATA0	GPIO2_IO2				SD1_DATA0	I2C6_SCL	UART1_CTS/RTS					NOT WB
60	SD1_DATA1	GPIO2_IO3				SD1_DATA1	I2C6_SDA	UART1_CTS/RTS					NOT WB
61	SD2_nCD	GPIO2_IO12				SD2_nCD							Always
62	ENET_TD2	GPIO1_IO19	SAI6_RXD0	ENET1_TD2 ENET1_TXC									NOT E1 AND NOT E2
63	CAN1_RX	GPIO4_IO25									CAN1_RX		Always
65	CAN1_TX	GPIO4_IO22						UART1_RX/TX			CAN1_TX		Always
66	SD1_DATA3	GPIO2_IO5				SD1_DATA3	I2C4_SDA	UART2_RX/TX					NOT WB
67	SD2_WP	GPIO2-IO20				SD2_WP							Always
68	SD1_DATA4	GPIO2_IO6				SD1_DATA4		UART2_CTS/RTS					Always
69	SD1_DATA2	GPIO4_IO2				SD1_DATA2	I2C4_SCL	UART2_RX/TX					NOT WB
70	SD1_DATA5	GPIO2_IO7				SD1_DATA5		UART2_CTS/RTS					Always
72	SD1_DATA6	GPIO2_IO8				SD1_DATA6	I2C2_SCL	UART3_RX/TX					Always
73	UART1_RXD	GPIO5_IO22						UART1_RX/TX	ECSPI3_CLK				NOT WB
74	SD1_STROBE	GPIO2_IO11				SD1_STROBE	I2C3_SDA	UART3_CTS/RTS					Always
75	UART1_TXD	GPIO5_IO23						UART1_RX/TX	ECSPI3_MOSI				NOT WB
76	SD1_DATA7	GPIO2_IO9				SD1_DATA7	I2C2_SDA	UART3_RX/TX					Always
77	UART1_CTS	GPIO5_IO26						UART1_CTS/RTS UART3_RX/TX		CAN2_TX			NOT WB

79	UART1_RTS	GPIO5_IO27						UART1_CTS /RTS UART3_RX/ TX		CAN2_RX			NOT WB
80	SD2_CLK	GPIO2_IO13				SD2_CLK		UART4_RX/ TX	ECSPI2_SCLK				Always
81	ECSPI1_SS0	GPIO5_IO9	SAI7_TX_SYNC				I2C2_SDA	UART3_RTS /CTS	ECSPI1_SS0				Always
82	SD2_CMD	GPIO2_IO14				SD2_CMD		UART4_RX/ TX	ECSPI2_MOSI				Always
84	SD2_DATA0	GPIO2_IO15				SD2_DATA0	I2C4_SDA	UART2_RX/ TX					Always
86	SD2_DATA1	GPIO2_IO16				SD2_DATA1	I2C4_SCL	UART2_RX/ TX					Always
88	SD2_DATA2	GPIO2_IO17				SD2_DATA2			ECSP2_SS0			SPDIF1_ OUT	Always
90	SD2_DATA3	GPIO2_IO18				SD2_DATA3			ECSP2_MISO			SPDIF1_ IN	Always
93	ECSP1_SCLK	GPIO5_IO6	SAI7_RX_SYNC					UART3_RX/ TX	ECSP1_SCLK				Always
95	ECSP1_MOSI	GPIO5_IO7	SAI7_RX_BCLK					UART3_RX/ TX	ECSP1_MOSI				Always
97	ENET_MDIO	GPIO1_IO17	SAI6_TX_SYNC	ENET1_MDI O									NOT E1 AND NOT E2
99	ECSP1_MISO	GPIO5_IO8	SAI7_RXD0				I2C2_SCL	UART3_RTS /CTS	ECSP1_MISO				Always
111	UART2_TXD	GPIO5_IO25						UART2_RX/ TX	ECSP3_SS0				Always
117	UART2_RXD	GPIO5_IO24						UART2_RX/ TX	ECSP3_MISO				Always
128	SAI1_TXD2	GPIO4_IO14			ENET2_TD2								NOT E2
130	SD1_RESET	GPIO2_IO10				SD1_RESET	I2C3_SCL	UART3_RTS /CTS					Always
134	GPIO1_IO11	GPIO1_IO11								PWM2_OU T			NOT E1 AND NOT E2
136	SAI2_RXFS	GPIO4_IO21						UART1_RX/ TX					NOT E2
140	GPIO1_IO05	GPIO1_IO05											NOT E2
146	ECSPI2_SS0	GPIO5_IO13					I2C4_SDA	UART4_RTS /CTS	ECSPI2_SS0				Always
147	HDMI_DDC_SC L	GPIO3_IO26					I2C5_SCL				CAN1_TX		Always
148	ECSPI2_MOSI	GPIO5_IO11	SAI7_TXD0			SD2_CD_B	I2C3_SDA	UART4_RX/ TX	ECSPI2_MOSI				Always

149	HDMI_DDC_SDA	GPIO3_IO27					I2C5_SDA				CAN1_RX		Always
151	HDMI_HPD	GPIO3_IO29					I2C6_SDA				CAN2_RX		Always
152	ECSPI2_MISO	GPIO5_IO12	SAI7_MCLK				I2C4_SCL	UART4_RTS/CTS	ECSPI2_MISO				Always
153	HDMI_CEC	GPIO3_IO28					I2C6_SCL				CAN2_TX		Always
154	ECSPI2_SCLK	GPIO5_IO10	SAI7_TX_BCLK				I2C3_SCL	UART4_RX/TX	ECSPI2_SCLK				Always
167	I2C3_SCL	GPIO5_IO18					I2C3_SCL		ECSPI2_SCLK	PWM4_OUT			Always
169	I2C3_SDA	GPIO5_IO19					I2C3_SDA		ECSPI2_MOSI	PWM3_OUT			Always
173	I2C4_SCL	GPIO5_IO20					I2C4_SCL		ECSPI2_MISO	PWM2_OUT			Always
175	I2C4_SDA	GPIO5_IO21					I2C4_SDA		ECSPI2_SS0	PWM1_OUT			Always
179	SD2_RESET	GPIO2_IO19				SD2_RESET							Always
187	SAI3_MCLK	GPIO5_IO2	SAI3_MCLK							PWM4_OUT		SPDIF1_OUT	Always
189	SAI3_TXFS	GPIO4_IO31	SAI3_TXFS SAI3_TXD1					UART2_RX/TX					Always
191	SAI3_TXC	GPIO5_IO0	SAI3_TXC					UART2_RX/TX					Always
192	CAN2_RX	GPIO4_IO27	SAI3_MCLK								CAN2_RX		Always
193	SAI3_TXD	GPIO5_IO1	SAI3_TXD0									SPDIF1_CLK	Always
194	CAN2_TX	GPIO4_IO26									CAN2_TX		Always
197	SAI3_RXFS	GPIO4_IO28	SAI3_RXFS SAI3_RXD1									SPDIF1_IN	Always
199	SAI3_RXC	GPIO4_IO29	SAI3_RXC					UART2_RTS/CTS					Always
201	SAI3_RXD	GPIO4_30	SAI3_RXD0					UART2_RTS/CTS					Always

5.6 RTC

CL-SOM-iMX8Plus features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about CL-SOM-iMX8Plus RTC please refer to the AM1805 datasheet.

5.7 LED

CL-SOM-iMX8Plus features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Plus. The LED is ON when GPIO1_IO[12] is logic LOW.

5.8 Reserved Signals

The following SOM-iMX8M-Plus signals are reserved and must be left unconnected.

Table 39 Reserved Signals

Pin#
142, 144, 156, 162, 203

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX8Plus CoM/SoM carrier board interface uses the SODIMM-204 edge connector. The SoM pinout is detailed in the table below.

6.1 Connector Pinout

Table 40 Connector P1

Pin #	CL-SOM-iMX8Plus Signal Name	Ref.		Pin #	CL-SOM-iMX8Plus Signal Name	Ref.
1	GND			2	PWM2_OUT GPIO1_IO09	
3	RESERVED			4	ENET1_RD1 SAI7_RX_SYNC GPIO1_IO27 ETH1_LED_ACT	
5	RESERVED			6	SPDIF1_OUT ENET_TX_CTL SAI6_MCLK GPIO1_IO22 ETH1_MDI0N	
7	CSI1_DP3			8	ENET1_TD3 SAI6-TX_BCLK GPIO1_IO18 ETH1_MDI0P	
9	CSI1_DN3			10	V_SOM	
11	UART2_CTS/RTS UART4_RX/TX I2C6_SCL GPIO5_IO28			12	ENET1_TD1 SAI6_RX_SYNC GPIO1_IO20 ETH1_MDI1N	
13	UART2_RTS/CTS UART4_RX/TX I2C6_SDA GPIO5_IO29			14	ENET1_RXC SAI7_TX_BCLK GPIO1_IO25 ETH1_MDI1P	
15	CSI1_DP2			16	ENET1_TD0 SAI6_RX_BCLK GPIO1_IO21 ETH1_LINK	
17	CSI1_DN2			18	ENET1_RX_CTL SAI7_TX_SYNC GPIO1_IO24 ETH1_MDI2N	
19	GND			20	ENET1_TXC SAI7_TXD0 GPIO1_IO23 ETH1_MDI2P	
21	CSI1_DP0			22	ENET1_RD0 SAI7_RXD0 GPIO1_IO26 ETH1_LINK-LED_10_100	
23	CSI1_DN0			24	SPDIF1_IN ENET1_RD3 SAI7_MCLK GPIO1_29 ETH1_MDI3N	
25	ENET2_RD1 SAI6_RXD0/TXD0 GPIO4_IO7 ETH2_LED_ACT			26	ENET_RD2 SAI6_RXD0/TXD0 GPIO1_IO28 ETH1_MDI3P	
27	CSI1_DP1			28	V_SOM	
29	CSI1_DN1			30	ENET2_TX_CTL SAI6_RX_BCLK/TX_BCLK GPIO4_IO16 ETH2_MDI0N	
31	SPDIF1_OUT CAN1_TX PWM3_OUT I2C5_SCL GPIO5_IO3			32	ENET2_TD3 GPIO4_IO15 ETH2_MDI0P	
33	LVDS1_CLK_P			34	ENET2_RXD0	

Pin #	CL-SOM-iMX8Plus Signal Name	Ref.		Pin #	CL-SOM-iMX8Plus Signal Name	Ref.
	DSI_CKP				SAI6_RX_BCLK/TX_BCLK GPIO4_IO6 ETH2_LINK-LED_10_100	
35	LVDS1_CLK_N DSI_CKN			36	ENET2_TXD1 GPIO4_IO13 ETH2_MDI1N	
37	GND			38	ENET2_RXC GPIO4_IO11 ETH2_MDI1P	
39	LVDS1_D0_P DSI_DP0			40	ENET2_TD0 GPIO4_IO12 ETH2_LINK-LED_1000	
41	LVDS1_D0_N DSI_DN0			42	ENET2_RX_CTL GPIO4_IO10 ETH2_MDI2N	
43	SPDIF1_IN CAN1_RX PWM2_OUT I2C5_SDA GPIO5_IO4			44	ENET2_TXC SAI1_TXD5 SAI6_TXD0/RXD0 GPIO4_IO17 ETH2_MDI2P	
45	LVDS1_D1_P DSI_DP1			46	V_SOM	
47	LVDS1_D1_N DSI_DN1			48	ENET2_RD2 SAI6_RX_SYNC/TX_SYNC GPIO4_IO8 ETH2_MDI3N	
49	SPDIF1_EXT_CLK PWM1_OUT GPIO5_IO5			50	ENET2_RD3 SAI6_MCLK ETH2_MDI3P GPIO4_IO9	
51	LVDS1_D2_P DSI_DP2			52	ENET_MDC GPIO1_IO16	
53	LVDS1_D2_N DSI_DN2			54	UART1_TX/RX I2C5_SCL SD1_CLK ENET2_MDC GPIO2_IO0	
55	GND			56	UART1_TX/RX I2C5_SDA SD1_CMD ENET2_MDIO GPIO2_IO1	
57	LVDS1_D3_P DSI_DP3			58	UART1_CTS/RTS I2C6_SCL SD1_DATA0 GPIO2_IO2	
59	LVDS1_D3_N DSI_DN3			60	UART1_CTS/RTS I2C6_SDA SD1_DATA1 GPIO2_IO3	
61	SD2_nCD GPIO2_IO12			62	ENET1_TD2 ENET1_TXC SAI6_RXD0 GPIO1_IO19	
63	CAN1_RX GPIO4_IO25			64	V_SOM	
65	UART1_RX/TX CAN1_TX GPIO4_IO22			66	UART2_RX/TX I2C4_SDA SD1_DATA3 GPIO2_IO5	
67	SD2_WP GPIO2_IO20			68	UART2_CTS/RTS SD1_DATA4 GPIO2_IO6	
69	UART2_RX/TX I2C4_SCL SD1_DATA2 GPIO4_IO2			70	UART2_CTS/RTS SD1_DATA5 GPIO2_IO7	
71	GND			72	UART3_RX/TX I2C2_SCL SD1_DATA6 GPIO2_IO8	

Pin #	CL-SOM-iMX8Plus Signal Name	Ref.		Pin #	CL-SOM-iMX8Plus Signal Name	Ref.
73	ECSPI3_CLK UART1_RX/TX GPIO5_IO22			74	UART3_CTS/RTS I2C3_SDA SD1_STROBE GPIO2_IO11	
75	ECSPI3_MOSI UART1_RX/TX GPIO5_IO23			76	UART3_RX/TX I2C2_SDA SD1_DATA7 GPIO2_IO9	
77	CAN2_TX UART1_CTS/RTS UART3_RX/TX GPIO5_IO26			78	V_SOM	
79	CAN2_RX UART1_CTS/RTS UART3_RX/TX GPIO5_IO27			80	SD2_CLK UART4_RX/TX ECSPI2_SCLK GPIO2_IO13	
81	UART3_RTS/CTS I2C2_SDA SAI7_TX_SYNC GPIO5_IO9			82	ECSPI2_MOSI UART4_RX/TX SD2_CMD GPIO2_IO14	
83	CSI2_CKN			84	UART2_RX/TX I2C4_SDA SD2_DATA0 GPIO2_IO15	
85	CSI2_CKP			86	UART2_RX/TX I2C4_SCL SD2_DATA1 GPIO2_IO16	
87	GND			88	SPDIF1_OUT ECSP2_SS0 SD2_DATA2 GPIO2_IO17	
89	CSI2_DN0			90	SPDIF1_IN ECSP2_MISO SD2_DATA3 GPIO2_IO18	
91	CSI2_DP0			92	LVDS0_D1_N	
93	ECSP1_SCLK UART3_RX/TX SAI7_RX_SYNC GPIO5_IO6			94	LVDS0_D1_P	
95	ECSP1_MOSI UART3_RX/TX SAI7_RX_BCLK GPIO5_IO7			96	V_SOM	
97	ENET_MDIO SAI6_TX_SYNC GPIO1_IO17			98	LVDS0_D2_N	
99	ECSP1_MISO UART3_RTS/CTS I2C2_SCL SAI7_RXD0 GPIO5_IO8			100	LVDS0_D2_P	
101	PCIE_CLKN			102	ENET_VIO	
103	PCIE_CLKP			104	LVDS0_CLK_N	
105	GND			106	LVDS0_CLK_P	
107	CSI2_DN1			108	JTAG_MOD	
109	CSI2_DP1			110	LVDS0_D0_N	
111	ECSP3_SS0 UART2_RX/TX GPIO5_IO25			112	LVDS0_D0_P	
113	CSI2_DN2			114	V_SOM	
115	CSI2_DP2			116	LVDS0_D3_N	
117	ECSP3_MISO UART2_RX/TX GPIO5_IO24			118	LVDS0_D3_P	
119	CSI2_DN3			120	JTAG_TDI	
121	CSI2_DP3			122	JTAG_TCK	
123	GND			124	JTAG_TMS	
125	PCIE_TXP			126	JTAG_TDO	
127	PCIE_TXN			128	ENET2_TD2	

Pin #	CL-SOM-iMX8Plus Signal Name	Ref.		Pin #	CL-SOM-iMX8Plus Signal Name	Ref.
					GPIO4_IO14	
129	EARC_N_HPD			130	UART3_RTS/CTS I2C3_SCL SD1_RESET GPIO2_IO10	
131	PCIE_RXP			132	V_SOM	
133	PCIE_RXN			134	PWM2_OUT GPIO1_IO11	
135	EARC_P_UTIL			136	UART1_RX/TX GPIO4_IO21	
137	HDMI_TXN0			138	RGMII_VIO2	
139	HDMI_TXP0			140	GPIO1_IO05	
141	GND			142	RESERVED	
143	HDMI_TXN1			144	RESERVED	
145	HDMI_TXP1			146	ECSPI2_SS0 UART4_RTS/CTS I2C4_SDA GPIO5_IO13	
147	HDMI_DDC_SCL CAN1_TX I2C5_SCL GPIO3_IO26			148	ECSPI2_MOSI UART4_RX/TX I2C3_SDA SD2_CD_B SAI7_TXD0 GPIO5_IO11	
149	HDMI_DDC_SDA CAN1_RX I2C5_SDA GPIO3_IO27			150	V_SOM	
151	HDMI_HPD CAN2_RX I2C6_SDA GPIO3_IO29			152	ECSPI2_MISO UART4_RTS/CTS I2C4_SCL SAI7_MCLK GPIO5_IO12	
153	HDMI_CEC CAN2_TX I2C6_SCL GPIO3_IO28			154	ECSPI2_SCLK UART4_RX/TX I2C3_SCL SAI7_TX_BCLK GPIO5_IO10	
155	HDMI_TXCN			156	RESERVED	
157	HDMI_TXCP			158	USB2_TXN	
159	GND			160	USB2_TXP	
161	HDMI_TXN2			162	RESERVED	
163	HDMI_TXP2			164	USB2_RXN	
165	ONOFF			166	USB2_RXP	
167	PWM4_OUT ECSPI2_SCLK I2C3_SCL SAI7_TX_BCLK GPIO5_IO18			168	V_SOM	
169	PWM3_OUT ECSPI2_MOSI I2C3_SDA GPIO5_IO19			170	USB2_DN	
171	COLD_RESET_IN			172	USB2_DP	
173	PWM2_OUT ECSPI2_MISO I2C4_SCL GPIO5_IO20			174	USB1_ID	
175	PWM1_OUT ECSPI2_SS0 I2C4_SDA GPIO5_IO21			176	USB1_DP	
177	GND			178	USB1_DN	
179	SD2_RESET GPIO2_IO19			180	USB1_VBUS_3V3	
181	PMIC_STBY_REQ			182	CSI1_CKP	
183	VCC_RTC			184	CSI1_CKN	
185	ALT_BOOT			186	V_SOM	
187	SPDIF1_OUT PWM4_OUT SAI3_MCLK			188	USB1_RXN	

Pin #	CL-SOM-iMX8Plus Signal Name	Ref.		Pin #	CL-SOM-iMX8Plus Signal Name	Ref.
	GPIO5_IO2					
189	UART2_RX/TX SAI3_TXFS SAI3_TXD1 GPIO4_IO31			190	USB1_RXP	
191	UART2_RX/TX SAI3_TXC GPIO5_IO0			192	CAN2_RX SAI3_MCLK GPIO4_IO27	
193	SPDIF1_CLK SAI3_TXD0 GPIO5_IO1			194	CAN2_TX GPIO4_IO26	
195	GND			196	USB2_VBUS_3V3	
197	SPDIF1_IN SAI3_RXFS SAI3_RXD1 GPIO4_IO28			198	USB1_TXN	
199	UART2_RTS/CTS SAI3_RXC GPIO4_IO29			200	USB1_TXP	
201	UART2_RTS/CTS SAI3_RXD0 GPIO4_30			202	PMIC_ON_REQ	
203	RESERVED			204	V_SOM	

6.2 Mating Connectors

Table 41 Connector type

CL-SOM-iMX8Plus connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 3 CL-SOM-iMX8Plus top

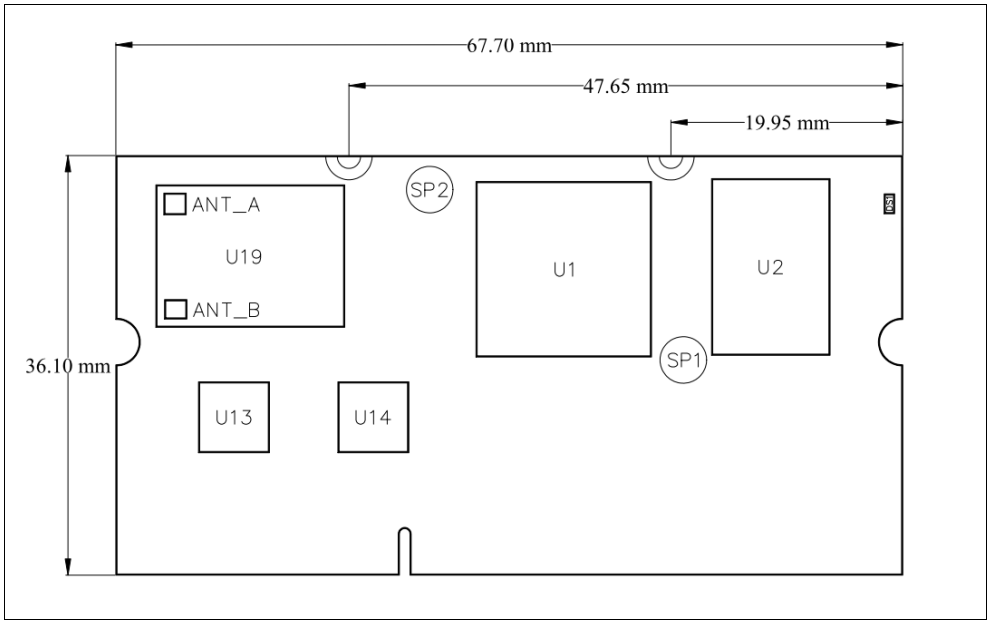
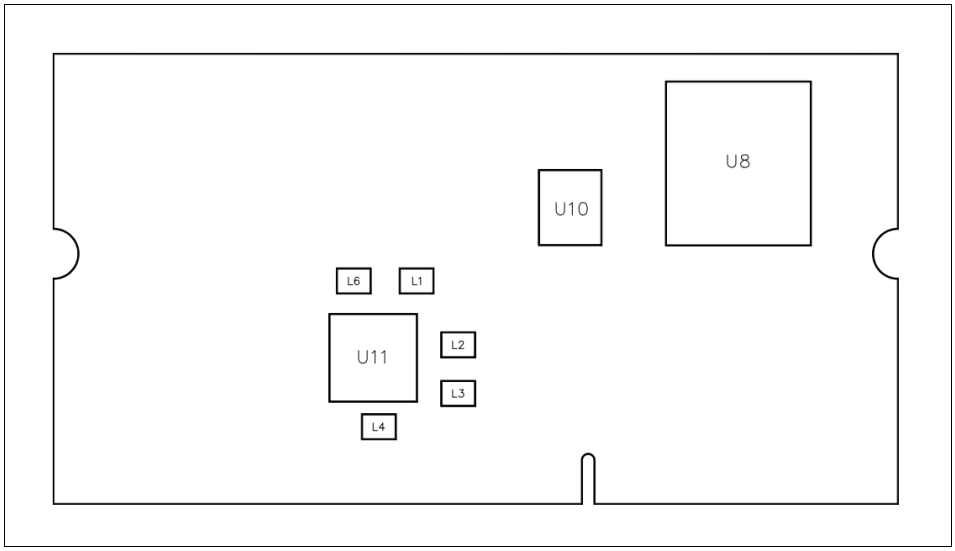


Figure 4 CL-SOM-iMX8Plus bottom



- All dimensions are in millimeters
- The height of all components is < 3.0mm
- Board thickness is 1.0mm
- 3D model and mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/cl-som-imx8plus-nxp-i-mx-8m-plus-system-on-module-computer/#devres

6.4 Standoffs/Spacers

CL-SOM-iMX8Plus provides two semi-circular mounting holes that can be used to secure the SoM to the carrier board by mounting two spacers with any adequate screws and nuts.

6.5 Heat Spreader and Cooling Solutions

CL-SOM-iMX8Plus is provided with an optional heat-spreader assembly. The CL-SOM-iMX8Plus heat-spreader is designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the CL-SOM-iMX8Plus temperature specifications. Various thermal management solutions can be used, including active and passive heat dissipation approaches.

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 42 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	4.8	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 43 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	4.4	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 Typical Power Consumption

Table 44 Typical Power Consumption

Use case	Use case description	I_{SOM}	P_{SOM}
Linux up – low-power	Linux up, Ethernet down, display output off	290mA	1090mW
Linux up – typical	Linux up, Ethernet link up, display output on	470mA	1762mW
Video playback	Video playback with GStreamer in Linux	650mA	2437mW
High CPU load	CPU stress test (stress-ng)	1015mA	3806mW
Heavy mixed load	GPU load + CPU stress test + Ethernet activity	1320mA	4950mW

Power consumption has been measured with the following setup:

1. Full stock configuration - SOM-iMX8PLUS-C1800QM-D4-N32-E2-WB-H
2. SB-IMX8PLUS carrier-board, V_SOM = 3.75V
3. 5" WXGA LCD panel
4. Ambient temperature of 25C

Table 45 RTC timekeeping current

Use case	Use case description	I_{VCC_RTC}
RTC only	VCC_RTC (3.0V) is supplied from external coin-cell battery V_SOM is not present	70nA

7.4 ESD Performance

Table 46 ESD Performance

Interface	ESD Performance
i.MX8M Plus pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for CL-SOM-iMX8Plus operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-iMX8Plus.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- The carrier board interface connectors provide 3mm mating height. Bear in mind that there are components on the bottom side of CL-SOM-iMX8Plus. It is not recommended to place any components underneath the CL-SOM-iMX8Plus module.
- Refer to the SB-IMX8PLUS carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX8Plus, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-IMX8PLUS carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.