

# UCM-iMX93

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Reference Guide



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**Table 1 Revision Notes**

| Date     | Description  |
|----------|--|
| Mar 2023 | <ul style="list-style-type: none"> <li>• Initial release</li> </ul>  |
| Aug 2023 | <ul style="list-style-type: none"> <li>• Added description of pin P1-17 in table 51</li> </ul>   |
| Sep 2023 | <ul style="list-style-type: none"> <li>• Added power consumption data in section 7.3</li> <li>• Updated V_SOM maximal allowed voltage</li> </ul>   |
| Oct 2023 | <ul style="list-style-type: none"> <li>• Updated specifications table – removed C1500D option</li> </ul>   |
| Jan 2024 | <ul style="list-style-type: none"> <li>• Updated availability of pins P1-28, P1-26, P1-30, P1-32, P1-98, P2-76, P1-60, P1-96 in multiple tables</li> <li>• Fixed alternate function names of UART_CTS pins in table 56 and table 59</li> <li>• Fixed signal type designations for UART_RTS and UART_CTS</li> </ul> |
| Feb 2024 | <ul style="list-style-type: none"> <li>• Fixed alternate function of pins P1-53 and P1-87</li> </ul>   |
| Apr 2024 | <ul style="list-style-type: none"> <li>• Unified DSI and CSI signal naming</li> </ul>  |

Please check for a newer revision of this manual at the CompuLab website <https://www.compulab.com>. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

# 1 INTRODUCTION

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## 1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab UCM-iMX93 System-on-Module.

## 1.2 UCM-iMX93 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the UCM-iMX93 part number: <https://www.compulab.com/products/computer-on-modules/ucm-imx93-nxp-i-mx9-som-system-on-module-computer/#ordering>.

## 1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

**Table 2 Related Documents**

| Document                      | Location  |
|-------------------------------|---|
| UCM-iMX93 Developer Resources | <a href="https://www.compulab.com/products/computer-on-modules/ucm-imx93-nxp-i-mx9-som-system-on-module-computer/#devres">https://www.compulab.com/products/computer-on-modules/ucm-imx93-nxp-i-mx9-som-system-on-module-computer/#devres</a>   |
| i.MX93 Reference Manual       | <a href="https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-93-applications-processor-family-arm-cortex-a55-ml-acceleration-power-efficient-mpu:i.MX93">https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-93-applications-processor-family-arm-cortex-a55-ml-acceleration-power-efficient-mpu:i.MX93</a> |
| i.MX93 Datasheet              |   |

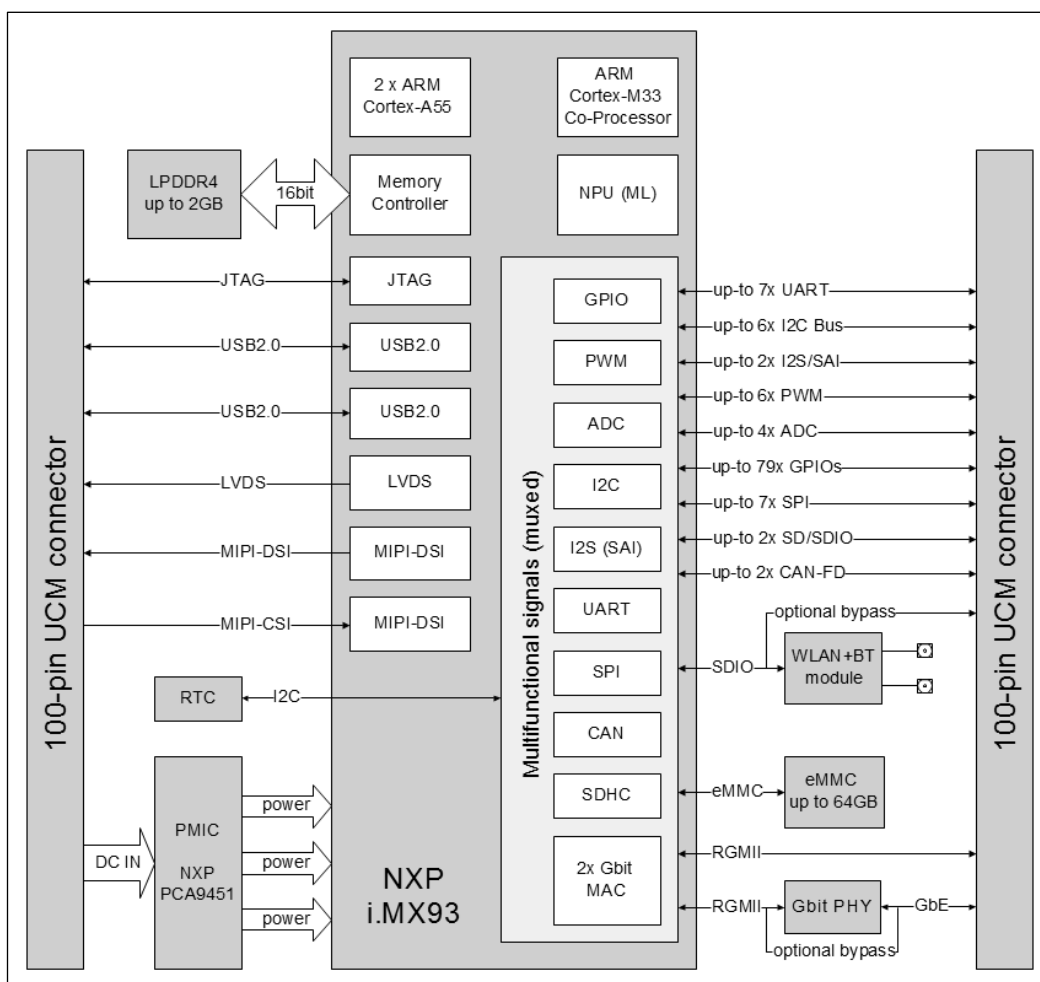
## 2 OVERVIEW

### 2.1 Highlights

- NXP i.MX93 processor, up-to 1.7GHz
- Up to 2GB LPDDR4 and 64GB eMMC
- Integrated AI/ML Neural Processing Unit
- LVDS, MIPI-DSI and MIPI-CSI
- Certified 802.11ac WiFi, BT 5.3
- GbE, RGMII, 2x USB, 2x CAN-FD, 7x UART
- Tiny size and weight - 28 x 38 x 4 mm, 7 gram

### 2.2 Block Diagram

Figure 1 UCM-iMX93 Block Diagram



## 2.3 Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by "NOT", the particular feature is only available when the option is not used.

"+" means that the feature is always available.

**Table 3 Features and Configuration options**

| Feature                          | Description  | Option |
|----------------------------------|--|--------|
| <b>CPU Core and Graphics</b>     |  |        |
| CPU                              | NXP i.MX9352, dual-core ARM Cortex-A55, 1.7GHz                       | C1700D |
|                                  | NXP i.MX9331, single-core ARM Cortex-A55, 1.7GHz                     | C1700S |
| NPU                              | AI/ML Neural Processing Unit<br>Arm® Ethos™ U-65 microNPU            | C1700D |
| Real-Time Co-processor           | ARM Cortex-M33, 250Mhz   | +      |
| <b>Memory and Storage</b>        |  |        |
| RAM                              | 512MB – 2GB, LPDDR4  | D      |
| Storage                          | eMMC flash, 8GB - 64GB   | N      |
| <b>Display, Camera and Audio</b> |  |        |
| Display                          | MIPI-DSI, 4 data lanes, up to 1080p60                                | +      |
|                                  | LVDS, 4 lanes, up to 1366x768 p60                                    | +      |
| Touchscreen                      | Capacitive touch-screen support through SPI and I2C interfaces       | +      |
| Camera                           | MIPI-CSI, 2 data lanes   | +      |
| Audio                            | Up-to 2x I2S / SAI   | +      |
|                                  | S/PDIF input/output  | +      |
| <b>Network</b>                   |  |        |
| Ethernet                         | Gigabit Ethernet port (MAC+PHY)                                      | +      |
| RGMII                            | Primary RGMII  | not E  |
|                                  | Secondary RGMII  | +      |
| WiFi                             | Certified 802.11ac WiFi<br>NXP 88W8997 chipset                       | WB     |
| Bluetooth                        | Bluetooth 5.3 BLE  |        |
| <b>I/O</b>                       |  |        |
| USB                              | 2x USB2.0 dual-role ports  | +      |
| UART                             | Up to 7x UART  | +      |
| CAN bus                          | Up-to 2x CAN-FD  | +      |
| SD/SDIO                          | 1x SD/SDIO   | +      |
|                                  | Additional 1x SD/SDIO  | not WB |
| SPI                              | Up to 7x SPI   | +      |
| I2C                              | Up to 6x I2C   | +      |
| ADC                              | 4x general-purpose ADC channels                                      |        |
| PWM                              | Up to 6x PWM signals   | +      |
| GPIO                             | Up to 79x GPIO (multifunctional signals shared with other functions) | +      |
| <b>System Logic</b>              |  |        |
| RTC                              | Real-time clock, powered by external battery                         | +      |
| JTAG                             | JTAG debug interface   | +      |



**Table 4 Electrical, Mechanical and Environmental Specifications**

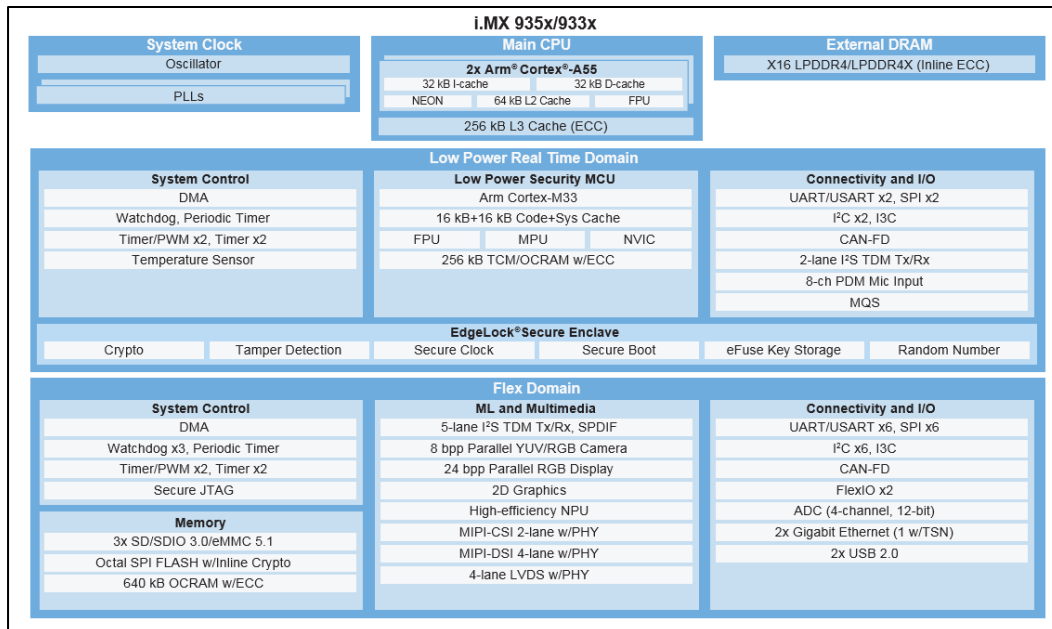
| Electrical Specifications     |   |
|-------------------------------|---|
| Supply Voltage                | 3.45V to 5.5V   |
| Digital I/O voltage           | 3.3V / 1.8V   |
| Power consumption             | 0.5 - 3 W, depending on system load and board configuration |
| Mechanical Specifications     |   |
| Dimensions                    | 28 x 38 x 4 mm  |
| Weight                        | 7 gram  |
| Connectors                    | 2 x 100 pin, 0.4mm pitch                                    |
| Environmental and Reliability |   |
| MTTF                          | > 200,000 hours   |
| Operation temperature (case)  | Commercial: 0° to 70° C                                     |
|                               | Extended: -20° to 70° C                                     |
|                               | Industrial: -40° to 85° C                                   |
| Storage temperature           | -40° to 85° C   |
| Relative humidity             | 10% to 90% (operation)                                      |
|                               | 05% to 95% (storage)  |
| Shock                         | 50G / 20 ms   |
| Vibration                     | 20G / 0 - 600 Hz  |

### 3 CORE SYSTEM COMPONENTS

#### 3.1 i.MX93 System-on-Chip

The i.MX 93 System-on-Chip (SoC) includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing.

Figure 2 i.MX 93 Block Diagram



#### 3.2 Memory

##### 3.2.1 DRAM

UCM-iMX93 is equipped with up to 2GB of onboard LPDDR4 memory. The LPDDR4 channel is 16-bits wide.

##### 3.2.2 Bootloader and General Purpose Storage

UCM-iMX93 uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

## 4 PERIPHERAL INTERFACES

UCM-iMX93 implements a variety of peripheral interfaces through two 100-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX93 SoM. The availability restrictions of each signal are described in the “Signals description” table for each interface.
- Some of the UCM-iMX93 carrier board interface pins are multifunctional. Up to 8 functions (ALT modes) are accessible through each multifunctional pin. For additional details, please refer to chapter 5.6.
- UCM-iMX93 uses different I/O voltage domains to power different groups of digital signals. Some pins operate at 3.3V, some at 1.8V. Voltage domain of each signal is specified in the “Signals description” table for each interface.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#”** – Pin number on the carrier board interface connector
- **“Type”** – Signal type, see the definition of different signal types below
- **“Description”** – Signal description with regards to the interface in question
- **“Voltage Domain”** – Voltage level of the particular signal
- **“Availability”** – Depending on UCM-iMX93 configuration options, certain carrier board interface pins are physically disconnected (floating). The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **“O”** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **“PD”** - Always pulled down onboard UCM-iMX93, followed by pull value.
- **“PU”** - Always pulled up onboard UCM-iMX93, followed by pull value.
- **“LVDS”** - Low-voltage differential signaling.

## 4.1 Display Interfaces

### 4.1.1 MIPI-DSI

The UCM-iMX93 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX93 SoC. The following main features are supported:

- Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- Maximum data rate per lane of 1.5 Gbps
- Maximum resolution ranges up to 1920 x 1200 p60

The following table below summarizes the MIPI-DSI interface signals.

**Table 5 MIPI-DSI Interface Signals**

| Signal Name | Pin # | Type | Description                                | Availability |
|-------------|-------|------|--|--------------|
| DSI_CLK_N   | P2-21 | AO   | Negative part of MIPI-DSI clock diff-pair  | Always       |
| DSI_CLK_P   | P2-23 | AO   | Positive part of MIPI-DSI clock diff-pair  | Always       |
| DSI_D0_N    | P2-1  | AO   | Negative part of MIPI-DSI data diff-pair 0 | Always       |
| DSI_D0_P    | P2-3  | AO   | Positive part of MIPI-DSI data diff-pair 0 | Always       |
| DSI_D1_N    | P2-15 | AO   | Negative part of MIPI-DSI data diff-pair 1 | Always       |
| DSI_D1_P    | P2-17 | AO   | Positive part of MIPI-DSI data diff-pair 1 | Always       |
| DSI_D2_N    | P2-5  | AO   | Negative part of MIPI-DSI data diff-pair 2 | Always       |
| DSI_D2_P    | P2-7  | AO   | Positive part of MIPI-DSI data diff-pair 2 | Always       |
| DSI_D3_N    | P2-11 | AO   | Negative part of MIPI-DSI data diff-pair 3 | Always       |
| DSI_D3_P    | P2-13 | AO   | Positive part of MIPI-DSI data diff-pair 3 | Always       |

### 4.1.2 LVDS Interface

UCM-iMX93 provides one LVDS interface derived from the i.MX93 LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366 x 768 p60 or 1280 x 800 p60

The table below summarizes the LVDS interface signals.

**Table 6 LVDS Interface Signals**

| Signal Name | Pin # | Type | Description                            | Availability |
|-------------|-------|------|--|--------------|
| LVDS_CLK_N  | P2-14 | AO   | Negative part of LVDS clock diff-pair  | Always       |
| LVDS_CLK_P  | P2-12 | AO   | Positive part of LVDS clock diff-pair  | Always       |
| LVDS_D0_N   | P2-26 | AO   | Negative part of LVDS data diff-pair 0 | Always       |
| LVDS_D0_P   | P2-24 | AO   | Positive part of LVDS data diff-pair 0 | Always       |
| LVDS_D1_N   | P2-20 | AO   | Negative part of LVDS data diff-pair 1 | Always       |
| LVDS_D1_P   | P2-18 | AO   | Positive part of LVDS data diff-pair 1 | Always       |
| LVDS_D2_N   | P2-8  | AO   | Negative part of LVDS data diff-pair 2 | Always       |
| LVDS_D2_P   | P2-6  | AO   | Positive part of LVDS data diff-pair 2 | Always       |
| LVDS_D3_N   | P2-4  | AO   | Negative part of LVDS data diff-pair 3 | Always       |
| LVDS_D3_P   | P2-2  | AO   | Positive part of LVDS data diff-pair 3 | Always       |

## 4.2 Camera Interface

UCM-iMX93 provides one MIPI-CSI interface, derived from the MIPI CSI host controller integrated into the i.MX93 SoC. The controller supports the following main features:

- Up to two data lanes and one clock lane
- Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes MIPI-CSI signals.

**Table 7 MIPI-CSI Interface Signals**

| Signal Name | Pin # | Type | Description                                 | Availability |
|-------------|-------|------|---|--------------|
| CSI_CLK_N   | P2-30 | AI   | Negative part of MIPI-CSI1 clock diff-pair  | Always       |
| CSI_CLK_P   | P2-32 | AI   | Positive part of MIPI-CSI1 clock diff-pair  | Always       |
| CSI_D0_N    | P2-31 | AI   | Negative part of MIPI-CSI1 data diff-pair 0 | Always       |
| CSI_D0_P    | P2-33 | AI   | Positive part of MIPI-CSI1 data diff-pair 0 | Always       |
| CSI_D1_N    | P2-35 | AI   | Negative part of MIPI-CSI1 data diff-pair 1 | Always       |
| CSI_D1_P    | P2-37 | AI   | Positive part of MIPI-CSI1 data diff-pair 1 | Always       |

## 4.3 Audio Interfaces

### 4.3.1 S/PDIF

UCM-iMX93 provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

**Table 8 S/PDIF Interface Signals**

| Signal Name | Pin # | Type | Description                   | Voltage Domain | Availability |
|-------------|-------|------|-------------------------------|----------------|--------------|
| SPDIF_IN    | P1-79 | I    | SPDIF input data line signal  | 3.3V           | Always       |
|             | P2-43 |      |                               | 1.8V           |              |
|             | P2-47 |      |                               | 1.8V           |              |
| SPDIF_OUT   | P1-81 | O    | SPDIF output data line signal | 3.3V           | Always       |
|             | P2-47 |      |                               | 1.8V           |              |

**NOTE: S/PDIF signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

### 4.3.2 SAI

UCM-iMX93 supports up-to two of the i.MX93 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX93 Reference manual for additional details. The tables below summarize the SAI interface signals.

**Table 9 SAI1 Signals**

| Signal Name     | Pin # | Type | Description   | Voltage Domain | Availability |
|-----------------|-------|------|---|----------------|--------------|
| SAI1_MCLK       | P1-19 | IO   | Audio master clock. An input when generated externally and an output when generated internally.   | 3.3V           | Always       |
|                 | P1-45 |      |   | 3.3V           | Always       |
| SAI1_RX_DATA[0] | P1-45 | I    | Receive data, sampled synchronously by the bit clock  | 3.3V           | Always       |
| SAI1_TX_DATA[0] | P1-53 | O    | Transmit data signal synchronous to bit clock.  | 3.3V           | Always       |
| SAI1_TX_DATA[1] | P1-87 | O    | Transmit data signal synchronous to bit clock.  | 3.3V           | Always       |
| SAI1_TX_BCLK    | P1-51 | O    | Transmit bit clock. An input when generated externally and an output when generated internally.   | 3.3V           | Always       |
| SAI1_TX_SYNC    | P1-87 | O    | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | 3.3V           | Always       |

**NOTE: SAI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 10 SAI2 Signals**

| Signal Name     | Pin # | Type | Description   | Voltage Domain | Availability |
|-----------------|-------|------|---|----------------|--------------|
| SAI2_MCLK       | P2-45 | IO   | Audio master clock. An input when generated externally and an output when generated internally. | 1.8V           | Always       |
| SAI2_RX_DATA[0] | P2-63 | I    | Receive data, sampled synchronously by the bit clock  | 1.8V           | Always       |
| SAI2_RX_DATA[1] | P2-65 | I    | Receive data, sampled synchronously by the bit clock  | 1.8V           | Always       |
| SAI2_RX_DATA[2] | P2-61 | I    | Receive data, sampled synchronously by the bit clock  | 1.8V           | Always       |
| SAI2_RX_DATA[3] | P2-59 | I    | Receive data, sampled synchronously by the bit clock  | 1.8V           | Always       |
| SAI2_RX_BCLK    | P2-70 | I    | Receive bit clock. An input when generated externally and an output when generated internally.  | 1.8V           | Always       |

| Signal Name     | Pin # | Type | Description   | Voltage Domain | Availability |
|-----------------|-------|------|---|----------------|--------------|
| SAI2_RX_SYNC    | P2-68 | I    | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.  | 1.8V           | Always       |
| SAI2_TX_DATA[0] | P2-53 | O    | Transmit data signal synchronous to bit clock.  | 1.8V           | Always       |
| SAI2_TX_DATA[1] | P2-55 | O    | Transmit data signal synchronous to bit clock.  | 1.8V           | Always       |
| SAI2_TX_DATA[2] | P2-41 | O    | Transmit data signal synchronous to bit clock.  | 1.8V           | Always       |
| SAI2_TX_DATA[3] | P2-43 | O    | Transmit data signal synchronous to bit clock.  | 1.8V           | Always       |
| SAI2_TX_BCLK    | P2-69 | O    | Transmit bit clock. An input when generated externally and an output when generated internally.   | 1.8V           | Always       |
| SAI2_TX_SYNC    | P2-67 | O    | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | 1.8V           | Always       |

**NOTE: SAI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

### 4.3.3 MQS

UCM-iMX93 supports up-to two MOQ interfaces that can be used to generate medium quality audio via standard GPIO.

Please refer to the i.MX93 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

**Table 11 MQS Signals**

| Signal Name | Pin # | Type | Description         | Voltage Domain | Availability |
|-------------|-------|------|---------------------|----------------|--------------|
| MQS1_LEFT   | P1-21 | O    | Left signal output  | 3.3V           | Always       |
|             | P1-87 |      |                     | 3.3V           | Always       |
| MQS1_RIGHT  | P1-23 | O    | Right signal output | 3.3V           | Always       |
|             | P1-45 |      |                     | 3.3V           | Always       |
| MQS2_LEFT   | P1-71 | O    | Left signal output  | 1.8            | Always       |
|             | P2-47 |      |                     | 1.8            | Always       |
| MQS2_RIGHT  | P1-67 | O    | Right signal output | 1.8            | Always       |
|             | P2-45 |      |                     | 1.8            | Always       |

**NOTE: MQS signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

## 4.4 Ethernet

### 4.4.1 Gigabit Ethernet

UCM-iMX93 incorporates an optional (“E” configuration option) full-featured 10/100/1000 Ethernet interface implemented with Realtek RTL8211E GbE PHY.

The following main features are supported:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- IEEE 802.3u compliant Auto-Negotiation
- Supports all IEEE 1588 frames - inside the MAC
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Activity and speed indicator LED controls

The table below summarizes the GbE interface signals.

**Table 12 GbE Interface Signals**

| Signal Name          | Pin # | Type | Description  | Availability    |
|----------------------|-------|------|--|-----------------|
| ETH0_LED_ACT         | P2-83 |      | Active High, activity LED driver. 3.3V signal, PHY strap                 | With 'E' option |
| ETH0_LINK-LED_10_100 | P2-86 |      | Active High, link, any speed LED driver. 3.3V signal                     | With 'E' option |
| ETH0_LINK-LED_1000   | P2-75 |      | Active High, link, any speed , blinking on transmit or receive PHY strap | With 'E' option |
| ETH0_MDI0N           | P2-73 | AIO  | Negative part of 100ohm diff-pair 0                                      | With 'E' option |
| ETH0_MDI0P           | P2-74 | AIO  | Positive part of 100ohm diff-pair 0                                      | With 'E' option |
| ETH0_MDI1N           | P2-80 | AIO  | Negative part of 100ohm diff-pair 1                                      | With 'E' option |
| ETH0_MDI1P           | P2-78 | AIO  | Positive part of 100ohm diff-pair 1                                      | With 'E' option |
| ETH0_MDI2N           | P2-81 | AIO  | Negative part of 100ohm diff-pair 2                                      | With 'E' option |
| ETH0_MDI2P           | P2-79 | AIO  | Positive part of 100ohm diff-pair 2                                      | With 'E' option |
| ETH0_MDI3N           | P2-85 | AIO  | Negative part of 100ohm diff-pair 3                                      | With 'E' option |
| ETH0_MDI3P           | P2-84 | AIO  | Positive part of 100ohm diff-pair 3                                      | With 'E' option |



## 4.4.2 RGMII

UCM-iMX93 features up-to two RGMII interfaces.

Primary RGMII interface ENET1 is available only when UCM-iMX93 is assembled without the “E” configuration option.

Secondary RGMII interface ENET2 is available with all UCM-iMX93 configurations.

The tables below summarize the Ethernet RGMII interface signals.

**Table 13 Primary RGMII ENET1 (QOS) Interface Signals**

| Signal Name           | Pin # | Type | Description   | Voltage Domain | Availability        |
|-----------------------|-------|------|---|----------------|---------------------|
| ENET1_MDC             | P2-60 | O    | Provides a timing reference to the PHY for data transfers on the MDIO signal  | 1.8V           | Only w/o 'E' option |
| ENET1_MDIO            | P2-62 | IO   | Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset | 1.8V           | Only w/o 'E' option |
|                       |       |      |   | 1.8V           | Only w/o 'E' option |
| ENET1_RD0             | P2-86 | I    | Ethernet input data from the PHY  | 1.8V           | Only w/o 'E' option |
| ENET1_RD1             | P2-83 | I    | Ethernet input data from the PHY  | 1.8V           | Only w/o 'E' option |
| ENET1_RD2             | P2-84 | I    | Ethernet input data from the PHY  | 1.8V           | Only w/o 'E' option |
| ENET1_RD3             | P2-85 | I    | Ethernet input data from the PHY  | 1.8V           | Only w/o 'E' option |
| ENET1_RX_CTL          | P2-81 | I    | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)                   | 1.8V           | Only w/o 'E' option |
| ENET1_RXC             | P2-78 | I    | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE  | 1.8V           | Only w/o 'E' option |
| ENET1_TD0             | P2-75 | O    | Ethernet output data to PHY   | 1.8V           | Only w/o 'E' option |
| ENET1_TD1             | P2-80 | O    | Ethernet output data to PHY   | 1.8V           | Only w/o 'E' option |
| ENET1_TD2             | P2-77 | O    | Ethernet output data to PHY   | 1.8V           | Only w/o 'E' option |
| ENET1_TD3             | P2-74 | O    | Ethernet output data to PHY   | 1.8V           | Only w/o 'E' option |
| ENET1_TXC             | P2-79 | O    | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE  | 1.8V           | Only w/o 'E' option |
| ENET1_TX_CTL          | P2-73 | O    | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)                   | 1.8V           | Only w/o 'E' option |
| ENET1_1588_EVENT0_IN  | P2-92 | I    | 1588 event input  | 3.3V/1.8V      | Always              |
| ENET1_1588_EVENT0_OUT | P2-96 | O    | 1588 event output   | 3.3V/1.8V      | Always              |

**NOTE: RGMII ENET1 interface operates at 1.8V voltage level.**

**NOTE: ENET1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 14 Secondary RGMII ENET2 Interface Signals**

| Signal Name           | Pin # | Type | Description   | Voltage Domain | Availability |
|-----------------------|-------|------|---|----------------|--------------|
| ENET2_MDC             | P2-68 | O    | Provides a timing reference to the PHY for data transfers on the MDIO signal  | 1.8V           | Always       |
| ENET2_MDIO            | P2-70 | IO   | Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset | 1.8V           | Always       |
| ENET2_RD0             | P2-41 | I    | Ethernet input data from the PHY  | 1.8V           | Always       |
| ENET2_RD1             | P2-43 | I    | Ethernet input data from the PHY  | 1.8V           | Always       |
| ENET2_RD2             | P2-45 | I    | Ethernet input data from the PHY  | 1.8V           | Always       |
| ENET2_RD3             | P2-47 | I    | Ethernet input data from the PHY  | 1.8V           | Always       |
| ENET2_RX_CTL          | P2-53 | I    | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)                   | 1.8V           | Always       |
| ENET2_RXC             | P2-55 | I    | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE  | 1.8V           | Always       |
| ENET2_TD0             | P2-59 | O    | Ethernet output data to PHY   | 1.8V           | Always       |
| ENET2_TD1             | P2-61 | O    | Ethernet output data to PHY   | 1.8V           | Always       |
| ENET2_TD2             | P2-65 | O    | Ethernet output data to PHY   | 1.8V           | Always       |
| ENET2_TD3             | P2-63 | O    | Ethernet output data to PHY   | 1.8V           | Always       |
| ENET2_TXC             | P2-69 | O    | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE  | 1.8V           | Always       |
| ENET2_TX_CTL          | P2-67 | O    | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)                   | 1.8V           | Always       |
| ENET2_1588_EVENT0_IN  | P2-99 | I    | 1588 event input  | 3.3V/1.8V      | Always       |
| ENET2_1588_EVENT0_OUT | P2-97 | O    | 1588 event output   | 3.3V/1.8V      | Always       |
| ENET2_1588_EVENT1_OUT | P2-94 | O    | 1588 event output   | 3.3V/1.8V      | Always       |

**NOTE: RGMII ENET2 signals operate at 1.8V voltage level.**

**NOTE: ENET2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

## 4.5 WiFi and Bluetooth Interfaces

UCM-iMX93 features optional 802.11ac WiFi and Bluetooth functions implemented with the AzureWave AW-CM276NF certified WiFi module (NXP 88W8997 chipset).

AzureWave AW-CM276NF provides the following key features:

- IEEE 802.11 ac/a/b/g/n, Wi-Fi compliant
- IEEE 802.11i for advanced security
- Multiple power saving modes for low power consumption
- Quality of Service (QoS) support
- Bluetooth 5.3 complaint

The wireless module is interfaced with i.MX93 SoC through SDIO3 interface.

The wireless module provides two on-board MHF4 antenna connectors:

- ANT\_A – main WiFi antenna
- ANT\_B – auxiliary WiFi / Bluetooth antenna

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**NOTE: WiFi and Bluetooth functions are available only with “WB” configuration option.**

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## 4.6 USB

UCM-iMX93 provides two dual-role USB2.0 ports. USB port #1 can be configured as host or device, while the second port is configured permanently for host mode.

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the USB interface signals.

**Table 15 USB port #1 Signals**

| Signal Name   | Pin # | Type | Description          | Availability |
|---------------|-------|------|----------------------|--------------|
| USB1_DN       | P1-14 | IO   | USB2.0 negative data | Always       |
| USB1_DP       | P1-12 | IO   | USB2.0 positive data | Always       |
| USB1_VBUS_DET | P1-24 | I    | USB1 VBUS detect     | Always       |
| USB1_ID       | P1-22 | I    | USB1 ID              | Always       |

**Table 16 USB port #2 Signals**

| Signal Name   | Pin # | Type | Description          | Availability |
|---------------|-------|------|----------------------|--------------|
| USB2_DN       | P1-5  | IO   | USB2.0 negative data | Always       |
| USB2_DP       | P1-3  | IO   | USB2.0 positive data | Always       |
| USB2_VBUS_DET | P1-1  | I    | USB2 VBUS detect     | Always       |
| USB2_ID       | P1-7  | I    | USB2 ID              | Always       |

## 4.7 MMC / SD /SDIO

UCM-iMX93 features two SD/SDIO ports. These ports are derived from the i.MX93 uSDHC2 and uSDHC3 controllers. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.0 command/response sets and physical layer

Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

**Table 17 SD2 Signals**

| Signal Name | Pin #  | Type | Description  | Voltage Domain | Availability |
|-------------|--------|------|--|----------------|--------------|
| SD2_CLK     | P2-96  | O    | Clock for MMC/SD/SDIO card   | 3.3V/1.8V      | Always       |
| SD2_CMD     | P2-100 | IO   | CMD line connect to card   | 3.3V/1.8V      | Always       |
| SD2_DATA0   | P2-97  | IO   | DATA0 line in all modes. Also used to detect busy state  | 3.3V/1.8V      | Always       |
| SD2_DATA1   | P2-99  | IO   | DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode   | 3.3V/1.8V      | Always       |
| SD2_DATA2   | P2-94  | IO   | DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode   | 3.3V/1.8V      | Always       |
| SD2_DATA3   | P2-98  | IO   | DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode. | 3.3V/1.8V      | Always       |
| SD2_RESET_B | P2-51  | O    | Card hardware reset signal, active LOW   | 3.3V/1.8V      | Always       |
| SD2_CD_B    | P2-92  | I    | Card detection pin   | 3.3V/1.8V      | Always       |

**NOTE: SD2 pins can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2\_VSELECT.**

**NOTE: SD2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 18 SD3 Signals**

| Signal Name | Pin # | Type | Description  | Voltage Domain | Availability         |
|-------------|-------|------|--|----------------|----------------------|
| SD3_CLK     | P2-36 | O    | Clock for MMC/SD/SDIO card   | 1.8V           | Only w/o 'WB' option |
| SD3_CMD     | P2-38 | IO   | CMD line connect to card   | 1.8V           | Only w/o 'WB' option |
| SD3_DATA0   | P2-42 | IO   | DATA0 line in all modes. Also used to detect busy state  | 1.8V           | Only w/o 'WB' option |
| SD3_DATA1   | P2-44 | IO   | DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode   | 1.8V           | Only w/o 'WB' option |
| SD3_DATA2   | P2-48 | IO   | DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode   | 1.8V           | Only w/o 'WB' option |
| SD3_DATA3   | P2-50 | IO   | DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode. | 1.8V           | Only w/o 'WB' option |

**NOTE: SD3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

## 4.8 FlexSPI

UCM-iMX93 provides one FlexSPI port that can support 4-bit serial flash memory or serial RAM devices. Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the FlexSPI interface signals.

**Table 19 FlexSPI Signals**

| Signal Name     | Pin # | Type | Description        | Voltage Domain | Availability         |
|-----------------|-------|------|--------------------|----------------|----------------------|
| FLEXSPI_SCLK    | P2-36 | O    | Flash serial clock | 1.8V           | Only w/o 'WB' option |
| FLEXSPI_SS0     | P2-38 | O    | Flash chip select  | 1.8V           | Only w/o 'WB' option |
| FLEXSPI_DATA[0] | P2-42 | IO   | Flash data 0       | 1.8V           | Only w/o 'WB' option |
| FLEXSPI_DATA[1] | P2-44 | IO   | Flash data 1       | 1.8V           | Only w/o 'WB' option |
| FLEXSPI_DATA[2] | P2-48 | IO   | Flash data 2       | 1.8V           | Only w/o 'WB' option |
| FLEXSPI_DATA[3] | P2-50 | IO   | Flash data 3       | 1.8V           | Only w/o 'WB' option |

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**NOTE: FlexSPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

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## 4.9 UART

UCM-iMX93 features up-to seven UART ports. The i.MX93 UART supports the following features:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 5 Mbps.
- Hardware flow control support for a request to send and clear to send signals.

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**NOTE: By default UART1 is assigned to be used as the main system console port.**

**NOTE: By default UART2 is assigned to be used as the M7 core debug port.**

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Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the UART interface signals.

**Table 20 UART1 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability |
|-------------|-------|------|----------------------|----------------|--------------|
| UART1_CTS   | P1-19 | I    | Clear to send        | 3.3V           | Always       |
| UART1_RTS   | P1-72 | O    | Request to send      | 3.3V           | Always       |
| UART1_DSR   | P1-51 | O    | Data set ready       | 3.3V           | Always       |
| UART1_RXD   | P1-76 | I    | Serial data receive  | 3.3V           | Always       |
| UART1_TXD   | P1-74 | O    | Serial data transmit | 3.3V           | Always       |

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**NOTE: UART1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 21 UART2 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability |
|-------------|-------|------|----------------------|----------------|--------------|
| UART2_CTS   | P1-51 | I    | Clear to send        | 3.3V           | Always       |
| UART2_RTS   | P1-53 | O    | Request to send      | 3.3V           | Always       |
| UART2_DSR   | P1-45 | O    | Data set ready       | 3.3V           | Always       |
| UART2_RXD   | P1-19 | I    | Serial data receive  | 3.3V           | Always       |
| UART2_TXD   | P1-72 | O    | Serial data transmit | 3.3V           | Always       |

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**NOTE: UART2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

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**Table 22 UART3 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability         |
|-------------|-------|------|----------------------|----------------|----------------------|
| UART3_CTS   | P1-96 | I    | Clear to send        | 3.3V           | Always               |
|             | P2-83 |      |                      | 1.8V           | Only w/o 'E' option  |
| UART3_RTS   | P1-95 | O    | Request to send      | 3.3V           | Only w/o 'WB' option |
|             | P2-80 |      |                      | 1.8V           | Only w/o 'E' option  |
| UART3_DTR   | P2-73 | I    | Data terminal ready  | 1.8V           | Only w/o 'E' option  |
| UART3_DSR   | P2-81 | O    | Data set ready       | 1.8V           | Only w/o 'E' option  |
| UART3_RIN   | P2-62 | I    | Ring indicator       | 1.8V           | Only w/o 'E' option  |
| UART3_RXD   | P1-60 | I    | Serial data receive  | 3.3V           | Always               |
|             | P2-86 |      |                      | 1.8V           | Only w/o 'E' option  |
| UART3_TXD   | P2-76 | O    | Serial data transmit | 3.3V           | Always               |
|             | P2-75 |      |                      | 1.8V           | Only w/o 'E' option  |

**NOTE: UART3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 23 UART4 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability         |
|-------------|-------|------|----------------------|----------------|----------------------|
| UART4_RXD   | P1-60 | I    | Serial data receive  | 3.3V           | Always               |
|             | P2-41 |      |                      | 1.8V           | Always               |
| UART4_TXD   | P2-76 | O    | Serial data transmit | 3.3V           | Always               |
|             | P2-59 |      |                      | 1.8V           | Always               |
| UART4_CTS   | P1-96 | I    | Clear to send        | 3.3V           | Always               |
|             | P2-45 |      |                      | 1.8V           | Always               |
| UART4_RTS   | P1-95 | O    | Request to send      | 3.3V           | Only w/o 'WB' option |
|             | P2-61 |      |                      | 1.8V           | Always               |
| UART4_DTR   | P2-67 | I    | Data terminal ready  | 1.8V           | Always               |
| UART4_DSR   | P2-53 | O    | Data set ready       | 1.8V           | Always               |
| UART4_RIN   | P2-70 | I    | Ring indicator       | 1.8V           | Always               |

**NOTE: UART4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 24 UART5 Signals**

| Signal Name | Pin # | Type | Description                 | Voltage Domain | Availability |
|-------------|-------|------|-----------------------------|----------------|--------------|
| UART5_RXD   | P1-26 | I    | UART-5 serial data receive  | 3.3V           | Always       |
|             | P1-71 |      |                             | 1.8V           | Always       |
| UART5_TXD   | P1-28 | O    | UART-5 serial data transmit | 3.3V           | Always       |
|             | P1-67 |      |                             | 1.8V           | Always       |
| UART5_CTS   | P1-30 | I    | UART-5 clear to send        | 3.3V           | Always       |
|             | P1-73 |      |                             | 1.8V           | Always       |
| UART5_RTS   | P1-32 | O    | UART-5 request to send      | 3.3V           | Always       |
|             | P1-65 |      |                             | 1.8V           | Always       |

**NOTE: UART5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 25 UART6 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability        |
|-------------|-------|------|----------------------|----------------|---------------------|
| UART6_RXD   | P2-56 | I    | Serial data receive  | 3.3V           | Only w/o 'E' option |
| UART6_TXD   | P2-58 | O    | Serial data transmit | 3.3V           | Only w/o 'E' option |
| UART6_CTS   | P2-52 | I    | Clear to send        | 3.3V           | Only w/o 'E' option |
| UART6_RTS   | P1-98 | O    | Request to send      | 3.3V           | Always              |

**NOTE: UART6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 26 UART7 Signals**

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability |
|-------------|-------|------|----------------------|----------------|--------------|
| UART7_RXD   | P1-41 | I    | Serial data receive  | 3.3V           | Always       |
| UART7_TXD   | P1-39 | O    | Serial data transmit | 3.3V           | Always       |
| UART7_CTS   | P1-35 | I    | Clear to send        | 3.3V           | Always       |
| UART7_RTS   | P1-37 | O    | Request to send      | 3.3V           | Always       |

**NOTE: UART7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**



## 4.10 CAN-FD

UCM-iMX93 features up-to two CAN-FD interfaces. These interfaces support the following key features:

- Full implementation of the CAN FD protocol and CAN protocol specification version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the CAN interface signals.

**Table 27 CAN1 Signals**

| Signal Name | Pin # | Type | Description      | Voltage Domain | Availability |
|-------------|-------|------|------------------|----------------|--------------|
| CAN1_TX     | P1-21 | O    | CAN transmit pin | 3.3V           | Always       |
|             | P1-53 |      |                  | 3.3V           |              |
| CAN1_RX     | P1-23 | I    | CAN receive pin  | 3.3V           | Always       |
|             | P1-51 |      |                  | 3.3V           |              |

**Table 28 CAN2 Signals**

| Signal Name | Pin # | Type | Description      | Voltage Domain | Availability        |
|-------------|-------|------|------------------|----------------|---------------------|
| CAN2_TX     | P1-33 | O    | CAN transmit pin | 3.3V           | Always              |
|             | P1-71 |      |                  | 1.8V           | Always              |
|             | P2-74 |      |                  | 1.8V           | Only w/o 'E' option |
|             | P2-97 |      |                  | 3.3V/1.8V      | Always              |
| CAN2_RX     | P1-49 | I    | CAN receive pin  | 3.3V           | Always              |
|             | P1-67 |      |                  | 1.8V           | Always              |
|             | P2-77 |      |                  | 1.8V           | Only w/o 'E' option |
|             | P2-99 |      |                  | 3.3V/1.8V      | Always              |

**NOTE: CAN signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**NOTE: Pins denoted "3.3V/1.8V" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2\_VSELECT.**

## 4.11 SPI

Up-to seven SPI interfaces are accessible through the UCM-iMX93 carrier board interface. The SPI interfaces are derived from i.MX93 integrated low-power SPI modules. The following key features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- One Chip Select (SS) signal
- Direct Memory Access (DMA) support

Please refer to the i.MX93 Reference manual for additional details.

SPI1 and SPI2 channels are limited to maximum frequency of 10MHz.

The following tables summarize the SPI interface signals.

**Table 29 SPI1 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability |
|-------------|-------|------|----------------------------------|----------------|--------------|
| SPI1_SIN    | P1-51 | I    | Serial data input                | 3.3V           | Always       |
| SPI1_SOUT   | P1-45 | O    | Master data out; slave data in   | 3.3V           | Always       |
| SPI1_SCLK   | P1-53 | O    | Master clock out; slave clock in | 3.3V           | Always       |
| SPI1_PCS0   | P1-87 | O    | Chip select 0                    | 3.3V           | Always       |
| SPI1_PCS1   | P1-23 | O    | Chip select 1                    | 3.3V           | Always       |

**NOTE: SPI1 maximum frequency is limited to 10MHz.**

**Table 30 SPI2 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability |
|-------------|-------|------|----------------------------------|----------------|--------------|
| SPI2_SIN    | P1-76 | I    | Master data in; slave data out   | 3.3V           | Always       |
| SPI2_SOUT   | P1-19 | O    | Master data out; slave data in   | 3.3V           | Always       |
| SPI2_SCLK   | P1-72 | O    | Master clock out; slave clock in | 3.3V           | Always       |
| SPI2_PCS0   | P1-74 | O    | Chip select 0                    | 3.3V           | Always       |

**NOTE: SPI2 maximum frequency is limited to 10MHz.**

**Table 31 SPI3 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability |
|-------------|-------|------|----------------------------------|----------------|--------------|
| SPI3_SIN    | P1-41 | I    | Master data in; slave data out   | 3.3V           | Always       |
| SPI3_SOUT   | P1-35 | O    | Master data out; slave data in   | 3.3V           | Always       |
| SPI3_SCLK   | P1-37 | O    | Master clock out; slave clock in | 3.3V           | Always       |
| SPI3_PCS0   | P1-39 | O    | Chip select 0                    | 3.3V           | Always       |
| SPI3_PCS1   | P1-98 | O    | Chip select 1                    | 3.3V           | Always       |

**NOTE: SPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 32 SPI4 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability         |
|-------------|-------|------|----------------------------------|----------------|----------------------|
| SPI4_SIN    | P1-59 | I    | Master data in; slave data out   | 3.3V           | Always               |
| SPI4_SOUT   | P1-61 | O    | Master data out; slave data in   | 3.3V           | Always               |
| SPI4_SCLK   | P1-63 | O    | Master clock out; slave clock in | 3.3V           | Always               |
| SPI4_PCS0   | P1-89 | O    | Chip select 0                    | 3.3V           | Always               |
| SPI4_PCS1   | P1-95 | O    | Chip select 1                    | 3.3V           | Only w/o 'WB' option |
| SPI4_PCS2   | P1-96 | O    | Chip select 2                    | 3.3V           | Always               |

**Table 33 SPI5 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability |
|-------------|-------|------|----------------------------------|----------------|--------------|
| SPI5_SIN    | P1-59 | I    | Master data in; slave data out   | 3.3V           | Always       |
| SPI5_SOUT   | P1-61 | O    | Master data out; slave data in   | 3.3V           | Always       |
| SPI5_SCLK   | P1-63 | O    | Master clock out; slave clock in | 3.3V           | Always       |
| SPI5_PCS0   | P1-89 | O    | Chip select 0                    | 3.3V           | Always       |
| SPI5_PCS1   | P1-49 | O    | Chip select 1                    | 3.3V           | Always       |

**Table 34 SPI6 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability |
|-------------|-------|------|----------------------------------|----------------|--------------|
| SPI6_SIN    | P1-26 | I    | Master data in; slave data out   | 3.3V           | Always       |
| SPI6_SOUT   | P1-30 | O    | Master data out; slave data in   | 3.3V           | Always       |
| SPI6_SCLK   | P1-32 | O    | Master clock out; slave clock in | 3.3V           | Always       |
| SPI6_PCS0   | P1-28 | O    | Chip select 0                    | 3.3V           | Always       |

**Table 35 SPI7 Signals**

| Signal Name | Pin # | Type | Description                      | Voltage Domain | Availability         |
|-------------|-------|------|----------------------------------|----------------|----------------------|
| SPI7_SIN    | P2-56 | I    | Master data in; slave data out   | 3.3V           | Only w/o 'E' option  |
| SPI7_SOUT   | P2-52 | O    | Master data out; slave data in   | 3.3V           | Only w/o 'E' option  |
| SPI7_SCLK   | P1-98 | O    | Master clock out; slave clock in | 3.3V           | Only w/o 'WB' option |
| SPI7_PCS0   | P2-58 | O    | Chip select 0                    | 3.3V           | Only w/o 'E' option  |
| SPI7_PCS1   | P1-33 | O    | Chip select 1                    | 3.3V           | Always               |

**NOTE: SPI signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

## 4.12 I2C

UCM-iMX93 features up-to six I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multi-master operation

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the I2C interface signals.

**Table 36 I2C3 Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability |
|-------------|-------|------|-----------------------|----------------|--------------|
| I2C3_SCL    | P1-26 | O    | I2C serial clock line | 3.3V           | Always       |
|             | P1-94 |      |                       | 3.3V           | Always       |
| I2C3_SDA    | P1-28 | IO   | I2C serial data line  | 3.3V           | Always       |
|             | P1-91 |      |                       | 3.3V           | Always       |

**Table 37 I2C4 Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability |
|-------------|-------|------|-----------------------|----------------|--------------|
| I2C4_SCL    | P1-32 | O    | I2C serial clock line | 3.3V           | Always       |
| I2C4_SDA    | P1-30 | IO   | I2C serial data line  | 3.3V           | Always       |

**Table 38 I2C5 Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability |
|-------------|-------|------|-----------------------|----------------|--------------|
| I2C5_SCL    | P1-26 | O    | I2C serial clock line | 3.3V           | Always       |
|             | P1-81 |      |                       | 3.3V           | Always       |
| I2C5_SDA    | P1-28 | IO   | I2C serial data line  | 3.3V           | Always       |
|             | P1-79 |      |                       | 3.3V           | Always       |

**Table 39 I2C6 Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability        |
|-------------|-------|------|-----------------------|----------------|---------------------|
| I2C6_SCL    | P1-32 | O    | I2C serial clock line | 3.3V           | Always              |
|             | P2-56 |      |                       | 3.3V           | Only w/o 'E' option |
| I2C6_SDA    | P1-30 | IO   | I2C serial data line  | 3.3V           | Always              |
|             | P2-58 |      |                       | 3.3V           | Only w/o 'E' option |

**NOTE: I2C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**Table 40 I2C7 Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability |
|-------------|-------|------|-----------------------|----------------|--------------|
| I2C7_SCL    | P1-41 | O    | I2C serial clock line | 3.3V           | Always       |

| Signal Name | Pin # | Type | Description          | Voltage Domain | Availability        |
|-------------|-------|------|----------------------|----------------|---------------------|
|             | P1-98 |      |                      | 3.3V           | Always              |
| I2C7_SDA    | P1-39 | IO   | I2C serial data line | 3.3V           | Always              |
|             | P2-52 |      |                      | 3.3V           | Only w/o 'E' option |

**Table 41 I2C8 Signals**

| Signal Name | Pin #  | Type | Description           | Voltage Domain | Availability |
|-------------|--------|------|-----------------------|----------------|--------------|
| I2C8_SCL    | P1-100 | O    | I2C serial clock line | 3.3V           | Always       |
|             | P1-37  |      |                       | 3.3V           |              |
| I2C8_SDA    | P1-35  | IO   | I2C serial data line  | 3.3V           | Always       |

**NOTE: I2C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

## 4.13 I3C

UCM-iMX93 supports one I3C bus interface.

Please refer to the i.MX93 Reference manual for additional details.

The tables below summarize the I3C interface signals.

**Table 42 I3C2 Signals**

| Signal Name | Pin #  | Type | Description  | Voltage Domain | Availability        |
|-------------|--------|------|--|----------------|---------------------|
| I3C2_SCL    | P2-60  | O    | Serial clock line  | 1.8V           | Only w/o 'E' option |
|             | P2-92  |      |  | 3.3V/1.8V      | Always              |
| I3C2_SDA    | P2-62  | IO   | Serial data line   | 1.8V           | Only w/o 'E' option |
|             | P2-96  |      |  | 3.3V/1.8V      | Always              |
| I3C2_PUR    | P2-80  | O    | Pull up resistance. There is internal pull-up resistance on SDA, which is controlled by the I3C controller. If the internal pullup is not enough, PUR can be used to control an external pull-up resistance on SDA actively. | 1.8            | Only w/o 'E' option |
|             | P2-100 |      |  | 3.3V/1.8V      | Always              |

**NOTE: I3C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**NOTE: Pins denoted "3.3V/1.8V" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2\_VSELECT.**

## 4.14 Timer/Pulse Width Modulation

i.MX93 supports multi-channel timer modules (TPM) that can be used for electric motor control and power management. The timer modules support:

- Input capture
- Output comparison
- Generation of PWM signals

Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the PDM interface signals.

**Table 43 TPM1 Signals**

| Signal Name | Pin # | Type | Description       | Voltage Domain | Availability |
|-------------|-------|------|-------------------|----------------|--------------|
| TPM1_EXTCLK | P1-23 | I    | External clock    | 3.3V           | Always       |
| TPM1_CH0    | P1-76 | IO   | Channel 0 I/O pin | 3.3V           | Always       |
| TPM1_CH2    | P1-19 | IO   | Channel 2 I/O pin | 3.3V           | Always       |

**Table 44 TPM3 Signals**

| Signal Name | Pin # | Type | Description       | Voltage Domain | Availability        |
|-------------|-------|------|-------------------|----------------|---------------------|
| TPM3_EXTCLK | P1-41 | I    | External clock    | 3.3V           | Always              |
| TPM3_CH0    | P2-58 | IO   | Channel 0 I/O pin | 3.3V           | Only w/o 'E' option |
| TPM3_CH1    | P1-61 | IO   | Channel 1 I/O pin | 3.3V           | Always              |

**Table 45 TPM4 Signals**

| Signal Name | Pin #  | Type | Description       | Voltage Domain | Availability        |
|-------------|--------|------|-------------------|----------------|---------------------|
| TPM4_EXTCLK | P1-35  | I    | External clock    | 3.3V           | Always              |
| TPM4_CH0    | P2-56  | IO   | Channel 0 I/O pin | 3.3V           | Only w/o 'E' option |
| TPM4_CH1    | P1-63  | IO   | Channel 1 I/O pin | 3.3V           | Always              |
| TPM4_CH2    | P1-100 | IO   | Channel 2 I/O pin | 3.3V           | Always              |
| TPM4_CH3    | P1-33  | IO   | Channel 3 I/O pin | 3.3V           | Always              |

**Table 46 TPM5 Signals**

| Signal Name | Pin # | Type | Description       | Voltage Domain | Availability        |
|-------------|-------|------|-------------------|----------------|---------------------|
| TPM5_EXTCLK | P1-37 | I    | External clock    | 3.3V           | Always              |
| TPM5_CH0    | P2-52 | IO   | Channel 0 I/O pin | 3.3V           | Only w/o 'E' option |
| TPM5_CH1    | P1-79 | IO   | Channel 1 I/O pin | 3.3V           | Always              |
| TPM5_CH2    | P1-89 | IO   | Channel 2 I/O pin | 3.3V           | Always              |

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**NOTE: TPM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

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## 4.15 ADC

UCM-iMX93 features a 4-channel 12-bit ADC implemented in the i.MX93 SoC.

Please refer to the i.MX93 Reference manual for additional details.

The following table summarizes ADC signals.

**Table 47 ADC Signals**

| Signal Name | Pin # | Type | Description         | Availability |
|-------------|-------|------|---------------------|--------------|
| ADC_IN0     | P2-89 | AI   | ADC input channel 0 | Always       |
| ADC_IN1     | P2-91 | AI   | ADC input channel 1 | Always       |
| ADC_IN2     | P2-93 | AI   | ADC input channel 2 | Always       |
| ADC_IN3     | P2-95 | AI   | ADC input channel 3 | Always       |

## 4.16 Tamper

i.MX93 supports two tamper pins – two passive or one active.

For additional details please refer to the i.MX93 Security Reference manual.

The following table summarizes tamper signals.

**Table 48 Tamper Signals**

| Signal Name | Pin # | Type | Description      | Availability |
|-------------|-------|------|------------------|--------------|
| TAMPER0     | P2-25 | IO   | Tamper channel 0 | Always       |
| TAMPER1     | P2-27 | IO   | Tamper channel 1 | Always       |

## 4.17 JTAG

UCM-iMX93 enables access to the i.MX93 JTAG port through the carrier board interface.

Please refer to the i.MX93 Reference manual for additional details.

The table below summarizes the JTAG interface signals.

**Table 49 JTAG Interface Signals**

| Signal Name | Pin # | Type | Description      | Voltage Domain | Availability |
|-------------|-------|------|------------------|----------------|--------------|
| JTAG_TCK    | P1-73 | I    | Test clock       | 1.8V           | Always       |
| JTAG_TDI    | P1-71 | I    | Test data in     | 1.8V           | Always       |
| JTAG_TDO    | P1-67 | O    | Test data out    | 1.8V           | Always       |
| JTAG_TMS    | P1-65 | I    | Test mode select | 1.8V           | Always       |

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**NOTE: JTAG interface operates at 1.8V voltage level.**

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## 4.18 GPIO

Up-to 79 of the i.MX93 general purpose input/output (GPIO) signals are available through the UCM-iMX93 carrier board interface. In addition, GPIO signals can produce interrupts.

Please refer to the i.MX93 Reference manual for additional details.

The following table summarizes the GPIO interface signals.

**Table 50 GPIO Signals**

| Signal Name  | Pin #  | Type | Description                  | Voltage Domain | Availability         |
|--------------|--------|------|------------------------------|----------------|----------------------|
| GPIO1_IO[4]  | P1-76  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO1_IO[6]  | P1-19  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO1_IO[8]  | P1-21  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO1_IO[9]  | P1-23  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO1_IO[12] | P1-51  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO1_IO[14] | P1-45  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[0]  | P1-28  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[1]  | P1-26  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[2]  | P1-30  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[3]  | P1-32  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[4]  | P2-58  | IO   | General-purpose input/output | 3.3V           | Only w/o 'E' option  |
| GPIO2_IO[5]  | P2-56  | IO   | General-purpose input/output | 3.3V           | Only w/o 'E' option  |
| GPIO2_IO[6]  | P2-52  | IO   | General-purpose input/output | 3.3V           | Only w/o 'E' option  |
| GPIO2_IO[7]  | P1-98  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[8]  | P1-39  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[9]  | P1-41  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[10] | P1-35  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[11] | P1-37  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[13] | P1-100 | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[14] | P2-76  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[15] | P1-60  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[16] | P1-96  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[17] | P1-95  | IO   | General-purpose input/output | 3.3V           | Only w/o 'WB' option |
| GPIO2_IO[18] | P1-89  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[19] | P1-59  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[20] | P1-61  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[21] | P1-63  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[22] | P1-79  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[23] | P1-81  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[25] | P1-33  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[27] | P1-49  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[28] | P1-91  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO2_IO[29] | P1-94  | IO   | General-purpose input/output | 3.3V           | Always               |
| GPIO3_IO[0]  | P2-92  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[1]  | P2-96  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[2]  | P2-100 | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[3]  | P2-97  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[30] | P1-73  | IO   | General-purpose input/output | 1.8V           | Always               |
| GPIO3_IO[31] | P1-67  | IO   | General-purpose input/output | 1.8V           | Always               |
| GPIO3_IO[4]  | P2-99  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[5]  | P2-94  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[6]  | P2-98  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[7]  | P2-51  | IO   | General-purpose input/output | 3.3V / 1.8V    | Always               |
| GPIO3_IO[20] | P2-36  | IO   | General-purpose input/output | 1.8V           | Only w/o 'WB' option |



|              |       |    |                              |      |                      |
|--------------|-------|----|------------------------------|------|----------------------|
| GPIO3_IO[21] | P2-38 | IO | General-purpose input/output | 1.8V | Only w/o 'WB' option |
| GPIO3_IO[22] | P2-42 | IO | General-purpose input/output | 1.8V | Only w/o 'WB' option |
| GPIO3_IO[23] | P2-44 | IO | General-purpose input/output | 1.8V | Only w/o 'WB' option |
| GPIO3_IO[24] | P2-48 | IO | General-purpose input/output | 1.8V | Only w/o 'WB' option |
| GPIO3_IO[25] | P2-50 | IO | General-purpose input/output | 1.8V | Only w/o 'WB' option |
| GPIO3_IO[28] | P1-71 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO3_IO[29] | P1-65 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[0]  | P2-60 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[1]  | P2-62 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[2]  | P2-74 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[3]  | P2-77 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[4]  | P2-80 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[5]  | P2-75 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[6]  | P2-73 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[7]  | P2-79 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[8]  | P2-81 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[9]  | P2-78 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[10] | P2-86 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[11] | P2-83 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[12] | P2-84 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[13] | P2-85 | IO | General-purpose input/output | 1.8V | Only w/o 'E' option  |
| GPIO4_IO[14] | P2-68 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[15] | P2-70 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[16] | P2-63 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[17] | P2-65 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[18] | P2-61 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[19] | P2-59 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[20] | P2-67 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[21] | P2-69 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[22] | P2-53 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[23] | P2-55 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[24] | P2-41 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[25] | P2-43 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[26] | P2-45 | IO | General-purpose input/output | 1.8V | Always               |
| GPIO4_IO[27] | P2-47 | IO | General-purpose input/output | 1.8V | Always               |

**NOTE: GPIO signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.**

**NOTE: Pins denoted "3.3V/1.8V" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2\_VSELECT.**

## 5 SYSTEM LOGIC

### 5.1 Power Supply

**Table 51 Power signals**

| Signal Name | Connector # | Pin#                                   | Type | Description  |
|-------------|-------------|--|------|--|
| V_SOM       | P1          | 11, 27, 43, 57, 69, 83                 | P    | Main power supply. Connect to a regulated DC supply or Li-Ion battery  |
|             | P2          | 9, 19, 29, 39, 57, 71, 87              |      |  |
| VCC_RTC     | P1          | 93                                     | P    | RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND. |
| VSD_3V3     | P1          | 17                                     | PO   | 3.3V regulator output. Should be used to supply power to SD card connected to SD2 interface  |
| GND         | P1          | 4, 10, 20, 40, 54, 64, 78, 88          | P    | Common ground  |
|             | P2          | 10, 16, 22, 28, 34, 40, 46, 54, 72, 82 |      |  |

### 5.2 I/O Voltage Domains

UCM-iMX93 utilizes three separate I/O voltage domains that are used to power different I/O modules of the i.MX93 SoC. Some pins operate at 3.3V, some at 1.8V.

Voltage domain of each signal is specified in the peripheral interface signals tables.

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**NOTE: Carrier-board designer must ensure that voltage level of the I/O pins matches the I/O voltage of the peripheral ICs on the carrier-board.**

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### 5.3 System and Miscellaneous Signals

#### 5.3.1 Power management

UCM-iMX93 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX93 SoC. The logic that controls both signals is supplied by the i.MX93 SoC SNVS power rail.

The PMIC\_STBY\_REQ output can be used to signal the carrier board power supply that UCM-iMX93 is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX93 Reference manual for additional details. The table below summarizes the external regulator control signals.

**Table 52 External regulator control signals**

| Signal Name   | Pin # | Type | Description   | Availability     |
|---------------|-------|------|---|------------------|
| PMIC_STBY_REQ | P1-66 | O    | When the processor enters SUSPEND mode, it will assert this signal. | Always available |
| PMIC_ON_REQ   | P1-68 | O    | Active high power-up request output from i.MX93 SoC.                | Always available |
| ONOFF         | P2-64 | I    | Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).  | Always available |

## 5.4 Reset

SYS\_RST\_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX93. Please refer to the i.MX93 Reference manual for additional details.

**Table 53 Reset signals**

| Signal Name  | Pin # | Type | Description   | Availability |
|--------------|-------|------|---|--------------|
| SYS_RST_PMIC | P1-2  | I    | Active Low cold reset input signal. Should be used as main system reset | Always       |
| POR_B        | P2-66 | I    | CPU power on reset input pin, active low                                | Always       |

## 5.5 Boot Sequence

UCM-iMX93 boot sequence defines which interface/media is used by UCM-iMX93 to load and execute the initial software (such as SPL or/and U-boot). UCM-iMX93 can load initial software from the following interfaces/media:

- On-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD2 interface
- Serial Download boot using USB1 interface

UCM-iMX93 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of three different boot sequences are supported by UCM-iMX93:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternative sequence: designed to allow recovery from an external bootable SD card in case of data corruption of the on-board primary boot device. Using the alternate sequence allows UCM-iMX93 to boot bypassing the onboard eMMC.
- Serial download mode: provides a means to download a program image to the i.MX93 system-on-chip over USB serial connection

Logic values of boot selections signals define which of the supported boot sequences is used by the system.

**Table 54 Boot selection signals**

| Signal Name  | Pin # | Type | Description  | Availability     |
|--------------|-------|------|--|------------------|
| ALT_BOOT_SD  | P1-90 | I    | Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence | Always available |
| ALT_BOOT_USB | P2-88 | I    | Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence | Always available |

**Table 55 UCM-iMX93 boot sequences**

| Mode        | ALT_BOOT_SD     | ALT_BOOT_USB    | Booting sequence                    |
|-------------|-----------------|-----------------|-------------------------------------|
| Standard    | Low or floating | Low or floating | Onboard eMMC (primary boot storage) |
| Alternative | High            | Low or floating | SD card on SD/SDIO2 interface       |
| SDP mode    | Low or floating | High            | Serial Downloader                   |

## 5.6 Signal Multiplexing Characteristics

Up to 83 of the UCM-iMX93 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX93 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 8 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX93 pins are derived from the i.MX93 SoC control module.

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**NOTE: Pin function selection is controlled by software.**

**NOTE: Each pin can be used for a single function at a time.**

**NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).**

**NOTE: An empty MUX mode is a “RESERVED” function and must not be used.**

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**Table 56 Multifunctional Signals**

| Pin # | SoC Pin Name    | Alt0              | Alt1       | Alt2      | Alt3        | Alt4        | Alt5         | Alt6      | Voltage Domain | Availability |
|-------|-----------------|-------------------|------------|-----------|-------------|-------------|--------------|-----------|----------------|--------------|
| P1-19 | UART2_RXD       | UART2_RX          | UART1_CTS  | SPI2_SOUT | TPM1_CH2    | SAI1_MCLK   | GPIO1_IO[6]  |           | 3.3V           | Always       |
| P1-21 | PDM_CLK         | PDM_CLK           | MQS1_LEFT  |           |             |             | GPIO1_IO[8]  | CAN1_TX   | 3.3V           | Always       |
| P1-23 | PDM_BIT_STREAM0 | PDM_BIT_STREAM[0] | MQS1_RIGHT | SPI1_PCS1 | TPM1_EXTCLK |             | GPIO1_IO[9]  | CAN1_RX   | 3.3V           | Always       |
| P1-26 | GPIO_IO01       | GPIO2_IO[1]       | I2C3_SCL   |           |             | SPI6_SIN    | UART5_RX     | I2C5_SCL  | 3.3V           | Always       |
| P1-28 | GPIO_IO00       | GPIO2_IO[0]       | I2C3_SDA   |           |             | SPI6_PCS0   | UART5_TX     | I2C5_SDA  | 3.3V           | Always       |
| P1-30 | GPIO_IO02       | GPIO2_IO[2]       | I2C4_SDA   |           |             | SPI6_SOUT   | UART5_CTS    | I2C6_SDA  | 3.3V           | Always       |
| P1-32 | GPIO_IO03       | GPIO2_IO[3]       | I2C4_SCL   |           |             | SPI6_SCK    | UART5_RTS    | I2C6_SCL  | 3.3V           | Always       |
| P1-33 | GPIO_IO25       | GPIO2_IO[25]      |            | CAN2_TX   |             | TPM4_CH3    |              | SPI7_PCS1 | 3.3V           | Always       |
| P1-35 | GPIO_IO10       | GPIO2_IO[10]      | SPI3_SOUT  |           |             | TPM4_EXTCLK | UART7_CTS    | I2C8_SDA  | 3.3V           | Always       |
| P1-37 | GPIO_IO11       | GPIO2_IO[11]      | SPI3_SCK   |           |             | TPM5_EXTCLK | UART7_RTS    | I2C8_SCL  | 3.3V           | Always       |
| P1-39 | GPIO_IO08       | GPIO2_IO[8]       | SPI3_PCS0  |           |             | TPM6_CH0    | UART7_TX     | I2C7_SDA  | 3.3V           | Always       |
| P1-41 | GPIO_IO09       | GPIO2_IO[9]       | SPI3_SIN   |           |             | TPM3_EXTCLK | UART7_RX     | I2C7_SCL  | 3.3V           | Always       |
| P1-45 | SAI1_RXD0       | SAI1_RX_DATA[0]   | SAI1_MCLK  | SPI1_SOUT | UART2_DSR   | MQS1_RIGHT  | GPIO1_IO[14] |           | 3.3V           | Always       |

|        |                  |                 |                 |                   |           |           |              |           |      |             |
|--------|------------------|-----------------|-----------------|-------------------|-----------|-----------|--------------|-----------|------|-------------|
| P1-49  | GPIO_IO27        | GPIO2_IO[27]    |                 | CAN2_RX           |           | TPM6_CH3  |              | SPI5_PCS1 | 3.3V | Always      |
| P1-51  | SAI1_TXC         | SAI1_TX_BCLK    | UART2_CTS       | SPI1_SIN          | UART1_DSR | CAN1_RX   | GPIO1_IO[12] |           | 3.3V | Always      |
| P1-53  | SAI1_TXD0        | SAI1_TX_DATA[0] | UART2_RTS       | SPI1_SCK          |           | CAN1_TX   |              |           | 3.3V | Output only |
| P1-59  | GPIO_IO19        | GPIO2_IO[19]    |                 | PDM_BIT_STREAM[3] |           | SPI5_SIN  | SPI4_SIN     | TPM6_CH2  | 3.3V | Always      |
| P1-60  | GPIO_IO15        | GPIO2_IO[15]    | UART3_RX        |                   |           |           |              | UART4_RX  | 3.3V | Always      |
| P1-61  | GPIO_IO20        | GPIO2_IO[20]    |                 | PDM_BIT_STREAM[0] |           | SPI5_SOUT | SPI4_SOUT    | TPM3_CH1  | 3.3V | Always      |
| P1-63  | GPIO_IO21        | GPIO2_IO[21]    |                 | PDM_CLK           |           | SPI5_SCK  | SPI4_SCK     | TPM4_CH1  | 3.3V | Always      |
| P1-65  | DAP_TMS_SWDIO    | JTAG_TMS        |                 |                   |           |           | GPIO3_IO[29] | UART5_RTS | 1.8V | Always      |
| P1-67  | DAP_TDO_TRACESWO | JTAG_TDO        | MQS2_RIGHT      |                   | CAN2_RX   |           | GPIO3_IO[31] | UART5_TX  | 1.8V | Always      |
| P1-71  | DAP_TDI          | JTAG_TDI        | MQS2_LEFT       |                   | CAN2_TX   |           | GPIO3_IO[28] | UART5_RX  | 1.8V | Always      |
| P1-72  | UART2_TXD        | UART2_TX        | UART1_RTS       | SPI2_SCK          |           |           |              |           | 3.3V | Output only |
| P1-73  | DAP_TCLK_SWCLK   | JTAG_TCLK       |                 |                   |           |           | GPIO3_IO[30] | UART5_CTS | 1.8V | Always      |
| P1-74  | UART1_TXD        | UART1_TX        |                 | SPI2_PCS0         |           |           |              |           | 3.3V | Output only |
| P1-76  | UART1_RXD        | UART1_RX        |                 | SPI2_SIN          | TPM1_CH0  |           | GPIO1_IO[4]  |           | 3.3V | Always      |
| P1-79  | GPIO_IO22        | GPIO2_IO[22]    |                 | SPDIF1_IN         |           | TPM5_CH1  | TPM6_EXTCLK  | I2C5_SDA  | 3.3V | Always      |
| P1-81  | GPIO_IO23        | GPIO2_IO[23]    |                 | SPDIF1_OUT        |           | TPM6_CH1  |              | I2C5_SCL  | 3.3V | Always      |
| P1-87  | SAI1_TXFS        | SAI1_TX_SYNC    | SAI1_TX_DATA[1] | SPI1_PCS0         |           | MQS1_LEFT |              |           | 3.3V | Output only |
| P1-89  | GPIO_IO18        | GPIO2_IO[18]    |                 |                   |           | SPI5_PCS0 | SPI4_PCS0    | TPM5_CH2  | 3.3V | Always      |
| P1-91  | GPIO_IO28        | GPIO2_IO[28]    | I2C3_SDA        |                   |           |           |              |           | 3.3V | Always      |
| P1-94  | GPIO_IO29        | GPIO2_IO[29]    | I2C3_SCL        |                   |           |           |              |           | 3.3V | Always      |
| P1-95  | GPIO_IO17        | GPIO2_IO[17]    |                 |                   |           | UART3_RTS | SPI4_PCS1    | UART4_RTS | 3.3V | not WB      |
| P1-96  | GPIO_IO16        | GPIO2_IO[16]    |                 | PDM_BIT_STREAM[2] |           | UART3_CTS | SPI4_PCS2    | UART4_CTS | 3.3V | Always      |
| P1-98  | GPIO_IO07        | GPIO2_IO[7]     | SPI3_PCS1       |                   |           | SPI7_SCK  | UART6_RTS    | I2C7_SCL  | 3.3V | Always      |
| P1-100 | GPIO_IO13        | GPIO2_IO[13]    | TPM4_CH2        | PDM_BIT_STREAM[3] |           |           |              | I2C8_SCL  | 3.3V | Always      |
| P2-36  | SD3_CLK          | SD3_CLK         | FLEXSPI_SCLK    |                   |           |           | GPIO3_IO[20] |           | 1.8V | not WB      |
| P2-38  | SD3_CMD          | SD3_CMD         | FLEXSPI_SS0     |                   |           |           | GPIO3_IO[21] |           | 1.8V | not WB      |
| P2-41  | ENET2_RD0        | ENET2_RD0       | UART4_RX        | SAI2_TX_DATA[2]   |           |           | GPIO4_IO[24] |           | 1.8V | Always      |
| P2-42  | SD3_DATA0        | SD3_DATA0       | FLEXSPI_DATA[0] |                   |           |           | GPIO3_IO[22] |           | 1.8V | not WB      |
| P2-43  | ENET2_RD1        | ENET2_RD1       | SPDIF1_IN       | SAI2_TX_DATA[3]   |           |           | GPIO4_IO[25] |           | 1.8V | Always      |

|       |              |              |                 |                   |            |           |              |          |           |        |
|-------|--------------|--------------|-----------------|-------------------|------------|-----------|--------------|----------|-----------|--------|
| P2-44 | SD3_DATA1    | SD3_DATA1    | FLEXSPI_DATA[1] |                   |            |           | GPIO3_IO[23] |          | 1.8V      | not WB |
| P2-45 | ENET2_RD2    | ENET2_RD2    | UART4_CTS       | SAI2_MCLK         | MQS2_RIGHT |           | GPIO4_IO[26] |          | 1.8V      | Always |
| P2-47 | ENET2_RD3    | ENET2_RD3    | SPDIF1_OUT      | SPDIF1_IN         | MQS2_LEFT  |           | GPIO4_IO[27] |          | 1.8V      | Always |
| P2-48 | SD3_DATA2    | SD3_DATA2    | FLEXSPI_DATA[2] |                   |            |           | GPIO3_IO[24] |          | 1.8V      | not WB |
| P2-50 | SD3_DATA3    | SD3_DATA3    | FLEXSPI_DATA[3] |                   |            |           | GPIO3_IO[25] |          | 1.8V      | not WB |
| P2-51 | SD2_RESET_B  | SD2_RESET    |                 |                   |            |           | GPIO3_IO[7]  |          | 3.3V/1.8V | Always |
| P2-52 | GPIO_IO06    | GPIO2_IO[6]  | TPM5_CH0        | PDM_BIT_STREAM[1] |            | SPI7_SOUT | UART6_CTS    | I2C7_SDA | 3.3V      | not E  |
| P2-53 | ENET2_RX_CTL | ENET2_RX_CTL | UART4_DSR       | SAI2_TX_DATA[0]   |            |           | GPIO4_IO[22] |          | 1.8V      | Always |
| P2-55 | ENET2_RXC    | ENET2_RXC    |                 | SAI2_TX_DATA[1]   |            |           | GPIO4_IO[23] |          | 1.8V      | Always |
| P2-56 | GPIO_IO05    | GPIO2_IO[5]  | TPM4_CH0        | PDM_BIT_STREAM[0] |            | SPI7_SIN  | UART6_RX     | I2C6_SCL | 3.3V      | not E  |
| P2-58 | GPIO_IO04    | GPIO2_IO[4]  | TPM3_CH0        | PDM_CLK           |            | SPI7_PCS0 | UART6_TX     | I2C6_SDA | 3.3V      | not E  |
| P2-59 | ENET2_TD0    | ENET2_TD0    | UART4_TX        | SAI2_RX_DATA[3]   |            |           | GPIO4_IO[19] |          | 1.8V      | Always |
| P2-60 | ENET1_MDC    | ENET1_MDC    | UART3_DCB       | I3C2_SCL          |            |           | GPIO4_IO[0]  |          | 1.8V      | not E  |
| P2-61 | ENET2_TD1    | ENET2_TD1    | UART4_RTS       | SAI2_RX_DATA[2]   |            |           | GPIO4_IO[18] |          | 1.8V      | Always |
| P2-62 | ENET1_MDIO   | ENET1_MDIO   | UART3_RIN       | I3C2_SDA          |            |           | GPIO4_IO[1]  |          | 1.8V      | not E  |
| P2-63 | ENET2_TD3    | ENET2_TD3    |                 | SAI2_RX_DATA[0]   |            |           | GPIO4_IO[16] |          | 1.8V      | Always |
| P2-65 | ENET2_TD2    | ENET2_TD2    |                 | SAI2_RX_DATA[1]   |            |           | GPIO4_IO[17] |          | 1.8V      | Always |
| P2-67 | ENET2_TX_CTL | ENET2_TX_CTL | UART4_DTR       | SAI2_TX_SYNC      |            |           | GPIO4_IO[20] |          | 1.8V      | Always |
| P2-68 | ENET2_MDC    | ENET2_MDC    | UART4_DCB       | SAI2_RX_SYNC      |            |           | GPIO4_IO[14] |          | 1.8V      | Always |
| P2-69 | ENET2_TXC    | ENET2_TXC    |                 | SAI2_TX_BCLK      |            |           | GPIO4_IO[21] |          | 1.8V      | Always |
| P2-70 | ENET2_MDIO   | ENET2_MDIO   | UART4_RIN       | SAI2_RX_BCLK      |            |           | GPIO4_IO[15] |          | 1.8V      | Always |
| P2-73 | ENET1_TX_CTL | ENET1_TX_CTL | UART3_DTR       |                   |            |           | GPIO4_IO[6]  |          | 1.8V      | not E  |
| P2-74 | ENET1_TD3    | ENET1_TD3    |                 | CAN2_TX           |            |           | GPIO4_IO[2]  |          | 1.8V      | not E  |
| P2-75 | ENET1_TD0    | ENET1_TD0    | UART3_TX        |                   |            |           | GPIO4_IO[5]  |          | 1.8V      | not E  |
| P2-76 | GPIO_IO14    | GPIO2_IO[14] | UART3_TX        |                   |            |           |              | UART4_TX | 3.3V      | Always |
| P2-77 | ENET1_TD2    | ENET1_TD2    |                 | CAN2_RX           |            |           | GPIO4_IO[3]  |          | 1.8V      | not E  |
| P2-78 | ENET1_RXC    | ENET1_RXC    |                 |                   |            |           | GPIO4_IO[9]  |          | 1.8V      | not E  |
| P2-79 | ENET1_TXC    | ENET1_TXC    |                 |                   |            |           | GPIO4_IO[7]  |          | 1.8V      | not E  |
| P2-80 | ENET1_TD1    | ENET1_TD1    | UART3_RTS       | I3C2_PUR          |            |           | GPIO4_IO[4]  |          | 1.8V      | not E  |

|        |              |              |                       |           |  |  |              |  |           |        |
|--------|--------------|--------------|-----------------------|-----------|--|--|--------------|--|-----------|--------|
| P2-81  | ENET1_RX_CTL | ENET1_RX_CTL | UART3_DSR             |           |  |  | GPIO4_IO[8]  |  | 1.8V      | not E  |
| P2-83  | ENET1_RD1    | ENET1_RD1    | UART3_CTS             |           |  |  | GPIO4_IO[11] |  | 1.8V      | not E  |
| P2-84  | ENET1_RD2    | ENET1_RD2    |                       |           |  |  | GPIO4_IO[12] |  | 1.8V      | not E  |
| P2-85  | ENET1_RD3    | ENET1_RD3    |                       |           |  |  | GPIO4_IO[13] |  | 1.8V      | not E  |
| P2-86  | ENET1_RD0    | ENET1_RD0    | UART3_RX              |           |  |  | GPIO4_IO[10] |  | 1.8V      | not E  |
| P2-92  | SD2_CD_B     | SD2_CD       | ENET1_1588_EVENT0_IN  | I3C2_SCL  |  |  | GPIO3_IO[0]  |  | 3.3V/1.8V | Always |
| P2-94  | SD2_DATA2    | SD2_DATA2    | ENET2_1588_EVENT1_OUT |           |  |  | GPIO3_IO[5]  |  | 3.3V/1.8V | Always |
| P2-96  | SD2_CLK      | SD2_CLK      | ENET1_1588_EVENT0_OUT | I3C2_SDA  |  |  | GPIO3_IO[1]  |  | 3.3V/1.8V | Always |
| P2-97  | SD2_DATA0    | SD2_DATA0    | ENET2_1588_EVENT0_OUT | CAN2_TX   |  |  | GPIO3_IO[3]  |  | 3.3V/1.8V | Always |
| P2-98  | SD2_DATA3    | SD2_DATA3    |                       | MQS2_LEFT |  |  | GPIO3_IO[6]  |  | 3.3V/1.8V | Always |
| P2-99  | SD2_DATA1    | SD2_DATA1    | ENET2_1588_EVENT1_IN  | CAN2_RX   |  |  | GPIO3_IO[4]  |  | 3.3V/1.8V | Always |
| P2-100 | SD2_CMD      | SD2_CMD      | ENET2_1588_EVENT0_IN  | I3C2_PUR  |  |  | GPIO3_IO[2]  |  | 3.3V/1.8V | Always |

## 5.7 RTC

UCM-iMX93 features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX93 SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about UCM-iMX93 RTC please refer to the AM1805 datasheet.

## 5.8 Reserved Pins

The following pins on UCM-iMX93 interface connectors are reserved and must be left unconnected.

**Table 57 Reserved Signals**

| Connector # | Pin#             |
|-------------|------------------|
| P1          | 25, 84, 92,97,99 |
| P2          | 90               |

## 5.9 Not Connected Pins

The following pins on UCM-iMX93 interface connectors are unconnected.

**Table 58 Unconnected Pins**

| Connector # | Pin#  |
|-------------|---|
| P1          | 9, 13, 15, 29, 31, 34, 36, 38, 42, 44, 46, 47, 48, 50, 52, 55, 56, 62, 70, 77, 85, 86 |
| P2          | 49  |



## 6 CARRIER BOARD INTERFACE

UCM-iMX93 carrier board interface uses two 100-pin carrier board connectors. SoM pinout is detailed in the table below.

### 6.1 Connectors Pinout

**Table 59 Connector P1**

| Pin # | UCM-iMX93 Signal Name   | Ref.                                | Pin # | UCM-iMX93 Signal Name  | Ref.  |
|-------|---|-------------------------------------|-------|--|---|
| 2     | SYS_RST_PMIC  | 5.4                                 | 1     | USB2_VBUS_DET  | 4.6   |
| 4     | GND   | 5.1                                 | 3     | USB2_DP  | 4.6   |
| 6     | NC  | 5.9                                 | 5     | USB2_DN  | 4.6   |
| 8     | NC  | 5.9                                 | 7     | USB2_ID  | 4.6   |
| 10    | GND   | 5.1                                 | 9     | NC   | 5.9   |
| 12    | USB1_DP   | 4.6                                 | 11    | V_SOM  | 5.1   |
| 14    | USB1_DN   | 4.6                                 | 13    | NC   | 5.9   |
| 16    | NC  | 5.9                                 | 15    | NC   | 5.9   |
| 18    | NC  | 5.9                                 | 17    | VSD_3V3  | 5.85.1                                      |
| 20    | GND   | 5.1                                 | 19    | UART2_RX<br>UART1_CTS<br>SPI2_SOUT<br>TPM1_CH2<br>SAI1_MCLK<br>GPIO1_IO[6] | 4.9<br>4.9<br>4.11<br>4.14<br>4.3.2<br>4.18 |
| 22    | USB1_ID   | 4.6                                 | 21    | MQS1_LEFT<br>GPIO1_IO[8]<br>CAN1_TX  | 4.3.3<br>4.18<br>4.10                       |
| 24    | USB1_VBUS_DET   | 4.6                                 | 23    | MQS1_RIGHT<br>SPI1_PCS1<br>TPM1_EXTCLK<br>GPIO1_IO[9]<br>CAN1_RX           | 4.3.3<br>4.11<br>4.14<br>4.18<br>4.10       |
| 26    | GPIO2_IO[1]<br>I2C3_SCL<br>SPI6_SIN<br>UART5_RX<br>I2C5_SCL   | 4.18<br>4.12<br>4.11<br>4.9<br>4.12 | 25    | RESERVED   | 5.8   |
| 28    | GPIO2_IO[0]<br>I2C3_SDA<br>SPI6_PCS0<br>UART5_TX<br>I2C5_SDA  | 4.18<br>4.12<br>4.11<br>4.9<br>4.12 | 27    | V_SOM  | 5.1   |
| 30    | GPIO2_IO[2]<br>I2C4_SDA<br>SPI6_SOUT<br>UART5_CTS<br>I2C6_SDA | 4.18<br>4.12<br>4.11<br>4.9<br>4.12 | 29    | NC   | 5.9   |
| 32    | GPIO2_IO[3]<br>I2C4_SCL<br>SPI6_SCK<br>UART5_RTS<br>I2C6_SCL  | 4.18<br>4.12<br>4.11<br>4.9<br>4.12 | 31    | NC   | 5.9   |
| 34    | NC  | 5.9                                 | 33    | GPIO2_IO[25]<br>CAN2_TX<br>TPM4_CH3<br>SPI7_PCS1                           | 4.18<br>4.10<br>4.14<br>4.11                |

|    |                                      |                    |  |    |  |  |
|----|--------------------------------------|--------------------|--|----|--|--|
| 36 | NC                                   | 5.9                |  | 35 | GPIO2_IO[10]<br>SPI3_SOUT<br>TPM4_EXTCLK<br>UART7_CTS<br>I2C8_SDA                    | 4.18<br>4.11<br>4.14<br>4.9<br>4.12            |
| 38 | NC                                   | 5.9                |  | 37 | GPIO2_IO[11]<br>SPI3_SCK<br>TPM5_EXTCLK<br>UART7_RTS<br>I2C8_SCL                     | 4.18<br>4.11<br>4.14<br>4.9<br>4.12            |
| 40 | GND                                  | 5.1                |  | 39 | GPIO2_IO[8]<br>SPI3_PCS0<br>TPM6_CH0<br>UART7_TX<br>I2C7_SDA                         | 4.18<br>4.11<br>4.14<br>4.9<br>4.12            |
| 42 | NC                                   | 5.9                |  | 41 | GPIO2_IO[9]<br>SPI3_SIN<br>TPM3_EXTCLK<br>UART7_RX<br>I2C7_SCL                       | 4.18<br>4.11<br>4.14<br>4.9<br>4.12            |
| 44 | NC                                   | 5.9                |  | 43 | V_SOM  | 5.1  |
| 46 | NC                                   | 5.9                |  | 45 | SAI1_RX_DATA[0]<br>SAI1_MCLK<br>SPI1_SOUT<br>UART2_DSR<br>MQS1_RIGHT<br>GPIO1_IO[14] | 4.3.2<br>4.3.2<br>4.11<br>4.9<br>4.3.3<br>4.18 |
| 48 | NC                                   | 5.9                |  | 47 | NC   | 5.9  |
| 50 | NC                                   | 5.9                |  | 49 | GPIO2_IO[27]<br>CAN2_RX<br>TPM6_CH3<br>SPI5_PCS1                                     | 4.18<br>4.10<br>4.14<br>4.11                   |
| 52 | NC                                   | 5.9                |  | 51 | SAI1_TX_BCLK<br>UART2_CTS<br>SPI1_SIN<br>UART1_DSR<br>CAN1_RX<br>GPIO1_IO[12]        | 4.3.2<br>4.9<br>4.11<br>4.9<br>4.10<br>4.18    |
| 54 | GND                                  | 5.1                |  | 53 | SAI1_TX_DATA[0]<br>UART2_RTS<br>SPI1_SCK<br>CAN1_TX                                  | 4.3.2<br>4.9<br>4.11<br>4.10                   |
| 56 | NC                                   | 5.9                |  | 55 | NC   | 5.9  |
| 58 | RESERVED                             | 5.8                |  | 57 | V_SOM  | 5.1  |
| 60 | GPIO2_IO[15]<br>UART3_RX<br>UART4_RX | 4.18<br>4.9<br>4.9 |  | 59 | GPIO2_IO[19]<br>SPI5_SIN<br>SPI4_SIN<br>TPM6_CH2                                     | 4.18<br>4.11<br>4.11<br>4.14                   |
| 62 | NC                                   | 5.9                |  | 61 | GPIO2_IO[20]<br>SPI5_SOUT<br>SPI4_SOUT<br>TPM3_CH1                                   | 4.18<br>4.11<br>4.11<br>4.14                   |
| 64 | GND                                  | 5.1                |  | 63 | GPIO2_IO[21]<br>SPI5_SCK<br>SPI4_SCK<br>TPM4_CH1                                     | 4.18<br>4.11<br>4.11<br>4.14                   |
| 66 | PMIC_STBY_REQ                        | 5.3.1              |  | 65 | JTAG_TMS<br>GPIO3_IO[29]<br>UART5_RTS  | 4.17<br>4.18<br>4.9                            |
| 68 | PMIC_ON_REQ                          | 5.3.1              |  | 67 | JTAG_TDO<br>MQS2_RIGHT<br>CAN2_RX<br>GPIO3_IO[31]<br>UART5_TX                        | 4.17<br>4.3.3<br>4.10<br>4.18<br>4.9           |
| 70 | NC                                   | 5.9                |  | 69 | V_SOM  | 5.1  |

|     |   |                                     |    |  |                                       |
|-----|---|-------------------------------------|----|--|---------------------------------------|
| 72  | UART2_TX<br>UART1_RTS<br>SPI2_SCK                             | 4.9<br>4.9<br>4.11                  | 71 | JTAG_TDI<br>MQS2_LEFT<br>CAN2_TX<br>GPIO3_IO[28]<br>UART5_RX     | 4.17<br>4.3.3<br>4.10<br>4.18<br>4.9  |
| 74  | UART1_TX<br>SPI2_PCS0   | 4.9<br>4.11                         | 73 | JTAG_TCLK<br>GPIO3_IO[30]<br>UART5_CTS                           | 4.17<br>4.18<br>4.9                   |
| 76  | UART1_RX<br>SPI2_SIN<br>TPM1_CH0<br>GPIO1_IO[4]               | 4.9<br>4.11<br>4.14<br>4.18         | 75 | RESERVED   | 5.8                                   |
| 78  | GND   | 5.1                                 | 77 | NC   |                                       |
| 80  | RESERVED  | 5.8                                 | 79 | GPIO2_IO[22]<br>SPDIF1_IN<br>TPM5_CH1<br>TPM6_EXTCLK<br>I2C5_SDA | 4.18<br>4.3.1<br>4.14<br>4.14<br>4.12 |
| 82  | RESERVED  | 5.8                                 | 81 | GPIO2_IO[23]<br>SPDIF1_OUT<br>TPM6_CH1<br>I2C5_SCL               | 4.18<br>4.3.1<br>4.14<br>4.12         |
| 84  | RESERVED  | 5.8                                 | 83 | V_SOM  | 5.1                                   |
| 86  | NC  | 5.9                                 | 85 | NC   | 5.9                                   |
| 88  | GND   | 5.1                                 | 87 | SAI1_TX_SYNC<br>SAI1_TX_DATA[1]<br>SPI1_PCS0<br>MQS1_LEFT        | 4.3.2<br>4.3.2<br>4.11<br>4.94<br>3.3 |
| 90  | ALT_BOOT  | 5.5                                 | 89 | GPIO2_IO[18]<br>SPI5_PCS0<br>SPI4_PCS0<br>TPM5_CH2               | 4.18<br>4.11<br>4.11<br>4.14          |
| 92  | RESERVED  | 5.8                                 | 91 | GPIO2_IO[28]<br>I2C3_SDA   | 4.18<br>4.12                          |
| 94  | GPIO2_IO[29]<br>I2C3_SCL                                      | 4.18<br>4.12                        | 93 | VCC_RTC  | 5.1                                   |
| 96  | GPIO2_IO[16]<br>UART3_CTS<br>SPI4_PCS2<br>UART4_CTS           | 4.18<br>4.9<br>4.11<br>4.9          | 95 | GPIO2_IO[17]<br>UART3_RTS<br>SPI4_PCS1<br>UART4_RTS              | 4.18<br>4.9<br>4.11<br>4.9            |
| 98  | GPIO2_IO[7]<br>SPI3_PCS1<br>SPI7_SCK<br>UART6_RTS<br>I2C7_SCL | 4.18<br>4.11<br>4.11<br>4.9<br>4.12 | 97 | RESERVED   | 5.8                                   |
| 100 | GPIO2_IO[13]<br>TPM4_CH2<br>I2C8_SCL                          | 4.18<br>4.14<br>4.12                | 99 | RESERVED   | 5.8                                   |

**Table 60 Connector P2**

| Pin # | UCM-iMX93<br>Signal Name | Ref.  | Pin # | UCM-iMX93<br>Signal Name | Ref.  |
|-------|--------------------------|-------|-------|--------------------------|-------|
| 2     | LVDS_TX3_P               | 4.1.2 | 1     | DSI_D0_N                 | 4.1.1 |
| 4     | LVDS_TX3_N               | 4.1.2 | 3     | DSI_D0_P                 | 4.1.1 |
| 6     | LVDS_TX2_P               | 4.1.2 | 5     | DSI_D2_N                 | 4.1.1 |
| 8     | LVDS_TX2_N               | 4.1.2 | 7     | DSI_D2_P                 | 4.1.1 |
| 10    | GND                      | 5.1   | 9     | V_SOM                    | 5.1   |
| 12    | LVDS_CLK_P               | 4.1.2 | 11    | DSI_D3_N                 | 4.1.1 |
| 14    | LVDS_CLK_N               | 4.1.2 | 13    | DSI_D3_P                 | 4.1.1 |
| 16    | GND                      | 5.1   | 15    | DSI_D1_N                 | 4.1.1 |
| 18    | LVDS_TX1_P               | 4.1.2 | 17    | DSI_D1_P                 | 4.1.1 |

|    |   |   |    |   |   |
|----|---|---|----|---|---|
| 20 | LVDS_TX1_N  | 4.1.2                                   | 19 | V_SOM   | 5.1                                       |
| 22 | GND   | 5.1                                     | 21 | DSI_CLK_N   | 4.1.1                                     |
| 24 | LVDS_TX0_P  | 4.1.2                                   | 23 | DSI_CLK_P   | 4.1.1                                     |
| 26 | LVDS_TX0_N  | 4.1.2                                   | 25 | TAMPER0   | 4.16                                      |
| 28 | GND   | 5.1                                     | 27 | TAMPER1   | 4.16                                      |
| 30 | CSI_CLK_N   | 4.2                                     | 29 | V_SOM   | 5.1                                       |
| 32 | CSI_CLK_P   | 4.2                                     | 31 | CSI_D0_N  | 4.2                                       |
| 34 | GND   | 5.1                                     | 33 | CSI_D0_P  | 4.2                                       |
| 36 | SD3_CLK<br>FLEXSPI_SCLK<br>GPIO3_IO[20]                       | 4.7<br>4.8<br>4.1.8                     | 35 | CSI_D1_N  | 4.2                                       |
| 38 | SD3_CMD<br>FLEXSPI_SSO<br>GPIO3_IO[21]                        | 4.7<br>4.8<br>4.1.8                     | 37 | CSI_D1_P  | 4.2                                       |
| 40 | GND   | 5.1                                     | 39 | V_SOM   | 5.1                                       |
| 42 | SD3_DATA0<br>FLEXSPI_DATA[0]<br>GPIO3_IO[22]                  | 4.7<br>4.8<br>4.1.8                     | 41 | ENET2_RD0<br>UART4_RX<br>SAI2_TX_DATA[2]<br>GPIO4_IO[24]          | 4.4.2<br>4.9<br>4.3.2<br>4.1.8            |
| 44 | SD3_DATA1<br>FLEXSPI_DATA[1]<br>GPIO3_IO[23]                  | 4.7<br>4.8<br>4.1.8                     | 43 | ENET2_RD1<br>SPDIF1_IN<br>SAI2_TX_DATA[3]<br>GPIO4_IO[25]         | 4.4.2<br>4.3.1<br>4.3.2<br>4.1.8          |
| 46 | GND   | 5.1                                     | 45 | ENET2_RD2<br>UART4_CTS<br>SAI2_MCLK<br>MQS2_RIGHT<br>GPIO4_IO[26] | 4.4.2<br>4.9<br>4.3.2<br>4.3.3<br>4.1.8   |
| 48 | SD3_DATA2<br>FLEXSPI_DATA[2]<br>GPIO3_IO[24]                  | 4.7<br>4.8<br>4.1.8                     | 47 | ENET2_RD3<br>SPDIF1_OUT<br>SPDIF1_IN<br>MQS2_LEFT<br>GPIO4_IO[27] | 4.4.2<br>4.3.1<br>4.3.1<br>4.3.3<br>4.1.8 |
| 50 | SD3_DATA3<br>FLEXSPI_DATA[3]<br>GPIO3_IO[25]                  | 4.7<br>4.8<br>4.1.8                     | 49 | NC  | 5.9                                       |
| 52 | GPIO2_IO[6]<br>TPM5_CH0<br>SPI7_SOUT<br>UART6_CTS<br>I2C7_SDA | 4.1.8<br>4.1.4<br>4.1.1<br>4.9<br>4.1.2 | 51 | SD2_RESET<br>GPIO3_IO[7]  | 4.7<br>4.1.8                              |
| 54 | GND   | 5.1                                     | 53 | ENET2_RX_CTL<br>UART4_DSR<br>SAI2_TX_DATA[0]<br>GPIO4_IO[22]      | 4.4.2<br>4.9<br>4.3.2<br>4.1.8            |
| 56 | GPIO2_IO[5]<br>TPM4_CH0<br>SPI7_SIN<br>UART6_RX<br>I2C6_SCL   | 4.1.8<br>4.1.4<br>4.1.1<br>4.9<br>4.1.2 | 55 | ENET2_RXC<br>SAI2_TX_DATA[1]<br>GPIO4_IO[23]                      | 4.4.2<br>4.3.2<br>4.1.8                   |
| 58 | GPIO2_IO[4]<br>TPM3_CH0<br>SPI7_PCS0<br>UART6_TX<br>I2C6_SDA  | 4.1.8<br>4.1.4<br>4.1.1<br>4.9<br>4.1.2 | 57 | V_SOM   | 5.1                                       |
| 60 | ENET1_MDC<br>UART3_DCB<br>I3C2_SCL<br>GPIO4_IO[0]             | 4.4.2<br>4.9<br>4.1.3<br>4.1.8          | 59 | ENET2_TD0<br>UART4_TX<br>SAI2_RX_DATA[3]<br>GPIO4_IO[19]          | 4.4.2<br>4.9<br>4.3.2<br>4.1.8            |
| 62 | ENET1_MDIO<br>UART3_RIN<br>I3C2_SDA<br>GPIO4_IO[1]            | 4.4.2<br>4.9<br>4.1.3<br>4.1.8          | 61 | ENET2_TD1<br>UART4_RTS<br>SAI2_RX_DATA[2]<br>GPIO4_IO[18]         | 4.4.2<br>4.9<br>4.3.2<br>4.1.8            |
| 64 | ONOFF   | 5.3.1                                   | 63 | ENET2_TD3<br>SAI2_RX_DATA[0]<br>GPIO4_IO[16]                      | 4.4.2<br>4.3.2<br>4.1.8                   |

|     |   |                                       |    |  |                               |
|-----|---|---------------------------------------|----|--|-------------------------------|
| 66  | POR_B   | 5.4                                   | 65 | ENET2_TD2<br>SAI2_RX_DATA[1]<br>GPIO4_IO[17]                 | 4.4.2<br>4.3.2<br>4.18        |
| 68  | ENET2_MDC<br>UART4_DCB<br>SAI2_RX_SYNC<br>GPIO4_IO[14]          | 4.4.2<br>4.9<br>4.3.2<br>4.18         | 67 | ENET2_TX_CTL<br>UART4_DTR<br>SAI2_TX_SYNC<br>GPIO4_IO[20]    | 4.4.2<br>4.9<br>4.3.2<br>4.18 |
| 70  | ENET2_MDIO<br>UART4_RIN<br>SAI2_RX_BCLK<br>GPIO4_IO[15]         | 4.4.2<br>4.9<br>4.3.2<br>4.18         | 69 | ENET2_TXC<br>SAI2_TX_BCLK<br>GPIO4_IO[21]                    | 4.4.2<br>4.3.2<br>4.18        |
| 72  | GND   | 5.1                                   | 71 | V_SOM  | 5.1                           |
| 74  | ETH0_MDI0P<br>ENET1_TD3<br>CAN2_TX<br>GPIO4_IO[2]               | 4.4.1<br>4.4.2<br>4.10<br>4.18        | 73 | ETH0_MDI0N<br>ENET1_TX_CTL<br>UART3_DTR<br>GPIO4_IO[6]       | 4.4.1<br>4.4.2<br>4.9<br>4.18 |
| 76  | GPIO2_IO[14]<br>UART3_TX<br>UART4_TX                            | 4.18<br>4.9<br>4.9                    | 75 | ETH0_LINK-LED_1000<br>ENET1_TD0<br>UART3_TX<br>GPIO4_IO[5]   | 4.4.1<br>4.4.2<br>4.9<br>4.18 |
| 78  | ETH0_MDI1P<br>ENET1_RXC<br>GPIO4_IO[9]                          | 4.4.1<br>4.4.2<br>4.18                | 77 | ENET1_TD2<br>CAN2_RX<br>GPIO4_IO[3]                          | 4.4.2<br>4.10<br>4.18         |
| 80  | ETH0_MDI1N<br>ENET1_TD1<br>UART3_RTS<br>I3C2_PUR<br>GPIO4_IO[4] | 4.4.1<br>4.4.2<br>4.9<br>4.13<br>4.18 | 79 | ETH0_MDI2P<br>ENET1_TXC<br>GPIO4_IO[7]                       | 4.4.1<br>4.4.2<br>4.18        |
| 82  | GND   | 5.1                                   | 81 | ETH0_MDI2N<br>ENET1_RX_CTL<br>UART3_DSR<br>GPIO4_IO[8]       | 4.4.1<br>4.4.2<br>4.9<br>4.18 |
| 84  | ETH0_MDI3P<br>ENET1_RD2<br>GPIO4_IO[12]                         | 4.4.1<br>4.4.2<br>4.18                | 83 | ETH0_LED_ACT<br>ENET1_RD1<br>UART3_CTS<br>GPIO4_IO[11]       | 4.4.1<br>4.4.2<br>4.9<br>4.18 |
| 86  | ETH0_LINK-LED_10_100<br>ENET1_RDO<br>UART3_RX<br>GPIO4_IO[10]   | 4.4.1<br>4.4.2<br>4.9<br>4.18         | 85 | ETH0_MDI3N<br>ENET1_RD3<br>GPIO4_IO[13]                      | 4.4.1<br>4.4.2<br>4.18        |
| 88  | ALT_BOOT_USB  | 5.5                                   | 87 | V_SOM  | 5.1                           |
| 90  | RESERVED  | 5.8                                   | 89 | ADC_IN0  | 4.15                          |
| 92  | SD2_CD<br>ENET1_1588_EVENT0_IN<br>I3C2_SCL<br>GPIO3_IO[0]       | 4.7<br>4.4.2<br>4.13<br>4.18          | 91 | ADC_IN1  | 4.15                          |
| 94  | SD2_DATA2<br>ENET2_1588_EVENT1_OUT<br>GPIO3_IO[5]               | 4.7<br>4.4.2<br>4.18                  | 93 | ADC_IN2  | 4.15                          |
| 96  | SD2_CLK<br>ENET1_1588_EVENT0_OUT<br>I3C2_SDA<br>GPIO3_IO[1]     | 4.7<br>4.4.2<br>4.13<br>4.18          | 95 | ADC_IN3  | 4.15                          |
| 98  | SD2_DATA3<br>MQS2_LEFT<br>GPIO3_IO[6]                           | 4.7<br>4.3.3<br>4.18                  | 97 | SD2_DATA0<br>ENET2_1588_EVENT0_OUT<br>CAN2_TX<br>GPIO3_IO[3] | 4.7<br>4.4.2<br>4.10<br>4.18  |
| 100 | SD2_CMD<br>ENET2_1588_EVENT0_IN<br>I3C2_PUR<br>GPIO3_IO[2]      | 4.7<br>4.4.2<br>4.13<br>4.18          | 99 | SD2_DATA1<br>ENET2_1588_EVENT1_IN<br>CAN2_RX<br>GPIO3_IO[4]  | 4.7<br>4.4.2<br>4.10<br>4.18  |

## 6.2 Mating Connectors

**Table 61 Connector type**

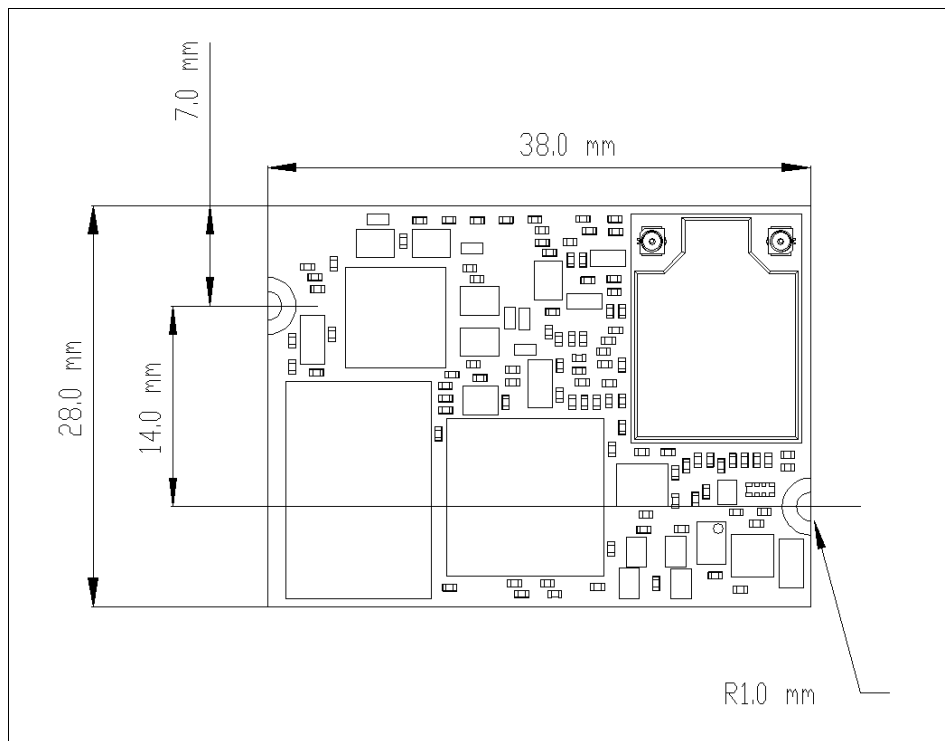
| UCM-iMX93 connector |                           | Carrier board (mating) connector P/N |                            |               |
|---------------------|---------------------------|--------------------------------------|----------------------------|---------------|
| Ref.                | Implementation            | Mfg.                                 | P/N                        | Mating Height |
| P1, P2              | Hirose DF40C-100DP-0.4V51 | Hirose                               | DF40HC(3.0)-100DS-0.4V(51) | 3.0mm         |
|                     |                           | Hirose                               | DF40C-100DS-0.4V51         | 1.5mm         |

## 6.3 Mechanical Drawings

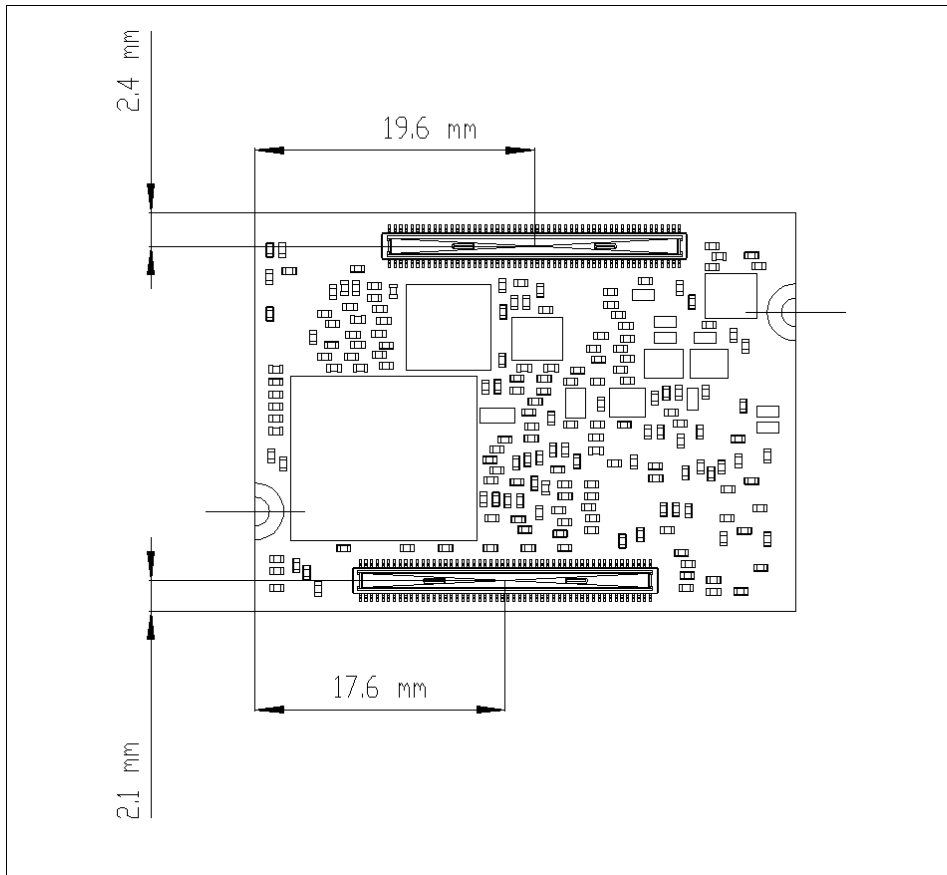
- All dimensions are in millimeters.
- The height of top side components is < 2.0mm.
- Carrier-board connectors provide  $1.5 \pm 0.15\text{mm}$  board-to-board clearance.
- Board thickness is 1.6mm.

3D model and mechanical drawings in DXF format are available at <https://www.compulab.com/products/computer-on-modules/ucm-imx93-nxp-i-mx9-som-system-on-module-computer/#devres>

**Figure 3 UCM-iMX93 top**



**Figure 4 UCM-iMX93 bottom**



## 7 OPERATIONAL CHARACTERISTICS

### 7.1 Absolute Maximum Ratings

**Table 62 Absolute Maximum ratings**

| Parameter                               | Min  | Max | Unit |
|---|------|-----|------|
| Main power supply voltage (V_SOM)       | -0.3 | 6.0 | V    |
| Voltage on any non-power supply pin     | -0.5 | 3.6 | V    |
| Backup battery supply voltage (VCC_RTC) | -0.3 | 3.8 | V    |

**NOTE:** Exceeding the absolute maximum ratings may damage the device.

### 7.2 Recommended Operating Conditions

**Table 63 Recommended Operating Conditions**

| Parameter                               | Min  | Typ. | Max | Unit |
|---|------|------|-----|------|
| Main power supply voltage (V_SOM)       | 3.45 | 3.7  | 5.5 | V    |
| Backup battery supply voltage (VCC_RTC) | 1.5  | 3.0  | 3.6 | V    |

### 7.3 Typical Power Consumption

**Table 64 SOM Typical Power Consumption**

| Use case              | Use case description                              | I <sub>SOM</sub> | P <sub>SOM</sub> |
|-----------------------|---|------------------|------------------|
| Linux up – low-power  | Linux up, Ethernet down, display output off       | 175mA            | 0.64W            |
| Linux up – typical    | Linux up, Ethernet link up, display output on LCD | 300mA            | 1.11W            |
| High CPU load         | CPU stress test (stress-ng)                       | 445mA            | 1.64W            |
| Mixed peripheral load | Ethernet activity + flashing large file to eMMC   | 570mA            | 2.11W            |

Power consumption has been measured with the following setup:

1. Stock module configuration - UCM-IMX93-C1500D-D2-N32-E-WB
2. SB-UCMIMX93 carrier-board, V\_SOM = 3.7V
3. 5" WXGA LCD panel
4. Ambient temperature of 25C

**Table 65 OFF Power Consumption**

| Use case | Use case description       | I <sub>SOM</sub> | P <sub>SOM</sub> |
|----------|----------------------------|------------------|------------------|
| OFF mode | Linux shutdown / power-off | 1mA              |                  |

**Table 66 RTC timekeeping current**

| Use case | Use case description   | I <sub>VCC_RTC</sub> |
|----------|--|----------------------|
| RTC only | VCC_RTC (3.0V) is supplied from external coin-cell battery<br>V_SOM is not present | 70nA                 |

### 7.4 ESD Performance

**Table 67 ESD Performance**

| Interface   | ESD Performance  |
|-------------|--|
| i.MX93 pins | 2kV Human Body Model (HBM), 500V Charge Device Model (CDM) |



## 8 APPLICATION NOTES

---

### 8.1 Carrier Board Design Guidelines

- Ensure that all V\_SOM and GND power pins are connected.
- Major power rails - V\_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V\_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX93 operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX93.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Bear in mind that there are components on the bottom side of UCM-iMX93. It is not recommended to place any components underneath the UCM-iMX93 module.
- Refer to the SB-UCMIMX93 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

### 8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V\_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX93, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX93 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.