

# UCM-iMX8M-Plus

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Reference Guide



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**Table 1 Revision Notes**

| Date           | Description                                                                                                                                                                                      |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Mar 2021       | <ul style="list-style-type: none"> <li>Initial release</li> </ul>                                                                                                                                |
| September 2021 | <ul style="list-style-type: none"> <li>Removed USB_ID signals from tables 17, 18, 44</li> </ul>                                                                                                  |
| November 2021  | <ul style="list-style-type: none"> <li>Updated RGMII VIO information in section 4.5.2</li> </ul>                                                                                                 |
| March 2022     | <ul style="list-style-type: none"> <li>Added clarifications for RGMII pins operating voltage in sections 4.5.2 and 4.17</li> </ul>                                                               |
| April 2022     | <ul style="list-style-type: none"> <li>Updated ECSPI section 4.14</li> <li>Updated section 4.5.1 to reflect PHY change in rev1.1</li> <li>Added power consumption data in section 7.3</li> </ul> |
| June 2022      | <ul style="list-style-type: none"> <li>Fixed GPIO4_IO17 pin number in section 4.17</li> <li>Added section 6.4</li> </ul>                                                                         |
| October 2022   | <ul style="list-style-type: none"> <li>Updated PCIe reference clock information in section 4.6</li> </ul>                                                                                        |
| January 2023   | <ul style="list-style-type: none"> <li>Corrected description of reserved signals in section 6.1</li> <li>Corrected description of RGMII0 VIO in section 5.1</li> </ul>                           |
| November 2023  | <ul style="list-style-type: none"> <li>Added voltage domain section 5.2</li> </ul>                                                                                                               |
| January 2026   | <ul style="list-style-type: none"> <li>Updated V_SOM range</li> </ul>                                                                                                                            |
| June 2026      | <ul style="list-style-type: none"> <li>Updated default voltage note in section 4.10</li> </ul>                                                                                                   |

Please check for a newer revision of this manual at the Compulab website <https://www.compulab.com>. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

# 1 INTRODUCTION

## 1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program Compulab UCM-iMX8M-Plus System-on-Module.

## 1.2 UCM-iMX8M-Plus Part Number Legend

Please refer to the Compulab website ‘Ordering information’ section to decode the UCM-iMX8M-Plus part number: <https://www.compulab.com/products/computer-on-modules/ucm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#ordering>.

## 1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

**Table 2** Related Documents

| Document                           | Location                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UCM-iMX8M-Plus Developer Resources | <a href="https://www.compulab.com/products/computer-on-modules/ucm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres">https://www.compulab.com/products/computer-on-modules/ucm-imx8m-plus-nxp-i-mx-8m-plus-som-system-on-module-computer/#devres</a>                                                                                                                                                                                                                               |
| i.MX8M Plus Reference Manual       | <a href="https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation">https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation</a> Tab |
| i.MX8M Plus Datasheet              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

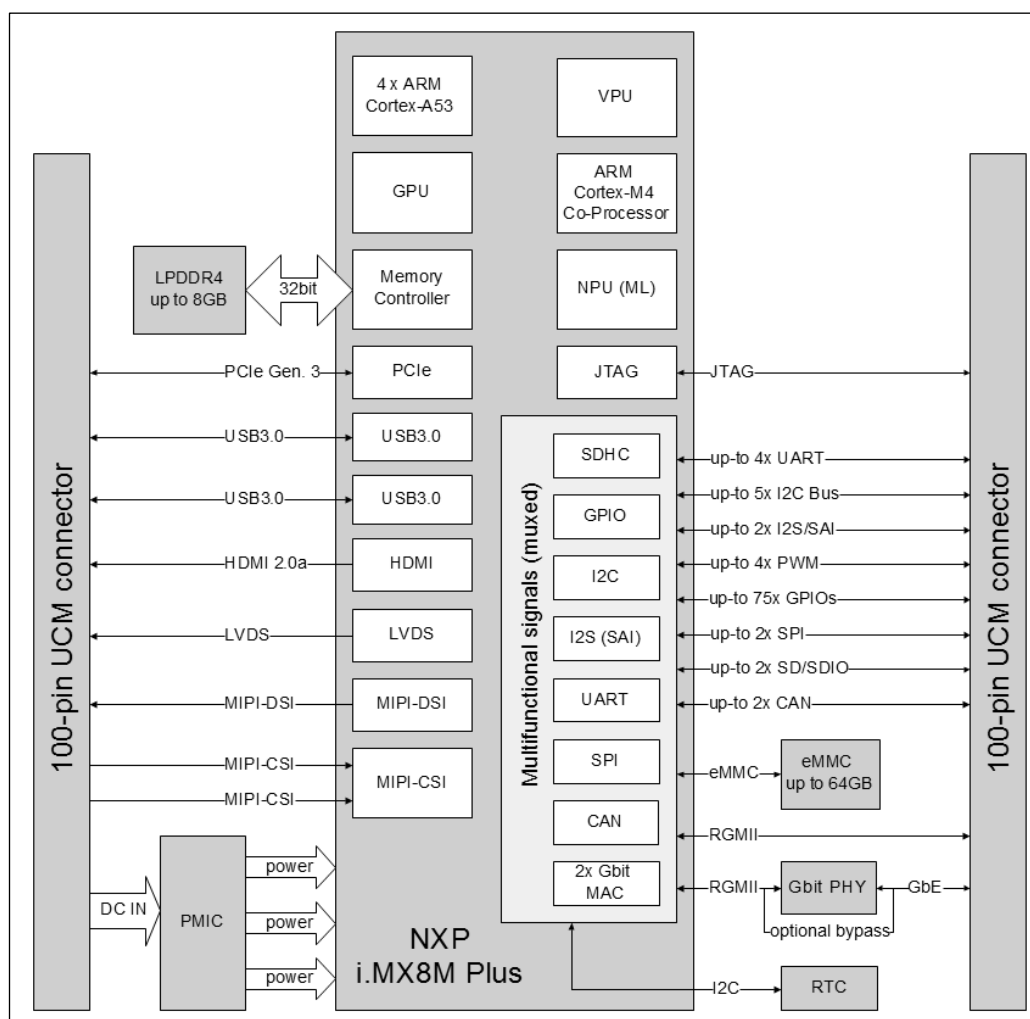
## 2 OVERVIEW

### 2.1 Highlights

- NXP i.MX8M Plus Processor, up-to 1.8GHz
- Up to 8GB LPDDR4 and 64GB eMMC
- 2D/3D GPU, 1080p VPU and audio DSP
- Integrated AI/ML Neural Processing Unit
- HDMI, LVDS, MIPI-DSI
- 2x MIPI-CSI camera inputs with dedicated ISP
- PCIe, GbE, RGMII, 2x USB3.0
- 2x CAN, 4x UART, 75x GPIO
- Tiny size and weight - 28 x 38 x 4 mm, 7 gram

### 2.2 Block Diagram

Figure 1 UCM-iMX8M-Plus Block Diagram



## 2.3 UCM-iMX8M-Plus Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by "NOT", the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the "Option" column.

"+" means that the feature is always available.

**Table 3 Features and Configuration options**

| Feature                      | Description                                                                                        | Option  |
|------------------------------|----------------------------------------------------------------------------------------------------|---------|
| <b>CPU Core and Graphics</b> |                                                                                                    |         |
| CPU                          | NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.8GHz                                             | C1800QM |
|                              | NXP i.MX8M Plus QuadLite, quad-core ARM Cortex-A53, 1.8GHz                                         | C1800Q  |
| Video Decode                 | 1080p60 HEVC/H.265, AVC/H.264, VP9, VP8                                                            | C1800QM |
| Video Encode                 | 1080p60 HEVC/H.265, AVC/H.264                                                                      | C1800QM |
| GPU                          | GC7000UL (3D): OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.1/1.2;<br>GC520L (2D): DirectFB, GDI/DirectDraw | +       |
| NPU                          | AI/ML Neural Processing Unit, up to 2.3 TOPS                                                       | C1800QM |
| Real-Time Co-processor       | ARM Cortex-M7 @ 800 Mhz                                                                            | +       |
| DSP                          | Tensilica® HiFi 4 DSP                                                                              | C1800QM |
| <b>Memory and Storage</b>    |                                                                                                    |         |
| RAM                          | 1GB – 8GB, LPDDR4                                                                                  | D       |
| Storage                      | eMMC flash, 16GB - 64GB                                                                            | N       |
| <b>Display and Camera</b>    |                                                                                                    |         |
| Display                      | HDMI 2.0a, up to 1080p60                                                                           | +       |
|                              | MIPI-DSI, 4 data lanes, up to 1080p60                                                              | +       |
|                              | LVDS, 4 lanes, up to 1366x768 p60                                                                  | +       |
| Touchscreen                  | Capacitive touch-screen support through eSPI and I2C interfaces                                    | +       |
| Camera                       | 2x MIPI-CSI, 4 data lanes                                                                          | +       |
| <b>Network</b>               |                                                                                                    |         |
| Ethernet                     | Gigabit Ethernet port (MAC+PHY)                                                                    | +       |
| RGMII                        | Primary RGMII                                                                                      | Not E   |
|                              | Secondary RGMII                                                                                    | +       |
| <b>Audio</b>                 |                                                                                                    |         |
| Digital Audio                | Up-to 2x I2S / SAI                                                                                 | +       |
|                              | eARC                                                                                               | +       |
|                              | S/PDIF input/output                                                                                | +       |
| <b>I/O</b>                   |                                                                                                    |         |
| PCI Express                  | PCIe Gen. 3.0 x1                                                                                   | +       |
| USB                          | 2x USB3.0 (one host, one dual-role)                                                                | +       |
| UART                         | Up to 4x UART                                                                                      | +       |
| CAN bus                      | Up-to 2x CAN                                                                                       | +       |
| MMC/SD/SDIO                  | Up to 2x SD/SDIO                                                                                   | +       |
| SPI                          | Up to 2x SPI                                                                                       | +       |
| I2C                          | Up to 5x I2C                                                                                       | +       |
| PWM                          | Up to 4x general purpose PWM signals                                                               | +       |
| GPIO                         | Up to 75x GPIO (multifunctional signals shared with other functions)                               | +       |
| <b>System Logic</b>          |                                                                                                    |         |
| RTC                          | Real-time clock, powered by external battery                                                       | +       |
| JTAG                         | JTAG debug interface                                                                               | +       |

**Table 4 Electrical, Mechanical and Environmental Specifications**

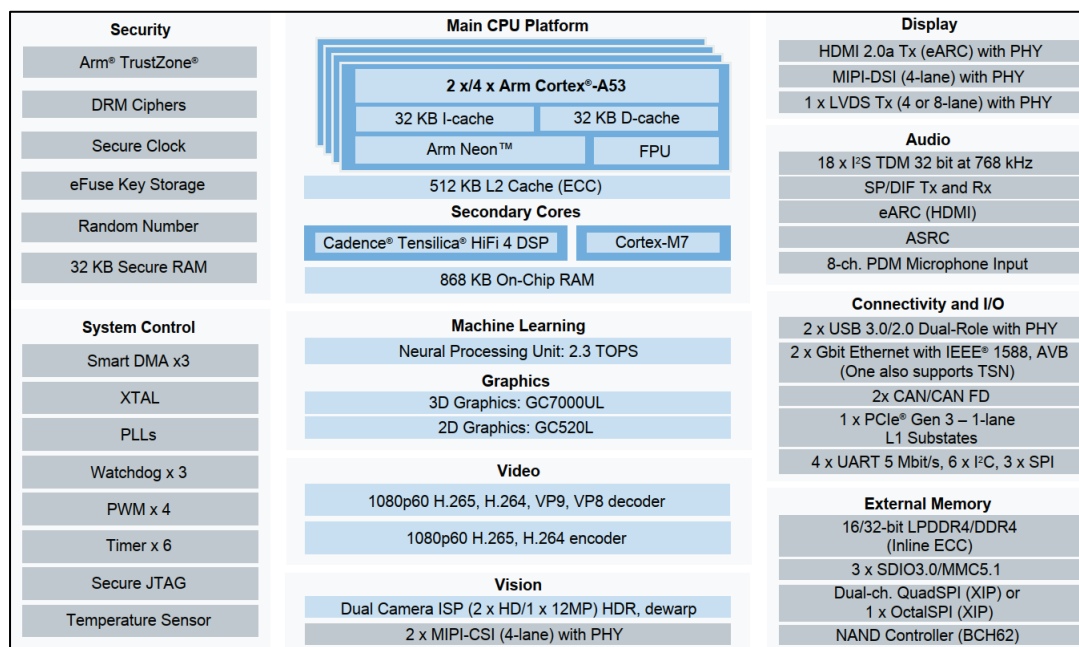
| Electrical Specifications     |                           |
|-------------------------------|---------------------------|
| Supply Voltage                | 3.45V to 5.5V             |
| Digital I/O voltage           | 3.3V                      |
| Mechanical Specifications     |                           |
| Dimensions                    | 28 x 38 x 4 mm            |
| Weight                        | 7 gram                    |
| Connectors                    | 2 x 100 pin, 0.4mm pitch  |
| Environmental and Reliability |                           |
| MTTF                          | > 200,000 hours           |
| Operation temperature (case)  | Commercial: 0° to 70° C   |
|                               | Extended: -20° to 70° C   |
|                               | Industrial: -40° to 85° C |
| Storage temperature           | -40° to 85° C             |
| Relative humidity             | 10% to 90% (operation)    |
|                               | 05% to 95% (storage)      |
| Shock                         | 50G / 20 ms               |
| Vibration                     | 20G / 0 - 600 Hz          |

## 3 CORE SYSTEM COMPONENTS

### 3.1 i.MX8M Plus SoC

The i.MX8M Plus family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M7 core processor enables low-power processing.

**Figure 2 i.MX8M Plus Block Diagram**



### 3.2 Memory

#### 3.2.1 DRAM

UCM-iMX8M-Plus is equipped with up to 8GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide.

#### 3.2.2 Bootloader and General Purpose Storage

UCM-iMX8M-Plus uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

## 4 PERIPHERAL INTERFACES

UCM-iMX8M-Plus implements a variety of peripheral interfaces through 2 x 100-pin (0.4mm pitch) carrier board connectors. The following notes apply to interfaces available through the carrier-board connectors:

- Some interfaces/signals are available only with/without certain configuration options of the UCM-iMX8M-Plus SoM. The availability restrictions of each signal are described in the “Signals description” table for each interface.
- Some of the UCM-iMX8M-Plus carrier board interface pins are multifunctional. Up to 4 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (\*). For additional details, please refer to chapter 5.6.
- All of the UCM-iMX8M-Plus digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#”** – The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **“Type”** – Signal type, see the definition of different signal types below
- **“Description”** – Signal description with regards to the interface in question.
- **“Availability”** – Depending on UCM-iMX8M-Plus configuration options, certain carrier board interface pins are physically disconnected (floating). The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **“O”** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **“PD”** - Always pulled down onboard UCM-IMX8-Plus, followed by pull value.
- **“PU”** - Always pulled up onboard UCM-IMX8-Plus, followed by pull value.
- **“LVDS”** - Low-voltage differential signaling.

## 4.1 HDMI

The UCM-iMX8M-Plus HDMI interface is implemented with the HDMI interface of the i.MX8M Plus SoC. It supports the following main features:

- Compliant with HDMI 2.0a
- HDMI 2.1 eARC
- Supports display resolutions of up-to 1080p60

The following table summarizes the HDMI interface signals.

**Table 5 HDMI Interface Signals**

| Signal Name  | Pin #  | Type | Description                            | Availability     |
|--------------|--------|------|----------------------------------------|------------------|
| HDMI_TXCN    | P1-25  | AO   | Negative part of HDMI clock diff-pair  | Always available |
| HDMI_TXCP    | P1-23  | AO   | Positive part of HDMI clock diff-pair  | Always available |
| HDMI_TX0N    | P1-31  | AO   | Negative part of HDMI data diff-pair 0 | Always available |
| HDMI_TX0P    | P1-29  | AO   | Positive part of HDMI data diff-pair 0 | Always available |
| HDMI_TX1N    | P1-41  | AO   | Negative part of HDMI data diff-pair 1 | Always available |
| HDMI_TX1P    | P1-39  | AO   | Positive part of HDMI data diff-pair 1 | Always available |
| HDMI_TX2N    | P1-47  | AO   | Negative part of HDMI data diff-pair 2 | Always available |
| HDMI_TX2P    | P1-45  | AO   | Positive part of HDMI data diff-pair 2 | Always available |
| HDMI_DDC_SCL | P1-70* | O    | VESA Data Display Channel clock        | Always available |
| HDMI_DDC_SDA | P1-63* | IO   | VESA Data Display Channel data signal  | Always available |
| HDMI_HPD     | P1-92* | AO   | Hot Plug Detect                        | Always available |
| HDMI_CEC     | P1-85* | O    | Consumer Electronics Control signal    | Always available |
| EARC_N_HPD   | P1-35  | AO   |                                        | Always available |
| EARC_P_UTIL  | P1-37  | AO   |                                        | Always available |

**NOTE:** Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document

## 4.2 MIPI-DSI Interface

The UCM-iMX8M-Plus MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Plus SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Maximum resolution ranges up to FHD (1920 x 1080 @ 60 Hz)

The table below summarizes the MIPI-DSI interface signals

**Table 6 MIPI-DSI Interface Signals**

| Signal Name | Pin # | Type | Description                                | Availability     |
|-------------|-------|------|--------------------------------------------|------------------|
| DSI_CKN     | P2-21 | AO   | Negative part of MIPI-DSI clock diff-pair  | Always available |
| DSI_CKP     | P2-23 | AO   | Positive part of MIPI-DSI clock diff-pair  | Always available |
| DSI_DN0     | P2-1  | AO   | Negative part of MIPI-DSI data diff-pair 0 | Always available |
| DSI_DP0     | P2-3  | AO   | Positive part of MIPI-DSI data diff-pair 0 | Always available |
| DSI_DN1     | P2-15 | AO   | Negative part of MIPI-DSI data diff-pair 1 | Always available |
| DSI_DP1     | P2-17 | AO   | Positive part of MIPI-DSI data diff-pair 1 | Always available |
| DSI_DN2     | P2-5  | AO   | Negative part of MIPI-DSI data diff-pair 2 | Always available |

| Signal Name | Pin # | Type | Description                                | Availability     |
|-------------|-------|------|--------------------------------------------|------------------|
| DSI_DP2     | P2-7  | AO   | Positive part of MIPI-DSI data diff-pair 2 | Always available |
| DSI_DN3     | P2-11 | AO   | Negative part of MIPI-DSI data diff-pair 3 | Always available |
| DSI_DP3     | P2-13 | AO   | Positive part of MIPI-DSI data diff-pair 3 | Always available |

## 4.3 LVDS Interface

The UCM-iMX8M-Plus provides one LVDS interface derived from the i.MX8M Plus LVDS display bridge. It supports the following key features:

- Single channel (4 lanes) output at up to 80MHz pixel clock
- Resolutions of up to 1366x768p60

The table below summarizes the LVDS interface signals

**Table 7 LVDS Interface Signals**

| Signal Name | Pin # | Type | Description                            | Availability     |
|-------------|-------|------|----------------------------------------|------------------|
| LVDS0_CLK_N | P1-82 | AO   | Negative part of LVDS clock diff-pair  | Always available |
| LVDS0_CLK_P | P1-80 | AO   | Positive part of LVDS clock diff-pair  | Always available |
| LVDS0_D0_N  | P1-44 | AO   | Negative part of LVDS data diff-pair 0 | Always available |
| LVDS0_D0_P  | P1-42 | AO   | Positive part of LVDS data diff-pair 0 | Always available |
| LVDS0_D1_N  | P1-48 | AO   | Negative part of LVDS data diff-pair 1 | Always available |
| LVDS0_D1_P  | P1-46 | AO   | Positive part of LVDS data diff-pair 1 | Always available |
| LVDS0_D2_N  | P1-52 | AO   | Negative part of LVDS data diff-pair 2 | Always available |
| LVDS0_D2_P  | P1-50 | AO   | Positive part of LVDS data diff-pair 2 | Always available |
| LVDS0_D3_N  | P1-58 | AO   | Negative part of LVDS data diff-pair 3 | Always available |
| LVDS0_D3_P  | P1-56 | AO   | Positive part of LVDS data diff-pair 3 | Always available |

## 4.4 Camera Serial Interface

UCM-iMX8M-Plus provides two MIPI-CSI interfaces, both derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Plus SoC with dedicated Image Signal Processor (ISP). The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Image Signal Processor (ISP):
  - Input formats: YCbCr420, YCbCr422, RAW8/10/12/14, RGB444/555/565/666/888
  - Image cropping, de-noising, LS and CA lens correction, AWB

Please refer to the i.MX8M Plus Reference manual for additional details. The following table summarizes MIPI-CSI signals.

**Table 8 MIPI-CSI Interface Signals**

| Signal Name     | Pin # | Type | Description                                 | Availability     |
|-----------------|-------|------|---------------------------------------------|------------------|
| MIPI_CSI1_CLK_N | P2-2  | AI   | Negative part of MIPI-CSI1 clock diff-pair  | Always available |
| MIPI_CSI1_CLK_P | P2-4  | AI   | Positive part of MIPI-CSI1 clock diff-pair  | Always available |
| MIPI_CSI1_D0_N  | P2-6  | AI   | Negative part of MIPI-CSI1 data diff-pair 0 | Always available |
| MIPI_CSI1_D0_P  | P2-8  | AI   | Positive part of MIPI-CSI1 data diff-pair 0 | Always available |
| MIPI_CSI1_D1_N  | P2-31 | AI   | Negative part of MIPI-CSI1 data diff-pair 1 | Always available |
| MIPI_CSI1_D1_P  | P2-33 | AI   | Positive part of MIPI-CSI1 data diff-pair 1 | Always available |
| MIPI_CSI1_D2_N  | P2-25 | AI   | Negative part of MIPI-CSI1 data diff-pair 2 | Always available |
| MIPI_CSI1_D2_P  | P2-27 | AI   | Positive part of MIPI-CSI1 data diff-pair 2 | Always available |
| MIPI_CSI1_D3_N  | P2-35 | AI   | Negative part of MIPI-CSI1 data diff-pair 3 | Always available |
| MIPI_CSI1_D3_P  | P2-37 | AI   | Positive part of MIPI-CSI1 data diff-pair 3 | Always available |
| MIPI_CSI2_CLK_N | P2-12 | AI   | Negative part of MIPI-CSI2 clock diff-pair  | Always available |
| MIPI_CSI2_CLK_P | P2-14 | AI   | Positive part of MIPI-CSI2 clock diff-pair  | Always available |
| MIPI_CSI2_D0_N  | P2-18 | AI   | Negative part of MIPI-CSI2 data diff-pair 0 | Always available |
| MIPI_CSI2_D0_P  | P2-20 | AI   | Positive part of MIPI-CSI2 data diff-pair 0 | Always available |
| MIPI_CSI2_D1_N  | P2-24 | AI   | Negative part of MIPI-CSI2 data diff-pair 1 | Always available |
| MIPI_CSI2_D1_P  | P2-26 | AI   | Positive part of MIPI-CSI2 data diff-pair 1 | Always available |
| MIPI_CSI2_D2_N  | P2-48 | AI   | Negative part of MIPI-CSI2 data diff-pair 2 | Always available |
| MIPI_CSI2_D2_P  | P2-50 | AI   | Positive part of MIPI-CSI2 data diff-pair 2 | Always available |
| MIPI_CSI2_D3_N  | P2-56 | AI   | Negative part of MIPI-CSI2 data diff-pair 3 | Always available |
| MIPI_CSI2_D3_P  | P2-58 | AI   | Positive part of MIPI-CSI2 data diff-pair 3 | Always available |

## 4.5 Ethernet

### 4.5.1 Gigabit Ethernet

UCM-iMX8M-Plus incorporates an optional (“E” configuration option) full-featured 10/100/1000 Ethernet interface.

UCM-iMX8M-Plus rev1.1 (and higher) implements Ethernet with an optional onboard Realtek RTL8211E GbE PHY.

UCM-iMX8M-Plus rev1.0 implements Ethernet with an optional onboard Atheros AR8033 GbE PHY.

The following main features are supported:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- IEEE 802.3u compliant Auto-Negotiation
- Supports all IEEE 1588 frames - inside the MAC
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Activity and speed indicator LED controls

The table below summarizes the GbE interface signals.

**Table 9 GbE Interface Signals**

| Signal Name          | Pin #  | Type     | Description                                                | Availability         |
|----------------------|--------|----------|------------------------------------------------------------|----------------------|
| ETH0_LED_ACT         | P2-83^ | IO;PD8K2 | Active High, activity LED driver. 2.5V signal, PHY strap   | Only with 'E' option |
| ETH0_LINK-LED_10_100 | P2-86  | IO       | Active High, 10/100Mbps link LED driver. 2.5V signal       | Only with 'E' option |
| ETH0_LINK-LED_1000   | P2-75^ | IO; PD   | Active High, 1Gbps link LED driver. 2.5V signal, PHY strap | Only with 'E' option |
| ETH0_MDI0N           | P2-73  | AIO      | Negative part of 100ohm diff-pair 0                        | Only with 'E' option |

| Signal Name | Pin # | Type | Description                         | Availability         |
|-------------|-------|------|-------------------------------------|----------------------|
| ETH0_MDI0P  | P2-74 | AIO  | Positive part of 100ohm diff-pair 0 | Only with 'E' option |
| ETH0_MDI1N  | P2-80 | AIO  | Negative part of 100ohm diff-pair 1 | Only with 'E' option |
| ETH0_MDI1P  | P2-78 | AIO  | Positive part of 100ohm diff-pair 1 | Only with 'E' option |
| ETH0_MDI2N  | P2-81 | AIO  | Negative part of 100ohm diff-pair 2 | Only with 'E' option |
| ETH0_MDI2P  | P2-79 | AIO  | Positive part of 100ohm diff-pair 2 | Only with 'E' option |
| ETH0_MDI3N  | P2-85 | AIO  | Negative part of 100ohm diff-pair 3 | Only with 'E' option |
| ETH0_MDI3P  | P2-84 | AIO  | Positive part of 100ohm diff-pair 3 | Only with 'E' option |

**NOTE: Pins denoted with "^" must not be pulled or driven by carrier board during SoM power-up or reset.**

## 4.5.2 RGMII

UCM-iMX8M-Plus features up-to two RGMII interfaces.

Primary RGMII interface ENET0 is available only when UCM-iMX8M-Plus is assembled without the “E” configuration option.

Secondary RGMII interface ENET1 is available with all UCM-iMX8M-Plus configurations.

The tables below summarize the Ethernet RGMII interface signals.

**Table 10 Primary RGMII ENET0 Interface Signals**

| Signal Name  | Pin #  | Type | Description                                                                                                                         | Availability        |
|--------------|--------|------|-------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| ENET_MDC     | P2-68* | O    | Provides a timing reference to the PHY for data transfers on the MDIO signal                                                        | Always available    |
| ENET_MDIO    | P2-70* | IO   | Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset | Always available    |
|              |        |      |                                                                                                                                     | Always available    |
| ENET0_RD0    | P2-86* | I    | Ethernet input data from the PHY                                                                                                    | Only w/o 'E' option |
| ENET0_RD1    | P2-83* | I    | Ethernet input data from the PHY                                                                                                    | Only w/o 'E' option |
| ENET0_RD2    | P2-84* | I    | Ethernet input data from the PHY                                                                                                    | Only w/o 'E' option |
| ENET0_RD3    | P2-85* | I    | Ethernet input data from the PHY                                                                                                    | Only w/o 'E' option |
| ENET0_RX_CTL | P2-79* | I    | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)                   | Only w/o 'E' option |
| ENET0_RXC    | P2-80* | I    | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE                                                                          | Only w/o 'E' option |
| ENET0_TD0    | P2-75* | O    | Ethernet output data to PHY                                                                                                         | Only w/o 'E' option |
| ENET0_TD1    | P2-78* | O    | Ethernet output data to PHY                                                                                                         | Only w/o 'E' option |
| ENET0_TD2    | P2-77* | O    | Ethernet output data to PHY                                                                                                         | Only w/o 'E' option |
| ENET0_TD3    | P2-73* | O    | Ethernet output data to PHY                                                                                                         | Only w/o 'E' option |
| ENET0_TXC    | P2-81* | O    | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE                                                                          | Only w/o 'E' option |
| ENET0_TX_CTL | P2-74* | O    | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)                   | Only w/o 'E' option |
| RGMII0_VIO   | P1-55  | P    | RGMII interface power supply input. This pin must be connected to 1.8V power rail                                                   | Only w/o 'E' option |

**NOTE: RGMII ENET0 interface must be operated at 1.8V voltage level. 1.8V must be supplied via the RGMII0\_VIO pin if RGMII ENET0 signals are used for RGMII function on the carrier-board**

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

**Table 11 Secondary RGMII ENET1 Interface Signals**

| Signal Name  | Pin #  | Type | Description                                                                                                                         | Availability     |
|--------------|--------|------|-------------------------------------------------------------------------------------------------------------------------------------|------------------|
| ENET_MDC     | P2-68* | O    | Provides a timing reference to the PHY for data transfers on the MDIO signal                                                        | Always available |
| ENET_MDIO    | P2-70* | IO   | Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset | Always available |
| ENET1_RD0    | P2-41* | I    | Ethernet input data from the PHY                                                                                                    | Always available |
| ENET1_RD1    | P2-43* | I    | Ethernet input data from the PHY                                                                                                    | Always available |
| ENET1_RD2    | P2-45* | I    | Ethernet input data from the PHY                                                                                                    | Always available |
| ENET1_RD3    | P2-47* | I    | Ethernet input data from the PHY                                                                                                    | Always available |
| ENET1_RX_CTL | P2-53* | I    | Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)                   | Always available |
| ENET1_RXC    | P2-55* | I    | Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE                                                                          | Always available |
| ENET1_TD0    | P2-60* | O    | Ethernet output data to PHY                                                                                                         | Always available |
|              | P2-59* |      |                                                                                                                                     |                  |
| ENET1_TD1    | P2-61* | O    | Ethernet output data to PHY                                                                                                         | Always available |
| ENET1_TD2    | P2-63* | O    | Ethernet output data to PHY                                                                                                         | Always available |
| ENET1_TD3    | P2-65* | O    | Ethernet output data to PHY                                                                                                         | Always available |
| ENET1_TXC    | P2-69* | O    | Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE                                                                          | Always available |
| ENET1_TX_CTL | P2-67* | O    | Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)                   | Always available |

**NOTE: In UCM-iMX8PLUS rev1.0 RGMII ENET1 signals operate at 3.3V voltage level**

**NOTE: In UCM-iMX8PLUS rev1.1 RGMII ENET1 signals operate at 1.8V voltage level**

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.6 PCI-Express

UCM-iMX8M-Plus provides one PCI Express port.

**Table 12 PCIe Interface Signals**

| Signal Name   | Pin #  | Type | Description                                               | Availability     |
|---------------|--------|------|-----------------------------------------------------------|------------------|
| PCIE_REF_CLKN | P2-44  | AO   | 100 MHz PCIe reference clock differential output negative | Always available |
| PCIE_REF_CLKP | P2-42  | AO   | 100 MHz PCIe reference clock differential output positive | Always available |
| PCIE_RXN_N    | P2-30  | I    | PCI Express receive data negative                         | Always available |
| PCIE_RXN_P    | P2-32  | I    | PCI Express receive data positive                         | Always available |
| PCIE_TXN_N    | P2-36  | O    | PCI Express transmit data negative                        | Always available |
| PCIE_TXN_P    | P2-38  | O    | PCI Express transmit data positive                        | Always available |
| PCIE_CLKREQ_B | P2-90* | O    | PCI Express Enable external clock generator               | Always available |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.7 Sony/Philips Digital Interface (S/PDIF)

UCM-iMX8M-Plus provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

**Table 13 S/PDIF Interface Signals**

| Signal Name   | Pin #  | Type | Description                   | Voltage Domain | Availability     |
|---------------|--------|------|-------------------------------|----------------|------------------|
| SPDIF_EXT_CLK | P1-77* | I    | External clock signal         | 3.3V           | Always available |
| SPDIF_RX      | P1-79* | I    | SPDIF input data line signal  | 3.3V           | Always available |
| SPDIF_TX      | P1-81* | O    | SPDIF output data line signal | 3.3V           | Always available |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.8 Digital Audio (SAI)

UCM-iMX8M-Plus enables access to three of the i.MX8M Plus integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Plus Reference manual for additional details. The tables below summarize the SAI interface signals.

**Table 14 SAI3 Interface Signals**

| Signal Name | Pin #  | Type | Description                                                                                                                            | Voltage Domain | Availability     |
|-------------|--------|------|----------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|
| SAI3_MCLK   | P1-49* | IO   | Audio master clock. An input when generated externally and an output when generated internally.                                        | 3.3V           | Always available |
|             | P1-30* |      |                                                                                                                                        | 3.3V           |                  |
| SAI3_RXD0   | P1-28* | I    | Receive data, sampled synchronously by the bit clock                                                                                   | 3.3V           | Always available |
| SAI3_RXC    | P1-32* | I    | Receive bit clock. An input when generated externally and an output when generated internally.                                         | 3.3V           | Always available |
| SAI3_RXFS   | P1-34* | I    | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | 3.3V           | Always available |
| SAI3_TXD0   | P1-26* | O    | Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word                                              | 3.3V           | Always available |
| SAI3_TXC    | P1-36* | O    | Transmit bit clock. An input when generated externally and an output when generated internally.                                        | 3.3V           | Always available |

| Signal Name | Pin #  | Type | Description                                                                                                                             | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|
| SAI3_TXFS   | P1-38* | O    | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | 3.3V           | Always available |

**Table 15 SAI5 Interface Signals**

| Signal Name | Pin #   | Type | Description                                                                                                                             | Voltage Domain | Availability     |
|-------------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|
| SAI5_MCLK   | P2-52*  | IO   | Audio master clock. An input when generated externally and an output when generated internally.                                         | 3.3V/1.8V      | Always available |
|             | P1-96*  |      |                                                                                                                                         | 3.3V/1.8V      |                  |
|             | P1-49*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_RXD0   | P1-100* | I    | Receive data 0, sampled synchronously by the bit clock                                                                                  | 3.3V/1.8V      | Always available |
|             | P1-28*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_RXD1   | P1-38*  | I    | Receive data 1, sampled synchronously by the bit clock                                                                                  | 3.3V           | Always available |
| SAI5_RXD2   | P1-36*  | I    | Receive data 2, sampled synchronously by the bit clock                                                                                  | 3.3V           | Always available |
| SAI5_RXD3   | P1-26*  | I    | Receive data 3, sampled synchronously by the bit clock                                                                                  | 3.3V           | Always available |
| SAI5_RXC    | P1-89*  | I    | Receive bit clock. An input when generated externally and an output when generated internally.                                          | 3.3V/1.8V      | Always available |
|             | P1-32*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_RXFS   | P1-87*  | I    | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.  | 3.3V/1.8V      | Always available |
|             | P1-34*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_TXD0   | P2-60*  | O    | Transmit data signal 0.Synchronous to bit clock.                                                                                        | 3.3V/1.8V      | Always available |
| SAI5_TXD1   | P2-88*  | O    | Transmit data signal 1.Synchronous to bit clock.                                                                                        | 3.3V           | Always available |
|             | P2-76*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_TXD2   | P2-63*  | O    | Transmit data signal 2.Synchronous to bit clock.                                                                                        | 3.3V/1.8V      | Always available |
|             | P1-51*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_TXD3   | P2-65*  | O    | Transmit data signal 3.Synchronous to bit clock.                                                                                        | 3.3V/1.8V      | Always available |
|             | P1-33*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_TXC    | P2-55*  | O    | Transmit bit clock. An input when generated externally and an output when generated internally.                                         | 3.3V/1.8V      | Always available |
|             | P1-53*  |      |                                                                                                                                         | 3.3V           |                  |
| SAI5_TXFS   | P2-53*  | O    | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | 3.3V/1.8V      | Always available |
|             | P2-88*  |      |                                                                                                                                         | 3.3V           |                  |

**Table 16 SAI7 Interface Signals**

| Signal Name | Pin #  | Type | Description                                                                                                                            | Voltage Domain | Availability        |
|-------------|--------|------|----------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------------|
| SAI7_MCLK   | P2-89* | IO   | Audio master clock. An input when generated externally and an output when generated internally.                                        | 3.3V           | Always available    |
|             | P2-85  |      |                                                                                                                                        | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_RXD0   | P2-86  | I    | Receive data, sampled synchronously by the bit clock                                                                                   | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_RXC    | P2-84* | I    | Receive bit clock. An input when generated externally and an output when generated internally.                                         | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_RXFS   | P2-83* | I    | Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_TXD0   | P2-95* | O    | Transmit data signal synchronous to bit clock. Tristated whenever not transmitting a word                                              | 3.3V           | Always available    |
|             | P2-81* |      |                                                                                                                                        | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_TXC    | P2-93* | O    |                                                                                                                                        | 3.3V           | Always available    |

| Signal Name | Pin #  | Type | Description                                                                                                                             | Voltage Domain | Availability        |
|-------------|--------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------------|
|             | P2-80* |      | Transmit bit clock. An input when generated externally and an output when generated internally.                                         | RGMII0_VIO     | Only w/o 'E' option |
| SAI7_TXFS   | P2-79  | O    | Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally. | RGMII0_VIO     | Only w/o 'E' option |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.9 USB

i.MX8M Plus SoC is equipped with two dual-role USB3.0 controllers and PHYs. USB port #1 can be configured as host or device, while the second port is configured permanently for host mode.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the USB3.0 interface signals.

**Table 17 USB port #1 Signals**

| Signal Name   | Pin # | Type | Description                   | Availability     |
|---------------|-------|------|-------------------------------|------------------|
| USB1_DN       | P1-14 | IO   | USB2.0 negative data          | Always available |
| USB1_DP       | P1-12 | IO   | USB2.0 positive data          | Always available |
| USB1_VBUS_DET | P1-24 | I    | USB1 VBUS detect              | Always available |
| USB1_TX_N     | P1-18 | AO   | USB3.0 transmit negative lane | Always available |
| USB1_TX_P     | P1-16 | AO   | USB3.0 transmit positive lane | Always available |
| USB1_RX_N     | P1-8  | AI   | USB3.0 receive negative lane  | Always available |
| USB1_RX_P     | P1-6  | AI   | USB3.0 receive positive lane  | Always available |

**Table 18 USB port #2 Signals**

| Signal Name   | Pin # | Type | Description                   | Availability     |
|---------------|-------|------|-------------------------------|------------------|
| USB2_DN       | P1-5  | IO   | USB2.0 negative data          | Always available |
| USB2_DP       | P1-3  | IO   | USB2.0 positive data          | Always available |
| USB2_VBUS_DET | P1-1  | I    | USB2 VBUS detect              | Always available |
| USB2_TX_N     | P1-15 | AO   | USB3.0 transmit negative lane | Always available |
| USB2_TX_P     | P1-13 | AO   | USB3.0 transmit positive lane | Always available |
| USB2_RX_N     | P1-9  | AI   | USB3.0 receive negative lane  | Always available |
| USB2_RX_P     | P1-7  | AI   | USB3.0 receive positive lane  | Always available |

## 4.10 MMC / SD /SDIO

UCM-iMX8M-Plus features two SD/SDIO ports. These ports are derived from the i.MX8M Plus SD/SDIO controllers uSDHC1 and uSDHC2. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.01 command/response sets and physical layer

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

**Table 19 SD/SDIO port #1 Interface Signals**

| Signal Name | Pin #  | Type | Description                                                                                                            | Voltage Domain | Availability     |
|-------------|--------|------|------------------------------------------------------------------------------------------------------------------------|----------------|------------------|
| SD1_CLK     | P2-68* | O    | Clock for MMC/SD/SDIO card                                                                                             | 3.3V/1.8V      | Always available |
| SD1_CMD     | P2-70* | IO   | CMD line connect to card                                                                                               | 3.3V/1.8V      | Always available |
| SD1_DATA0   | P2-61* | IO   | DATA0 line in all modes. Also used to detect busy state                                                                | 3.3V/1.8V      | Always available |
| SD1_DATA1   | P2-59* | IO   | DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode                                              | 3.3V/1.8V      | Always available |
| SD1_DATA2   | P2-41* | IO   | DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode                                                         | 3.3V/1.8V      | Always available |
| SD1_DATA3   | P2-43* | IO   | DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode. | 3.3V/1.8V      | Always available |
| SD1_RESET_B | P2-62* | O    | Card hardware reset signal, active LOW                                                                                 | 3.3V/1.8V      | Always available |

**NOTE: By default SD/SDIO port #1 is pre-configured to operate at 1.8V voltage levels**

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

**Table 20 SD/SDIO port #2 Interface Signals**

| Signal Name | Pin #   | Type | Description                                                                                                            | Voltage Domain | Availability     |
|-------------|---------|------|------------------------------------------------------------------------------------------------------------------------|----------------|------------------|
| SD2_nCD     | P2-92*  | I    | Card detection pin                                                                                                     | SD2            | Always available |
| SD2_CLK     | P2-96*  | O    | Clock for MMC/SD/SDIO card                                                                                             | SD2            | Always available |
| SD2_CMD     | P2-100* | IO   | CMD line connect to card                                                                                               | SD2            | Always available |
| SD2_DATA0   | P2-97*  | IO   | DATA0 line in all modes. Also used to detect busy state                                                                | SD2            | Always available |
| SD2_DATA1   | P2-99*  | IO   | DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode                                              | SD2            | Always available |
| SD2_DATA2   | P2-94*  | IO   | DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode                                                         | SD2            | Always available |
| SD2_DATA3   | P2-98*  | IO   | DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode. | SD2            | Always available |
| SD2_RESET_B | P2-51*  | O    | Card hardware reset signal, active LOW                                                                                 | SD2            | Always available |
| SD2_WP      | P2-49*  | I    | Card write protect detection                                                                                           | SD2            | Always available |

**NOTE: SD/SDIO port #2 can be configured to operate at 3.3V or 1.8V voltage levels. SD2 voltage domain level is controlled by SoC pin GPIO1\_IO04.**

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.11 UART

UCM-iMX8M-Plus enables access to up-to four i.MX8M Plus universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Plus UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX\_DATA input and TX\_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

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**NOTE: By default UART2 is assigned to be used as the main system console port.**

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**NOTE: By default UART4 is assigned to be used as the M7 core debug port.**

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Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the UART interface signals.

**Table 21 UART1 Signals**

| Signal Name | Pin #  | Type | Description                 | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------------|----------------|------------------|
| UART1_CTS_B | P1-21* | O    | UART-1 clear to send        | 3.3V           | Always available |
|             | P2-76* |      |                             | 3.3V           |                  |
| UART1_RTS_B | P1-61* | I    | UART-1 request to send      | 3.3V           | Always available |
|             | P2-61* |      |                             | 3.3V/1.8V      |                  |
| UART1_RXD   | P1-19* | I    | UART-1 serial data receive  | 3.3V           | Always available |
|             | P1-53* |      |                             | 3.3V           |                  |
|             | P2-70* |      |                             | 3.3V/1.8V      |                  |
| UART1_TXD   | P1-72* | O    | UART-1 serial data transmit | 3.3V           | Always available |
|             | P2-68* |      |                             | 3.3V/1.8V      |                  |
|             | P2-88* |      |                             | 3.3V           |                  |

**Table 22 UART2 Signals**

| Signal Name | Pin #  | Type | Description                | Voltage Domain | Availability     |
|-------------|--------|------|----------------------------|----------------|------------------|
| UART2_CTS_B | P1-32* | O    | UART-2 clear to send       | 3.3V           | Always available |
|             | P1-84* |      |                            | 3.3V           |                  |
| UART2_RTS_B | P1-28* | I    | UART-2 request to send     | 3.3V           | Always available |
|             | P1-86* |      |                            | 3.3V           |                  |
| UART2_RXD   | P1-76* | I    | UART-2 serial data receive | 3.3V           | Always available |
|             | P1-38* |      |                            | 3.3V           |                  |
|             | P2-43* |      |                            | 3.3V/1.8V      |                  |

| Signal Name | Pin #  | Type | Description                 | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------------|----------------|------------------|
|             | P2-97* |      |                             | SD2            |                  |
| UART2_TXD   | P1-74* | O    | UART-2 serial data transmit | 3.3V           | Always available |
|             | P1-36* |      |                             | 3.3V           |                  |
|             | P2-41  |      |                             | 3.3V/1.8V      |                  |
|             | P2-99  |      |                             | SD2            |                  |

**Table 23 UART3 Signals**

| Signal Name | Pin #  | Type | Description                 | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------------|----------------|------------------|
| UART3_RXD   | P1-21* | I    | UART-3 serial data receive  | 3.3V           | Always available |
| UART3_TXD   | P1-61* | O    | UART-3 serial data transmit | 3.3V           | Always available |

**Table 24 UART4 Signals**

| Signal Name | Pin #   | Type | Description                 | Voltage Domain | Availability     |
|-------------|---------|------|-----------------------------|----------------|------------------|
| UART4_RXD   | P1-84*  | I    | UART-4 serial data receive  | 3.3V           | Always available |
|             | P2-93*  |      |                             | 3.3V           |                  |
|             | P2-96*  |      |                             | SD2            |                  |
| UART4_TXD   | P1-86*  | O    | UART-4 serial data transmit | 3.3V           | Always available |
|             | P2-95*  |      |                             | 3.3V           |                  |
|             | P2-100* |      |                             | SD2            |                  |
| UART4_CTS_B | P2-89*  | O    | UART-4 clear to send        | 3.3V           | Always available |
| UART4_RTS_B | P2-91*  | I    | UART-4 request to send      | 3.3V           | Always available |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.12 CAN Bus

UCM-iMX8M-Plus features up-to two CAN bus interfaces. These interfaces support the following key features:

- Full implementation of the CAN version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the CAN interface signals.

**Table 25 CAN1 Interface Signals**

| Signal Name | Pin #  | Type | Description      | Voltage Domain | Availability     |
|-------------|--------|------|------------------|----------------|------------------|
| CAN1_TX     | P1-53* | O    | CAN transmit pin | 3.3V           | Always available |
|             | P1-81* |      |                  | 3.3V           |                  |
|             | P1-70* |      |                  | 3.3V           |                  |
| CAN1_RX     | P1-51* | I    | CAN receive pin  | 3.3V           | Always available |
|             | P1-79* |      |                  | 3.3V           |                  |
|             | P1-63* |      |                  | 3.3V           |                  |

**Table 26 CAN2 Interface Signals**

| Signal Name | Pin #  | Type | Description      | Voltage Domain | Availability     |
|-------------|--------|------|------------------|----------------|------------------|
| CAN2_TX     | P1-21* | O    | CAN transmit pin | 3.3V           | Always available |
|             | P1-33* |      |                  | 3.3V           |                  |
|             | P1-85* |      |                  | 3.3V           |                  |
| CAN2_RX     | P1-49* | I    | CAN receive pin  | 3.3V           | Always available |
|             | P1-61* |      |                  | 3.3V           |                  |
|             | P1-96* |      |                  | 3.3V/1.8V      |                  |
|             | P1-92* |      |                  | 3.3V           |                  |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.13 I2C

UCM-iMX8M-Plus features up-to five I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode

Please refer to the i.MX8M Plus Reference manual for additional details.

**NOTE: I2C2 is the system I2C channel utilized for the following on-board functions: RTC, EEPROM.**

The tables below summarize the I2C interface signals.

**Table 27 I2C2 Interface Signals**

| Signal Name | Pin # | Type | Description           | Voltage Domain | Availability     |
|-------------|-------|------|-----------------------|----------------|------------------|
| I2C2_SCL    | P1-99 | O    | I2C serial clock line | 3.3V           | Always available |
| I2C2_SDA    | P1-97 | IO   | I2C serial data line  | 3.3V           | Always available |

**Table 28 I2C3 Interface Signals**

| Signal Name | Pin #  | Type | Description           | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------|----------------|------------------|
| I2C3_SCL    | P1-94* | O    | I2C serial clock line | 3.3V           | Always available |
|             | P2-93* |      |                       | 3.3V           |                  |
|             | P2-62* |      |                       | 3.3V/1.8V      |                  |
| I2C3_SDA    | P1-91* | IO   | Always available      | 3.3V           | Always available |
|             | P2-95* |      |                       | 3.3V           |                  |

**Table 29 I2C4 Interface Signals**

| Signal Name | Pin #  | Type | Description           | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------|----------------|------------------|
| I2C4_SCL    | P2-90* | O    | I2C serial clock line | 3.3V           | Always available |
|             | P2-89* |      |                       | 3.3V           |                  |
|             | P2-41* |      |                       | 3.3V/1.8V      |                  |

| Signal Name | Pin #  | Type | Description      | Voltage Domain | Availability     |
|-------------|--------|------|------------------|----------------|------------------|
|             | P2-99* |      |                  | SD2            |                  |
| I2C4_SDA    | P2-91* | IO   | Always available | 3.3V           | Always available |
|             | P2-43* |      |                  | 3.3V/1.8V      |                  |
|             | P2-97* |      |                  | SD2            |                  |

**Table 30 I2C5 Interface Signals**

| Signal Name | Pin #   | Type | Description           | Voltage Domain | Availability     |
|-------------|---------|------|-----------------------|----------------|------------------|
| I2C5_SCL    | P1-70*  | O    | I2C serial clock line | 3.3V           | Always available |
|             | P1-81*  |      |                       | 3.3V           |                  |
|             | P1-100* |      |                       | 3.3V/1.8V      |                  |
|             | P2-68*  |      |                       | 3.3V/1.8V      |                  |
| I2C5_SDA    | P1-63*  | IO   | Always available      | 3.3V           | Always available |
|             | P1-79*  |      |                       | 3.3V           |                  |
|             | P1-96*  |      |                       | 3.3V/1.8V      |                  |
|             | P2-70*  |      |                       | 3.3V/1.8V      |                  |

**Table 31 I2C6 Interface Signals**

| Signal Name | Pin #  | Type | Description           | Voltage Domain | Availability     |
|-------------|--------|------|-----------------------|----------------|------------------|
| I2C6_SCL    | P1-84* | O    | I2C serial clock line | 3.3V           | Always available |
|             | P1-85* |      |                       | 3.3V           |                  |
|             | P1-87* |      |                       | 3.3V/1.8V      |                  |
|             | P2-61* |      |                       | 3.3V/1.8V      |                  |
| I2C6_SDA    | P1-86* | IO   | Always available      | 3.3V           | Always available |
|             | P1-89* |      |                       | 3.3V/1.8V      |                  |
|             | P1-92* |      |                       | 3.3V           |                  |
|             | P2-59* |      |                       | 3.3V/1.8V      |                  |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.14 ECSPI

Up-to two SPI interfaces are accessible through the UCM-iMX8M-Plus carrier board interface. The SPI interfaces are derived from i.MX8M Plus integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s
- Full-duplex synchronous serial interface
- Master/Slave configurable
- One Chip Select (SS) signal
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

**Table 32 ECSPi2 Interface Signals**

| Signal Name | Pin #   | Type | Description                            | Voltage Domain | Availability     |
|-------------|---------|------|----------------------------------------|----------------|------------------|
| ECSPi2_MISO | P2-89*  | I    | SPI-2 Master data in; slave data out   | 3.3V           | Always available |
|             | P2-90*  |      |                                        | 3.3V           |                  |
|             | P2-98*  |      |                                        | SD2            |                  |
| ECSPi2_MOSI | P1-91*  | O    | SPI-2 Master data out; slave data in   | 3.3V           | Always available |
|             | P2-95*  |      |                                        | 3.3V           |                  |
|             | P2-100* |      |                                        | SD2            |                  |
| ECSPi2_SCLK | P1-94*  | O    | SPI-2 Master clock out; slave clock in | 3.3V           | Always available |
|             | P2-93*  |      |                                        | 3.3V           |                  |
|             | P2-96*  |      |                                        | SD2            |                  |
| ECSPi2_SS0  | P2-91*  | O    | SPI-2 Chip select 0                    | 3.3V           | Always available |
|             | P2-94*  |      |                                        | SD2            |                  |

**Table 33 ECSPi3 Interface Signals**

| Signal Name | Pin #  | Type | Description                            | Voltage Domain | Availability     |
|-------------|--------|------|----------------------------------------|----------------|------------------|
| ECSPi3_MISO | P1-76* | I    | SPI-3 Master data in; slave data out   | 3.3V           | Always available |
| ECSPi3_MOSI | P1-72* | O    | SPI-3 Master data out; slave data in   | 3.3V           | Always available |
| ECSPi3_SCLK | P1-19* | O    | SPI-3 Master clock out; slave clock in | 3.3V           | Always available |
| ECSPi3_SS0  | P1-74* | O    | SPI-3 Chip select 0                    | 3.3V           | Always available |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.15 PWM

UCM-iMX8M-Plus features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the PWM interface signals.

**Table 34 PWM Interface Signals**

| Signal Name | Pin #   | Type | Description            | Voltage Domain | Availability     |
|-------------|---------|------|------------------------|----------------|------------------|
| PWM1_OUT    | P1-77*  | O    | PWM1 functional output | 3.3V           | Always available |
|             | P1-96*  |      |                        | 3.3V/1.8V      |                  |
|             | P1-98*  |      |                        | 3.3V           |                  |
| PWM2_OUT    | P1-79*  | O    | PWM2 functional output | 3.3V           | Always available |
|             | P1-100* |      |                        | 3.3V/1.8V      |                  |
|             | P2-90*  |      |                        | 3.3V           |                  |
| PWM3_OUT    | P1-81*  | O    | PWM3 functional output | 3.3V           | Always available |

| Signal Name | Pin #  | Type | Description            | Voltage Domain | Availability     |
|-------------|--------|------|------------------------|----------------|------------------|
| PWM4_OUT    | P1-89* |      |                        | 3.3V/1.8V      |                  |
|             | P1-91* |      |                        | 3.3V           |                  |
|             | P1-30* | O    | PWM4 functional output | 3.3V           | Always available |
|             | P1-87* |      |                        | 3.3V/1.8V      |                  |
|             | P1-94* |      |                        | 3.3V           |                  |

**NOTE: Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document**

## 4.16 JTAG

UCM-iMX8M-Plus enables access to the i.MX8M Plus JTAG port through the carrier board interface.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the JTAG interface signals.

**Table 35 JTAG Interface Signals**

| Signal Name | Pin # | Type | Description      | Availability     |
|-------------|-------|------|------------------|------------------|
| JTAG_MOD    | P1-75 | I    | JTAG MODE        | Always available |
| JTAG_nTRST  | P1-63 | I    | Test Reset       | Always available |
| JTAG_TCK    | P1-73 | I    | Test Clock       | Always available |
| JTAG_TDI    | P1-71 | I    | Test Data In     | Always available |
| JTAG_TDO    | P1-67 | O    | Test Data Out    | Always available |
| JTAG_TMS    | P1-65 | I    | Test Mode Select | Always available |

## 4.17 GPIO

Up-to 79 of the i.MX8M Plus general purpose input/output (GPIO) signals are available through the UCM-iMX8M-Plus carrier board interface. When configured as an output, it is possible to write to an i.MX8M Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Plus register. In addition, GPIO signals can produce interrupts.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the GPIO interface signals.

**Table 36 GPIO Signals**

| Signal Name | Pin #   | Type | Description | Voltage Domain | Always available    |
|-------------|---------|------|-------------|----------------|---------------------|
| GPIO1_IO0   | P1-59*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO1_IO1   | P1-98*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO1_IO18  | P2-73*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO19  | P2-77*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO20  | P2-78*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO21  | P2-75*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO22  | P2-74*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO23  | P2-81*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO24  | P2-79*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO25  | P2-80*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO26  | P2-86*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO27  | P2-83*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO28  | P2-84*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO1_IO29  | P2-85*  | IO   | GPIO        | RGMII0_VIO     | Only w/o "E" option |
| GPIO2_IO0   | P2-68*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO1   | P2-70*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO10  | P2-62*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO12  | P2-92*  | O    | GPIO        | SD2            | Always available    |
| GPIO2_IO13  | P2-96*  | O    | GPIO        | SD2            | Always available    |
| GPIO2_IO14  | P2-100* | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO15  | P2-97*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO16  | P2-99*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO17  | P2-94*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO18  | P2-98*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO19  | P2-51*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO2   | P2-61*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO20  | P2-49*  | IO   | GPIO        | SD2            | Always available    |
| GPIO2_IO3   | P2-59*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO4   | P2-41*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO2_IO5   | P2-43*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO3_IO19  | P1-87*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO3_IO20  | P1-89*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO3_IO21  | P1-100* | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO3_IO25  | P1-96*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO3_IO26  | P1-70*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO3_IO27  | P1-63*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO3_IO28  | P1-85*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO3_IO29  | P1-92*  | IO   | GPIO        | 3.3V           | Always available    |
| GPIO4_IO10  | P2-53*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |
| GPIO4_IO11  | P2-55*  | IO   | GPIO        | 3.3V/1.8V      | Always available    |

| Signal Name | Pin #  | Type | Description | Voltage Domain | Always available |
|-------------|--------|------|-------------|----------------|------------------|
| GPIO4_IO12  | P2-60* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO14  | P2-63* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO15  | P2-65* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO16  | P2-67* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO17  | P2-69* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO19  | P1-60* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO20  | P2-52* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO21  | P2-88* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO22  | P1-53* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO24  | P2-76* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO25  | P1-51* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO26  | P1-33* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO27  | P1-49* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO28  | P1-34* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO29  | P1-32* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO30  | P1-28* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO31  | P1-38* | IO   | GPIO        | 3.3V           | Always available |
| GPIO4_IO8   | P2-45* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO4_IO9   | P2-47* | IO   | GPIO        | 3.3V/1.8V      | Always available |
| GPIO5_IO0   | P1-36* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO1   | P1-26* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO10  | P2-93* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO11  | P2-95* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO12  | P2-89* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO13  | P2-91* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO18  | P1-94* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO19  | P1-91* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO2   | P1-30* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO20  | P2-90* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO22  | P1-19* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO23  | P1-72* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO24  | P1-76* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO25  | P1-74* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO26  | P1-21* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO27  | P1-61* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO28  | P1-84* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO29  | P1-86* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO3   | P1-81* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO4   | P1-79* | IO   | GPIO        | 3.3V           | Always available |
| GPIO5_IO5   | P1-77* | IO   | GPIO        | 3.3V           | Always available |

**NOTE:** Pins denoted with "\*" are multifunctional. For additional details please refer to chapter 5 of this document

**NOTE:** GPIOs that belong to the RGMII0\_VIO power domain can operate at 1.8V or 2.5V or 3.3V voltage levels. Required voltage must be supplied via the RGMII0\_VIO pin if any of these signals are used as GPIOs on the carrier-board

## 5 SYSTEM LOGIC

### 5.1 Power Supply

**Table 37 Power signals**

| Signal Name | Connector # | Pin#                                   | Type | Description                                                                                                                          |
|-------------|-------------|----------------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------|
| V_SOM       | P1          | 11, 27, 43, 57, 69, 83                 | P    | Main power supply. Connect to a regulated DC supply or Li-Ion battery                                                                |
|             | P2          | 9, 19, 29, 39, 57, 71, 87              |      |                                                                                                                                      |
| VCC_RTC     | P1          | 93                                     | P    | RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. If RTC back-up is not required, connect this pin to GND. |
| GND         | P1          | 4, 10, 20, 40, 54, 64, 78, 88          | P    | Common ground                                                                                                                        |
|             | P2          | 10, 16, 22, 28, 34, 40, 46, 54, 72, 82 |      |                                                                                                                                      |
| RGMII0_VIO  | P1          | 55                                     | P    | RGMII interface power supply input. This pin must be connected to 1.8V or 3.3V power rail depending on the PHY requirements          |

### 5.2 I/O Voltage Domains

UCM-iMX8M-Plus utilizes four separate I/O voltage domains to power different I/O modules of the i.MX8M Plus SoC:

**Table 38 Power signals**

| I/O Voltage Domain | Description                                                                                                                                                                                                                           | Default Voltage                                                   | Control                       |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|-------------------------------|
| 3.3V domain        | Main SOM 3.3V                                                                                                                                                                                                                         | 3.3V                                                              | N/A                           |
| RGMII0_VIO domain  | RGMII0 interface power supply.<br>When “E” option is present this domain is supplied from on-board 1.8V LDO.<br>When UCM-iMX8PLUS is assembled without “E” option this domain must be supplied from carrier-board via pin RGMII0_VIO. | With “E” option:<br>1.8V<br><br>Without “E” option:<br>RGMII0_VIO | N/A                           |
| SD2 domain         | SD interface power supply.<br>Powered with PMIC LDO5.                                                                                                                                                                                 | 3.3V                                                              | SoC pin<br>GPIO1_IO04         |
| 3.3V/1.8V domain   | Software programmable 3.3V/1.8V voltage rail.<br>Powered with PMIC LDO4.                                                                                                                                                              | 1.8V                                                              | Configuring<br>LDO4 in u-boot |

## 5.3 System and Miscellaneous Signals

### 5.3.1 External regulator control and power management

UCM-iMX8M-Plus supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Plus SoC. The logic that controls both signals is supplied by the i.MX8M Plus SoC SNVS power rail.

The PMIC\_STBY\_REQ output can be used to signal the carrier board power supply that UCM-iMX8M-Plus is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the external regulator control signals.

**Table 39 External regulator control signals**

| Signal Name   | Pin # | Type | Description                                                         | Availability     |
|---------------|-------|------|---------------------------------------------------------------------|------------------|
| PMIC_STBY_REQ | P1-66 | O    | When the processor enters SUSPEND mode, it will assert this signal. | Always available |
| PMIC_ON_REQ   | P1-68 | O    | Active high power-up request output from i.MX8M Plus SoC.           | Always available |
| PWRBTN        | P2-64 | I    | Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).  | Always available |

## 5.4 Reset

SYS\_RST\_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on UCM-iMX8M-Plus. Please refer to the i.MX8M Plus Reference manual for additional details.

**Table 40 Reset signals**

| Signal Name  | Pin # | Type | Description                                                             | Availability     |
|--------------|-------|------|-------------------------------------------------------------------------|------------------|
| SYS_RST_PMIC | P1-2  | I    | Active Low cold reset input signal. Should be used as main system reset | Always available |

## 5.5 Boot Sequence

UCM-iMX8M-Plus boot sequence defines which interface/media is used by UCM-iMX8M-Plus to load and execute the initial software (such as SPL or/and U-boot). UCM-iMX8M-Plus can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD/SDIO 2 interface

UCM-iMX8M-Plus will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by UCM-iMX8M-Plus:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows UCM-iMX8M-Plus to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT\_BOOT signal defines which of the supported boot sequences is used by the system.

**Table 41 Alternative Boot selection signal**

| Signal Name | Pin # | Type | Description                                                                                               | Availability     |
|-------------|-------|------|-----------------------------------------------------------------------------------------------------------|------------------|
| ALT_BOOT    | P1-90 | I    | Active high alternate boot sequence select input.<br>Leave floating or tie low for standard boot sequence | Always available |

**Table 42 UCM-iMX8M-Plus Boot sequences**

| Sequence  | ALT_BOOT        | First                               |
|-----------|-----------------|-------------------------------------|
| Standard  | Low or floating | Onboard eMMC (primary boot storage) |
| Alternate | High            | SD card on SD/SDIO2 interface       |

## 5.6 Signal Multiplexing Characteristics

Up to 80 of the UCM-iMX8M-Plus carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the UCM-iMX8M-Plus CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of UCM-iMX8M-Plus pins are derived from the i.MX8M Plus SoC control module

**NOTE:** Pin function selection is controlled by software.

**NOTE:** Each pin can be used for a single function at a time.

**NOTE:** Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

**NOTE:** An empty MUX mode is a “RESERVED” function and must not be used.

**Table 43 Multifunctional Signals**

| Pin # | SoC Pin Name | GPIO       | SAI                                 | ENET1 | SDIO | I2C | UART                    | SPI         | PWM      | CAN     | SPDIF             | Availability |
|-------|--------------|------------|-------------------------------------|-------|------|-----|-------------------------|-------------|----------|---------|-------------------|--------------|
| P1-19 | UART1_RXD    | GPIO5_IO22 |                                     |       |      |     | UART1_RX                | ECSPI3_SCLK |          |         |                   | Always       |
| P1-21 | UART3_RXD    | GPIO5_IO26 |                                     |       |      |     | UART3_RX<br>UART1_CTS_B |             |          | CAN2_TX |                   | Always       |
| P1-26 | SAI3_TXD     | GPIO5_IO1  | SAI3_TXD0<br>SAI5_RXD3              |       |      |     |                         |             |          |         | SPDIF1_EXT<br>CLK | Always       |
| P1-28 | SAI3_RXD     | GPIO4_IO30 | SAI3_RXD0<br>SAI5_RXD0              |       |      |     | UART2_RTS_B             |             |          |         |                   | Always       |
| P1-30 | SAI3_MCLK    | GPIO5_IO2  | SAI3_MCLK<br>SAI5_MCLK              |       |      |     |                         |             | PWM4_OUT |         | SPDIF1_OU<br>T    | Always       |
| P1-32 | SAI3_RXC     | GPIO4_IO29 | SAI3_RXC<br>SAI5_RXC                |       |      |     | UART2_CTS_B             |             |          |         |                   | Always       |
| P1-33 | SAI2_TXD0    | GPIO4_IO26 | SAI5_TXD3                           |       |      |     |                         |             |          | CAN2_TX |                   | Always       |
| P1-34 | SAI3_RXFS    | GPIO4_IO28 | SAI3_RXFS<br>SAI3_RXD1              |       |      |     |                         |             |          |         | SPDIF1_IN         | Always       |
| P1-36 | SAI3_TXC     | GPIO5_IO0  | SAI3_TXC<br>SAI5_RXD2               |       |      |     | UART2_TX                |             |          |         |                   | Always       |
| P1-38 | SAI3_TXFS    | GPIO4_IO31 | SAI3_TXFX<br>SAI5_RXD1<br>SAI3_TXD1 |       |      |     | UART2_RX                |             |          |         |                   | Always       |
| P1-49 | SAI2_MCLK    | GPIO4_IO27 | SAI5_MCLK<br>SAI3_MCLK              |       |      |     |                         |             |          | CAN2_RX |                   | Always       |

|        |               |            |           |                    |             |          |                          |             |          |         |                |        |
|--------|---------------|------------|-----------|--------------------|-------------|----------|--------------------------|-------------|----------|---------|----------------|--------|
| P1-51  | SAI2_TXC      | GPIO4_IO25 | SAI5_TXD2 |                    |             |          |                          |             |          | CAN1_RX |                | Always |
| P1-53  | SAI2_RXC      | GPIO4_IO22 | SAI5_TXC  |                    |             |          | UART1_RXD                |             |          | CAN1_TX |                | Always |
| P1-59  | GPIO1_IO00    | GPIO1_IO0  |           |                    |             |          |                          |             |          |         |                | Always |
| P1-60  | SAI1_TXD7     | GPIO4_IO19 |           |                    |             |          |                          |             |          |         |                | Always |
| P1-61  | UART3_TXD     | GPIO5_IO27 |           |                    |             |          | UART3_TXD<br>UART1_RTS_B |             |          | CAN2_RX |                | Always |
| P1-63  | HDMI_DDC_SDA  | GPIO3_IO27 |           |                    |             | I2C5_SDA |                          |             |          | CAN1_RX |                | Always |
| P1-70  | HDMI_DDC_SCL  | GPIO3_IO26 |           |                    |             | I2C5_SCL |                          |             |          | CAN1_TX |                | Always |
| P1-72  | UART1_TXD     | GPIO5_IO23 |           |                    |             |          | UART1_TXD                | ECSPI3_MOSI |          |         |                | Always |
| P1-74  | UART2_TXD     | GPIO5_IO25 |           |                    |             |          | UART2_TXD                | ECSPI3_SS0  |          |         |                | Always |
| P1-76  | UART2_RXD     | GPIO5_IO24 |           |                    |             |          | UART2_RXD                | ECSPI3_MISO |          |         |                | Always |
| P1-77  | SPDIF_EXT_CLK | GPIO5_IO5  |           |                    |             |          |                          |             | PWM1_OUT |         | SPDIF1_EXT_CLK | Always |
| P1-79  | SPDIF_RX      | GPIO5_IO4  |           |                    |             | I2C5_SDA |                          |             | PWM2_OUT | CAN1_RX | SPDIF1_IN      | Always |
| P1-81  | SPDIF_TX      | GPIO5_IO3  |           |                    |             | I2C5_SCL |                          |             | PWM3_OUT | CAN1_TX | SPDIF1_OUT     | Always |
| P1-84  | UART4_RXD     | GPIO5_IO28 |           |                    |             | I2C6_SCL | UART4_RXD<br>UART2_CTS_B |             |          |         |                | Always |
| P1-85  | HDMI_CEC      | GPIO3_IO28 |           |                    |             | I2C6_SCL |                          |             |          | CAN2_TX |                |        |
| P1-86  | UART4_TXD     | GPIO5_IO29 |           |                    |             | I2C6_SDA | UART4_TXD<br>UART2_RTS_B |             |          |         |                | Always |
| P1-87  | SAI5_RXFS     | GPIO3_IO19 | SAI5_RXFS |                    |             | I2C6_SCL |                          |             | PWM4_OUT |         |                | Always |
| P1-89  | SAI5_RXC      | GPIO3_IO20 | SAI5_RXC  |                    |             | I2C6_SDA |                          |             | PWM3_OUT |         |                | Always |
| P1-91  | I2C3_SDA      | GPIO5_IO19 |           |                    |             | I2C3_SDA |                          | ECSPI2_MOSI | PWM3_OUT |         |                | Always |
| P1-92  | HDMI_HPD      | GPIO3_IO29 |           |                    |             | I2C6_SDA |                          |             |          | CAN2_RX |                | Always |
| P1-94  | I2C3_SCL      | GPIO5_IO18 |           |                    |             | I2C3_SCL |                          | ECSPI2_SCLK | PWM4_OUT |         |                | Always |
| P1-96  | SAI5_MCLK     | GPIO3_IO25 | SAI5_MCLK |                    |             | I2C5_SDA |                          |             | PWM1_OUT | CAN2_RX |                | Always |
| P1-98  | GPIO1_IO01    | GPIO1_IO1  |           |                    |             |          |                          |             | PWM1_OUT |         |                | Always |
| P1-100 | SAI5_RXD0     | GPIO3_IO21 | SAI5_RXD0 |                    |             | I2C5_SCL |                          |             | PWM2_OUT |         |                | Always |
| P2-41  | SD1_DATA2     | GPIO2_IO4  |           | ENET1_RGMII_RD0    | SD1_DATA2   | I2C4_SCL | UART2_TXD                |             |          |         |                | Always |
| P2-43  | SD1_DATA3     | GPIO2_IO5  |           | ENET1_RGMII_RD1    | SD1_DATA3   | I2C4_SDA | UART2_RXD                |             |          |         |                | Always |
| P2-45  | SAI1_RXD6     | GPIO4_IO8  |           | ENET1_RGMII_RD2    |             |          |                          |             |          |         |                | Always |
| P2-47  | SAI1_RXD7     | GPIO4_IO9  |           | ENET1_RGMII_RD3    |             |          |                          |             |          |         |                | Always |
| P2-49  | SD2_WP        | GPIO2_IO20 |           |                    | SD2_WP      |          |                          |             |          |         |                | Always |
| P2-51  | SD2_RESET_B   | GPIO2_IO19 |           |                    | SD2_RESET_B |          |                          |             |          |         |                | Always |
| P2-52  | SAI1_MCLK     | GPIO4_IO20 | SAI5_MCLK |                    |             |          |                          |             |          |         |                | Always |
| P2-53  | SAI1_TXFS     | GPIO4_IO10 | SAI5_TXFS | ENET1_RGMII_RX_CTL |             |          |                          |             |          |         |                | Always |
| P2-55  | SAI1_TXC      | GPIO4_IO11 | SAI5_TXC  | ENET1_RGMII_RXC    |             |          |                          |             |          |         |                | Always |

|        |             |            |           |                    |             |          |             |             |          |  |            |         |
|--------|-------------|------------|-----------|--------------------|-------------|----------|-------------|-------------|----------|--|------------|---------|
| P2-59  | SD1_DATA1   | GPIO2_IO3  |           | ENET1_RGMII_TD0    | SD1_DATA1   | I2C6_SDA | UART1_CTS_B |             |          |  |            | Always  |
| P2-60  | SAI1_TXD0   | GPIO4_IO12 | SAI5_TXD0 | ENET1_RGMII_TD0    |             |          |             |             |          |  |            | Always  |
| P2-61  | SD1_DATA0   | GPIO2_IO2  |           | ENET1_RGMII_TD1    | SD1_DATA0   | I2C6_SCL | UART1_RTS_B |             |          |  |            | Always  |
| P2-62  | SD1_RESET_B | GPIO2_IO10 |           |                    | SD1_RESET_B | I2C3_SCL | UART3_RTS_B |             |          |  |            | Always  |
| P2-63  | SAI1_TXD2   | GPIO4_IO14 | SAI5_TXD2 | ENET1_RGMII_TD2    |             |          |             |             |          |  |            | Always  |
| P2-65  | SAI1_TXD3   | GPIO4_IO15 | SAI5_TXD3 | ENET1_RGMII_TD3    |             |          |             |             |          |  |            | Always  |
| P2-67  | SAI1_TXD4   | GPIO4_IO16 |           | ENET1_RGMII_TX_CTL |             |          |             |             |          |  |            | Always  |
| P2-68  | SD1_CLK     | GPIO2_IO0  |           | ENET1_MDC          | SD1_CLK     | I2C5_SCL | UART1_TXD   |             |          |  |            | Always  |
| P2-69  | SAI1_TXD5   | GPIO4_IO17 |           | ENET1_RGMII_TXC    |             |          |             |             |          |  |            | Always  |
| P2-70  | SD1_CMD     | GPIO2_IO1  |           | ENET1_MDIO         | SD1_CMD     | I2C5_SDA | UART1_RXD   |             |          |  |            | Always  |
| P2-73  | ENET_TD3    | GPIO1_IO18 |           |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-74  | ENET_TX_CTL | GPIO1_IO22 |           |                    |             |          |             |             |          |  | SPDIF1_OUT | NOT "E" |
| P2-75  | ENET_TD0    | GPIO1_IO21 |           |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-76  | SAI2_TXFS   | GPIO4_IO24 | SAI5_TXD1 |                    |             |          | UART1_CTS_B |             |          |  |            | Always  |
| P2-77  | ENET_TD2    | GPIO1_IO19 |           |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-78  | ENET_TD1    | GPIO1_IO20 |           |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-79  | ENET_RX_CTL | GPIO1_IO24 | SAI7_TXFS |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-80  | ENET_RXC    | GPIO1_IO25 | SAI7_TXC  |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-81  | ENET_TXC    | GPIO1_IO23 | SAI7_TXD0 |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-83  | ENET_RD1    | GPIO1_IO27 | SAI7_RXFS |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-84  | ENET_RD2    | GPIO1_IO28 | SAI7_RXC  |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-85  | ENET_RD3    | GPIO1_IO29 | SAI7_MCLK |                    |             |          |             |             |          |  | SPDIF1_IN  | NOT "E" |
| P2-86  | ENET_RD0    | GPIO1_IO26 | SAI7_RXD0 |                    |             |          |             |             |          |  |            | NOT "E" |
| P2-88  | SAI2_RXFS   | GPIO4_IO21 | SAI5_TXFS |                    |             |          | UART1_TX    |             |          |  |            | Always  |
| P2-89  | ECSPi2_MISO | GPIO5_IO12 | SAI7_MCLK |                    |             | I2C4_SCL | UART4_CTS_B | ECSPi2_MISO |          |  |            | Always  |
| P2-90  | I2C4_SCL    | GPIO5_IO20 |           |                    |             | I2C4_SCL |             | ECSPi2_MISO | PWM2_OUT |  |            | Always  |
| P2-91  | ECSPi2_SS0  | GPIO5_IO13 |           |                    |             | I2C4_SDA | UART4_RTS_B | ECSPi2_SS0  |          |  |            | Always  |
| P2-92  | SD2_CD_B    | GPIO2_IO12 |           |                    | SD2_CD_B    |          |             |             |          |  |            | Always  |
| P2-93  | ECSPi2_SCLK | GPIO5_IO10 | SAI7_TXC  |                    |             | I2C3_SCL | UART4_RXD   | ECSPi2_SCLK |          |  |            | Always  |
| P2-94  | SD2_DATA2   | GPIO2_IO17 |           |                    | SD2_DATA2   |          |             | ECSPi2_SS0  |          |  | SPDIF1_OUT | Always  |
| P2-95  | ECSPi2_MOSI | GPIO5_IO11 | SAI7_TXD0 |                    |             | I2C3_SDA | UART4_TXD   | ECSPi2_MOSI |          |  |            | Always  |
| P2-96  | SD2_CLK     | GPIO2_IO13 |           |                    | SD2_CLK     |          | UART4_RXD   | ECSPi2_SCLK |          |  |            | Always  |
| P2-97  | SD2_DATA0   | GPIO2_IO15 |           |                    | SD2_DATA0   | I2C4_SDA | UART2_RXD   |             |          |  |            | Always  |
| P2-98  | SD2_DATA3   | GPIO2_IO18 |           |                    | SD2_DATA3   |          |             | ECSPi2_MISO |          |  | SPDIF1_IN  | Always  |
| P2-99  | SD2_DATA1   | GPIO2_IO16 |           |                    | SD2_DATA1   | I2C4_SCL | UART2_TXD   |             |          |  |            | Always  |
| P2-100 | SD2_CMD     | GPIO2_IO14 |           |                    | SD2_CMD     |          | UART4_TXD   | ECSPi2_MOSI |          |  |            | Always  |

## 5.7 RTC

UCM-iMX8M-Plus features an on-board ultra-low-power AM1805 real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface at address 0xD2/D3.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about UCM-iMX8M-Plus RTC please refer to the AM1805 datasheet.

## 5.8 LED

UCM-iMX8M-Plus features a single general purpose green LED controlled by GPIO1\_IO[12] signal of the i.MX8M Plus. The LED is ON when GPIO1\_IO[12] is logic LOW.

## 5.9 Reserved Signals

The following UCM-iMX8M-Plus signals are reserved and must be left unconnected.

**Table 44** Reserved Signals

| Connector # | Pin#   |
|-------------|--------|
| P1          | 62, 95 |
| P2          | 66     |

## 6 CARRIER BOARD INTERFACE

The UCM-iMX8M-Plus CoM/SoM carrier board interface uses 2 x 100 Pin carrier board connectors. The SoM pinout is detailed in the table below.

### 6.1 Connectors Pinout

**Table 45 Connector P1**

| Pin # | UCM-iMX8M-Plus<br>Signal Name                                      | Ref. | Pin # | UCM-iMX8M-Plus<br>Signal Name                     | Ref. |
|-------|--------------------------------------------------------------------|------|-------|---------------------------------------------------|------|
| 2     | SYS_RST_PMIC                                                       |      | 1     | USB2_VBUS                                         |      |
| 4     | GND                                                                |      | 3     | USB2_DP                                           |      |
| 6     | USB1_RX_P                                                          |      | 5     | USB2_DN                                           |      |
| 8     | USB1_RX_N                                                          |      | 7     | USB2_RX_P                                         |      |
| 10    | GND                                                                |      | 9     | USB2_RX_N                                         |      |
| 12    | USB1_DP                                                            |      | 11    | V_SOM                                             |      |
| 14    | USB1_DN                                                            |      | 13    | USB2_TX_P                                         |      |
| 16    | USB1_TX_P                                                          |      | 15    | USB2_TX_N                                         |      |
| 18    | USB1_TX_N                                                          |      | 17    | RESERVED                                          |      |
| 20    | GND                                                                |      | 19    | UART1_RXD<br>ECSP13_SCLK<br>GPIO5_IO22            |      |
| 22    | RESERVED                                                           |      | 21    | UART3_RXD<br>UART1_CTS_B<br>CAN2_TX<br>GPIO5_IO26 |      |
| 24    | USB1_VBUS                                                          |      | 23    | HDMI_TXCP                                         |      |
| 26    | SAI3_TXD0<br>SAI5_RXD3<br>GPIO5_IO1                                |      | 25    | HDMI_TXCN                                         |      |
| 28    | SAI3_RXD0<br>SAI5_RXD0<br>UART2_RTS_B<br>UART2_RTS_B<br>GPIO4_IO30 |      | 27    | V_SOM                                             |      |
| 30    | SAI3_MCLK<br>SAI5_MCLK<br>PWM4_OUT<br>GPIO5_IO2                    |      | 29    | HDMI_TX0P                                         |      |
| 32    | SAI3_RXC<br>SAI5_RXC<br>UART2_CTS_B<br>GPIO4_IO29                  |      | 31    | HDMI_TX0N                                         |      |
| 34    | SAI3_RXFS<br>SAI5_RXFX<br>SAI3_RXD1<br>GPIO4_IO28                  |      | 33    | SAI5_TXD3<br>CAN2_TX<br>GPIO4_IO26                |      |
| 36    | SAI3_TXC<br>SAI5_RXD2<br>UART2_TXD<br>GPIO5_IO0                    |      | 35    | EARC_N_HPD                                        |      |
| 38    | SAI3_TXFS<br>SAI5_RXD1<br>SAI3_TXD1<br>UART2_RXD<br>GPIO4_IO31     |      | 37    | EARC_P_UTIL                                       |      |
| 40    | GND                                                                |      | 39    | HDMI_TX1P                                         |      |
| 42    | LVDS0_D0_P                                                         |      | 41    | HDMI_TX1N                                         |      |
| 44    | LVDS0_D0_N                                                         |      | 43    | V_SOM                                             |      |
| 46    | LVDS0_D1_P                                                         |      | 45    | HDMI_TX2P                                         |      |
| 48    | LVDS0_D1_N                                                         |      | 47    | HDMI_TX2N                                         |      |
| 50    | LVDS0_D2_P                                                         |      | 49    | SAI3_MCLK<br>CAN2_RX<br>GPIO4_IO27                |      |
| 52    | LVDS0_D2_N                                                         |      | 51    | SAI5_TXD2<br>CAN1_RX<br>GPIO4_IO25                |      |

|    |                                                            |  |    |                                                          |  |
|----|------------------------------------------------------------|--|----|----------------------------------------------------------|--|
| 54 | GND                                                        |  | 53 | SAI5_TXC<br>UART1_RXD<br>CAN1_TX<br>GPIO4_IO22           |  |
| 56 | LVDS0_D3_P                                                 |  | 55 | RGMII0_VIO                                               |  |
| 58 | LVDS0_D3_N                                                 |  | 57 | V_SOM                                                    |  |
| 60 | GPIO4_IO19                                                 |  | 59 | GPIO1_IO00                                               |  |
| 62 | RESERVED                                                   |  | 61 | UART3_TXD<br>UART1_RTS_B<br>CAN2_RX<br>GPIO5_IO27        |  |
| 64 | GND                                                        |  | 63 | HDMI_DDC_SDA<br>I2C5_SDA<br>CAN1_RX<br>GPIO3_IO27        |  |
| 66 | PMIC_STBY_REQ                                              |  | 65 | JTAG_TMS                                                 |  |
| 68 | PMIC_ON_REQ                                                |  | 67 | JTAG_TDO                                                 |  |
| 70 | HDMI_DDC_SCL<br>I2C5_SCL<br>CAN1_TX<br>GPIO3_IO26          |  | 69 | V_SOM                                                    |  |
| 72 | UART1_TXD<br>ECSPI3_MOSI<br>GPIO5_IO23                     |  | 71 | JTAG_TDI                                                 |  |
| 74 | UART2_TXD<br>ECSPI3_SS0<br>GPIO5_IO25                      |  | 73 | JTAG_TCK                                                 |  |
| 76 | UART2_RXD<br>ECSPI3_MISO<br>GPIO5_IO24                     |  | 75 | JTAG_MOD                                                 |  |
| 78 | GND                                                        |  | 77 | SPDIF_EXT_CLK<br>PWM1_OUT<br>GPIO5_IO5                   |  |
| 80 | LVDS0_CLK_P                                                |  | 79 | SPDIF_RX<br>I2C5_SDA<br>PWM2_OUT<br>CAN1_RX<br>GPIO5_IO4 |  |
| 82 | LVDS0_CLK_N                                                |  | 81 | SPDIF_TX<br>I2C5_SCL<br>PWM3_OUT<br>CAN1_TX<br>GPIO5_IO3 |  |
| 84 | UART4_RXD<br>I2C6_SCL<br>UART2_CTS_B<br>GPIO5_IO28         |  | 83 | V_SOM                                                    |  |
| 86 | UART4_TXD<br>I2C6_SDA<br>UART2_RTS_B<br>GPIO5_IO29         |  | 85 | HDMI_CEC<br>I2C6_SCL<br>CAN2_TX<br>GPIO3_IO28            |  |
| 88 | GND                                                        |  | 87 | SAI5_RXFS<br>I2C6_SCL<br>PWM4_OUT<br>GPIO3_IO19          |  |
| 90 | ALT_BOOT                                                   |  | 89 | SAI5_RXC<br>I2C6_SDA<br>PWM3_OUT<br>GPIO3_IO20           |  |
| 92 | HDMI_HPD<br>I2C6_SDA<br>CAN2_RX<br>GPIO3_IO29              |  | 91 | I2C3_SDA<br>ECSPI2_MOSI<br>PWM3_OUT<br>GPIO5_IO19        |  |
| 94 | I2C3_SCL<br>ECSPI2_SCLK<br>PWM4_OUT<br>GPIO5_IO18          |  | 93 | VCC_RTC                                                  |  |
| 96 | SAI5_MCLK<br>I2C5_SDA<br>PWM1_OUT<br>CAN2_RX<br>GPIO3_IO25 |  | 95 | RESERVED                                                 |  |
| 98 | PWM1_OUT<br>GPIO1_IO1                                      |  | 97 | SYS_I2C_SDA                                              |  |

|     |                                                 |  |  |    |             |  |
|-----|-------------------------------------------------|--|--|----|-------------|--|
| 100 | SAI5_RXD0<br>I2C5_SCL<br>PWM2_OUT<br>GPIO3_IO21 |  |  | 99 | SYS_I2C_SCL |  |
|-----|-------------------------------------------------|--|--|----|-------------|--|

**Table 46 Connector P2**

| Pin # | UCM-iMX8M-Plus<br>Signal Name                        | Ref. | Pin # | UCM-iMX8M-Plus<br>Signal Name                                        | Ref. |
|-------|------------------------------------------------------|------|-------|----------------------------------------------------------------------|------|
| 2     | MIPI_CSI1_CLK_N                                      |      | 1     | MIPI_DSI1_D0_N                                                       |      |
| 4     | MIPI_CSI1_CLK_P                                      |      | 3     | MIPI_DSI1_D0_P                                                       |      |
| 6     | MIPI_CSI1_D0_N                                       |      | 5     | MIPI_DSI1_D2_N                                                       |      |
| 8     | MIPI_CSI1_D0_P                                       |      | 7     | MIPI_DSI1_D2_P                                                       |      |
| 10    | GND                                                  |      | 9     | V_SOM                                                                |      |
| 12    | MIPI_CSI2_CLK_N                                      |      | 11    | MIPI_DSI1_D3_N                                                       |      |
| 14    | MIPI_CSI2_CLK_P                                      |      | 13    | MIPI_DSI1_D3_P                                                       |      |
| 16    | GND                                                  |      | 15    | MIPI_DSI1_D1_N                                                       |      |
| 18    | MIPI_CSI2_D0_N                                       |      | 17    | MIPI_DSI1_D1_P                                                       |      |
| 20    | MIPI_CSI2_D0_P                                       |      | 19    | V_SOM                                                                |      |
| 22    | GND                                                  |      | 21    | MIPI_DSI1_CLK_N                                                      |      |
| 24    | MIPI_CSI2_D1_N                                       |      | 23    | MIPI_DSI1_CLK_P                                                      |      |
| 26    | MIPI_CSI2_D1_P                                       |      | 25    | MIPI_CSI1_D2_N                                                       |      |
| 28    | GND                                                  |      | 27    | MIPI_CSI1_D2_P                                                       |      |
| 30    | PCIE_RXN_N                                           |      | 29    | V_SOM                                                                |      |
| 32    | PCIE_RXN_P                                           |      | 31    | MIPI_CSI1_D1_N                                                       |      |
| 34    | GND                                                  |      | 33    | MIPI_CSI1_D1_P                                                       |      |
| 36    | PCIE_TXN_N                                           |      | 35    | MIPI_CSI1_D3_N                                                       |      |
| 38    | PCIE_TXN_P                                           |      | 37    | MIPI_CSI1_D3_P                                                       |      |
| 40    | GND                                                  |      | 39    | V_SOM                                                                |      |
| 42    | PCIE_REF_CLKP                                        |      | 41    | SD1_DATA2<br>I2C4_SCL<br>UART2_TXD<br>ENET1_RGMII_RD0<br>GPIO2_IO4   |      |
| 44    | PCIE_REF_CLKN                                        |      | 43    | SD1_DATA3<br>I2C4_SDA<br>UART2_RXD<br>ENET1_RGMII_RD1<br>GPIO2_IO5   |      |
| 46    | GND                                                  |      | 45    | ENET1_RGMII_RD2<br>GPIO4_IO8                                         |      |
| 48    | MIPI_CSI2_D2_N                                       |      | 47    | ENET1_RGMII_RD3<br>GPIO4_IO9                                         |      |
| 50    | MIPI_CSI2_D2_P                                       |      | 49    | SD2_WP<br>GPIO2_IO20                                                 |      |
| 52    | SAI5_MCLK<br>GPIO4_IO20                              |      | 51    | SD2_RESET_B<br>GPIO2_IO19                                            |      |
| 54    | GND                                                  |      | 53    | SAI5_TXFS<br>ENET1_RGMII_RX_CTL<br>GPIO4_IO10                        |      |
| 56    | MIPI_CSI2_D3_N                                       |      | 55    | SAI5_TXC<br>ENET1_RGMII_RXC<br>GPIO4_IO11                            |      |
| 58    | MIPI_CSI2_D3_P                                       |      | 57    | V_SOM                                                                |      |
| 60    | SAI5_TXD0<br>ENET1_RGMII_TD0<br>GPIO4_IO12           |      | 59    | SD1_DATA1<br>I2C6_SDA<br>UART1_CTS_B<br>ENET1_RGMII_TD0<br>GPIO2_IO3 |      |
| 62    | SD1_RESET_B<br>I2C3_SCL<br>UART3_RTS_B<br>GPIO2_IO10 |      | 61    | SD1_DATA0<br>I2C6_SCL<br>UART1_RTS_B<br>ENET1_RGMII_TD1<br>GPIO2_IO2 |      |
| 64    | PWRBTN                                               |      | 63    | SAI5_TXD2<br>ENET1_RGMII_TD2<br>GPIO4_IO14                           |      |
| 66    | RESERVED                                             |      | 65    | SAI5_TXD3<br>ENET1_RGMII_TD3<br>GPIO4_IO15                           |      |

|     |                                                                    |  |    |                                                                   |  |
|-----|--------------------------------------------------------------------|--|----|-------------------------------------------------------------------|--|
| 68  | SD1_CLK<br>I2C5_SCL<br>UART1_TXD<br>ENET_MDC<br>GPIO2_IO0          |  | 67 | ENET1_RGMII_TX_CTL<br>GPIO4_IO16                                  |  |
| 70  | SD1_CMD<br>I2C5_SDA<br>UART1_RXD<br>ENET_MDIO<br>GPIO2_IO1         |  | 69 | ENET1_RGMII_TXC<br>GPIO4_IO17                                     |  |
| 72  | GND                                                                |  | 71 | V_SOM                                                             |  |
| 74  | ETH0_MDI0P<br>ENET_TX_CTL<br>GPIO1_IO22                            |  | 73 | ETH0_MDI0N<br>ENET_TD3<br>GPIO1_IO18                              |  |
| 76  | SAI5_TXD1<br>UART1_CTS_B<br>GPIO4_IO24                             |  | 75 | ETH0_LINK-LED_1000<br>ENET_TD0<br>GPIO1_IO21                      |  |
| 78  | ETH0_MDI1P<br>ENET_TD1<br>GPIO1_IO20                               |  | 77 | ENET_TD2<br>GPIO1_IO19                                            |  |
| 80  | ETH0_MDI1N<br>ENET_RXC<br>SAI7_TXC<br>GPIO1_IO25                   |  | 79 | ETH0_MDI2P<br>ENET_RX_CTL<br>SAI7_TX_SYNC<br>GPIO1_IO24           |  |
| 82  | GND                                                                |  | 81 | ETH0_MDI2N<br>ENET_TXC<br>SAI7_TXD0<br>GPIO1_IO23                 |  |
| 84  | ETH0_MDI3P<br>ENET_RD2<br>SAI7_RXC<br>GPIO1_IO28                   |  | 83 | ETH0_LED_ACT<br>ENET_RD1<br>SAI7_RXFS<br>GPIO1_IO27               |  |
| 86  | ETH0_LINK-LED_10_100<br>ENET_RD0<br>SAI7_RXD0<br>GPIO1_IO26        |  | 85 | ETH0_MDI3N<br>ENET_RD3<br>SAI7_MCLK<br>GPIO1_IO29                 |  |
| 88  | SAI5_TXFS<br>SAI5_TXD1<br>UART1_TXD<br>GPIO4_IO21                  |  | 87 | V_SOM                                                             |  |
| 90  | I2C4_SCL<br>ECSPi2_MISO<br>PWM2_OUT<br>PCIE_CLKREQ_B<br>GPIO5_IO20 |  | 89 | ECSPi2_MISO<br>SAI7_MCLK<br>I2C4_SCL<br>UART4_CTS_B<br>GPIO5_IO12 |  |
| 92  | SD2_CD_B<br>GPIO2_IO12                                             |  | 91 | ECSPi2_SS0<br>I2C4_SDA<br>UART4_RTS_B<br>GPIO5_IO13               |  |
| 94  | SD2_DATA2<br>ECSPi2_SS0<br>GPIO2_IO17                              |  | 93 | ECSPi2_SCLK<br>SAI7_TXC<br>I2C3_SCL<br>UART4_RXD<br>GPIO5_IO10    |  |
| 96  | SD2_CLK<br>UART4_RXD<br>ECSPi2_SCLK<br>GPIO2_IO13                  |  | 95 | ECSPi2_MOSI<br>SAI7_TXD0<br>I2C3_SDA<br>UART4_TXD<br>GPIO5_IO11   |  |
| 98  | SD2_DATA3<br>ECSPi2_MISO<br>GPIO2_IO18                             |  | 97 | SD2_DATA0<br>I2C4_SDA<br>UART2_RXD<br>GPIO2_IO15                  |  |
| 100 | SD2_CMD<br>UART4_TXD<br>ECSPi2_MOSI<br>GPIO2_IO14                  |  | 99 | SD2_DATA1<br>I2C4_SCL<br>UART2_TXD<br>GPIO2_IO16                  |  |

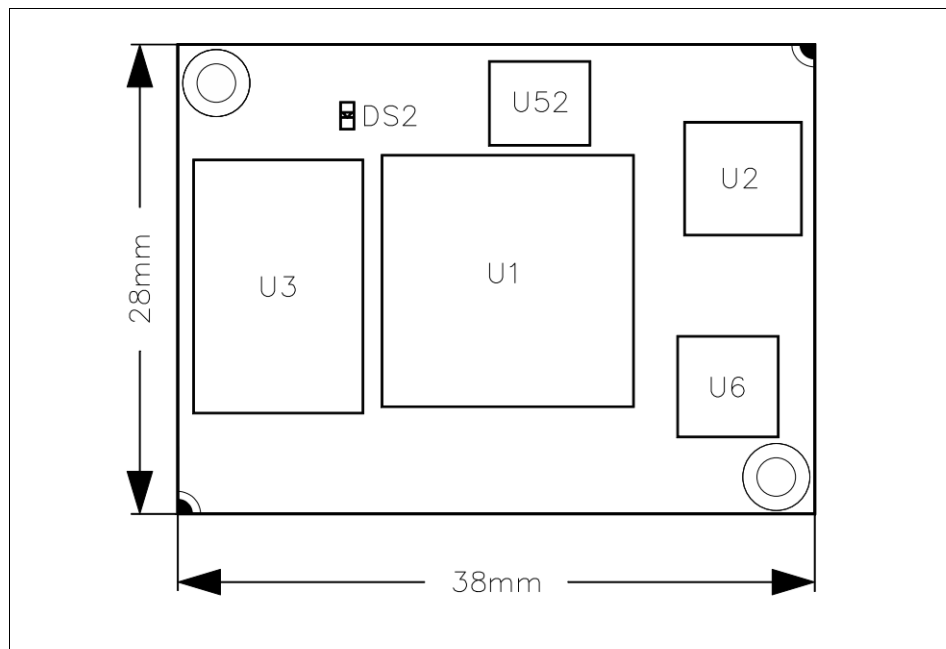
## 6.2 Mating Connectors

**Table 47 Connector type**

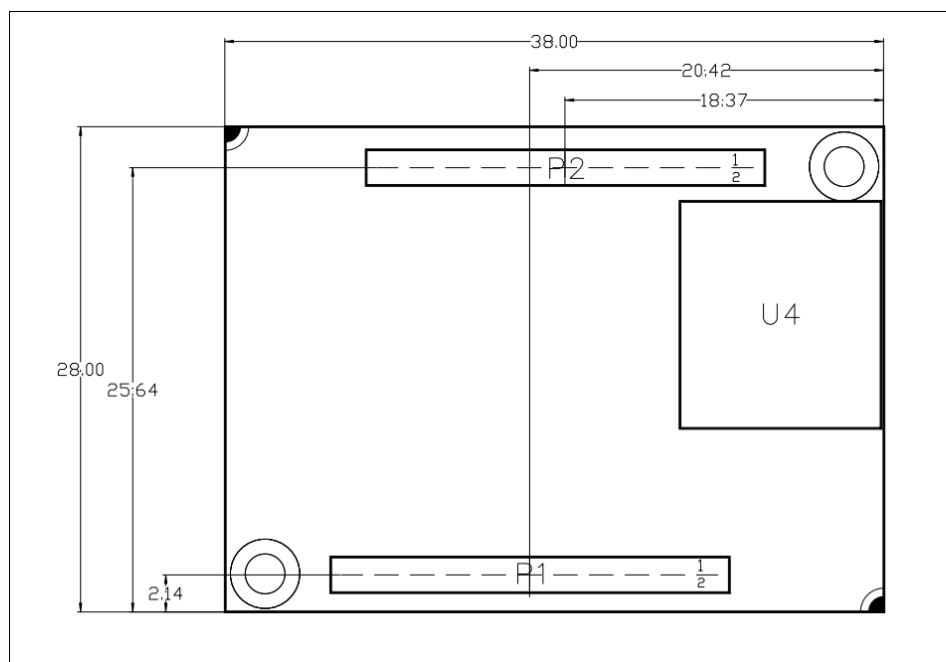
| UCM-iMX8M-Plus connector |                           | Carrier board (mating) connector P/N |                            |               |
|--------------------------|---------------------------|--------------------------------------|----------------------------|---------------|
| Ref.                     | Implementation            | Mfg.                                 | P/N                        | Mating Height |
| P1, P2                   | Hirose DF40C-100DP-0.4V51 | Hirose                               | DF40HC(3.0)-100DS-0.4V(51) | 3.0mm         |
|                          |                           | Hirose                               | DF40C-100DS-0.4V51         | 1.5mm         |

## 6.3 Mechanical Drawings

**Figure 3 UCM-iMX8M-Plus top**



**Figure 4 UCM-iMX8M-Plus bottom**



1. All dimensions are in millimeters.
2. The height of all components is  $< 2.0\text{mm}$ .
3. Baseboard connectors provide  $3 \pm 0.15\text{mm}$  board-to-board clearance.
4. Board thickness is  $1.6\text{mm}$ .

3D model and mechanical drawings in DXF format are available at

<https://www.compulab.com/products/computer-on-modules/UCM-iMX8M-Plus-nxp-i-mx-8m-mini-som-system-on-module-computer/#devres>

## 6.4 Heat Spreader and Cooling Solutions

UCM-iMX8M-Plus is provided with an optional heat-spreader assembly. The UCM-iMX8M-Plus heat-spreader is designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the UCM-iMX8M-Plus temperature specifications. Various thermal management solutions can be used, including active and passive heat dissipation approaches.

## 7 OPERATIONAL CHARACTERISTICS

### 7.1 Absolute Maximum Ratings

**Table 48 Absolute Maximum ratings**

| Parameter                               | Min  | Max | Unit |
|-----------------------------------------|------|-----|------|
| Main power supply voltage (V_SOM)       | -0.3 | 5.5 | V    |
| Voltage on any non-power supply pin     | -0.5 | 3.6 | V    |
| Backup battery supply voltage (VCC_RTC) | -0.3 | 3.8 | V    |

**NOTE:** Exceeding the absolute maximum ratings may damage the device.

### 7.2 Recommended Operating Conditions

**Table 49 Recommended Operating Conditions**

| Parameter                               | Min  | Typ. | Max | Unit |
|-----------------------------------------|------|------|-----|------|
| Main power supply voltage (V_SOM)       | 3.45 | 3.7  | 5.5 | V    |
| Backup battery supply voltage (VCC_RTC) | 1.5  | 3.0  | 3.6 | V    |

### 7.3 Typical Power Consumption

**Table 50 SOM Typical Power Consumption**

| Use case             | Use case description                           | I <sub>SOM</sub> | P <sub>SOM</sub> |
|----------------------|------------------------------------------------|------------------|------------------|
| Linux up – low-power | Linux up, Ethernet down, display output off    | 270mA            | 1012mW           |
| Linux up – typical   | Linux up, Ethernet link up, display output on  | 405mA            | 1518mW           |
| Video playback       | Video playback with GStreamer in Linux         | 600mA            | 2250mW           |
| High CPU load        | CPU stress test (stress-ng)                    | 970mA            | 3637mW           |
| GPU load             | GPU load on 1280x720 @60Hz                     | 720mA            | 2700mW           |
| Heavy mixed load     | GPU load + CPU stress test + Ethernet activity | 1180mA           | 4425mW           |

Power consumption has been measured with the following setup:

1. Stock module configuration - UCM-iMX8PLUS-C1800QM-D4-N32-E-H
2. SB-UCMIMX8PLUS carrier-board, V\_SOM = 3.75V
3. 5" WXGA LCD panel
4. Ambient temperature of 25C

**Table 51 Deep Sleep and OFF Power Consumption**

| Use case        | Use case description                     | I <sub>SOM</sub> | P <sub>SOM</sub> |
|-----------------|------------------------------------------|------------------|------------------|
| Deep sleep mode | CPU in deep sleep. DRAM in self-refresh. | 10mA             | 37mW             |
| OFF mode        | Linux shutdown / poweroff                | 2mA              | 7.5mW            |

**Table 52 RTC timekeeping current**

| Use case | Use case description                                                               | I <sub>VCC_RTC</sub> |
|----------|------------------------------------------------------------------------------------|----------------------|
| RTC only | VCC_RTC (3.0V) is supplied from external coin-cell battery<br>V_SOM is not present | 70nA                 |

## 7.4 ESD Performance

**Table 53 ESD Performance**

| Interface        | ESD Performance                                            |
|------------------|------------------------------------------------------------|
| i.MX8M Plus pins | 2kV Human Body Model (HBM), 500V Charge Device Model (CDM) |

## 8 APPLICATION NOTES

### 8.1 Carrier Board Design Guidelines

- Ensure that all V\_SOM and GND power pins are connected.
- Major power rails - V\_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V\_SOM and GND near the mating connectors.
- Except for a power connection, no other connection is mandatory for UCM-iMX8M-Plus operation. All power-up circuitry and all required pullups/pulldowns are available onboard UCM-iMX8M-Plus.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- The carrier board interface connectors provide 3mm mating height. Bear in mind that there are components on the bottom side of UCM-iMX8M-Plus. It is not recommended to place any components underneath the UCM-iMX8M-Plus module.
- Refer to the SB-UCMIMX8PLUS carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

### 8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise, corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V\_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First, perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.

- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from UCM-iMX8M-Plus, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-UCMIMX8PLUS carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.