MCM-iMX95

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
September 2025	• Initial release

Please check for a newer revision of this manual at the Compulab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program Compulab MCM-iMX95 System-on-Module.

1.2 MCM-iMX95 Part Number Legend

Please refer to the Compulab website 'Ordering information' section to decode the MCM-iMX95 part number: https://www.compulab.com/products/computer-on-modules/mcm-imx95-nxp-i-mx-95-som-smd-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
MCM-iMX95 Developer Resources	https://www.compulab.com/products/computer-on-modules/ucm-imx95-nxp-i-mx95-som-system-on-module-computer/#devres
i.MX95 Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-95-applications-processor-family-high-performance-safety-enabled-platform-with-eiq-neutron-npu:iMX95
i.MX95 Datasheet	

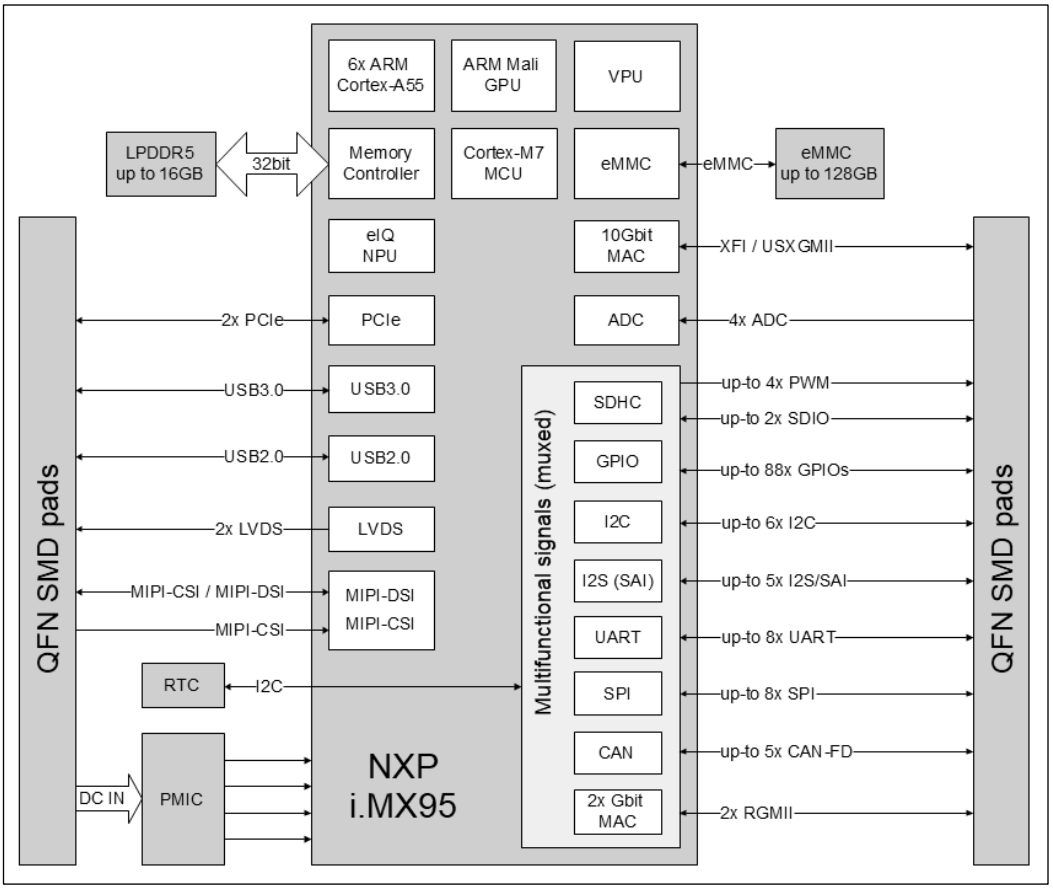
2 OVERVIEW

2.1 Highlights

- NXP i.MX95 processor, up-to 2.0 GHz
- Up to 16GB LPDDR5 and 128GB eMMC
- ARM Mali GPU and 4K VPU
- Integrated eIQ® Neutron NPU
- 2x LVDS, MIPI-DSI, 2x MIPI-CSI with ISP
- 10GbE, 2x RGMII, 2x PCIe, USB3.0
- 5x CAN, 8x UART, 8xSPI, 88x GPIO
- Tiny size and weight - 34 x 42 x 3 mm, 8 gram

2.2 Block Diagram

Figure 1 MCM-iMX95 Block Diagram



2.3 Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX95, 6x ARM Cortex-A55, 2.0 GHz	C1800HM
VPU	4K video decode and encode	C1800HM
GPU	ARM Mali-G310 GPU OpenGL® ES 3.2, Vulkan® 1.2, OpenCL 3.0	+
NPU	eIQ® Neutron NPU	C1800HM
Real-Time Co-processor	ARM Cortex-M7 + ARM Cortex-M33	+
Memory and Storage		
RAM	4GB-16GB, LPDDR5	D
Storage	eMMC flash, 16GB - 128GB	N
Display, Camera and Audio		
Display	LVDS, 2x 4-lane or 1x 8-lane , up to 1080p60	+
	MIPI-DSI, 4 data lanes, up to 4kp30 or 3840x1440p60	+
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Audio	Up-to 5x I2S / SAI	+
	S/PDIF input/output	+
Network		
10 Gbit Ethernet	10 GbE MAC	+
RGMII	2x Ethernet RGMII	+
I/O		
PCI Express	2x PCIe Gen 3.0 1x lane	+
USB	1x USB3.0 + 1x USB2.0	+
UART	Up-to 8x UART	+
CAN bus	Up-to 5x CAN	+
SD/SDIO	Up-to 2x SD/SDIO	+
SPI	Up to 8x SPI	+
I2C	Up to 6x I2C	+
ADC	Up-to 4x general-purpose ADC inputs	
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 88x GPIO (multifunctional signals shared with other functions)	+
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

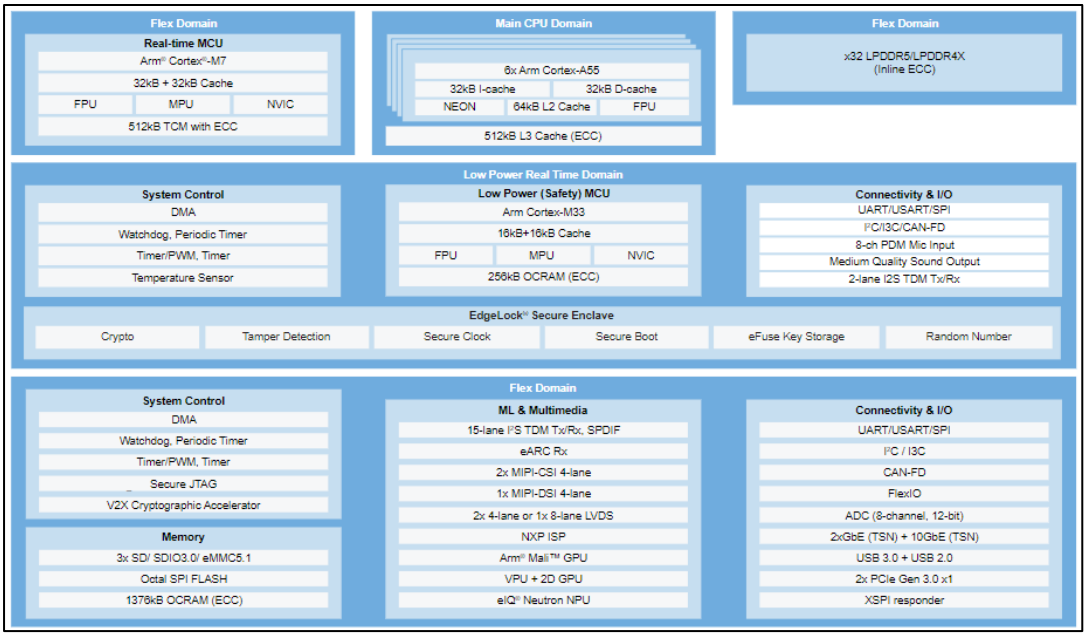
Electrical Specifications	
Supply Voltage	3.45V to 5.0V
Digital I/O voltage	3.3V
Mechanical Specifications	
Dimensions	34 x 42 x 3 mm
Weight	8 gram
Package	180-pin, 0.8mm pitch QFN
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX95 System-on-Chip

The i.MX 95 System-on-Chip (SoC) includes powerful 6x Arm® Cortex®-A55 processors with speeds up to 2.0 GHz integrated with a NPU that accelerates machine learning inference. An Arm® Cortex®-M33 running up to 333 MHz and Cortex®-M7 running up to 800 MHz for real-time and low-power processing.

Figure 2 i.MX 95 Block Diagram



3.2 Memory

3.2.1 DRAM

MCM-iMX95 is equipped with up to 16GB of onboard LPDDR5 memory. The LPDDR5 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

MCM-iMX95 uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

MCM-iMX95 implements a variety of peripheral interfaces through the 180-pad carrier board footprint. The following notes apply to interfaces available through the carrier-board connectors:

- Some of the MCM-iMX95 carrier board interface pads are multifunctional. Up to 8 functions (ALT modes) are accessible through each multifunctional pin. For additional details, please refer to chapter 5.6.
- All of the MCM-iMX95 digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#” –** Pin number on the carrier board interface footprint
- **“Type” –** Signal type, see the definition of different signal types below
- **“Description” –** Signal description with regards to the interface in question
- **“Voltage Domain”** – Voltage level of the particular signal

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **"O"** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **"PD" -** Always pulled down onboard MCM-iMX95, followed by pull value.
- **"PU" -** Always pulled up onboard MCM-iMX95, followed by pull value.
- **“LVDS” -** Low-voltage differential signaling.

4.1 Display Interfaces

4.1.1 MIPI-DSI

The MCM-iMX95 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX95 SoC. It is mutually exclusive with one of the MIPI-CSI interfaces. Both DSI and CSI are routed directly to the carrier board interface. The following main features are supported:

- Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- Maximum data rate per lane of 2.5 Gbps
- Resolution ranges: 4Kp30 or 3840 x 1440 p60

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the MIPI-DSI interface signals.

Table 5 MIPI-DSI Interface Signals

Signal Name	Pin #	Type	Description
MIPI_DSICSI_CLK_N	15	AO	Negative part of MIPI-DSICSI clock diff-pair
MIPI_DSICSI_CLK_P	16	AO	Positive part of MIPI-DSICSI clock diff-pair
MIPI_DSICSI_D0_N	11	AO	Negative part of MIPI-DSICSI data diff-pair 0
MIPI_DSICSI_D0_P	12	AO	Positive part of MIPI-DSICSI data diff-pair 0
MIPI_DSICSI_D1_N	13	AO	Negative part of MIPI-DSICSI data diff-pair 1
MIPI_DSICSI_D1_P	14	AO	Positive part of MIPI-DSICSI data diff-pair 1
MIPI_DSICSI_D2_N	17	AO	Negative part of MIPI-DSICSI data diff-pair 2
MIPI_DSICSI_D2_P	18	AO	Positive part of MIPI-DSICSI data diff-pair 2
MIPI_DSICSI_D3_N	19	AO	Negative part of MIPI-DSICSI data diff-pair 3
MIPI_DSICSI_D3_P	20	AO	Positive part of MIPI-DSICSI data diff-pair 3

4.1.2 LVDS

MCM-iMX95 provides a dual LVDS interface derived from the i.MX95 LVDS display bridge. It supports the following key features:

- 2x 4-lane or 1x 8-lane operation modes
- Resolutions of up to 1080p60

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the LVDS interface signals.

Table 6 LVDS Interface Signals

Signal Name	Pin #	Type	Description
LVDS0_CLK_N	29	AO	Negative part of LVDS0 clock diff-pair
LVDS0_CLK_P	30	AO	Positive part of LVDS0 clock diff-pair
LVDS0_D0_N	25	AO	Negative part of LVDS0 data diff-pair 0
LVDS0_D0_P	26	AO	Positive part of LVDS0 data diff-pair 0
LVDS0_D1_N	27	AO	Negative part of LVDS0 data diff-pair 1
LVDS0_D1_P	28	AO	Positive part of LVDS0 data diff-pair 1
LVDS0_D2_N	23	AO	Negative part of LVDS0 data diff-pair 2
LVDS0_D2_P	24	AO	Positive part of LVDS0 data diff-pair 2
LVDS0_D3_N	21	AO	Negative part of LVDS0 data diff-pair 3
LVDS0_D3_P	22	AO	Positive part of LVDS0 data diff-pair 3
LVDS1_CLK_N	35	AO	Negative part of LVDS1 clock diff-pair
LVDS1_CLK_P	36	AO	Positive part of LVDS1 clock diff-pair

Signal Name	Pin #	Type	Description
LVDS1_D0_N	31	AO	Negative part of LVDS1 data diff-pair 0
LVDS1_D0_P	32	AO	Positive part of LVDS1 data diff-pair 0
LVDS1_D1_N	33	AO	Negative part of LVDS1 data diff-pair 1
LVDS1_D1_P	34	AO	Positive part of LVDS1 data diff-pair 1
LVDS1_D2_N	37	AO	Negative part of LVDS1 data diff-pair 2
LVDS1_D2_P	38	AO	Positive part of LVDS1 data diff-pair 2
LVDS1_D3_N	39	AO	Negative part of LVDS1 data diff-pair 3
LVDS1_D3_P	40	AO	Positive part of LVDS1 data diff-pair 3

4.2 Camera Interface

MCM-iMX95 provides two MIPI-CSI interfaces, derived from the MIPI CSI host controllers integrated into the i.MX95 SoC. One MIPI-CSI interface is mutually exclusive with MIPI-DSI interface. Both DSI and CSI are routed directly to the carrier board interface. The following main features are supported:

- Up-to four data lanes and one clock lane for each interface
- Complaint with MIPI CSI-2 specification v2.0 and MIPI D-PHY specification v1.2

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 7 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description
MIPI_DSICSI_CLK_N	15	AO	Negative part of MIPI-DSICSI clock diff-pair
MIPI_DSICSI_CLK_P	16	AO	Positive part of MIPI- DSICSI clock diff-pair
MIPI_DSICSI_D0_N	11	AO	Negative part of MIPI- DSICSI data diff-pair 0
MIPI_DSICSI_D0_P	12	AO	Positive part of MIPI- DSICSI data diff-pair 0
MIPI_DSICSI_D1_N	13	AO	Negative part of MIPI- DSICSI data diff-pair 1
MIPI_DSICSI_D1_P	14	AO	Positive part of MIPI- DSICSI data diff-pair 1
MIPI_DSICSI_D2_N	17	AO	Negative part of MIPI- DSICSI data diff-pair 2
MIPI_DSICSI_D2_P	18	AO	Positive part of MIPI- DSICSI data diff-pair 2
MIPI_DSICSI_D3_N	19	AO	Negative part of MIPI- DSICSI data diff-pair 3
MIPI_DSICSI_D3_P	20	AO	Positive part of MIPI- DSICSI data diff-pair 3
MIPI_CSI_CLK_N	5	AO	Negative part of MIPI-CSI clock diff-pair
MIPI_CSI_CLK_P	6	AO	Positive part of MIPI- CSI clock diff-pair
MIPI_CSI_D0_N	1	AO	Negative part of MIPI- CSI data diff-pair 0
MIPI_CSI_D0_P	2	AO	Positive part of MIPI- CSI data diff-pair 0
MIPI_CSI_D1_N	3	AO	Negative part of MIPI- CSI data diff-pair 1
MIPI_CSI_D1_P	4	AO	Positive part of MIPI- CSI data diff-pair 1
MIPI_CSI_D2_N	7	AO	Negative part of MIPI- CSI data diff-pair 2
MIPI_CSI_D2_P	8	AO	Positive part of MIPI- CSI data diff-pair 2
MIPI_CSI_D3_N	9	AO	Negative part of MIPI- CSI data diff-pair 3
MIPI_CSI_D3_P	10	AO	Positive part of MIPI- CSI data diff-pair 3

4.3 Audio Interfaces

4.3.1 S/PDIF

MCM-iMX95 provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 8 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPDIF_IN	112	I	SPDIF input data line signal	3.3V
	54			ENET
	56			ENET
SPDIF_OUT	109	O	SPDIF output data line signal	3.3V
	56			ENET

NOTE: Pins denoted "ENET" can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: S/PDIF signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.2 SAI

MCM-iMX95 supports up-to five of the i.MX95 integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 2 data lines. One receiver with independent bit clock and frame sync supporting 2 data lines.
- Maximum Frame Size of 32 words per data line.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive data line

Please refer to the i.MX95 Reference manual for additional details. The tables below summarize the SAI interface signals.

Table 9 SAI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI1_MCLK	134	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V
	130			3.3V
SAI1_RX_DATA[0]	130	I	Receive data, sampled synchronously by the bit clock	3.3V
SAI1_TX_DATA[0]	83	O	Transmit data signal synchronous to bit clock.	3.3V
SAI1_TX_DATA[1]	84	O	Transmit data signal synchronous to bit clock.	3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI1_TXC	131	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V
SAI1_TXFS	84	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V

NOTE: SAI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 10 SAI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI2_MCLK	55	IO	Audio master clock. An input when generated externally and an output when generated internally.	ENET
SAI2_TX_DATA[0]	52	O	Transmit data signal synchronous to bit clock.	ENET
SAI2_TX_DATA[1]	51	O	Transmit data signal synchronous to bit clock.	ENET
SAI2_TX_DATA[2]	53	O	Transmit data signal synchronous to bit clock.	ENET
SAI2_TX_DATA[3]	54	O	Transmit data signal synchronous to bit clock.	ENET
SAI2_TX_BCLK	45	O	Transmit bit clock. An input when generated externally and an output when generated internally.	ENET
SAI2_TXFS	46	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET

NOTE: Pins denoted "ENET" can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: SAI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 11 SAI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI3_MCLK	115	IO	Audio master clock. An input when generated externally and an output when generated internally.	3.3V
SAI3_RX_BCLK	57 60	I	Receive bit clock. An input when generated externally and an output when generated internally.	3.3V
SAI3_RXFS	59 114	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V
SAI3_RX_DATA[0]	58	I	Receive data, sampled synchronously by the bit clock	3.3V
SAI3_TX_DATA[0]	57 59	O	Transmit data signal synchronous to bit clock.	3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI3_TX_BCLK	119	O	Transmit bit clock. An input when generated externally and an output when generated internally.	3.3V
SAI3_TXFS	108	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	3.3V

NOTE: SAI3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 12 SAI4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI4_RX_BCLK	53	I	Receive bit clock. An input when generated externally and an output when generated internally.	ENET
SAI4_RXFS	51	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET
SAI4_RX_DATA[0]	54	I	Receive data, sampled synchronously by the bit clock	ENET
SAI4_TX_DATA[0]	47	O	Transmit data signal synchronous to bit clock.	ENET
SAI4_TX_BCLK	48	O	Transmit bit clock. An input when generated externally and an output when generated internally.	ENET
SAI4_TXFS	49	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	ENET

NOTE: Pins denoted "ENET" can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: SAI4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 13 SAI5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI5_RX_DATA[0]	85	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI5_RX_DATA[1]	86	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI5_RX_DATA[2]	90	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI5_RX_DATA[3]	89	I	Receive data, sampled synchronously by the bit clock	1.8V
SAI5_RX_BCLK	87	I	Receive bit clock. An input when generated externally and an output when generated internally.	1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI5_RXFS	88	I	Receive frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V
SAI5_TX_DATA[0]	86	O	Transmit data signal synchronous to bit clock.	1.8V
SAI5_TX_DATA[1]	85	O	Transmit data signal synchronous to bit clock.	1.8V
SAI5_TX_DATA[2]	88	O	Transmit data signal synchronous to bit clock.	1.8V
SAI5_TX_DATA[3]	87	O	Transmit data signal synchronous to bit clock.	1.8V
SAI5_TX_BCLK	89	O	Transmit bit clock. An input when generated externally and an output when generated internally.	1.8V
SAI5_TXFS	90	O	Transmit frame sync. An input sampled by bit clock when generated externally. A bit clock synchronous output when generated internally.	1.8V

NOTE: SAI5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.3 MQS

MCM-iMX95 supports up-to two MOQ interfaces that can be used to generate medium quality audio via standard GPIO.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the S/PDIF interface signals.

Table 14 MQS Signals

Signal Name	Pin #	Type	Description	Voltage Domain
MQS1_LEFT	84	O	Left signal output	3.3V
MQS1_RIGHT	130	O	Right signal output	3.3V
	138			
MQS2_LEFT	44	O	Left signal output	1.8
	56			ENET
	98			SD2
MQS2_RIGHT	43	O	Right signal output	1.8
	55			ENET
	97			SD2

NOTE: Pins denoted “SD2” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

NOTE: Pins denoted “ENET” can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: MQS signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.3.4 PDM

MCM-iMX95 supports up-to four microphone PDM interfaces that delivers audio from microphones to the processor.

Please refer to the i.MX95 Reference manual for additional details. The following table summarizes the PDM interface signals.

Table 15 PDM Signals

Signal Name	Pin #	Type	Description	Voltage Domain
PDM_CLK	133 57	I	Clock signal that synchronizes the generation and processing of the PDM bit streams	3.3V
PDM_BIT_STREAM0	132 58 138	I	PDM input channel 0	3.3V
PDM_BIT_STREAM1	122 108	I	PDM input channel 1	3.3V
PDM_BIT_STREAM2	114 119	I	PDM input channel 2	3.3V
PDM_ BIT_STREAM3	117 59	I	PDM input channel 3	3.3V

NOTE: PDM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.4 Ethernet

4.4.1 10 Gigabit Ethernet

MCM-iMX95 provides one 10 Gigabit Ethernet controller. The controller supports XFI, SGMII (2.5G and 1G), and 10G-USXGMII (single 10GE mode only).

The tables below summarize the 10GbE interface signals.

Table 16 10GbE Interface Signals

Signal Name	Pin #	Type	Description
ETH_CLKIN_N	61	I	10GbE reference clock negative
ETH_CLKIN_P	62	I	10GbE reference clock positive
ETH_RX0_N	63	I	10GbE receive data negative
ETH_RX0_P	64	I	10GbE receive data positive
ETH_TX0_N	65	O	10GbE transmit data negative
ETH_TX0_P	66	O	10GbE transmit data positive

4.4.2 RGMII

MCM-iMX95 features two RMGII interfaces.

The tables below summarize the Ethernet RGMII interface signals.

Table 17 RGMII ENET1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET1_MDC	82	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	ENET
ENET1_MDIO	81	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	ENET
ENET1_RD0	76	I	Ethernet input data from the PHY	ENET
ENET1_RD1	77	I	Ethernet input data from the PHY	ENET
ENET1_RD2	79	I	Ethernet input data from the PHY	ENET
ENET1_RD3	80	I	Ethernet input data from the PHY	ENET
ENET1_RX_CTL	75	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	ENET
ENET1_RXC	74	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	ENET
ENET1_TD0	69	O	Ethernet output data to PHY	ENET
ENET1_TD1	71	O	Ethernet output data to PHY	ENET
ENET1_TD2	72	O	Ethernet output data to PHY	ENET
ENET1_TD3	73	O	Ethernet output data to PHY	ENET
ENET1_TXC	67	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	ENET
ENET1_TX_CTL	68	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	ENET

NOTE: ENET1 signals can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: ENET1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 18 RGMII ENET2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ENET2_RD0	53	I	Ethernet input data from the PHY	ENET
ENET2_RD1	54	I	Ethernet input data from the PHY	ENET
ENET2_RD2	55	I	Ethernet input data from the PHY	ENET
ENET2_RD3	56	I	Ethernet input data from the PHY	ENET
ENET2_RX_CTL	52	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	ENET
ENET2_RXC	51	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII MODE	ENET
ENET2_TD0	47	O	Ethernet output data to PHY	ENET
ENET2_TD1	48	O	Ethernet output data to PHY	ENET
ENET2_TD2	49	O	Ethernet output data to PHY	ENET

Signal Name	Pin #	Type	Description	Voltage Domain
ENET2_TD3	50	O	Ethernet output data to PHY	ENET
ENET2_TXC	45	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII MODE	ENET
ENET2_TX_CTL	46	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	ENET

NOTE: ENET2 signals can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: ENET2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.5 PCI-Express

MCM-iMX95 provides two PCI Express Gen 3.0 ports.

The tables below summarize the PCIe interface signals.

Table 19 PCIE1 Interface Signals

Signal Name	Pin #	Type	Description
PCIE_CLKOUT_N	161	O	100 MHz PCIe reference clock differential output negative
PCIE_CLKOUT_P	162	O	100 MHz PCIe reference clock differential output positive
PCIE1_CLKIN_N	157	I	100 MHz PCIe reference clock differential input negative
PCIE1_CLKIN_P	158	I	100 MHz PCIe reference clock differential input positive
PCIE1_RX0_N	159	I	PCI Express receive data negative
PCIE1_RX0_P	160	I	PCI Express receive data positive
PCIE1_TX0_N	146	O	PCI Express transmit data negative
PCIE1_TX0_P	147	O	PCI Express transmit data positive
PCIE1_CLK_REQ	106	O	PCI Express Enable external clock generator

NOTE: PCIE1_CLK_REQ signal is multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 20 PCIE2 Interface Signals

Signal Name	Pin #	Type	Description
PCIE_CLKOUT_N	161	O	100 MHz PCIe reference clock differential output negative
PCIE_CLKOUT_P	162	O	100 MHz PCIe reference clock differential output positive
PCIE2_CLKIN_N	155	I	100 MHz PCIe reference clock differential input negative
PCIE2_CLKIN_P	156	I	100 MHz PCIe reference clock differential input positive
PCIE2_RX0_N	153	I	PCI Express receive data negative
PCIE2_RX0_P	154	I	PCI Express receive data positive
PCIE2_TX0_N	144	O	PCI Express transmit data negative
PCIE2_TX0_P	145	O	PCI Express transmit data positive
PCIE2_CLK_REQ	100	O	PCI Express Enable external clock generator

NOTE: PCIE2_CLK_REQ signal is multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.6 USB

MCM-iMX95 provides one USB3.0 port and one USB2.0 port. Both can be configured as host or device. USB3.0 integrates two pairs of TX/RX signals which can be connected to a type-C connector directly without external high-speed switch chip.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the USB interface signals.

Table 21 USB port #1 Signals

Signal Name	Pin #	Type	Description
USB1_DN	174	IO	USB2.0 negative data
USB1_DP	173	IO	USB2.0 positive data
USB1_VBUS	179	I	USB1 VBUS detect
USB1_ID	177	I	USB1 ID
USB1_TX0_N	150	AO	USB3.0 transmit negative lane
USB1_TX0_P	149	AO	USB3.0 transmit positive lane
USB1_RX0_N	172	AI	USB3.0 receive negative lane
USB1_RX0_P	171	AI	USB3.0 receive positive lane
USB1_TX1_N	151	AO	USB3.0 transmit negative lane
USB1_TX1_P	152	AO	USB3.0 transmit positive lane
USB1_RX1_N	175	AI	USB3.0 receive negative lane
USB1_RX1_P	176	AI	USB3.0 receive positive lane

Table 22 USB port #2 Signals

Signal Name	Pin #	Type	Description
USB2_DN	163	IO	USB2.0 negative data
USB2_DP	164	IO	USB2.0 positive data
USB2_VBUS	180	I	USB2 VBUS detect
USB2_ID	178	I	USB2 ID

4.7 MMC / SD /SDIO

MCM-iMX95 features two SD/SDIO ports. These ports are derived from the i.MX95 uSDHC2 and uSDHC3 controllers. uSDHC IP supports the following main features:

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.0 command/response sets and physical layer

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 23 SD2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SD2_CLK	96	O	Clock for MMC/SD/SDIO card	SD2
SD2_CMD	95	IO	CMD line connect to card	SD2
SD2_DATA0	94	IO	DATA0 line in all modes. Also used to detect busy state	SD2
SD2_DATA1	93	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	SD2
SD2_DATA2	97	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	SD2
SD2_DATA3	98	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	SD2
SD2_RESET#	78	O	Card hardware reset signal, active LOW	SD2
SD2_CD#	92	I	Card detection pin	SD2

NOTE: SD2 pins can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

NOTE: SD2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 24 SD3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SD3_CLK	85	O	Clock for MMC/SD/SDIO card	1.8V
	112			3.3V
SD3_CMD	88	IO	CMD line connect to card	1.8V
	109			3.3V
SD3_DATA0	87	IO	DATA0 line in all modes. Also used to detect busy state	1.8V
SD3_DATA1	105	IO	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4- bit mode	3.3V
	86			1.8V
SD3_DATA2	108	IO	DATA2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	3.3V
	90			1.8V
SD3_DATA3	102	IO	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode.	3.3V
	89			1.8V

NOTE: SD3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.8 UART

MCM-iMX95 features up-to eight UART ports. The i.MX95 UART supports the following features:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 5 Mbps.
- Hardware flow control support for a request to send and clear to send signals.

NOTE: By default UART1 is assigned to be used as the main system console port.

NOTE: UART2 is assigned to be used as the M33 core debug port.

NOTE: UART3 is assigned to be used as the M7 core debug port.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the UART interface signals.

Table 25 UART1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART1_CTS_B	134	O	Clear to send	3.3V
UART1_RTS_B	137	I	Request to send	3.3V
UART1_DSR_B	131	I	Data set ready	3.3V
UART1_DTR_B	83	O	Data terminal ready	3.3V
UART1_RXD	135	I	Serial data receive	3.3V
UART1_TXD/BT_MODE0	148	O	Serial data transmit	3.3V

NOTE: UART1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 26 UART2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART2_CTS_B	131	O	Clear to send	3.3V
UART2_RTS_B	83	I	Request to send	3.3V
UART2_DSR_B	130	I	Data set ready	3.3V
UART2_DTR_B	84	O	Data terminal ready	3.3V
UART2_RXD	134	I	Serial data receive	3.3V
UART2_TXD/BT_MODE1	137	O	Serial data transmit	3.3V

NOTE: UART2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 27 UART3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART3_CTS_B	119	O	Clear to send	3.3V
	77			ENET
UART3_RTS_B	115	I	Request to send	3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
	71			ENET
UART3_RX	113	I	Serial data receive	3.3V
	76			ENET
UART3_TX	110	O	Serial data transmit	3.3V
	69			ENET
UART3_DTR_B	68	O	Data terminal ready	ENET
UART3_DSR_B	75	I	Data set ready	ENET
UART3_RIN_B	81	I	Receive interrupt number	ENET
UART3_DCB_B	82	O	Device control block	ENET

NOTE: ENET3 signals can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: UART3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 28 UART4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART4_RXD	113	I	Serial data receive	3.3V
	53			ENET
UART4_TXD	110	O	Serial data transmit	3.3V
	47			ENET
UART4_CTS_B	119	O	Clear to send	3.3V
	55			ENET
UART4_RTS_B	115	I	Request to send	3.3V
	48			ENET
UART4_DTR_B	46	O	Data terminal ready	ENET
UART4_DSR_B	52	I	Data set ready	ENET

NOTE: Pins denoted “ENET” can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

NOTE: UART4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 29 UART5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART5_RX	128	I	UART-5 serial data receive	3.3V
	44			1.8V
UART5_TX	129	O	UART-5 serial data transmit	3.3V
	43			1.8V
UART5_CTS_B	127	O	UART-5 clear to send	3.3V
	41			1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
UART5_RTS_B	126	I	UART-5 request to send	3.3V
	42			1.8V

NOTE: UART5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 30 UART6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART6_RXD	132	I	Serial data receive	3.3V
	99			
UART6_TXD	133	O	Serial data transmit	3.3V
	106			
UART6_CTS_B	122	O	Clear to send	3.3V
UART6_RTS_B	121	I	Request to send	3.3V
	100			

NOTE: UART6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 31 UART7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART7_RXD	116	I	Serial data receive	3.3V
UART7_TXD	118	O	Serial data transmit	3.3V
UART7_CTS_B	120	O	Clear to send	3.3V
UART7_RTS_B	111	I	Request to send	3.3V

NOTE: UART7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 32 UART8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART8_RXD	117	I	Serial data receive	3.3V
UART8_TXD	114	O	Serial data transmit	3.3V
UART8_CTS_B	110	O	Clear to send	3.3V
UART8_RTS_B	113	I	Request to send	3.3V

NOTE: UART8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.9 CAN-FD

MCM-iMX95 features up-to five CAN-FD interfaces. These interfaces support the following key features:

- Full implementation of the CAN FD protocol and CAN protocol specification version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 33 CAN1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN1_TX	83	O	CAN transmit pin	3.3V
				3.3V
CAN1_RX	131	I	CAN receive pin	3.3V
	138			3.3V

NOTE: CAN1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 34 CAN2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN2_TX	105	O	CAN transmit pin	3.3V
	44			1.8V
	94			SD2
	73			ENET
CAN2_RX	102	I	CAN receive pin	3.3V
	43			1.8V
	93			SD2
	72			ENET

NOTE: CAN2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted “SD2” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL (GPIO3_IO19).

NOTE: Pins denoted “ENET” can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

Table 35 CAN3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN3_TX	103	O	CAN transmit pin	3.3V
CAN3_RX	107	I	CAN receive pin	3.3V

NOTE: CAN3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 36 CAN4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN4_TX	133	O	CAN transmit pin	3.3V
	42			1.8V
CAN4_RX	132	I	CAN receive pin	3.3V
	41			1.8V

NOTE: CAN4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 37 CAN5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN5_TX	112	O	CAN transmit pin	3.3V
	104			3.3V
CAN5_RX	109	I	CAN receive pin	3.3V
	101			3.3V

NOTE: CAN5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.10 SPI

Up-to eight SPI interfaces are accessible through the MCM-iMX95 carrier board interface. The SPI interfaces are derived from i.MX95 integrated low-power SPI modules. The following key features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Direct Memory Access (DMA) support

Please refer to the i.MX95 Reference manual for additional details.

The following tables summarize the SPI interface signals.

Table 38 SPI1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI1_SIN	131	I	Serial data input	3.3V
SPI1_SOUT	130	O	Master data out; slave data in	3.3V
SPI1_SCLK	83	O	Master clock out; slave clock in	3.3V
SPI1_PCS0	84	O	Chip select 0	3.3V
SPI1_PCS1	138	O	Chip select 1	3.3V

NOTE: SPI1 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 39 SPI2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI2_SIN	135	I	Master data in; slave data out	3.3V
SPI2_SOUT	134	O	Master data out; slave data in	3.3V
SPI2_SCLK	137	O	Master clock out; slave clock in	3.3V
SPI2_PCS0	148	O	Chip select 0	3.3V

NOTE: SPI2 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 40 SPI3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI3_SIN	116	I	Master data in; slave data out	3.3V
SPI3_SOUT	120	O	Master data out; slave data in	3.3V
SPI3_SCLK	111	O	Master clock out; slave clock in	3.3V
SPI3_PCS0	118	O	Chip select 0	3.3V
SPI3_PCS1	121	O	Chip select 1	3.3V

NOTE: SPI3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 41 SPI4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI4_SIN	59 100	I	Master data in; slave data out	3.3V
SPI4_SOUT	58	O	Master data out; slave data in	3.3V
SPI4_SCLK	57	O	Master clock out; slave clock in	3.3V
SPI4_PCS0	60	O	Chip select 0	3.3V
SPI4_PCS1	115 99	O	Chip select 1	3.3V
SPI4_PCS2	119 106	O	Chip select 2	3.3V

NOTE: SPI4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 42 SPI5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI5_SIN	59	I	Master data in; slave data out	3.3V
SPI5_SOUT	58	O	Master data out; slave data in	3.3V
SPI5_SCLK	57	O	Master clock out; slave clock in	3.3V
SPI5_PCS0	60	O	Chip select 0	3.3V
SPI5_PCS1	102	O	Chip select 1	3.3V

NOTE: SPI5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 43 SPI6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI6_SIN	128	I	Master data in; slave data out	3.3V
SPI6_SOUT	127	O	Master data out; slave data in	3.3V
SPI6_SCLK	126	O	Master clock out; slave clock in	3.3V
SPI6_PCS0	129	O	Chip select 0	3.3V

NOTE: SPI6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 44 SPI7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI7_SIN	132	I	Master data in; slave data out	3.3V
SPI7_SOUT	122	O	Master data out; slave data in	3.3V
SPI7_SCLK	121	O	Master clock out; slave clock in	3.3V
SPI7_PCS0	133	O	Chip select 0	3.3V
SPI7_PCS1	105	O	Chip select 1	3.3V

NOTE: SPI7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 45 SPI8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPI8_SIN	117	I	Master data in; slave data out	3.3V
SPI8_SOUT	110	O	Master data out; slave data in	3.3V
SPI8_SCLK	113	O	Master clock out; slave clock in	3.3V
SPI8_PCS0	114	O	Chip select 0	3.3V
SPI8_PCS1	108	O	Chip select 1	3.3V

NOTE: SPI8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.11 I2C

MCM-iMX95 features up-to six I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Multi-master operation

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the I2C interface signals.

Table 46 I2C3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C3_SCL	107 128	O	I2C serial clock line	3.3V
I2C3_SDA	103 129	IO	I2C serial data line	3.3V

NOTE: I2C3 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 47 I2C4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C4_SCL	126 101	O	I2C serial clock line	3.3V
I2C4_SDA	127 104	IO	I2C serial data line	3.3V

NOTE: I2C4 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 48 I2C5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C5_SCL	109 128	O	I2C serial clock line	3.3V
I2C5_SDA	112 129	IO	I2C serial data line	3.3V

NOTE: I2C5 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 49 I2C6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C6_SCL	132 127	O	I2C serial clock line	3.3V
I2C6_SDA	133 126	IO	I2C serial data line	3.3V

NOTE: I2C6 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 50 I2C7 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C7_SCL	121 116	O	I2C serial clock line	3.3V
I2C7_SDA	122 118	IO	I2C serial data line	3.3V

NOTE: I2C7 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

Table 51 I2C8 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C8_SCL	111 117	O	I2C serial clock line	3.3V
I2C8_SDA	120 114	IO	I2C serial data line	3.3V

NOTE: I2C8 signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.12 I3C

MCM-iMX95 supports one I3C bus interface.

Please refer to the i.MX95 Reference manual for additional details.

The tables below summarize the I3C interface signals.

Table 52 I3C2 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I3C2_SCL	92	O	Serial clock line	SD2
	82			ENET
I3C2_SDA	96	IO	Serial data line	SD2
	81			ENET
I3C2_PUR	95	O	Pull up resistance. There is internal pull-up resistance on SDA, which is controlled by the I3C controller. If the internal pullup is not enough, PUR can be used to control an external pull-up resistance on SDA actively.	SD2
	71			ENET

NOTE: I3C signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted "SD2" can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

NOTE: Pins denoted "ENET" can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

4.13 Timer/Pulse Width Modulation

i.MX95 supports five multi-channel timer modules (TPM) that can be used for electric motor control and power management. The timer modules support:

- Input capture
- Output comparison
- Generation of PWM signals

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the PDM interface signals.

Table 53 TPM1 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM1_EXTCLK	138	I	External clock	3.3V
TPM1_CH0	135	IO	Channel 0 I/O pin	3.3V
TPM1_CH1	148	IO	Channel 1 I/O pin	3.3V
TPM1_CH2	134	IO	Channel 2 I/O pin	3.3V
TPM1_CH3	137	IO	Channel 3 I/O pin	3.3V

Table 54 TPM3 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM3_EXTCLK	116	I	External clock	3.3V
TPM3_CH0	133	IO	Channel 0 I/O pin	3.3V
TPM3_CH1	58	IO	Channel 1 I/O pin	3.3V
TPM3_CH2	114	IO	Channel 2 I/O pin	3.3V

Table 55 TPM4 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM4_EXTCLK	120	I	External clock	3.3V
TPM4_CH0	132	IO	Channel 0 I/O pin	3.3V
TPM4_CH1	57	IO	Channel 1 I/O pin	3.3V
TPM4_CH2	117	IO	Channel 2 I/O pin	3.3V
TPM4_CH3	105	IO	Channel 3 I/O pin	3.3V

Table 56 TPM5 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM5_EXTCLK	111	I	External clock	3.3V
TPM5_CH0	122	IO	Channel 0 I/O pin	3.3V
TPM5_CH1	112	IO	Channel 1 I/O pin	3.3V
TPM5_CH2	60	IO	Channel 2 I/O pin	3.3V
TPM5_CH3	108	IO	Channel 3 I/O pin	3.3V

Table 57 TPM6 Signals

Signal Name	Pin #	Type	Description	Voltage Domain
TPM6_EXTCLK	112	I	External clock	3.3V
TPM6_CH0	118	IO	Channel 0 I/O pin	3.3V
TPM6_CH1	109	IO	Channel 1 I/O pin	3.3V
TPM6_CH2	59	IO	Channel 2 I/O pin	3.3V
TPM6_CH3	102	IO	Channel 3 I/O pin	3.3V

NOTE: TPM signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.14 ADC

MCM-iMX95 features a 4-channel 12-bit ADC implemented in the i.MX95 SoC.

Please refer to the i.MX95 Reference manual for additional details.

The following table summarizes ADC signals.

Table 58 ADC Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ADC_IN0	143	AI	ADC input channel 0	1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
ADC_IN1	142	AI	ADC input channel 1	1.8V
ADC_IN2	141	AI	ADC input channel 2	1.8V
ADC_IN3	139	AI	ADC input channel 3	1.8V

4.15 JTAG

MCM-iMX95 enables access to the i.MX95 JTAG port through the carrier board interface.

Please refer to the i.MX95 Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 59 JTAG Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
JTAG_TCK	41	I	Test clock	1.8V
JTAG_TDI	44	I	Test data in	1.8V
JTAG_TDO	43	O	Test data out	1.8V
JTAG_TMS	42	I	Test mode select	1.8V

NOTE: JTAG signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

4.16 GPIO

Up-to 88 of the i.MX95 general purpose input/output (GPIO) signals are available through the MCM-iMX95 carrier board interface. In addition, GPIO signals can produce interrupts.

Please refer to the i.MX95 Reference manual for additional details.

The following table summarizes the GPIO interface signals.

Table 60 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO2_IO[0]	129	IO	General-purpose input/output	3.3V
GPIO2_IO[1]	128	IO	General-purpose input/output	3.3V
GPIO2_IO[2]	127	IO	General-purpose input/output	3.3V
GPIO2_IO[3]	126	IO	General-purpose input/output	3.3V
GPIO2_IO[4]	133	IO	General-purpose input/output	3.3V
GPIO2_IO[5]	132	IO	General-purpose input/output	3.3V
GPIO2_IO[6]	122	IO	General-purpose input/output	3.3V
GPIO2_IO[7]	121	IO	General-purpose input/output	3.3V
GPIO2_IO[8]	118	IO	General-purpose input/output	3.3V
GPIO2_IO[9]	116	IO	General-purpose input/output	3.3V
GPIO2_IO[10]	120	IO	General-purpose input/output	3.3V
GPIO2_IO[11]	111	IO	General-purpose input/output	3.3V
GPIO2_IO[12]	114	IO	General-purpose input/output	3.3V
GPIO2_IO[13]	117	IO	General-purpose input/output	3.3V

GPIO2_IO[14]	110	IO	General-purpose input/output	3.3V
GPIO2_IO[15]	113	IO	General-purpose input/output	3.3V
GPIO2_IO[16]	119	IO	General-purpose input/output	3.3V
GPIO2_IO[17]	115	IO	General-purpose input/output	3.3V
GPIO2_IO[18]	60	IO	General-purpose input/output	3.3V
GPIO2_IO[19]	59	IO	General-purpose input/output	3.3V
GPIO2_IO[20]	58	IO	General-purpose input/output	3.3V
GPIO2_IO[21]	57	IO	General-purpose input/output	3.3V
GPIO2_IO[22]	112	IO	General-purpose input/output	3.3V
GPIO2_IO[23]	109	IO	General-purpose input/output	3.3V
GPIO2_IO[25]	105	IO	General-purpose input/output	3.3V
GPIO2_IO[26]	108	IO	General-purpose input/output	3.3V
GPIO2_IO[27]	102	IO	General-purpose input/output	3.3V
GPIO2_IO[28]	103	IO	General-purpose input/output	3.3V
GPIO2_IO[29]	107	IO	General-purpose input/output	3.3V
GPIO2_IO[30]	104	IO	General-purpose input/output	3.3V
GPIO2_IO[31]	101	IO	General-purpose input/output	3.3V
GPIO5_IO[12]	106	IO	General-purpose input/output	3.3V
GPIO5_IO[13]	99	IO	General-purpose input/output	3.3V
GPIO5_IO[15]	100	IO	General-purpose input/output	3.3V
GPIO3_IO[28]	44	IO	General-purpose input/output	1.8V
GPIO3_IO[29]	42	IO	General-purpose input/output	1.8V
GPIO3_IO[30]	41	IO	General-purpose input/output	1.8V
GPIO3_IO[31]	43	IO	General-purpose input/output	1.8V
GPIO4_IO[0]	82	IO	General-purpose input/output	ENET
GPIO4_IO[1]	81	IO	General-purpose input/output	ENET
GPIO4_IO[2]	73	IO	General-purpose input/output	ENET
GPIO4_IO[3]	72	IO	General-purpose input/output	ENET
GPIO4_IO[4]	71	IO	General-purpose input/output	ENET
GPIO4_IO[5]	69	IO	General-purpose input/output	ENET
GPIO4_IO[6]	68	IO	General-purpose input/output	ENET
GPIO4_IO[7]	67	IO	General-purpose input/output	ENET
GPIO4_IO[8]	75	IO	General-purpose input/output	ENET
GPIO4_IO[9]	74	IO	General-purpose input/output	ENET
GPIO4_IO[10]	76	IO	General-purpose input/output	ENET
GPIO4_IO[11]	77	IO	General-purpose input/output	ENET
GPIO4_IO[12]	79	IO	General-purpose input/output	ENET
GPIO4_IO[13]	80	IO	General-purpose input/output	ENET
GPIO4_IO[16]	50	IO	General-purpose input/output	ENET
GPIO4_IO[17]	49	IO	General-purpose input/output	ENET
GPIO4_IO[18]	48	IO	General-purpose input/output	ENET
GPIO4_IO[19]	47	IO	General-purpose input/output	ENET
GPIO4_IO[20]	46	IO	General-purpose input/output	ENET
GPIO4_IO[21]	45	IO	General-purpose input/output	ENET
GPIO4_IO[22]	52	IO	General-purpose input/output	ENET
GPIO4_IO[23]	51	IO	General-purpose input/output	ENET
GPIO4_IO[24]	53	IO	General-purpose input/output	ENET

GPIO4_IO[25]	54	IO	General-purpose input/output	ENET
GPIO4_IO[26]	55	IO	General-purpose input/output	ENET
GPIO4_IO[27]	56	IO	General-purpose input/output	ENET
GPIO3_IO[19]	91	IO	General-purpose input/output	1.8V
GPIO3_IO[20]	85	IO	General-purpose input/output	1.8V
GPIO3_IO[21]	88	IO	General-purpose input/output	1.8V
GPIO3_IO[22]	87	IO	General-purpose input/output	1.8V
GPIO3_IO[23]	86	IO	General-purpose input/output	1.8V
GPIO3_IO[24]	90	IO	General-purpose input/output	1.8V
GPIO3_IO[25]	89	IO	General-purpose input/output	1.8V
GPIO3_IO[0]	92	IO	General-purpose input/output	SD
GPIO3_IO[1]	96	IO	General-purpose input/output	SD
GPIO3_IO[2]	95	IO	General-purpose input/output	SD
GPIO3_IO[3]	94	IO	General-purpose input/output	SD
GPIO3_IO[4]	93	IO	General-purpose input/output	SD
GPIO3_IO[5]	97	IO	General-purpose input/output	SD
GPIO3_IO[6]	98	IO	General-purpose input/output	SD
GPIO3_IO[7]	78	IO	General-purpose input/output	SD
GPIO1_IO[4]	135	IO	General-purpose input/output	1.8V
GPIO1_IO[5]	148	IO	General-purpose input/output	1.8V
GPIO1_IO[6]	134	IO	General-purpose input/output	1.8V
GPIO1_IO[7]	137	IO	General-purpose input/output	1.8V
GPIO1_IO[9]	138	IO	General-purpose input/output	1.8V
GPIO1_IO[11]	84	IO	General-purpose input/output	1.8V
GPIO1_IO[12]	131	IO	General-purpose input/output	1.8V
GPIO1_IO[13]	83	IO	General-purpose input/output	1.8V
GPIO1_IO[14]	130	IO	General-purpose input/output	1.8V

NOTE: GPIO signals are multiplexed with other functions. For additional details please refer to chapter 5.6 of this document.

NOTE: Pins denoted “SD2” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

NOTE: Pins denoted “ENET can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

5 SYSTEM LOGIC

5.1 Power Supply

Table 61 Power signals

Signal Name	Pin#	Type	Description
V_SOM	123,124,125	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery
VCC_RTC	136	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery via a Schottky diode. If RTC back-up is not required, connect this pin to GND.
EXT_ENET	70	P	ENET domain power supply input. External power MUST be supplied from the carrier-board via EXT_ENET pin.
GND	G1-G70	P	Common ground

5.2 I/O Voltage Domains

MCM-iMX95 utilizes four separate I/O voltage domains that are used to power different I/O modules of the i.MX95 SoC. Some pins operate at 3.3V, some at 1.8V. Voltage domain of each signal is specified in the peripheral interface signals tables.

NOTE: Carrier-board designer must ensure that voltage level of the I/O pins matches the I/O voltage of the peripheral ICs on the carrier-board.

5.3 System and Miscellaneous Signals

5.3.1 Power management

MCM-iMX95 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX95 SoC. The logic that controls both signals is supplied by the i.MX95 SoC BBSM power rail.

The PMIC_STBY output can be used to signal the carrier board power supply that MCM-iMX95 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX95 Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 62 External regulator control signals

Signal Name	Pin #	Type	Description
PMIC_STBY	170	O	When the processor enters SUSPEND mode, it will assert this signal.
PMIC_ON_REQ	169	O	Active high power-up request output from i.MX95 SoC.
ONOFF	140	I	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch).

5.3.2 SD2 control

SD2_VSEL signal controls the voltage of the SD2 interface. By default there is an internal 1-4M ohm pull down resistor, and the voltage level is 3.3V. Changing the voltage level to 1.8V can be done by pulling SD2_VSEL up using a 10-100K ohm pull up resistor to 1.8/3.3V. Please refer to the i.MX95 Reference manual for additional details.

Table 63 SD2 control

Signal Name	Pin #	Type	Description
SD2_VSEL	91	I	SD2 voltage control

5.4 Reset

COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on MCM-iMX95. Please refer to the i.MX95 Reference manual for additional details.

Table 64 Reset signals

Signal Name	Pin #	Type	Description
COLD_RESET_IN	168	I	Active Low cold reset input signal. Should be used as main system reset
POR_B_3V3	167	I	CPU power on reset input pin, active low

5.5 Boot Sequence

MCM-iMX95 boot sequence defines which interface/media is used by MCM-iMX95 to load and execute the initial software (such as SPL or/and U-boot). MCM-iMX95 can load initial software from the following interfaces/media:

- On-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD2 interface
- Serial Download boot using USB1 interface

MCM-iMX95 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of three different boot sequences are supported by MCM-iMX95:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternative sequence: designed to allow recovery from an external bootable SD card in case of data corruption of the on-board primary boot device. Using the alternate sequence allows MCM-iMX95 to boot bypassing the onboard eMMC.
- Serial download mode: provides a means to download a program image to the i.MX95 system-on-chip over USB serial connection

Logic values of boot selections signals define which of the supported boot sequences is used by the system.

Table 65 Boot selection signals

Signal Name	Pin #	Type	Description
ALT_BOOT#	166	I	Active low alternate boot sequence select input. Leave floating or tie high for standard boot sequence
SDP_BOOT#	165	I	Active low alternate boot sequence select input. Leave floating or tie high for standard boot sequence

Table 66 MCM-iMX95 boot sequences

Mode	ALT_BOOT#	SDP_BOOT#	Booting sequence
Standard	High or floating	High or floating	Onboard eMMC (primary boot storage)
Alternative	Low	Low, high or floating	SD card on SD2 interface
SDP mode	High or floating	Low	Serial Downloader

5.6 Signal Multiplexing Characteristics

Up to 88 of the MCM-iMX95 carrier board interface pads are multifunctional. Multifunctional pins enable extensive functional flexibility of the MCM-iMX95 CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 8 functions (MUX modes) are accessible through each multifunctional carrier board interface pad. The multifunctional capabilities of MCM-iMX95 pads are derived from the i.MX95 SoC control module.

NOTE: Pad function selection is controlled by software.

NOTE: Each pad can be used for a single function at a time.

NOTE: Only one pad can be used for each function (in case a function is available on more than one carrier board interface pad).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 67 Multifunctional Signals

Pad #	SoC Pin Name	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7	Voltage Domain	Availability
41	JTAG_TCK	JTAG_TCK		CAN4_RX			GPIO3_IO[30]	UART5_CTS_B		1.8V	Always
42	JTAG_TMS	JTAG_TMS		CAN4_TX			GPIO3_IO[29]	UART5_RTS_B		1.8V	Always
43	JTAG_TDO	JTAG_TDO	MQS2_RIGHT		CAN2_RX		GPIO3_IO[31]	UART5_TX		1.8V	Always
44	JTAG_TDI	JTAG_TDI	MQS2_LEFT		CAN2_TX		GPIO3_IO[28]	UART5_RX		1.8V	Always
45	ENET2_TXC	ETH1_RGMII_TX_CLK		SAI2_TX_BCLK			GPIO4_IO[21]			ENET	Always
46	ENET2_TX_CTL	ETH1_RGMII_TX_CTL	UART4_DTR_B	SAI2_TXFS			GPIO4_IO[20]			ENET	Always
47	ENET2_TD0	ETH1_RGMII_TXD[0]	UART4_TX	SAI2_RX_DATA[3]	SAI4_TX_DATA[0]		GPIO4_IO[19]			ENET	Always
48	ENET2_TD1	ETH1_RGMII_TXD[1]	UART4_RTS_B	SAI2_RX_DATA[2]	SAI4_TX_BCLK		GPIO4_IO[18]			ENET	Always
49	ENET2_TD2	ETH1_RGMII_TXD[2]		SAI2_RX_DATA[1]	SAI4_TXFS		GPIO4_IO[17]			ENET	Always
50	ENET2_TD3	ETH1_RGMII_TXD[3]		SAI2_RX_DATA[0]			GPIO4_IO[16]			ENET	Always
51	ENET2_RXC	ETH1_RGMII_RX_CLK		SAI2_TX_DATA[1]	SAI4_RXFS		GPIO4_IO[23]			ENET	Always
52	ENET2_RX_CTL	ETH1_RGMII_RX_CTL	UART4_DSR_B	SAI2_TX_DATA[0]			GPIO4_IO[22]			ENET	Always
53	ENET2_RD0	ETH1_RGMII_RXD[0]	UART4_RX	SAI2_TX_DATA[2]	SAI4_RX_BCLK		GPIO4_IO[24]			ENET	Always

54	ENET2_RD1	ETH1_RGMII_RXD[1]	SPDIF_IN	SAI2_TX_DATA[3]	SAI4_RX_DATA[0]		GPIO4_IO[25]			ENET	Always
55	ENET2_RD2	ETH1_RGMII_RXD[2]	UART4_CTS_B	SAI2_MCLK	MQS2_RIGHT		GPIO4_IO[26]			ENET	Always
56	ENET2_RD3	ETH1_RGMII_RXD[3]	SPDIF_OUT	SPDIF_IN	MQS2_LEFT		GPIO4_IO[27]			ENET	Always
57	GPIO_IO21	GPIO2_IO[21]	SAI3_TX_DATA[0]	PDM_CLK		SPI5_SCK	SPI4_SCK	TPM4_CH1	SAI3_RX_BCLK	3.3V	Always
58	GPIO_IO20	GPIO2_IO[20]	SAI3_RX_DATA[0]	PDM_BIT_STREAM[0]		SPI5_SOUT	SPI4_SOUT	TPM3_CH1		3.3V	Always
59	GPIO_IO19	GPIO2_IO[19]	SAI3_RXFS	PDM_BIT_STREAM[3]		SPI5_SIN	SPI4_SIN	TPM6_CH2	SAI3_TX_DATA[0]	3.3V	Always
60	GPIO_IO18	GPIO2_IO[18]	SAI3_RX_BCLK			SPI5_PCS0	SPI4_PCS0	TPM5_CH2		3.3V	Always
67	ENET1_TXC	ETH0_RGMII_TX_CLK					GPIO4_IO[7]			ENET	Always
68	ENET1_TX_CTL	ETH0_RGMII_TX_CTL	UART3_DTR_B				GPIO4_IO[6]			ENET	Always
69	ENET1_TD0	ETH0_RGMII_TXD[0]	UART 3_TX				GPIO4_IO[5]			ENET	Always
71	ENET1_TD1	ETH0_RGMII_TXD[1]	UART 3_RTS_B	I3C2_PUR	USB1_OTG_OC		GPIO4_IO[4]	I3C2_PUR_B		ENET	Always
72	ENET1_TD2	ETH0_RGMII_TXD[2]		CAN2_RX	USB 2_OTG_OC		GPIO4_IO[3]			ENET	Always
73	ENET1_TD3	ETH0_RGMII_TXD[3]		CAN2_TX	USB 2_OTG_ID		GPIO4_IO[2]			ENET	Always
74	ENET1_RXC	ETH0_RGMII_RX_CLK					GPIO4_IO[9]			ENET	Always
75	ENET1_RX_CTL	ETH0_RGMII_RX_CTL	UART 3_DSR_B		USB 2_OTG_PWR		GPIO4_IO[8]			ENET	Always
76	ENET1_RD0	ETH0_RGMII_RXD[0]	UART 3_RX				GPIO4_IO[10]			ENET	Always
77	ENET1_RD1	ETH0_RGMII_RXD[1]	UART 3_CTS_B				GPIO4_IO[11]			ENET	Always
78	SD2_RESET#	SD2_RESET#					GPIO3_IO[7]			SD2	Always
79	ENET1_RD2	ETH0_RGMII_RXD[2]					GPIO4_IO[12]			ENET	Always
80	ENET1_RD3	ETH0_RGMII_RXD[3]					GPIO4_IO[13]			ENET	Always
81	ENET1_MDIO	ETH0_MDIO	UART3_RIN_B	I3C2_SDA	USB1_OTG_PWR		GPIO4_IO[1]			ENET	Always
82	ENET1_MDC	ETH0_MDC	UART 3_DCB_B	I3C2_SCL	USB1_OTG_ID		GPIO4_IO[0]			ENET	Always
83	SAI1_TXD/BT_MODE3	SAI1_TX_DATA[0]	UART2_RTS_B	SPI1_SCK	UART1_DTR_B	CAN1_TX	GPIO1_IO[13]			3.3V	Output only
84	SAI1_TXFS/BT_MODE2	SAI1_TXFS	SAI1_TX_DATA[1]	SPI1_PCS0	UART2_DTR_B	MQS1_LEFT	GPIO1_IO[11]			3.3V	Output only
85	SD3_CLK	SD3_CLK		SAI5_TX_DATA[1]	SAI5_RX_DATA[0]		GPIO3_IO[20]			1.8V	Always
86	SD3_DATA1	SD3_DATA1		SAI5_RX_DATA[1]	SAI5_TX_DATA[0]		GPIO3_IO[23]			1.8V	Always
87	SD3_DATA0	SD3_DATA0		SAI5_TX_DATA[3]	SAI5_RX_BCLK		GPIO3_IO[22]			1.8V	Always
88	SD3_CMD	SD3_CMD		SAI5_TX_DATA[2]	SAI5_RXFS		GPIO3_IO[21]			1.8V	Always

89	SD3_DATA3	SD3_DATA3		SAI5_RX_DATA[3]	SAI5_TX_BCLK		GPIO3_IO[25]			1.8V	Always
90	SD3_DATA2	SD3_DATA2		SAI5_RX_DATA[2]	SAI5_TXFS		GPIO3_IO[24]			1.8V	Always
91	SD2_VSEL	USDHC2_VSELECT					GPIO3_IO[19]			1.8V	Always
92	SD2_CD#	USDHC2_CD_B		I3C2_SCL			GPIO3_IO[0]			SD2	Always
93	SD2_DATA1	USDHC2_DATA1		CAN2_RX			GPIO3_IO[4]			SD2	Always
94	SD2_DATA0	USDHC2_DATA0		CAN2_TX			GPIO3_IO[3]			SD2	Always
95	SD2_CMD	USDHC2_CMD		I3C2_PUR			GPIO3_IO[2]			SD2	Always
96	SD2_CLK	USDHC2_CLK		I3C2_SDA			GPIO3_IO[1]			SD2	Always
97	SD2_DATA2	USDHC2_DATA2		MQS2_RIGHT			GPIO3_IO[5]			SD2	Always
98	SD2_DATA3	USDHC2_DATA3		MQS2_LEFT			GPIO3_IO[6]			SD2	Always
99	GPIO_IO33	GPIO5_IO[13]		UART6_RX		SPI4_PCS1				3.3V	Always
100	PCIE2_CLK_REQ	GPIO5_IO[15]	PCIE2_CLKREQ_B	UART6_RTS_B		SPI4_SIN				3.3V	Always
101	GPIO_IO31	GPIO2_IO[31]	I2C4_SCL	CAN5_RX						3.3V	Always
102	GPIO_IO27	GPIO2_IO[27]	SD3_DATA3	CAN2_RX		TPM6_CH3		SPI5_PCS1		3.3V	Always
103	GPIO_IO28	GPIO2_IO[28]	I2C3_SDA	CAN3_TX						3.3V	Always
104	GPIO_IO30	GPIO2_IO[30]	I2C4_SDA	CAN5_TX						3.3V	Always
105	GPIO_IO25	GPIO2_IO[25]	SD3_DATA1	CAN2_TX		TPM4_CH3		SPI7_PCS1		3.3V	Always
106	PCIE1_CLK_REQ	GPIO5_IO[12]	PCIE1_CLKREQ	UART6_TXD		SPI4_PCS2				3.3V	Always
107	GPIO_IO29	GPIO2_IO[29]	I2C3_SCL	CAN3_RX						3.3V	Always
108	GPIO_IO26	GPIO2_IO[26]	SD3_DATA2	PDM_BIT_STREAM[1]		TPM5_CH3		SPI8_PCS1	SAI3_TXFS	3.3V	Always
109	GPIO_IO23	GPIO2_IO[23]	SD3_CMD	SPDIF_OUT	CAN5_RX	TPM6_CH1		I2C5_SCL		3.3V	Always
110	UART3_TX	GPIO2_IO[14]	UART3_TX			SPI8_SOUT	UART8_CTS_B	UART4_TX		3.3V	Always
111	GPIO_IO11	GPIO2_IO[11]	SPI3_SCLK			TPM5_EXTCLK	UART7_RTS_B	I2C8_SCL		3.3V	Always
112	GPIO_IO22	GPIO2_IO[22]	SD3_CLK	SPDIF_IN	CAN5_TX	TPM5_CH1	TPM6_EXTCLK	I2C5_SDA		3.3V	Always
113	UART3_RX	GPIO2_IO[15]	UART3_RX			SPI8_SCK	UART8_RTS_B	UART4_RX		3.3V	Always
114	GPIO_IO12	GPIO2_IO[12]	TPM3_CH2	PDM_BIT_STREAM[2]		SPI8_PCS0	UART8_TX	I2C8_SDA	SAI3_RXFS	3.3V	Always
115	GPIO_IO17	GPIO2_IO[17]	SAI3_MCLK			UART3_RTS_B	SPI4_PCS1	UART4_RTS_B		3.3V	Always

116	GPIO_IO09	GPIO2_IO[9]	SPI3_SIN			TPM3_EXTCLK	UART7_RX	I2C7_SCL		3.3V	Always
117	GPIO_IO13	GPIO2_IO[13]	TPM4_CH2	PDM_BIT_STREAM[3]		SPI8_SIN	UART8_RX	I2C8_SCL		3.3V	Always
118	GPIO_IO08	GPIO2_IO[8]	SPI3_PCS0			TPM6_CH0	UART7_TX	I2C7_SDA		3.3V	Always
119	GPIO_IO16	GPIO2_IO[16]	SAI3_TX_BCLK	PDM_BIT_STREAM[2]		UART3_CTS_B	SPI4_PCS2	UART 4_CTS_B		3.3V	Always
120	GPIO_IO10	GPIO2_IO[10]	SPI3_SOUT			TPM4_EXTCLK	UART7_CTS_B	I2C8_SDA		3.3V	Always
121	GPIO_IO07	GPIO2_IO[7]	SPI3_PCS1			SPI7_SCLK	UART6_RTS_B	I2C7_SCL		3.3V	Always
122	GPIO_IO06	GPIO2_IO[6]	TPM5_CH0	PDM_BIT_STREAM[1]		SPI7_SOUT	UART6_CTS_B	I2C7_SDA		3.3V	Always
126	UART5_RTS_B	GPIO2_IO[3]	I2C4_SCL			SPI6_SCK	UART5_RTS_B	I2C6_SCL		3.3V	Always
127	UART5_CTS_B	GPIO2_IO[2]	I2C4_SDA			SPI6_SOUT	UART5_CTS_B	I2C6_SDA		3.3V	Always
128	UART5_RX	GPIO2_IO[1]	I2C3_SCL			SPI6_SIN	UART5_RX	I2C5_SCL		3.3V	Always
129	UART5_TX	GPIO2_IO[0]	I2C3_SDA			SPI6_PCS0	UART5_TX	I2C5_SDA		3.3V	Always
130	SAI1_RXD	SAI1_RX_DATA[0]	SAI1_MCLK	SPI1_SOUT	UART2_DSR_B	MQS1_RIGHT	GPIO1_IO[14]			3.3V	Always
131	SAI1_TXC	SAI1_TXC	UART2_CTS_B	SPI1_SIN	UART1_DSR_B	CAN1_RX	GPIO1_IO[12]			3.3V	Always
132	GPIO_IO05	GPIO2_IO[5]	TPM4_CH0	PDM_BIT_STREAM[0]	CAN4_RX	SPI7_SIN	UART6_RX	I2C6_SCL		3.3V	Always
133	GPIO_IO04	GPIO2_IO[4]	TPM3_CH0	PDM_CLK	CAN4_TX	SPI7_PCS0	UART6_TXD	I2C6_SDA		3.3V	Always
134	UART2_RXD	UART2_RXD	UART1_CTS_B	SPI2_SOUT	TPM1_CH2	SAI1_MCLK	GPIO1_IO[6]			3.3V	Always
135	UART1_RXD	UART1_RXD		SPI2_SIN	TPM1_CH0		GPIO1_IO[4]			3.3V	Always
137	UART2_TXD/BT_MODE1	UART2_TXD/BT_MODE1	UART1_RTS	SPI2_SCK	TPM1_CH3		GPIO1_IO[7]			3.3V	Output only
138	PDM_BIT_STREAM0	PDM_BIT_STREAM[0]	MQS1_RIGHT	SPI1_PCS1	TPM1_EXTCLK		GPIO1_IO[9]	CAN1_RX		3.3V	Always
148	UART1_TXD/BT_MODE0	UART1_TX		SPI2_PCS0	TPM1_CH1		GPIO1_IO[5]			3.3V	Output only

NOTE: Pins denoted “SD2” can be configured to operate at 3.3V or 1.8V voltage levels. Voltage level is controlled by SoC pin SD2_VSEL.

NOTE: Pins denoted “ENET can be configured to operate at 3.3V or 1.8V voltage levels. The voltage level is controlled by carrier board +EXT_ENET (Pin 70).

5.7 RTC

MCM-iMX95 features an on-board ultra-low-power RX8900CE real time clock (RTC). The RTC is connected to the i.MX95 SoC using I2C2 interface at address 0x32.

Back-up power supply is required in order to keep the RTC running and maintain clock and time information when main supply is not present.

For more information about MCM-iMX95 RTC please refer to the RX8900CE datasheet.

5.8 LED

MCM-iMX95 features a single general purpose green LED controlled by PWR_LED (GPIO2_IO[24]) signal of the i.MX95. The LED is ON when PWR_LED is logic LOW.

6 CARRIER BOARD INTERFACE

MCM-iMX95 carrier board interface uses 180-pin QFN package. SoM pinout is detailed in the table below.

6.1 Package Pinout

Table 68 Package Pinout

Pad #	Pad Functions	Ref.		Pad #	Pad Functions	Ref.
1	MIPI_CSI_D0_N	4.2		91	SD2_VSEL GPIO3_IO[19]	5.3.2 4.16
2	MIPI_CSI_D0_P	4.2		92	SD2_CD# I3C2_SCL GPIO3_IO[0]	4.7 4.12 4.16
3	MIPI_CSI_D1_N	4.2		93	SD2_DATA1 CAN2_RX GPIO3_IO[4]	4.7 4.9 4.16
4	MIPI_CSI_D1_P	4.2		94	SD2_DATA0 CAN2_TX GPIO3_IO[3]	4.7 4.9 4.16
5	MIPI_CSI_CLK_N	4.2		95	SD2_CMD I3C2_PUR GPIO3_IO[2]	4.7 4.12 4.16
6	MIPI_CSI_CLK_P	4.2		96	SD2_CLK I3C2_SDA GPIO3_IO[1]	4.7 4.12 4.16
7	MIPI_CSI_D2_N	4.2		97	MQS2_RIGHT SD2_DATA2 GPIO3_IO[5]	4.3.3 4.7 4.16
8	MIPI_CSI_D2_P	4.2		98	MQS2_LEFT SD2_DATA3 GPIO3_IO[6]	4.3.3 4.7 4.16
9	MIPI_CSI_D3_N	4.2		99	UART6_RX SPI4_PCS1 GPIO5_IO[13]	4.8 4.10 4.16
10	MIPI_CSI_D3_P	4.2		100	PCIE2_CLK_REQ UART6_RTS SPI4_SIN GPIO5_IO[15]	4.5 4.8 4.10 4.16
11	MIPI_DSICSI_D0_N	4.2		101	CAN5_RX I2C4_SCL GPIO2_IO[31]	4.9 4.13 4.16
12	MIPI_DSICSI_D0_P	4.2		102	SD3_DATA3 CAN2_RX SPI5_PCS1 TPM6_CH3 GPIO2_IO[27]	4.7 4.9 4.10 4.13 4.16
13	MIPI_DSICSI_D1_N	4.2		103	CAN3_TX I2C3_SDA GPIO2_IO[28]	4.9 4.13 4.16
14	MIPI_DSICSI_D1_P	4.2		104	CAN5_TX I2C4_SDA GPIO2_IO[30]	4.9 4.13 4.16
15	MIPI_DSICSI_CLK_N	4.2		105	CAN2_TX SPI7_PCS1 TPM4_CH3 SD3_DATA1 GPIO2_IO[25]	4.9 4.10 4.13 4.7 4.16
16	MIPI_DSICSI_CLK_P	4.2		106	PCIE1_CLK_REQ UART6_TXD SPI4_PCS2 GPIO5_IO[12]	4.5 4.8 4.10 4.16
17	MIPI_DSICSI_D2_N	4.2		107	CAN3_RX I2C3_SCL GPIO2_IO[29]	4.9 4.13 4.16

18	MIPI_DSICSI_D2_P	4.2		108	SAI3_TXFS PDM_BIT_STREAM1 SD3_DATA2 SPI8_PCS1 TPM5_CH3 GPIO2_IO[26]	4.3.2 4.3.4 4.7 4.10 4.13 4.16
19	MIPI_DSICSI_D3_N	4.2		109	SPDIF_OUT SD3_CMD CAN5_RX I2C5_SCL TPM6_CH1 GPIO2_IO[23]	4.3.1 4.7 4.9 4.13 4.13 4.16
20	MIPI_DSICSI_D3_P	4.2		110	UART3_TX UART4_TXD UART8_CTS SPI8_SOUT GPIO2_IO[14]	4.8 4.8 4.8 4.10 4.16
21	LVDS0_D3_N	4.1.2		111	UART7_RTS SPI3_SCLK I2C8_SCL TPM5_EXTCLK GPIO2_IO[11]	4.8 4.10 4.13 4.13 4.16
22	LVDS0_D3_P	4.1.2		112	SPDIF_IN SD3_CLK CAN5_TX I2C5_SDA TPM5_CH1 TPM6_EXTCLK GPIO2_IO[22]	4.3.1 4.7 4.9 4.13 4.13 4.13 4.16
23	LVDS0_D2_N	4.1.2		113	UART3_RX UART4_RXD UART8_RTS SPI8_SCLK GPIO2_IO[15]	4.8 4.8 4.8 4.10 4.16
24	LVDS0_D2_P	4.1.2		114	SAI3_RXFS PDM_BIT_STREAM2 UART8_TXD SPI8_PCS0 I2C8_SDA TPM3_CH2 GPIO2_IO[12]	4.3.2 4.3.4 4.8 4.10 4.13 4.13 4.16
25	LVDS0_D0_N	4.1.2		115	SAI3_MCLK UART3_RTS UART4_RTS SPI4_PCS1 GPIO2_IO[17]	4.3.2 4.8 4.8 4.10 4.16
26	LVDS0_D0_P	4.1.2		116	UART7_RXD SPI3_SIN I2C7_SCL TPM3_EXTCLK GPIO2_IO[9]	4.8 4.10 4.13 4.13 4.16
27	LVDS0_D1_N	4.1.2		117	PDM_ BIT_STREAM3 UART8_RXD SPI8_SIN I2C8_SCL TPM4_CH2 GPIO2_IO[13]	4.3.4 4.8 4.10 4.13 4.13 4.19
28	LVDS0_D1_P	4.1.2		118	UART7_TXD SPI3_PCS0 I2C7_SDA TPM6_CH0 GPIO2_IO[8]	4.8 4.10 4.13 4.13 4.16
29	LVDS0_CLK_N	4.1.2		119	SAI3_TX_BCLK PDM_BIT_STREAM2 UART3_CTS UART4_CTS SPI4_PCS2 GPIO2_IO[16]	4.3.2 4.3.4 4.8 4.8 4.10 4.16
30	LVDS0_CLK_P	4.1.2		120	UART7_CTS SPI3_SOUT	4.8 4.10

					I2C8_SDA TPM4_EXTCLK GPIO2_IO[10]	4.13 4.13 4.16
31	LVDS1_D0_N	4.1.2		121	UART6_RTS SPI3_PCS1 SPI7_SCLK I2C7_SCL GPIO2_IO[7]	4.8 4.10 4.10 4.13 4.16
32	LVDS1_D0_P	4.1.2		122	PDM_BIT_STREAM1 UART6_CTS SPI7_SOUT I2C7_SDA TPM5_CH0 GPIO2_IO[6]	4.3.4 4.8 4.10 4.13 4.13 4.16
33	LVDS1_D1_N	4.1.2		123	+V_SOM	5.1
34	LVDS1_D1_P	4.1.2		124	+V_SOM	5.1
35	LVDS1_CLK_N	4.1.2		125	+V_SOM	5.1
36	LVDS1_CLK_P	4.1.2		126	UART5_RTS_B SPI6_SCLK I2C4_SCL I2C6_SCL GPIO2_IO[3]	4.8 4.10 4.13 4.13 4.16
37	LVDS1_D2_N	4.1.2		127	UART5_CTS_B SPI6_SOUT I2C4_SDA I2C6_SDA GPIO2_IO[2]	4.8 4.10 4.13 4.13 4.16
38	LVDS1_D2_P	4.1.2		128	UART5_RX SPI6_SIN I2C3_SCL I2C5_SCL GPIO2_IO[1]	4.8 4.10 4.13 4.13 4.16
39	LVDS1_D3_N	4.1.2		129	UART5_TX SPI6_PCS0 I2C3_SDA I2C5_SDA GPIO2_IO[0]	4.8 4.10 4.13 4.13 4.16
40	LVDS1_D3_P	4.1.2		130	SAI1_MCLK SAI1_RX_DATA[0] MQS1_RIGHT UART2_DSR SPI1_SOUT GPIO1_IO[14]	4.3.2 4.3.2 4.3.3 4.8 4.10 4.16
41	UART5_CTS_B CAN4_RX JTAG_TCK GPIO3_IO[30]	4.8 4.9 4.15 4.16		131	SAI1_TXC UART1_DSR UART2_CTS CAN1_RX SPI1_SIN GPIO1_IO[12]	4.3.2 4.8 4.8 4.9 4.10 4.16
42	UART5_RTS_B CAN4_TX JTAG_TMS GPIO3_IO[29]	4.8 4.9 4.15 4.16		132	PDM_BIT_STREAM0 UART6_RXD CAN4_RX SPI7_SIN I2C6_SCL TPM4_CH0 GPIO2_IO[5]	4.3.4 4.8 4.9 4.10 4.13 4.13 4.16
43	MQS2_RIGHT UART5_TX CAN2_RX JTAG_TDO GPIO3_IO[31]	4.3.3 4.8 4.9 4.15 4.16		133	PDM_CLK UART6_TXD CAN4_TX SPI7_PCS0 I2C6_SDA TPM3_CH0 GPIO2_IO[4]	4.3.4 4.8 4.9 4.10 4.13 4.13 4.16
44	MQS2_LEFT UART5_RX CAN2_TX JTAG_TDI GPIO3_IO[28]	4.3.3 4.8 4.9 4.15 4.16		134	SAI1_MCLK UART1_CTS UART2_RXD SPI2_SOUT TPM1_CH2 GPIO1_IO[6]	4.3.2 4.8 4.8 4.10 4.13 4.16

45	SAI2_TX_BCLK ENET2_TXC GPIO4_IO[21]	4.3.2 4.4.2 4.16		135	UART1_RXD SPI2_SIN TPM1_CH0 GPIO1_IO[4]	4.8 4.10 4.13 4.16
46	SAI2_TXFS ENET2_TX_CTL UART4_DTR GPIO4_IO[20]	4.3.2 4.4.2 4.8 4.16		136	+VCC_RTC	5.1
47	SAI2_RX_DATA[3] SAI4_TX_DATA[0] ENET2_TD0 UART4_TXD GPIO4_IO[19]	4.3.2 4.3.2 4.4.2 4.8 4.16		137	UART1_RTS UART2_TXD/BT_MODE1 SPI2_SCLK TPM1_CH3 GPIO1_IO[7]	4.8 4.8 4.10 4.13 4.16
48	SAI2_RX_DATA[2] SAI4_TX_BCLK ENET2_TD1 UART4_RTS GPIO4_IO[18]	4.3.2 4.3.2 4.4.2 4.8 4.16		138	MQS1_RIGHT PDM_BIT_STREAM0 CAN1_RX SPI1_PCS1 TPM1_EXTCLK GPIO1_IO[9]	4.3.3 4.3.4 4.9 4.10 4.13 4.16
49	SAI2_RX_DATA[1] SAI4_TXFS ENET2_TD2 GPIO4_IO[17]	4.3.2 4.3.2 4.4.2 4.16		139	ADC_IN3	4.14_ ADC
50	SAI2_RX_DATA[0] ENET2_TD3 GPIO4_IO[16]	4.3.2 4.4.2 4.16		140	ONOFF	5.3.1
51	SAI2_TX_DATA[1] SAI4_RXFS ENET2_RXC GPIO4_IO[23]	4.3.2 4.3.2 4.4.2 4.16		141	ADC_IN2	4.14
52	SAI2_TX_DATA[0] ENET2_RX_CTL UART4_DSR GPIO4_IO[22]	4.3.2 4.4.2 4.8 4.16		142	ADC_IN1	4.14
53	SAI2_TX_DATA[2] SAI4_RX_BCLK ENET2_RD0 UART4_RXD GPIO4_IO[24]	4.3.2 4.3.2 4.4.2 4.8 4.16		143	ADC_IN0	4.14
54	SPDIF_IN SAI2_TX_DATA[3] SAI4_RX_DATA[0] ENET2_RD1 GPIO4_IO[25]	4.3.1 4.3.2 4.3.2 4.4.2 4.16		144	PCIE2_TX0_N	4.5
55	SAI2_MCLK MQS2_RIGHT ENET2_RD2 UART4_CTS GPIO4_IO[26]	4.3.2 4.3.3 4.4.2 4.8 4.16		145	PCIE2_TX0_P	4.5
56	SPDIF_IN SPDIF_OUT MQS2_LEFT ENET2_RD3 GPIO4_IO[27]	4.3.1 4.3.1 4.3.3 4.4.2 4.16		146	PCIE1_TX0_N	4.5
57	SAI3_RX_BCLK SAI3_TX_DATA[0] PDM_CLK SPI4_SCLK SPI5_SCLK TPM4_CH1 GPIO2_IO[21]	4.3.2 4.3.2 4.3.4 4.10 4.10 4.13 4.16		147	PCIE1_TX0_P	4.5
58	SAI3_RX_DATA[0] PDM_BIT_STREAM0 SPI4_SOUT SPI5_SOUT TPM3_CH1 GPIO2_IO[20]	4.3.2 4.3.4 4.10 4.10 4.13 4.16		148	UART1_TXD/BT_MODE0 SPI2_PCS0 TPM1_CH1 GPIO1_IO[5]	4.8 4.10 4.13 4.16
59	SAI3_RXFS SAI3_TX_DATA[0] PDM_ BIT_STREAM3	4.3.2 4.3.2 4.3.4		149	USB1_TX0_P	4.6

	SPI4_SIN SPI5_SIN TPM6_CH2 GPIO2_IO[19]	4.10 4.10 4.13 4.16				
60	SAI3_RX_BCLK SPI4_PCS0 SPI5_PCS0 TPM5_CH2 GPIO2_IO[18]	4.3.2 4.10 4.10 4.13 4.16		150	USB1_TX0_N	4.6
61	ETH_CLKIN_N	4.4.1		151	USB1_TX1_N	4.6
62	ETH_CLKIN_P	4.4.1		152	USB1_TX1_P	4.6
63	ETH_RX0_N	4.4.1		153	PCIE2_RX0_N	5.8
64	ETH_RX0_P	4.4.1		154	PCIE2_RX0_P	4.5
65	ETH_TX0_N	4.4.1		155	PCIE2_CLKIN_N	4.5
66	ETH_TX0_P	4.4.1		156	PCIE2_CLKIN_P	4.5
67	ENET1_TXC GPIO4_IO[7]	4.4.2 4.16		157	PCIE1_CLKIN_N	4.5
68	ENET1_TX_CTL UART3_DTR_B GPIO4_IO[6]	4.4.2 4.8 4.16		158	PCIE1_CLKIN_P	4.5
69	ENET1_TD0 UART 3_TX GPIO4_IO[5]	4.4.2 4.8 4.16		159	PCIE1_RX0_N	4.5
70	+EXT_ENET	5.1_RGMII1		160	PCIE1_RX0_P	4.2
71	ENET1_TD1 UART 3_RTS_B I3C2_PUR I3C2_PUR_B USB1_OTG_OC GPIO4_IO[4]	4.4.2 4.8 4.12 4.12 4.6 4.16		161	PCIE_CLKOUT_N	4.5
72	ENET1_TD2 CAN2_RX USB 2_OTG_OC GPIO4_IO[3]	4.4.2 4.9 4.6 4.16		162	PCIE_CLKOUT_P	4.5
73	ENET1_TD3 CAN2_TX USB 2_OTG_ID GPIO4_IO[2]	4.4.2 4.9 4.6 4.16		163	USB2_DN	4.6
74	ENET1_RXC GPIO4_IO[9]	4.4.2 4.16		164	USB2_DP	4.6
75	ENET1_RX_CTL UART 3_DSR_B USB 2_OTG_PWR GPIO4_IO[8]	4.4.2 4.8 4.6 4.16		165	SDP_BOOT#	5.5
76	ENET1_RD0 UART 3_RX GPIO4_IO[10]	4.4.2 4.8 4.16		166	ALT_BOOT#	5.5
77	ENET1_RD1 UART 3_CTS_B GPIO4_IO[11]	4.4.2 4.8 4.16		167	POR_B_3V3	5.4
78	SD2_RESET# GPIO3_IO[7]	4.7 4.16		168	COLD_RESET_IN	5.4
79	ENET1_RD2 GPIO4_IO[12]	4.4.2 4.16		169	PMIC_ON_REQ	5.3.1
80	ENET1_RD3 GPIO4_IO[13]	4.4.2 4.16		170	PMIC_STBY	5.3.1
81	ENET1_MDIO UART3_RIN_B I3C2_SDA USB1_OTG_PWR GPIO4_IO[1]	4.4.2 4.8 4.12 4.6 4.16		171	USB1_RX0_P	4.6
82	ENET1_MDC UART 3_DCB_B I3C2_SCL	4.4.2 4.8 4.12		172	USB1_RX0_N	4.6

	USB1_OTG_ID GPIO4_IO[0]	4.6 4.16				
83	SAI1_TXD/BT_MODE3 UART1_DTR UART2_RTS CAN1_TX SPI1_SCLK GPIO1_IO[13]	4.3.2 4.8 4.8 4.9 4.10 4.16		173	USB1_DP	4.6
84	SAI1_TX_DATA[1] SAI1_TXFS/BT_MODE2 MQS1_LEFT UART2_DTR SPI1_PCS0 GPIO1_IO[11]	4.3.2 4.3.2 4.3.3 4.8 4.10 4.16		174	USB1_DN	4.6
85	SAI5_RX_DATA[0] SAI5_TX_DATA[1] SD3_CLK GPIO3_IO[20]	4.3.2 4.3.2 4.7 4.16		175	USB1_RX1_N	4.6
86	SAI5_RX_DATA[1] SAI5_TX_DATA[0] SD3_DATA1 GPIO3_IO[23]	4.3.2 4.3.2 4.7 4.16		176	USB1_RX1_P	4.6
87	SAI5_RX_BCLK SAI5_TX_DATA[3] SD3_DATA0 GPIO3_IO[22]	4.3.2 4.3.2 4.7 4.16		177	USB1_ID	4.6
88	SAI5_RXFS SAI5_TX_DATA[2] SD3_CMD GPIO3_IO[21]	4.3.2 4.3.2 4.7 4.16		178	USB2_ID	4.6
89	SAI5_RX_DATA[3] SAI5_TX_BCLK SD3_DATA3 GPIO3_IO[25]	4.3.2 4.3.2 4.7 4.16		179	USB1_VBUS	4.6
90	SAI5_RX_DATA[2] SAI5_TXFS SD3_DATA2 GPIO3_IO[24]	4.3.2 4.3.2 4.7 4.16		180	USB2_VBUS	4.6

Table 69 Ground Pads

Pad #	Pad Functions	Ref.		Pad #	Pad Functions	Ref.
G1	GND	5.1		G36	GND	5.1
G2				G37		
G3				G38		
G4				G39		
G5				G40		
G6				G41		
G7				G42		
G8				G43		
G9				G44		
G10				G45		
G11				G46		
G12				G47		
G13				G48		
G14				G49		
G15				G50		
G16				G51		
G17				G52		
G18				G53		
G19				G54		

G20				G55		
G21				G56		
G22				G57		
G23				G58		
G24				G59		
G25				G60		
G26				G61		
G27				G62		
G28				G63		
G29				G64		
G30				G65		
G31				G66		
G32				G67		
G33				G68		
G34				G69		
G35				G70		

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 70 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	6.0	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 71 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	5.5	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 ESD Performance

Table 72 ESD Performance

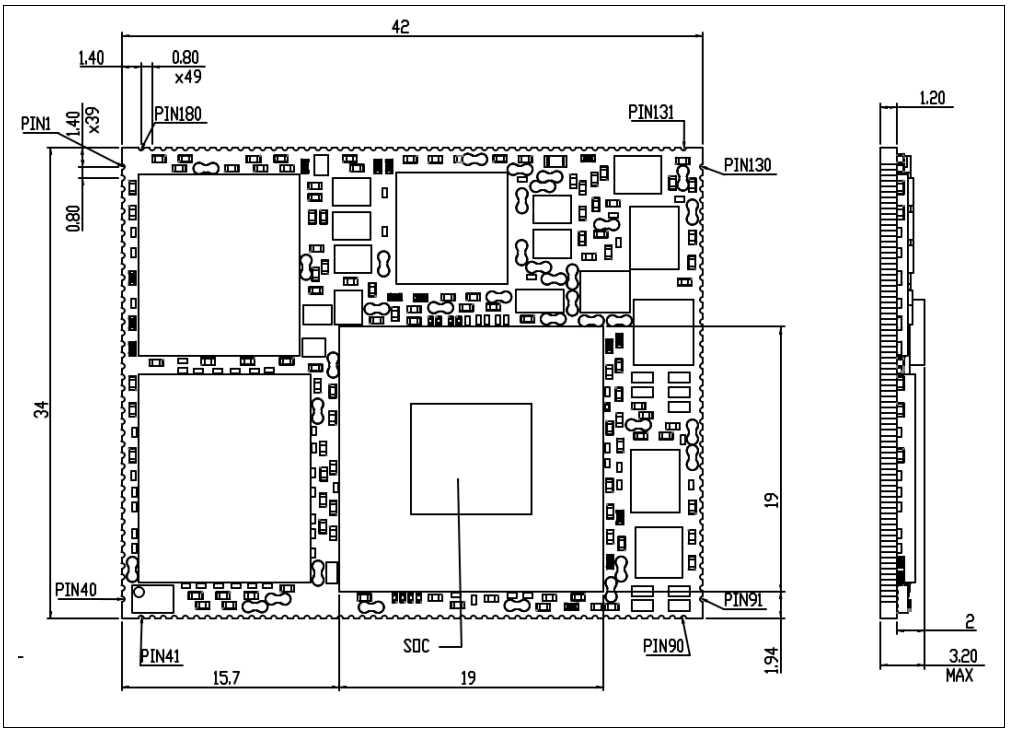
Interface	ESD Performance
i.MX95 pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 MECHANICAL SPECIFICATIONS

8.1 Mechanical Drawings

3D model and mechanical drawings in DXF format are available at https://www.compulab.com/products/computer-on-modules/mcm-imx95-nxp-i-mx-95-som-smd-system-on-module/#devres

Figure 3 MCM-iMX95 mechanical drawing - top

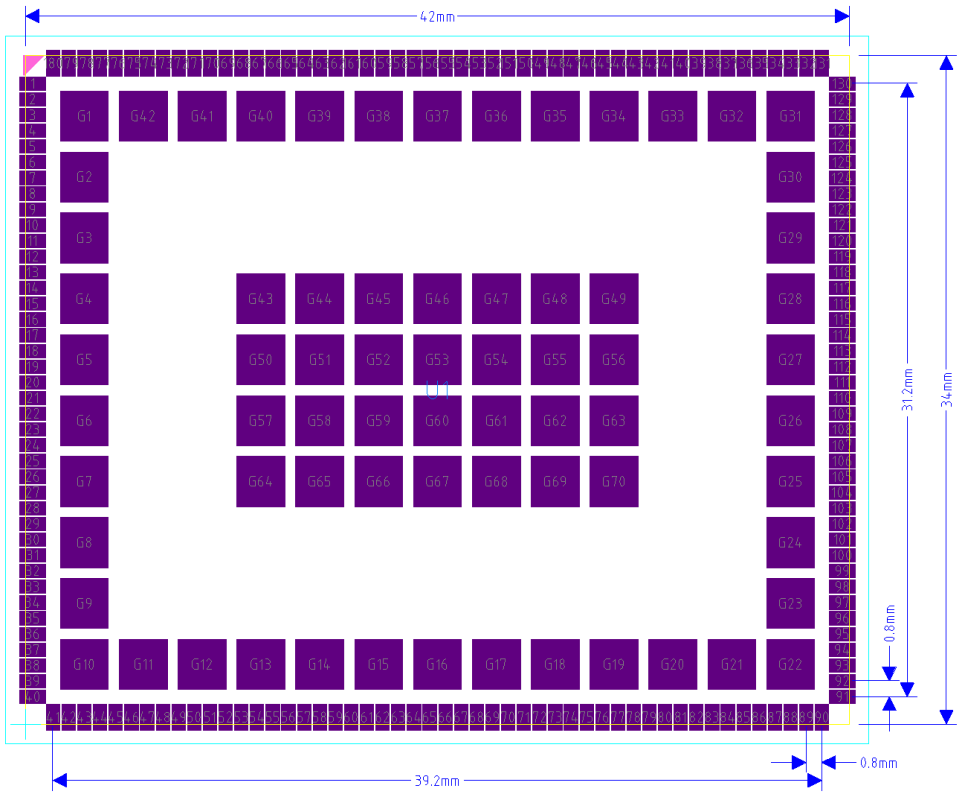


- All dimensions are specified in mm

8.2 Recommended Footprint

MCM-iMX95 footprint in DXF and HKP formats is available at https://www.compulab.com/products/computer-on-modules/mcm-imx95-nxp-i-mx-95-som-smd-system-on-module/#devres

Figure 4 MCM-iMX95 footprint



8.3 Heat Spreader and Cooling Solutions

Compulab provides MCM-iMX95 with an optional heat-spreader assembly. The MCM-iMX95 heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature on any spot of the heat-spreader surface is maintained according to the MCM-iMX95 temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

9 ASSEMBLY AND STORAGE GUIDELINES

9.1 Packaging

MCM-iMX95 modules are supplied in JEDEC-compliant trays. Each tray can hold 18 MCM modules.

9.2 Storage Conditions

MCM-iMX95 modules are supplied in moisture barrier bags. Before use, these must be stored at a temperature of less than 30°C, with humidity under 85% RH.

The calculated shelf-life for the dry-packed product is 12 months from the date the bag is sealed.

9.3 Baking Requirements

MCM-iMX95 modules are rated MSL3. Storage and assembly processes must comply with IPC/JEDEC J-STD-033C. MCM-iMX95 modules have a total thickness of < 3mm and are comparable to a die package. As such, baking instructions must comply with Table 4-1 of J-STD-033C.

Table 73 Baking requirements - JEDEC table extract

Package Body	MSL Level	Bake @ 125C		Bake @ 90°C ≤ 5% RH		Bake @ 40°C ≤ 5% RH	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness > 2.0 mm ≤ 4.5 mm	3	48 hours	48 hours	10 days	8 days	79 days	67 days

9.4 Reflow Profile

Will be added in a later revision of the document.

10 APPLICATION NOTES

10.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the SOM.
- Except for a power connection, no other connection is mandatory for MCM-iMX95 operation. All power-up circuitry and all required pullups/pulldowns are available onboard MCM-iMX95.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - Ethernet, MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Refer to the SB-MCMIMX95 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

10.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches.
- Using an oscilloscope, verify that the SOM GND pins are indeed at zero voltage level and that there is no ground bouncing.
- Create a "minimum system" - only power, the SOM and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.

- Check for the existence of soldering shorts between the SOM pads. Even if the signals are not used on the carrier board, shorting them can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.