MCM-iMX8PV2

Reference Guide

Compulab

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Table 1 Revision Notes

Date	Description
September 2026	• Initial release

Please check for a newer revision of this manual at the Compulab website https://www.compulab.com. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

Compulab System on Module (SOM) products are fully featured, miniature board computers designed for integration into custom industrial applications

This document is part of a set of reference documents providing information necessary to operate and program Compulab MCM-iMX8PV2 System-on-Module.

1.2 MCM-iMX8PV2 Part Number Legend

Please refer to the Compulab website 'Ordering Info' section to decode the MCM-iMX8PV2 part number: https://www.compulab.com/products/computer-on-modules/mcm-imx8pv2-nxp-i-mx-8m-plus-som-smd-system-on-module/#ordering .

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
MCM-iMX8PV2 Developer Resources	https://www.compulab.com/products/computer-on-modules/mcm-imx8pv2-nxp-i-mx-8m-plus-som-smd-system-on-module/#devres
i.MX8M Plus Reference Manual	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8m-plus-arm-cortex-a53-machine-learning-vision-multimedia-and-industrial-iot:IMX8MPLUS?tab=Documentation_Tab
i.MX8M Plus Datasheet	

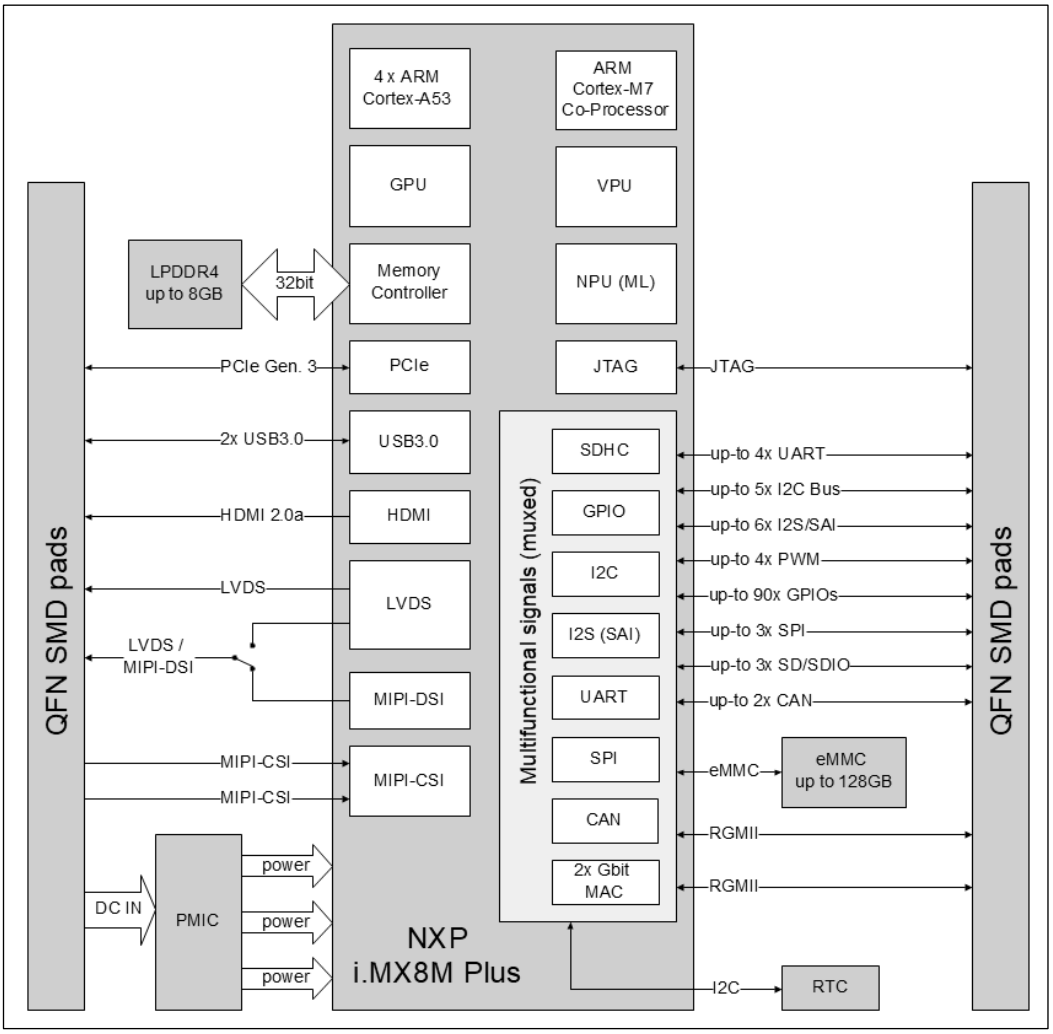
2 OVERVIEW

2.1 Highlights

- NXP i.MX8M Plus Processor, up-to 1.8GHz
- Up to 8GB LPDDR4 and 128GB eMMC
- 2D/3D GPU, 1080p VPU and audio DSP
- Integrated AI/ML Neural Processing Unit
- HDMI, LVDS, MIPI-DSI
- 2x MIPI-CSI camera inputs with dedicated ISP
- PCIe, 2x RGMII, 2x USB3.0
- 2x CAN, 4x UART, 90x GPIO
- Tiny size and weight - 34 x 42 x 3 mm, 8 gram

2.2 Block Diagram

Figure 1 MCM-iMX8PV2 Block Diagram



2.3 MCM-iMX8PV2 Specifications

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.8GHz	C1800QM
	NXP i.MX8M Plus Quad, quad-core ARM Cortex-A53, 1.6GHz, industrial temp. grade	C1600QM
Video Decode	1080p60 HEVC/H.265, AVC/H.264, VP9, VP8	+
Video Encode	1080p60 HEVC/H.265, AVC/H.264	
GPU	GC7000UL (3D): OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.1/1.2; GC520L (2D): DirectFB, GDI/DirectDraw	+
NPU	AI/ML Neural Processing Unit, up to 2.3 TOPS	+
Real-Time Co-processor	ARM Cortex-M7 @ 800 Mhz	+
DSP	Tensilica® HiFi 4 DSP	+
Memory and Storage		
RAM	1GB – 8GB, LPDDR4	D
Storage	eMMC flash, 16GB - 128GB	N
Display and Camera		
Display	HDMI 2.0a, up to 1080p60	+
	MIPI-DSI, 4 data lanes, up to 1080p60	not L2
	LVDS, 4 lanes, up to 1366x768 p60	+
	Dual-channel LVDS, up to 1080p60	L2
Touchscreen	Capacitive touch-screen support through SPI and I2C interfaces	+
Camera	2x MIPI-CSI, 4 data lanes	+
Network		
Ethernet	2x RGMII	+
Audio		
Digital Audio	Up-to 6x I2S / SAI	+
	eARC	+
	S/PDIF input/output	+
I/O		
PCI Express	PCIe Gen. 3.0 x1	+
USB	2x USB3.0	+
UART	Up to 4x UART	+
CAN bus	Up-to 2x CAN	+
MMC/SD/SDIO	Up to 3x SD/SDIO	+
SPI	Up to 3x SPI	+
I2C	Up to 5x I2C	+
PWM	Up to 4x general purpose PWM signals	+
GPIO	Up to 90x GPIO (multifunctional signals shared with other functions)	+

Feature	Description	Option
System Logic		
RTC	Real-time clock, powered by external battery	+
JTAG	JTAG debug interface	+

Table 4 Electrical, Mechanical and Environmental Specifications

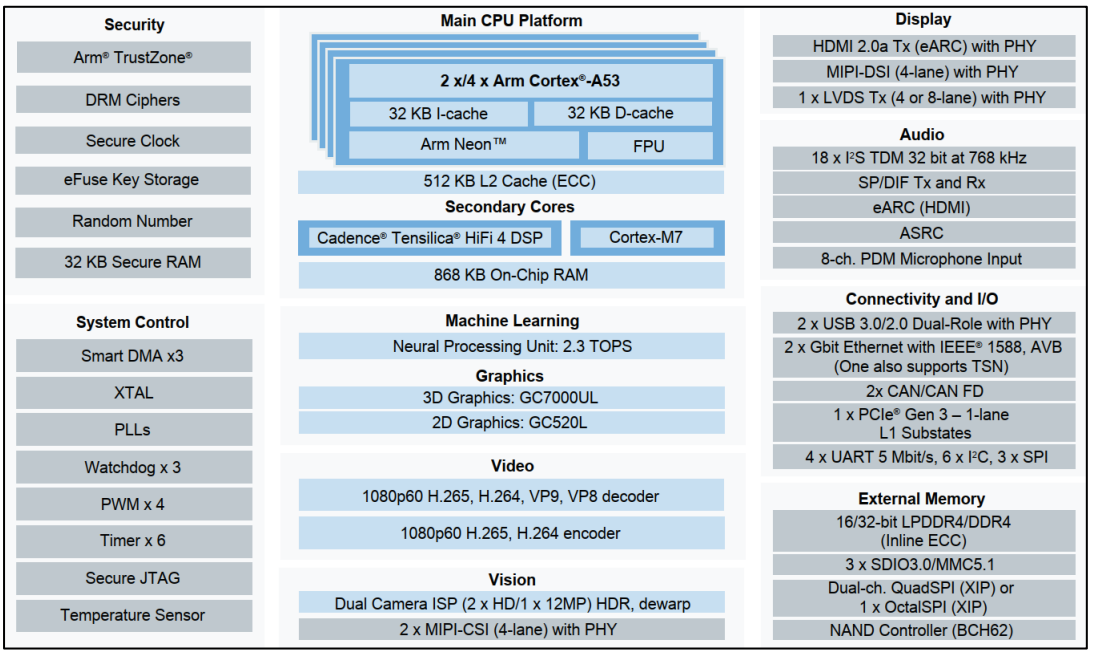
Electrical Specifications	
Supply Voltage	3.45V to 5.5V
Digital I/O voltage	3.3V/1.8V
Mechanical Specifications	
Dimensions	34 x 42 x 3 mm
Weight	8 gram
Foot-print	180-pin, 0.8mm pitch QFN
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 i.MX8M Plus SoC

The i.MX8M Plus family of processors features advanced implementation of a quad ARM® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M7 core processor enables low-power processing.

Figure 2 i.MX8M Plus Block Diagram



3.2 Memory

3.2.1 DRAM

MCM-iMX8PV2 is equipped with up to 8GB of onboard LPDDR4 memory. The LPDDR4 channel is 32-bits wide.

3.2.2 Bootloader and General Purpose Storage

MCM-iMX8PV2 uses on-board non-volatile memory (eMMC) storage for storing the bootloader. The remaining eMMC space is intended to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

MCM-iMX8PV2 implements a variety of peripheral interfaces through its 180-pad carrier board interface. The following notes apply to interfaces available through the carrier-board interface:

- Some interfaces/signals are available only with/without certain configuration options of the MCM-iMX8PV2 SoM. The availability restrictions of each signal are described in the “Signals description” table for each interface.
- Some of the MCM-iMX8PV2 carrier board interface pins are multifunctional. Up to 6 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the MCM-iMX8PV2 digital interfaces operate at 3.3V voltage levels unless noted otherwise.

The signals for each interface are described in the “Signal description” table for the interface in question. The following notes provide information on the “Signal description” tables:

- **“Signal name”** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **“Pin#” –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **“Type” –** Signal type, see the definition of different signal types below
- **“Description” –** Signal description with regards to the interface in question.
- **“Availability” –** Depending on MCM-iMX8PV2 configuration options, certain carrier board interface pins are physically disconnected (floating). The “Availability” column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be “available” unless noted otherwise.

Each described signal can be one of the following types. Signal type is noted in the “Signal description” tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The “Type” column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **“AI”** – Analog Input
- **“AO”** – Analog Output
- **“AIO”** – Analog Input/Output
- **“AP”** – Analog Power Output
- **“I”** – Digital Input
- **"O"** – Digital Output
- **“IO”** – Digital Input/Output
- **“P”** – Power
- **"PD" -** Always pulled down onboard MCM-iMX8PV2, followed by pull value.
- **"PU" -** Always pulled up onboard MCM-iMX8PV2, followed by pull value.
- **“LVDS” -** Low-voltage differential signaling.

4.1 HDMI

The MCM-iMX8PV2 HDMI interface is implemented with the HDMI interface of the i.MX8M Plus SoC. It supports the following main features:

- Compliant with HDMI 2.0a
- Supports HDCP 2.2 and eARC

The following table summarizes the HDMI interface signals.

Table 5 HDMI Interface Signals

Signal Name	Pin #	Type	Description
HDMI_TXCN	101	AO	Negative part of HDMI clock differential pair
HDMI_TXCP	102	AO	Positive part of HDMI clock differential pair
HDMI_TX2N	110	AO	Negative part of HDMI data differential pair 2
HDMI_TX2P	111	AO	Positive part of HDMI data differential pair 2
HDMI_TX1N	107	AO	Negative part of HDMI data differential pair 1
HDMI_TX1P	108	AO	Positive part of HDMI data differential pair 1
HDMI_TX0N	104	AO	Negative part of HDMI data differential pair 0
HDMI_TX0P	105	AO	Positive part of HDMI data differential pair 0
HDMI_DDC_SCL	138*	O	Display Data Channel clock
HDMI_DDC_SDA	137*	IO	Display Data Channel data
HDMI_HPD	91*	I	Hot Plug Detect input
HDMI_CEC	139*	IO	Consumer Electronics Control signal
EARC_N_HPD	44	AO	Negative part of eARC differential pair (HDMI HPD)
EARC_P_UTIL	43	AO	Positive part of eARC differential pair (HDMI Utility)

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.2 MIPI-DSI Interface

The MCM-iMX8PV2 MIPI-DSI interface is derived from the four-lane MIPI display interface available on the i.MX8M Plus SoC. The following main features are supported:

- Scalable data lane support, 1 to 4 data lanes
- Supports MIPI Standard for D-PHY
- Supports display resolutions up to UWHD (2560 x 1080) and WUXGA (1920 x 1200)

MIPI-DSI signals are multiplexed with secondary LVDS signals. MIPI-DSI interface is only available without “L2” configuration option.

The table below summarizes the MIPI-DSI interface signals:

Table 6 MIPI-DSI Interface Signals

Signal Name	Pad #	Type	Description	Availability
DSI1_CLK_N	117	AO	Negative part of MIPI-DSI clock diff-pair	Only without ‘L2' option
DSI1_CLK_P	118	AO	Positive part of MIPI-DSI clock diff-pair	Only without ‘L2' option
DSI1_D0_N	121	AO	Negative part of MIPI-DSI data diff-pair 0	Only without ‘L2' option
DSI1_D0_P	122	AO	Positive part of MIPI-DSI data diff-pair 0	Only without ‘L2' option
DSI1_D1_N	119	AO	Negative part of MIPI-DSI data diff-pair 1	Only without ‘L2' option
DSI1_D1_P	120	AO	Positive part of MIPI-DSI data diff-pair 1	Only without ‘L2' option

Signal Name	Pad #	Type	Description	Availability
DSI1_D2_N	115	AO	Negative part of MIPI-DSI data diff-pair 2	Only without ‘L2' option
DSI1_D2_P	116	AO	Positive part of MIPI-DSI data diff-pair 2	Only without ‘L2' option
DSI1_D3_N	113	AO	Negative part of MIPI-DSI data diff-pair 3	Only without ‘L2' option
DSI1_D3_P	114	AO	Positive part of MIPI-DSI data diff-pair 3	Only without ‘L2' option

4.3 LVDS Interface

The MCM-iMX8PV2 provides up-to two LVDS interfaces derived from the i.MX8M Plus LVDS display bridge. The following key features are supported:

- Two single-channel (4-lane) or one dual channel (8-lanes) output at up to 80 MHz pixel clock
- Resolutions up to 1080p60

LVDS0 interface is always available. LVDS1 signals are multiplexed with MIPI-DSI signals. LVDS1 interface is only available with “L2” configuration option.

The tables below summarize the LVDS interface signals.

Table 7 LVDS0 Interface Signals

Signal Name	Pad #	Type	Description	Availability
LVDS0_CLK_N	29	AO	Negative part of LVDS0 clock diff-pair	Always available
LVDS0_CLK_P	30	AO	Positive part of LVDS0 clock diff-pair	Always available
LVDS0_D0_N	25	AO	Negative part of LVDS0 data diff-pair 0	Always available
LVDS0_D0_P	26	AO	Positive part of LVDS0 data diff-pair 0	Always available
LVDS0_D1_N	27	AO	Negative part of LVDS0 data diff-pair 1	Always available
LVDS0_D1_P	28	AO	Positive part of LVDS0 data diff-pair 1	Always available
LVDS0_D2_N	23	AO	Negative part of LVDS0 data diff-pair 2	Always available
LVDS0_D2_P	24	AO	Positive part of LVDS0 data diff-pair 2	Always available
LVDS0_D3_N	21	AO	Negative part of LVDS0 data diff-pair 3	Always available
LVDS0_D3_P	22	AO	Positive part of LVDS0 data diff-pair 3	Always available

Table 8 LVDS1 Interface Signals

Signal Name	Pad #	Type	Description	Availability
LVDS1_CLK_N	117	AO	Negative part of LVDS1 clock diff-pair	Only with 'L2' option
LVDS1_CLK_P	118	AO	Positive part of LVDS1 clock diff-pair	Only with 'L2' option
LVDS1_D0_N	121	AO	Negative part of LVDS1 data diff-pair 0	Only with 'L2' option
LVDS1_D0_P	122	AO	Positive part of LVDS1 data diff-pair 0	Only with 'L2' option
LVDS1_D1_N	119	AO	Negative part of LVDS1 data diff-pair 1	Only with 'L2' option
LVDS1_D1_P	120	AO	Positive part of LVDS1 data diff-pair 1	Only with 'L2' option
LVDS1_D2_N	115	AO	Negative part of LVDS1 data diff-pair 2	Only with 'L2' option
LVDS1_D2_P	116	AO	Positive part of LVDS1 data diff-pair 2	Only with 'L2' option
LVDS1_D3_N	113	AO	Negative part of LVDS1 data diff-pair 3	Only with 'L2' option
LVDS1_D3_P	114	AO	Positive part of LVDS1 data diff-pair 3	Only with 'L2' option

4.4 Camera Serial Interface

MCM-iMX8PV2 provides two MIPI-CSI interfaces, both derived from the four-lane MIPI CSI host controller integrated into the i.MX8M Plus SoC with dedicated Image Signal Processor (ISP). The controller supports the following main features:

- Up-to four data lanes and one clock lane
- MIPI D-PHY specification V1.2
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature
- Supports primary and secondary image format:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Image Signal Processor (ISP):
  - Input formats: YCbCr420, YCbCr422, RAW8/10/12/14, RGB444/555/565/666/888
  - Image cropping, de-noising, LS and CA lens correction, AWB

Please refer to the i.MX8M Plus Reference manual for additional details. The following table summarizes MIPI-CSI signals.

Table 9 MIPI-CSI Interface Signals

Signal Name	Pin #	Type	Description
MIPI_CSI1_CLK_N	5	AI	Negative part of MIPI-CSI1 clock diff-pair
MIPI_CSI1_CLK_P	6	AI	Positive part of MIPI-CSI1 clock diff-pair
MIPI_CSI1_D0_N	9	AI	Negative part of MIPI-CSI1 data diff-pair 0
MIPI_CSI1_D0_P	10	AI	Positive part of MIPI-CSI1 data diff-pair 0
MIPI_CSI1_D1_N	7	AI	Negative part of MIPI-CSI1 data diff-pair 1
MIPI_CSI1_D1_P	8	AI	Positive part of MIPI-CSI1 data diff-pair 1
MIPI_CSI1_D2_N	3	AI	Negative part of MIPI-CSI1 data diff-pair 2
MIPI_CSI1_D2_P	4	AI	Positive part of MIPI-CSI1 data diff-pair 2
MIPI_CSI1_D3_N	1	AI	Negative part of MIPI-CSI1 data diff-pair 3
MIPI_CSI1_D3_P	2	AI	Positive part of MIPI-CSI1 data diff-pair 3
MIPI_CSI2_CLK_N	15	AI	Negative part of MIPI-CSI2 clock diff-pair
MIPI_CSI2_CLK_P	16	AI	Positive part of MIPI-CSI2 clock diff-pair
MIPI_CSI2_D0_N	11	AI	Negative part of MIPI-CSI2 data diff-pair 0
MIPI_CSI2_D0_P	12	AI	Positive part of MIPI-CSI2 data diff-pair 0
MIPI_CSI2_D1_N	13	AI	Negative part of MIPI-CSI2 data diff-pair 1
MIPI_CSI2_D1_P	14	AI	Positive part of MIPI-CSI2 data diff-pair 1
MIPI_CSI2_D2_N	17	AI	Negative part of MIPI-CSI2 data diff-pair 2
MIPI_CSI2_D2_P	18	AI	Positive part of MIPI-CSI2 data diff-pair 2
MIPI_CSI2_D3_N	19	AI	Negative part of MIPI-CSI2 data diff-pair 3
MIPI_CSI2_D3_P	20	AI	Positive part of MIPI-CSI2 data diff-pair 3

4.5 RGMII

MCM-iMX8PV2 features two RGMII interfaces.

The tables below summarize the RGMII interface signals.

Table 10 Primary RGMII ENET Interface Signals

Signal Name	Pin #	Type	Description	Voltage
ENET_MDC	82	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	1.8V/3.3V
ENET_MDIO	81	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	1.8V/3.3V
ENET_RD0	76	I	Ethernet input data from the PHY	1.8V/3.3V
ENET_RD1	77	I	Ethernet input data from the PHY	1.8V/3.3V
ENET_RD2	79	I	Ethernet input data from the PHY	1.8V/3.3V
ENET_RD3	80	I	Ethernet input data from the PHY	1.8V/3.3V
ENET_RX_CTL	75	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	1.8V/3.3V
ENET_RXC	74	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII mode	1.8V/3.3V
ENET_TD0	69	O	Ethernet output data to PHY	1.8V/3.3V
ENET_TD1	71	O	Ethernet output data to PHY	1.8V/3.3V
ENET_TD2	72	O	Ethernet output data to PHY	1.8V/3.3V
ENET_TD3	73	O	Ethernet output data to PHY	1.8V/3.3V
ENET_TXC	67	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII mode	1.8V/3.3V
ENET_TX_CTL	68	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	1.8V/3.3V
ENET_VIO	70	P	RGMII interface power-supply input; connect to the selected 1.8V or 3.3V rail	1.8V/3.3V

NOTE: The primary RGMII ENET interface voltage is selected by the voltage supplied to ENET_VIO. Use either 1.8V or 3.3V for the complete interface.

NOTE: For additional pin-multiplexing details, refer to chapter 5 of this document.

Table 11 Secondary RGMII ENET1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage
ENET1_MDC	37*	O	Provides a timing reference to the PHY for data transfers on the MDIO signal	1.8V/3.3V
ENET1_MDIO	38*	IO	Transfers control information between the external PHY and the MAC. Data is synchronous to MDC. This signal is an input after reset	1.8V/3.3V
ENET1_RD0	53*	I	Ethernet input data from the PHY	1.8V/3.3V
ENET1_RD1	54*	I	Ethernet input data from the PHY	1.8V/3.3V
ENET1_RD2	55*	I	Ethernet input data from the PHY	1.8V/3.3V
ENET1_RD3	56*	I	Ethernet input data from the PHY	1.8V/3.3V
ENET1_RX_CTL	52*	I	Contains RX_EN on the rising edge of RGMII_RXC, and RX_EN XOR RX_ER on the falling edge of RGMII_RXC (RGMII mode)	1.8V/3.3V
ENET1_RXC	51*	I	Timing reference for RX_DATA[3:0] and RX_CTL in RGMII mode	1.8V/3.3V
ENET1_TD0	47*	O	Ethernet output data to PHY	1.8V/3.3V

Signal Name	Pin #	Type	Description	Voltage
ENET1_TD1	48*	O	Ethernet output data to PHY	1.8V/3.3V
ENET1_TD2	49*	O	Ethernet output data to PHY	1.8V/3.3V
ENET1_TD3	50*	O	Ethernet output data to PHY	1.8V/3.3V
ENET1_TXC	45*	O	Timing reference for TX_DATA[3:0] and TX_CTL in RGMII mode	1.8V/3.3V
ENET1_TX_CTL	46*	O	Contains TX_EN on the rising edge of RGMII_TXC, and TX_EN XOR TX_ER on the falling edge of RGMII_TXC (RGMII mode)	1.8V/3.3V

NOTE: The secondary RGMII ENET1 signals use the NVCC_SD1 voltage domain. Use either 1.8V or 3.3V for the complete shared I/O bank.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.6 PCI-Express

MCM-iMX8PV2 provides one PCI Express Gen 3.0 x1 port.

Table 12 PCIE Interface Signals

Signal Name	Pin #	Type	Description
PCIE_REF_CLKN	159	AO	100 MHz PCIe reference clock differential output negative
PCIE_REF_CLKP	160	AO	100 MHz PCIe reference clock differential output positive
PCIE_RX_N	158	AI	PCI Express receive data negative
PCIE_RX_P	157	AI	PCI Express receive data positive
PCIE_TX_N	156	AO	PCI Express transmit data negative
PCIE_TX_P	155	AO	PCI Express transmit data positive
PCIE_CLKREQ_B	42*	I	Active-low PCI Express reference-clock request input

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.7 Sony/Philips Digital Interface (S/PDIF)

MCM-iMX8PV2 provides one S/PDIF transmitter with one output and one S/PDIF receiver with one input.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the S/PDIF interface signals.

Table 13 S/PDIF Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SPDIF1_EXT_CLK	84*	I	External clock signal	3.3V
	144*			3.3V
SPDIF1_IN	66*	I	S/PDIF input data line signal	3.3V
	80*			ENET_VIO

Signal Name	Pin #	Type	Description	Voltage Domain
	86*			3.3V
	98*			SD2
	143*			3.3V
SPDIF1_OUT	68*	O	S/PDIF output data line signal	ENET_VIO
	86*			3.3V
	97*			SD2
	142*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.8 Digital Audio (SAI)

MCM-iMX8PV2 enables access to six of the i.MX8M Plus integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

Please refer to the i.MX8M Plus Reference manual for additional details.

For SAI signal details please refer to the Signal Multiplexing table in section 5.6.

The tables below summarize the SAI interface signals.

Table 14 SAI1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI1_TX_BCLK	51*	IO	Transmit bit clock	3.3V/1.8V
SAI1_TX_SYNC	52*	IO	Transmit frame sync	3.3V/1.8V
	56*			3.3V/1.8V
SAI1_TX_DATA0	47*	O	Transmit data line 0	3.3V/1.8V
SAI1_TX_DATA1	48*	O	Transmit data line 1	3.3V/1.8V
	57*			3.3V/1.8V
SAI1_TX_DATA2	49*	O	Transmit data line 2	3.3V/1.8V
SAI1_TX_DATA3	50*	O	Transmit data line 3	3.3V/1.8V
SAI1_TX_DATA4	46*	O	Transmit data line 4	3.3V/1.8V
	56*			3.3V/1.8V
SAI1_TX_DATA5	45*	O	Transmit data line 5	3.3V/1.8V
SAI1_RX_SYNC	54*	IO	Receive frame sync	3.3V/1.8V
SAI1_RX_DATA2	37*	I	Receive data line 2	3.3V/1.8V
SAI1_RX_DATA3	38*	I	Receive data line 3	3.3V/1.8V
SAI1_RX_DATA4	53*	I	Receive data line 4	3.3V/1.8V
SAI1_RX_DATA5	54*	I	Receive data line 5	3.3V/1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI1_RX_DATA6	55*	I	Receive data line 6	3.3V/1.8V
SAI1_RX_DATA7	56*	I	Receive data line 7	3.3V/1.8V

Table 15 SAI2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI2_MCLK	61*	IO	Master clock	3.3V
SAI2_TX_BCLK	62*	IO	Transmit bit clock	3.3V
SAI2_TX_SYNC	60*	IO	Transmit frame sync	3.3V
SAI2_TX_DATA0	58*	O	Transmit data line 0	3.3V
SAI2_TX_DATA1	60*	O	Transmit data line 1	3.3V
	83*			3.3V
SAI2_TX_DATA2	85*	O	Transmit data line 2	3.3V
SAI2_TX_DATA3	84*	O	Transmit data line 3	3.3V
SAI2_RX_BCLK	63*	IO	Receive bit clock	3.3V
SAI2_RX_SYNC	59*	IO	Receive frame sync	3.3V
SAI2_RX_DATA1	59*	I	Receive data line 1	3.3V
	66*			3.3V
SAI2_RX_DATA2	65*	I	Receive data line 2	3.3V
SAI2_RX_DATA3	64*	I	Receive data line 3	3.3V

Table 16 SAI3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI3_MCLK	61*	IO	Master clock	3.3V
	86*			3.3V
SAI3_TX_BCLK	85*	IO	Transmit bit clock	3.3V
SAI3_TX_SYNC	83*	IO	Transmit frame sync	3.3V
SAI3_TX_DATA0	84*	O	Transmit data line 0	3.3V
SAI3_TX_DATA1	83*	O	Transmit data line 1	3.3V
SAI3_RX_BCLK	65*	IO	Receive bit clock	3.3V
SAI3_RX_SYNC	66*	IO	Receive frame sync	3.3V
SAI3_RX_DATA0	64*	I	Receive data line 0	3.3V
SAI3_RX_DATA1	66*	I	Receive data line 1	3.3V

Table 17 SAI5 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI5_MCLK	61*	IO	Master clock	3.3V
	86*			3.3V
SAI5_TX_BCLK	63*	IO	Transmit bit clock	3.3V
SAI5_TX_SYNC	59*	IO	Transmit frame sync	3.3V
SAI5_TX_DATA1	59*	O	Transmit data line 1	3.3V
	60*			3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI5_TX_DATA2	62*	O	Transmit data line 2	3.3V
SAI5_TX_DATA3	58*	O	Transmit data line 3	3.3V
SAI5_RX_BCLK	57*	IO	Receive bit clock	3.3V/1.8V
	65*			3.3V
SAI5_RX_SYNC	66*	IO	Receive frame sync	3.3V
SAI5_RX_DATA0	64*	I	Receive data line 0	3.3V
SAI5_RX_DATA1	83*	I	Receive data line 1	3.3V
SAI5_RX_DATA2	85*	I	Receive data line 2	3.3V
SAI5_RX_DATA3	84*	I	Receive data line 3	3.3V

Table 18 SAI6 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI6_MCLK	56*	IO	Master clock	3.3V/1.8V
	68*			ENET_VIO
SAI6_TX_BCLK	46*	IO	Transmit bit clock	3.3V/1.8V
	53*			3.3V/1.8V
	73*			ENET_VIO
SAI6_TX_SYNC	55*	IO	Transmit frame sync	3.3V/1.8V
	81*			ENET_VIO
SAI6_TX_DATA0	45*	O	Transmit data line 0	3.3V/1.8V
	54*			3.3V/1.8V
	82*			ENET_VIO
SAI6_RX_BCLK	46*	IO	Receive bit clock	3.3V/1.8V
	53*			3.3V/1.8V
	69*			ENET_VIO
SAI6_RX_SYNC	55*	IO	Receive frame sync	3.3V/1.8V
	71*			ENET_VIO
SAI6_RX_DATA0	45*	I	Receive data line 0	3.3V/1.8V
	54*			3.3V/1.8V
	72*			ENET_VIO

Table 19 SAI7 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
SAI7_MCLK	80*	IO	Master clock	ENET_VIO
	90*			3.3V
SAI7_TX_BCLK	74*	IO	Transmit bit clock	ENET_VIO
	87*			3.3V
SAI7_TX_SYNC	75*	IO	Transmit frame sync	ENET_VIO
	103*			3.3V
SAI7_TX_DATA0	67*	O	Transmit data line 0	ENET_VIO
	89*			3.3V
SAI7_RX_BCLK	79*	IO	Receive bit clock	ENET_VIO
	109*			3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
SAI7_RX_SYNC	77*	IO	Receive frame sync	ENET_VIO
	112*			3.3V
SAI7_RX_DATA0	76*	I	Receive data line 0	ENET_VIO
	106*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.9 USB

i.MX8M Plus SoC is equipped with two dual-role USB3.0 controllers and PHYs.

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the USB3.0 interface signals.

Table 20 USB port #1 Signals

Signal Name	Pin #	Type	Description
USB1_DN	174	IO	USB2.0 negative data
USB1_DP	173	IO	USB2.0 positive data
USB1_VBUS	179	I	USB1 VBUS detect
USB1_TX_N	150	AO	USB3.0 transmit negative lane
USB1_TX_P	149	AO	USB3.0 transmit positive lane
USB1_RX_N	172	AI	USB3.0 receive negative lane
USB1_RX_P	171	AI	USB3.0 receive positive lane

Table 21 USB port #2 Signals

Signal Name	Pin #	Type	Description
USB2_DN	163	IO	USB2.0 negative data
USB2_DP	164	IO	USB2.0 positive data
USB2_VBUS	180	I	USB2 VBUS detect
USB2_TX_N	161	AO	USB3.0 transmit negative lane
USB2_TX_P	162	AO	USB3.0 transmit positive lane
USB2_RX_N	170	AI	USB3.0 receive negative lane
USB2_RX_P	169	AI	USB3.0 receive positive lane

4.10 MMC / SD /SDIO

MCM-iMX8PV2i.MX8M Plus

- Fully compliant with MMC 5.1 command/response sets and physical layer
- Fully compliant with SD 3.01 command/response sets and physical layer

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals.

Table 22 SD/SDIO port #1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC1_CLK	134*	O	Clock for MMC/SD/SDIO card	3.3V/1.8V
USDHC1_CMD	132*	IO	CMD line connected to card	3.3V/1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC1_DATA0	129*	IO	DATA0 line in all modes; also used to detect busy state	3.3V/1.8V
USDHC1_DATA1	130*	IO	DATA1 line in 4/8-bit mode; also used to detect interrupt in 1/4-bit mode	3.3V/1.8V
USDHC1_DATA2	131*	IO	DATA2 line or Read Wait in 4-bit mode; Read Wait in 1-bit mode	3.3V/1.8V
USDHC1_DATA3	133*	IO	DATA3 line in 4/8-bit mode or card-detection input	3.3V/1.8V
USDHC1_STROBE	128*	I	MMC data strobe input	3.3V/1.8V

NOTE: SD/SDIO port #1 supports 1.8V or 3.3V operation.

NOTE: SDIO pads are multifunctional. For additional details please refer to chapter 5 of this document

Table 23 SD/SDIO port #2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC2_CD_B	92*	I	Card-detection input, active low	SD2
USDHC2_CLK	96*	O	Clock for MMC/SD/SDIO card	SD2
USDHC2_CMD	95*	IO	CMD line connected to card	SD2
USDHC2_DATA0	94*	IO	DATA0 line in all modes; also used to detect busy state	SD2
USDHC2_DATA1	93*	IO	DATA1 line in 4/8-bit mode; also used to detect interrupt in 1/4-bit mode	SD2
USDHC2_DATA2	97*	IO	DATA2 line or Read Wait in 4-bit mode; Read Wait in 1-bit mode	SD2
USDHC2_DATA3	98*	IO	DATA3 line in 4/8-bit mode or card-detection input	SD2
USDHC2_RESET_B	78*	O	Card hardware reset signal, active low	SD2
USDHC2_WP	141*	I	Card write-protect detection input	SD2

NOTE: SD/SDIO port #2 can be configured to operate at 3.3V or 1.8V voltage levels. SD2 voltage domain level is controlled by SoC pin GPIO1_IO04.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

Table 24 SD/SDIO port #3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC3_CD_B	71*	I	Card-detection input, active low	ENET_VIO
USDHC3_CLK	79*	O	Clock for MMC/SD/SDIO card	ENET_VIO
USDHC3_CMD	80*	IO	CMD line connected to card	ENET_VIO
USDHC3_DATA0	68*	IO	DATA0 line in all modes; also used to detect busy state	ENET_VIO
USDHC3_DATA1	67*	IO	DATA1 line in 4/8-bit mode; also used to detect interrupt in 1/4-bit mode	ENET_VIO
USDHC3_DATA2	75*	IO	DATA2 line or Read Wait in 4-bit mode; Read Wait in 1-bit mode	ENET_VIO
USDHC3_DATA3	74*	IO	DATA3 line in 4/8-bit mode or card-detection input	ENET_VIO

Signal Name	Pin #	Type	Description	Voltage Domain
USDHC3_DATA4	76*	IO	DATA4 line in 8-bit mode	ENET_VIO
USDHC3_DATA5	81*	IO	DATA5 line in 8-bit mode	ENET_VIO
USDHC3_DATA6	73*	IO	DATA6 line in 8-bit mode	ENET_VIO
USDHC3_DATA7	72*	IO	DATA7 line in 8-bit mode	ENET_VIO
USDHC3_RESET_B	34*	O	Card hardware reset signal, active low	3.3V
	77*			ENET_VIO
USDHC3_STROBE	82*	I	MMC data strobe input	ENET_VIO
USDHC3_VSELECT	33*	O	I/O voltage-select output	3.3V
	175*			3.3V
USDHC3_WP	69*	I	Card write-protect detection input	ENET_VIO

NOTE: ENET_VIO must be supplied from carrier-board for proper operation of SDIO #3

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.11 UART

MCM-iMX8PV2 enables access to up-to four i.MX8M Plus universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The i.MX8M Plus UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: By default UART2 is assigned to be used as the main system console port.

NOTE: By default UART4 is assigned to be used as the M7 core debug port.

Please refer to the i.MX8M Plus Reference manual for additional details.

For UART signal details please refer to the Signal Multiplexing table in section 5.6.

The tables below summarize the UART interface signals.

Table 25 UART1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART1_TX	31*	O	Transmit data	3.3V
	59*			3.3V
	134*			3.3V/1.8V
UART1_RX	32*	I	Receive data	3.3V
	63*			3.3V
	132*			3.3V/1.8V
UART1_RTS_B	33*	O	Active-low RTS output	3.3V
	129*			3.3V/1.8V
UART1_CTS_B	34*	I	Active-low CTS input	3.3V
	60*			3.3V
	130*			3.3V/1.8V

Table 26 UART2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART2_TX	85*	O	Transmit data	3.3V
	93*			SD2
	131*			3.3V/1.8V
	148*			3.3V
UART2_RX	83*	I	Receive data	3.3V
	94*			SD2
	133*			3.3V/1.8V
	135*			3.3V
UART2_RTS_B	36*	O	Active-low RTS output	3.3V
	64*			3.3V
UART2_CTS_B	35*	I	Active-low CTS input	3.3V
	65*			3.3V

Table 27 UART3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART3_TX	33*	O	Transmit data	3.3V
	109*			3.3V
UART3_RX	34*	I	Receive data	3.3V
	112*			3.3V
UART3_RTS_B	103*	O	Active-low RTS output	3.3V
UART3_CTS_B	106*	I	Active-low CTS input	3.3V
	128*			3.3V/1.8V

Table 28 UART4 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
UART4_TX	36*	O	Transmit data	3.3V
	89*			3.3V
	95*			SD2
UART4_RX	35*	I	Receive data	3.3V
	87*			3.3V
	96*			SD2
UART4_RTS_B	88*	O	Active-low RTS output	3.3V
UART4_CTS_B	90*	I	Active-low CTS input	3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.12 CAN Bus

MCM-iMX8PV2 features up-to two CAN bus interfaces. These interfaces support the following key features:

- Full implementation of the CAN version 2.0B
- Compliant with the ISO 11898-1 standard

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the CAN interface signals.

Table 29 CAN1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN1_TX	63*	O	CAN transmit pin	3.3V
	138*			3.3V
	142*			3.3V
CAN1_RX	62*	I	CAN receive pin	3.3V
	137*			3.3V
	143*			3.3V

Table 30 CAN2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
CAN2_TX	34*	O	CAN transmit pin	3.3V
	58*			3.3V
	139*			3.3V
CAN2_RX	33*	I	CAN receive pin	3.3V
	61*			3.3V
	91*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.13 I2C

MCM-iMX8PV2 features up-to six I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode

Please refer to the i.MX8M Plus Reference manual for additional details.

NOTE: I2C2 is the system I2C channel utilized for the following on-board functions: RTC, EEPROM.

The tables below summarize the I2C interface signals.

Table 31 I2C1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C1_SCL	112*	IO	I2C-1 serial clock signal	3.3V
I2C1_SDA	109*	IO	I2C-1 serial data signal	3.3V

Table 32 I2C3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C3_SCL	39*	IO	I2C-3 serial clock signal	3.3V
	87*			3.3V
I2C3_SDA	40*	IO	I2C-3 serial data signal	3.3V
	89*			3.3V
	128*			3V3/1V8

Table 33 I2C4 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C4_SCL	42*	IO	I2C-4 serial clock signal	3.3V
	90*			3.3V
	93*			SD2
	131*			3V3/1V8
I2C4_SDA	41*	IO	I2C-4 serial data signal	3.3V
	88*			3.3V
	94*			SD2
	133*			3V3/1V8

Table 34 I2C5 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C5_SCL	134*	IO	I2C-5 serial clock signal	3V3/1V8
	138*			3.3V
	142*			3.3V
I2C5_SDA	132*	IO	I2C-5 serial data signal	3V3/1V8
	137*			3.3V
	143*			3.3V

Table 35 I2C6 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
I2C6_SCL	35*	IO	I2C-6 serial clock signal	3.3V
	129*			3V3/1V8
	139*			3.3V
I2C6_SDA	36*	IO	I2C-6 serial data signal	3.3V
	57*			3V3/1V8
	91*			3.3V
	130*			3V3/1V8

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.14 ECSPI

Up-to three SPI interfaces are accessible through the MCM-iMX8PV2 carrier board interface. The SPI interfaces are derived from i.MX8M Plus integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s
- Full-duplex synchronous serial interface
- Master/Slave configurable
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support

Please refer to the i.MX8M Plus Reference manual for additional details.

The tables below summarize the ECSPI interface signals.

Table 36 ECSPI1 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI1_MISO	106*	I	SPI-1 master data in; slave data out	3.3V
ECSPI1_MOSI	109*	O	SPI-1 master data out; slave data in	3.3V
ECSPI1_SCLK	112*	O	SPI-1 master clock out; slave clock in	3.3V
ECSPI1_SS0	103*	O	SPI-1 chip select 0	3.3V

Table 37 ECSPI2 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI2_MISO	42*	I	SPI-2 master data in; slave data out	3.3V
	90*			3.3V
	98*			SD2
ECSPI2_MOSI	40*	O	SPI-2 master data out; slave data in	3.3V
	89*			3.3V
	95*			SD2
ECSPI2_SCLK	39*	O	SPI-2 master clock out; slave clock in	3.3V
	87*			3.3V
	96*			SD2

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI2_SS0	41*	O	SPI-2 chip select 0	3.3V
	88*			3.3V
	97*			SD2

Table 38 ECSPI3 Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
ECSPI3_MISO	135*	I	SPI-3 master data in; slave data out	3.3V
ECSPI3_MOSI	31*	O	SPI-3 master data out; slave data in	3.3V
ECSPI3_SCLK	32*	O	SPI-3 master clock out; slave clock in	3.3V
ECSPI3_SS0	148*	O	SPI-3 chip select 0	3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.15 PWM

MCM-iMX8PV2 features up to four independent PWM output signals. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the PWM interface signals.

Table 39 PWM Interface Signals

Signal Name	Pin #	Type	Description	Voltage Domain
PWM1_OUT	41*	O	PWM1 functional output	3.3V
	100*			3.3V
	144*			3.3V
PWM2_OUT	42*	O	PWM2 functional output	3.3V
	143*			3.3V
	175*			3.3V
PWM3_OUT	40*	O	PWM3 functional output	3.3V
	57*			3.3V/1.8V
	142*			3.3V
	167*			3.3V
PWM4_OUT	39*	O	PWM4 functional output	3.3V
	86*			3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

4.16 JTAG

MCM-iMX8PV2 enables access to the i.MX8M Plus JTAG port through the carrier board interface.

Please refer to the i.MX8M Plus Reference manual for additional details.

The table below summarizes the JTAG interface signals.

Table 40 JTAG Interface Signals

Signal Name	Pin #	Type	Description
JTAG_MOD	145	I	JTAG mode select
JTAG_TDI	151	I	Test data in
JTAG_TDO	153	O	Test data out
JTAG_TMS	154	I	Test mode select
JTAG_TCK	152	I	Test clock

4.17 GPIO

Up-to 90 of the i.MX8M Plus general purpose input/output (GPIO) signals are available through the MCM-iMX8PV2 carrier board interface. When configured as an output, it is possible to write to an i.MX8M Plus register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an i.MX8M Plus register. In addition, GPIO signals can produce interrupts.
Please refer to the i.MX8M Plus Reference manual for additional details.
The table below summarizes the GPIO interface signals.

Table 41 GPIO Signals

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO1_IO0	165*	IO	GPIO	3.3V
GPIO1_IO1	100*	IO	GPIO	3.3V
GPIO1_IO5	99*	IO	GPIO	3.3V
GPIO1_IO10	167*	IO	GPIO	3.3V
GPIO1_IO11	175*	IO	GPIO	3.3V
GPIO1_IO16	82*	IO	GPIO	ENET_VIO
GPIO1_IO17	81*	IO	GPIO	ENET_VIO
GPIO1_IO18	73*	IO	GPIO	ENET_VIO
GPIO1_IO19	72*	IO	GPIO	ENET_VIO
GPIO1_IO20	71*	IO	GPIO	ENET_VIO
GPIO1_IO21	69*	IO	GPIO	ENET_VIO
GPIO1_IO22	68*	IO	GPIO	ENET_VIO
GPIO1_IO23	67*	IO	GPIO	ENET_VIO
GPIO1_IO24	75*	IO	GPIO	ENET_VIO
GPIO1_IO25	74*	IO	GPIO	ENET_VIO
GPIO1_IO26	76*	IO	GPIO	ENET_VIO
GPIO1_IO27	77*	IO	GPIO	ENET_VIO
GPIO1_IO28	79*	IO	GPIO	ENET_VIO
GPIO1_IO29	80*	IO	GPIO	ENET_VIO
GPIO2_IO0	134*	IO	GPIO	3.3V/1.8V
GPIO2_IO1	132*	IO	GPIO	3.3V/1.8V
GPIO2_IO2	129*	IO	GPIO	3.3V/1.8V
GPIO2_IO3	130*	IO	GPIO	3.3V/1.8V
GPIO2_IO4	131*	IO	GPIO	3.3V/1.8V
GPIO2_IO5	133*	IO	GPIO	3.3V/1.8V
GPIO2_IO11	128*	IO	GPIO	3.3V/1.8V

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO2_IO12	92*	IO	GPIO	SD2
GPIO2_IO13	96*	IO	GPIO	SD2
GPIO2_IO14	95*	IO	GPIO	SD2
GPIO2_IO15	94*	IO	GPIO	SD2
GPIO2_IO16	93*	IO	GPIO	SD2
GPIO2_IO17	97*	IO	GPIO	SD2
GPIO2_IO18	98*	IO	GPIO	SD2
GPIO2_IO19	78*	IO	GPIO	SD2
GPIO2_IO20	141*	IO	GPIO	SD2
GPIO3_IO20	57*	IO	GPIO	3.3V/1.8V
GPIO3_IO26	138*	IO	GPIO	3.3V
GPIO3_IO27	137*	IO	GPIO	3.3V
GPIO3_IO28	139*	IO	GPIO	3.3V
GPIO3_IO29	91*	IO	GPIO	3.3V
GPIO4_IO4	37*	IO	GPIO	3.3V/1.8V
GPIO4_IO5	38*	IO	GPIO	3.3V/1.8V
GPIO4_IO6	53*	IO	GPIO	3.3V/1.8V
GPIO4_IO7	54*	IO	GPIO	3.3V/1.8V
GPIO4_IO8	55*	IO	GPIO	3.3V/1.8V
GPIO4_IO9	56*	IO	GPIO	3.3V/1.8V
GPIO4_IO10	52*	IO	GPIO	3.3V/1.8V
GPIO4_IO11	51*	IO	GPIO	3.3V/1.8V
GPIO4_IO12	47*	IO	GPIO	3.3V/1.8V
GPIO4_IO13	48*	IO	GPIO	3.3V/1.8V
GPIO4_IO14	49*	IO	GPIO	3.3V/1.8V
GPIO4_IO15	50*	IO	GPIO	3.3V/1.8V
GPIO4_IO16	46*	IO	GPIO	3.3V/1.8V
GPIO4_IO17	45*	IO	GPIO	3.3V/1.8V
GPIO4_IO21	59*	IO	GPIO	3.3V
GPIO4_IO22	63*	IO	GPIO	3.3V
GPIO4_IO24	60*	IO	GPIO	3.3V
GPIO4_IO25	62*	IO	GPIO	3.3V
GPIO4_IO26	58*	IO	GPIO	3.3V
GPIO4_IO27	61*	IO	GPIO	3.3V
GPIO4_IO28	66*	IO	GPIO	3.3V
GPIO4_IO29	65*	IO	GPIO	3.3V
GPIO4_IO30	64*	IO	GPIO	3.3V
GPIO4_IO31	83*	IO	GPIO	3.3V
GPIO5_IO0	85*	IO	GPIO	3.3V
GPIO5_IO1	84*	IO	GPIO	3.3V
GPIO5_IO2	86*	IO	GPIO	3.3V
GPIO5_IO3	142*	IO	GPIO	3.3V
GPIO5_IO4	143*	IO	GPIO	3.3V
GPIO5_IO5	144*	IO	GPIO	3.3V
GPIO5_IO6	112*	IO	GPIO	3.3V
GPIO5_IO7	109*	IO	GPIO	3.3V
GPIO5_IO8	106*	IO	GPIO	3.3V
GPIO5_IO9	103*	IO	GPIO	3.3V
GPIO5_IO10	87*	IO	GPIO	3.3V
GPIO5_IO11	89*	IO	GPIO	3.3V

Signal Name	Pin #	Type	Description	Voltage Domain
GPIO5_IO12	90*	IO	GPIO	3.3V
GPIO5_IO13	88*	IO	GPIO	3.3V
GPIO5_IO18	39*	IO	GPIO	3.3V
GPIO5_IO19	40*	IO	GPIO	3.3V
GPIO5_IO20	42*	IO	GPIO	3.3V
GPIO5_IO21	41*	IO	GPIO	3.3V
GPIO5_IO22	32*	IO	GPIO	3.3V
GPIO5_IO23	31*	IO	GPIO	3.3V
GPIO5_IO24	135*	IO	GPIO	3.3V
GPIO5_IO25	148*	IO	GPIO	3.3V
GPIO5_IO26	34*	IO	GPIO	3.3V
GPIO5_IO27	33*	IO	GPIO	3.3V
GPIO5_IO28	35*	IO	GPIO	3.3V
GPIO5_IO29	36*	IO	GPIO	3.3V

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5 of this document

NOTE: GPIO voltage is determined by the associated voltage domain shown in Table 43. ENET_VIO and the 3.3V/1.8V domains support 1.8V or 3.3V operation; all other listed GPIOs operate at the voltage shown.

5 SYSTEM LOGIC

5.1 Power Supply

Table 42 Power signals

Signal Name	Pin#	Type	Description
V_SOM	123, 124, 125	P	Main power supply. Connect to a regulated DC supply or Li-Ion battery.
VCC_RTC	136	P	RTC backup battery input. Connect to a 3.3V backup source when RTC backup is required; otherwise leave this pin unconnected.
ENET_VIO	70	P	RGMII interface I/O power supply input. Connect to a 1.8 V or 3.3 V rail according to the external PHY requirements.

5.2 I/O Voltage Domains

MCM-iMX8PV2 utilizes four separate I/O voltage domains to power different I/O modules of the i.MX8M Plus SoC:

Table 43 I/O Voltage Domains

I/O Voltage Domain	Description	Default Voltage	Control
3.3V domain	Main SoM 3.3 V I/O rail, powered by PMIC BUCK4.	3.3V	N/A
ENET_VIO domain	RGMII interface I/O supply. The carrier board must supply this domain through MCM pad 70 (ENET_VIO).	ENET_VIO	N/A
SD2 domain	SD2 interface I/O supply, powered by PMIC LDO5.	3.3V	SD2_VSEL / GPIO1_IO04
3.3V/1.8V domain	Software-programmable 3.3 V/1.8 V I/O rail, powered by PMIC LDO4.	1.8V	U-Boot PMIC LDO4 setting

5.3 System and Miscellaneous Signals

5.3.1 External regulator control and power management

MCM-iMX8PV2 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX8M Plus SoC. The logic that controls both signals is supplied by the i.MX8M Plus SoC SNVS power rail.

The PMIC_STBY_REQ output can be used to signal the carrier board power supply that MCM-iMX8PV2 is in ‘standby’ or ‘OFF’ mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the i.MX8M Plus Reference manual for additional details. The table below summarizes the external regulator control signals.

Table 44 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	147	O	Asserted by the i.MX8M Plus processor when it enters SUSPEND mode.	Always available
PMIC_ON_REQ	146	O	Active-high power-up request output from the i.MX8M Plus processor.i.MX8M Plus	Always available

Signal Name	Pin #	Type	Description	Availability
PWRBTN	140	I	Active-low ON/OFF input with an on-module pull-up, intended for a momentary push button.	Always available

5.4 Reset

SYS_RST_PMIC signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on MCM-iMX8PV2. Please refer to the i.MX8M Plus Reference manual for additional details.

Table 45 Reset signals

Signal Name	Pin #	Type	Description	Availability
SYS_RST_PMIC	168	I	Active-low cold-reset input. Use as the main system reset.	Always available

5.5 Boot Sequence

MCM-iMX8PV2 boot sequence defines which interface/media is used by MCM-iMX8PV2 to load and execute the initial software (such as SPL or/and U-boot). MCM-iMX8PV2 can load initial software from the following interfaces/media:

- The on-board primary boot device (eMMC with pre-flashed boot-loader)
- An external SD card using the SD/SDIO 2 interface

MCM-iMX8PV2 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by MCM-iMX8PV2:

- Standard sequence: designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: designed to allow recovery from an external boot device in case of data corruption of the on-board primary boot device. Using the alternate sequence allows MCM-iMX8PV2 to boot from an external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 46 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	166	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 47 MCM-iMX8PV2 Boot sequences

Sequence	ALT_BOOT	First
Standard	Low or floating	Onboard eMMC (primary boot storage)
Alternate	High	SD card on SD/SDIO2 interface

5.6 Signal Multiplexing Characteristics

Up to 90 of the MCM-iMX8PV2 pads are multifunctional. Multifunctional pads enable extensive functional flexibility of the MCM-iMX8PV2 CoM/SoM by allowing usage of a single pad for one of several functions. Up-to 6 functions (MUX modes) are accessible through each multifunctional pad. The multifunctional capabilities of MCM-iMX8PV2 pads are derived from the i.MX8M Plus SoC control module

NOTE: Pad function selection is controlled by software.

NOTE: Each pad can be used for a single function at a time.

NOTE: Only one pad can be used for each function (in case a function is available on more than one pad).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 48 Multifunctional Signals

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
106	ECSPI1_MISO	3.3V	GPIO5_IO8	SAI7_RX_DATA0			UART3_CTS_B			ECSPI1_MISO					
109	ECSPI1_MOSI	3.3V	GPIO5_IO7	SAI7_RX_BCLK		I2C1_SDA	UART3_TX			ECSPI1_MOSI					
112	ECSPI1_SCLK	3.3V	GPIO5_IO6	SAI7_RX_SYNC		I2C1_SCL	UART3_RX			ECSPI1_SCLK					
103	ECSPI1_SS0	3.3V	GPIO5_IO9	SAI7_TX_SYNC			UART3_RTS_B			ECSPI1_SS0					
90	ECSPI2_MISO	3.3V	GPIO5_IO12	SAI7_MCLK		I2C4_SCL	UART4_CTS_B			ECSPI2_MISO					
89	ECSPI2_MOSI	3.3V	GPIO5_IO11	SAI7_TX_DATA0		I2C3_SDA	UART4_TX			ECSPI2_MOSI					
87	ECSPI2_SCLK	3.3V	GPIO5_IO10	SAI7_TX_BCLK		I2C3_SCL	UART4_RX			ECSPI2_SCLK					
88	ECSPI2_SS0	3.3V	GPIO5_IO13			I2C4_SDA	UART4_RTS_B			ECSPI2_SS0					
82	ENET_MDC	ENET_VIO	GPIO1_IO16	SAI6_TX_DATA0	USDHC3_STROBE				ENET_QOS_MDC						
81	ENET_MDIO	ENET_VIO	GPIO1_IO17	SAI6_TX_SYNC	USDHC3_DATA5				ENET_QOS_MDIO						
76	ENET_RD0	ENET_VIO	GPIO1_IO26	SAI7_RX_DATA0	USDHC3_DATA4				ENET_QOS_RD0						
77	ENET_RD1	ENET_VIO	GPIO1_IO27	SAI7_RX_SYNC	USDHC3_RESET_B				ENET_QOS_RD1						
79	ENET_RD2	ENET_VIO	GPIO1_IO28	SAI7_RX_BCLK	USDHC3_CLK				ENET_QOS_RD2						
80	ENET_RD3	ENET_VIO	GPIO1_IO29	SAI7_MCLK	USDHC3_CMD				ENET_QOS_RD3						SPDIF1_IN

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
75	ENET_RX_CTL	ENET_VIO	GPIO1_IO24	SAI7_TX_SYNC	USDHC3_DATA2				ENET_QOS_RX_CTL						
74	ENET_RXC	ENET_VIO	GPIO1_IO25	SAI7_TX_BCLK	USDHC3_DATA3				ENET_QOS_RXC ENET_QOS_RX_ER						
69	ENET_TD0	ENET_VIO	GPIO1_IO21	SAI6_RX_BCLK	USDHC3_WP				ENET_QOS_TD0						
71	ENET_TD1	ENET_VIO	GPIO1_IO20	SAI6_RX_SYNC	USDHC3_CD_B				ENET_QOS_TD1						
72	ENET_TD2	ENET_VIO	GPIO1_IO19	SAI6_RX_DATA0	USDHC3_DATA7				ENET_QOS_TD2 ENET_QOS_TX_CLK						
73	ENET_TD3	ENET_VIO	GPIO1_IO18	SAI6_TX_BCLK	USDHC3_DATA6				ENET_QOS_TD3						
68	ENET_TX_CTL	ENET_VIO	GPIO1_IO22	SAI6_MCLK	USDHC3_DATA0				ENET_QOS_TX_CTL						SPDIF1_OUT
67	ENET_TXC	ENET_VIO	GPIO1_IO23	SAI7_TX_DATA0	USDHC3_DATA1				ENET_QOS_TXC ENET_QOS_TX_ER						
165	GPIO1_IO00	3.3V	GPIO1_IO0												
100	GPIO1_IO01	3.3V	GPIO1_IO1								PWM1_OUT				
99	GPIO1_IO05	3.3V	GPIO1_IO5												
167	GPIO1_IO10	3.3V	GPIO1_IO10								PWM3_OUT				
175	GPIO1_IO11	3.3V	GPIO1_IO11		USDHC3_VSELECT						PWM2_OUT				
139	HDMI_CEC	3.3V	GPIO3_IO28			I2C6_SCL						CAN2_TX		HDMI_CEC	
138	HDMI_DDC_SCL	3.3V	GPIO3_IO26			I2C5_SCL						CAN1_TX		HDMI_SCL	
137	HDMI_DDC_SDA	3.3V	GPIO3_IO27			I2C5_SDA						CAN1_RX		HDMI_SDA	
91	HDMI_HPD	3.3V	GPIO3_IO29			I2C6_SDA						CAN2_RX		HDMI_HPD	
39	I2C3_SCL	3.3V	GPIO5_IO18			I2C3_SCL				ECSPI2_SCLK	PWM4_OUT				
40	I2C3_SDA	3.3V	GPIO5_IO19			I2C3_SDA				ECSPI2_MOSI	PWM3_OUT				
42	I2C4_SCL	3.3V	GPIO5_IO20			I2C4_SCL				ECSPI2_MISO	PWM2_OUT				
41	I2C4_SDA	3.3V	GPIO5_IO21			I2C4_SDA				ECSPI2_SS0	PWM1_OUT				
37	SAI1_RXD2	3V3/1V8	GPIO4_IO4	SAI1_RX_DATA2				ENET1_MDC							
38	SAI1_RXD3	3V3/1V8	GPIO4_IO5	SAI1_RX_DATA3				ENET1_MDIO							
53	SAI1_RXD4	3V3/1V8	GPIO4_IO6	SAI1_RX_DATA4 SAI6_TX_BCLK SAI6_RX_BCLK				ENET1_RD0							
54	SAI1_RXD5	3V3/1V8	GPIO4_IO7	SAI1_RX_DATA5/SAI6_TX_DATA0/SAI6_RX_DATA0/SAI1_RX_SYNC				ENET1_RD1							

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
55	SAI1_RXD6	3V3/1V8	GPIO4_IO8	SAI1_RX_DATA6/SAI6_TX_SYNC/SAI6_RX_SYNC				ENET1_RD2							
56	SAI1_RXD7	3V3/1V8	GPIO4_IO9	SAI1_RX_DATA7 SAI6_MCLK SAI1_TX_SYNC SAI1_TX_DATA4				ENET1_RD3							
51	SAI1_TXC	3V3/1V8	GPIO4_IO11	SAI1_TX_BCLK				ENET1_RXC							
47	SAI1_TXD0	3V3/1V8	GPIO4_IO12	SAI1_TX_DATA0				ENET1_TD0							
48	SAI1_TXD1	3V3/1V8	GPIO4_IO13	SAI1_TX_DATA1				ENET1_TD1							
49	SAI1_TXD2	3V3/1V8	GPIO4_IO14	SAI1_TX_DATA2				ENET1_TD2							
50	SAI1_TXD3	3V3/1V8	GPIO4_IO15	SAI1_TX_DATA3				ENET1_TD3							
46	SAI1_TXD4	3V3/1V8	GPIO4_IO16	SAI1_TX_DATA4 SAI6_RX_BCLK SAI6_TX_BCLK				ENET1_TX_CTL							
45	SAI1_TXD5	3V3/1V8	GPIO4_IO17	SAI1_TX_DATA5 SAI6_RX_DATA0 SAI6_TX_DATA0				ENET1_TXC							
52	SAI1_TXFS	3V3/1V8	GPIO4_IO10	SAI1_TX_SYNC				ENET1_RX_CTL							
61	SAI2_MCLK	3.3V	GPIO4_IO27	SAI2_MCLK SAI5_MCLK SAI3_MCLK								CAN2_RX			
63	SAI2_RXC	3.3V	GPIO4_IO22	SAI2_RX_BCLK SAI5_TX_BCLK			UART1_RX					CAN1_TX			
59	SAI2_RXFS	3.3V	GPIO4_IO21	SAI2_RX_SYNC SAI5_TX_SYNC SAI5_TX_DATA1 SAI2_RX_DATA1			UART1_TX								
62	SAI2_TXC	3.3V	GPIO4_IO25	SAI2_TX_BCLK SAI5_TX_DATA2								CAN1_RX			
58	SAI2_TXD0	3.3V	GPIO4_IO26	SAI2_TX_DATA0 SAI5_TX_DATA3								CAN2_TX			
60	SAI2_TXFS	3.3V	GPIO4_IO24	SAI2_TX_SYNC SAI5_TX_DATA1 SAI2_TX_DATA1			UART1_CTS_B		ENET_QOS_1588_EVENT3_OUT						
86	SAI3_MCLK	3.3V	GPIO5_IO2	SAI3_MCLK SAI5_MCLK							PWM4_OUT				SPDIF1_OUT/SPDIF1_IN
65	SAI3_RXC	3.3V	GPIO4_IO29	SAI3_RX_BCLK SAI2_RX_DATA2 SAI5_RX_BCLK			UART2_CTS_B								
64	SAI3_RXD	3.3V	GPIO4_IO30	SAI3_RX_DATA0 SAI2_RX_DATA3 SAI5_RX_DATA0			UART2_RTS_B								
66	SAI3_RXFS	3.3V	GPIO4_IO28	SAI3_RX_SYNC SAI2_RX_DATA1											SPDIF1_IN

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
				SAI5_RX_SYNC SAI3_RX_DATA1											
85	SAI3_TXC	3.3V	GPIO5_IO0	SAI3_TX_BCLK SAI2_TX_DATA2 SAI5_RX_DATA2			UART2_TX								
84	SAI3_TXD	3.3V	GPIO5_IO1	SAI3_TX_DATA0 SAI2_TX_DATA3 SAI5_RX_DATA3											SPDIF1_EXT_CLK
83	SAI3_TXFS	3.3V	GPIO4_IO31	SAI3_TX_SYNC SAI2_TX_DATA1 SAI5_RX_DATA1 SAI3_TX_DATA1			UART2_RX								
57	SAI5_RXC	3V3/1V8	GPIO3_IO20	SAI5_RX_BCLK SAI1_TX_DATA1		I2C6_SDA					PWM3_OUT				
134	SD1_CLK	3V3/1V8	GPIO2_IO0		USDHC1_CLK	I2C5_SCL	UART1_TX	ENET1_MDC							
132	SD1_CMD	3V3/1V8	GPIO2_IO1		USDHC1_CMD	I2C5_SDA	UART1_RX	ENET1_MDIO							
129	SD1_DATA0	3V3/1V8	GPIO2_IO2		USDHC1_DATA0	I2C6_SCL	UART1_RTS_B	ENET1_TD1							
130	SD1_DATA1	3V3/1V8	GPIO2_IO3		USDHC1_DATA1	I2C6_SDA	UART1_CTS_B	ENET1_TD0							
131	SD1_DATA2	3V3/1V8	GPIO2_IO4		USDHC1_DATA2	I2C4_SCL	UART2_TX	ENET1_RD0							
133	SD1_DATA3	3V3/1V8	GPIO2_IO5		USDHC1_DATA3	I2C4_SDA	UART2_RX	ENET1_RD1							
128	SD1_STROBE	3V3/1V8	GPIO2_IO11		USDHC1_STROBE	I2C3_SDA	UART3_CTS_B								
92	SD2_CD_B	SD2	GPIO2_IO12		USDHC2_CD_B										
96	SD2_CLK	SD2	GPIO2_IO13		USDHC2_CLK		UART4_RX			ECSPI2_SCLK					
95	SD2_CMD	SD2	GPIO2_IO14		USDHC2_CMD		UART4_TX			ECSPI2_MOSI					
94	SD2_DATA0	SD2	GPIO2_IO15		USDHC2_DATA0	I2C4_SDA	UART2_RX								
93	SD2_DATA1	SD2	GPIO2_IO16		USDHC2_DATA1	I2C4_SCL	UART2_TX								
97	SD2_DATA2	SD2	GPIO2_IO17		USDHC2_DATA2					ECSPI2_SS0					SPDIF1_OUT
98	SD2_DATA3	SD2	GPIO2_IO18		USDHC2_DATA3					ECSPI2_MISO					SPDIF1_IN
78	SD2_RESET_B	SD2	GPIO2_IO19		USDHC2_RESET_B										
141	SD2_WP	SD2	GPIO2_IO20		USDHC2_WP										
144	SPDIF_EXT_CLK	3.3V	GPIO5_IO5								PWM1_OUT				SPDIF1_EXT_CLK
143	SPDIF_RX	3.3V	GPIO5_IO4			I2C5_SDA					PWM2_OUT	CAN1_RX			SPDIF1_IN
142	SPDIF_TX	3.3V	GPIO5_IO3			I2C5_SCL					PWM3_OUT	CAN1_TX			SPDIF1_OUT

MCM Pad	Pin name	Voltage Domain	GPIO	SAI	USDHC	I2C	UART	ENET1	ENET_QOS	ECSPI	PWM	CAN	QSPI	HDMI	SPDIF
32	UART1_RXD	3.3V	GPIO5_IO22				UART1_RX			ECSPI3_SCLK					
31	UART1_TXD	3.3V	GPIO5_IO23				UART1_TX			ECSPI3_MOSI					
135	UART2_RXD	3.3V	GPIO5_IO24				UART2_RX			ECSPI3_MISO					
148	UART2_TXD	3.3V	GPIO5_IO25				UART2_TX			ECSPI3_SS0					
34	UART3_RXD	3.3V	GPIO5_IO26		USDHC3_RESET_B		UART3_RX UART1_CTS_B					CAN2_TX			
33	UART3_TXD	3.3V	GPIO5_IO27		USDHC3_VSELECT		UART3_TX UART1_RTS_B					CAN2_RX			
35	UART4_RXD	3.3V	GPIO5_IO28			I2C6_SCL	UART4_RX UART2_CTS_B								
36	UART4_TXD	3.3V	GPIO5_IO29			I2C6_SDA	UART4_TX UART2_RTS_B								

5.7 RTC

MCM-iMX8PV2 features an on-board ultra-low-power RX8900CE real time clock (RTC). The RTC is connected to the i.MX8M SoC using I2C2 interface.

The RTC is powered from the 3.3 V rail during normal operation. An external 3V backup source can be connected to VCC_RTC (MCM pad 136) to maintain time when V_SOM is not present.

For more information about the MCM-iMX8PV2 RTC, refer to the RX8900CE datasheet.

5.8 LED

MCM-iMX8PV2 features a single general purpose green LED controlled by GPIO1_IO[12] signal of the i.MX8M Plus. The LED is ON when GPIO1_IO[12] is logic LOW.

6 CARRIER BOARD INTERFACE

The MCM-iMX8PV2 SoM carrier board interface uses 180-pin QFN package. The SoM pinout is detailed in the table below.

6.1 Package Pinout

Table 49 External Pads

Pad #	MCM-iMX8PV2		Pad #	MCM-iMX8PV2
1	MIPI_CSI1_D3_N		91	HDMI_HPD
2	MIPI_CSI1_D3_P		92	SD2_NCD
3	MIPI_CSI1_D2_N		93	SD2_DATA1
4	MIPI_CSI1_D2_P		94	SD2_DATA0
5	MIPI_CSI1_CLK_N		95	SD2_CMD
6	MIPI_CSI1_CLK_P		96	SD2_CLK
7	MIPI_CSI1_D1_N		97	SD2_DATA2
8	MIPI_CSI1_D1_P		98	SD2_DATA3
9	MIPI_CSI1_D0_N		99	ENET_INT
10	MIPI_CSI1_D0_P		100	ENET_NRST
11	MIPI_CSI2_D0_N		101	HDMI_TXCN
12	MIPI_CSI2_D0_P		102	HDMI_TXCP
13	MIPI_CSI2_D1_N		103	ECSPI1_SS0
14	MIPI_CSI2_D1_P		104	HDMI_TX0N
15	MIPI_CSI2_CLK_N		105	HDMI_TX0P
16	MIPI_CSI2_CLK_P		106	ECSPI1_MISO
17	MIPI_CSI2_D2_N		107	HDMI_TX1N
18	MIPI_CSI2_D2_P		108	HDMI_TX1P
19	MIPI_CSI2_D3_N		109	ECSPI1_MOSI
20	MIPI_CSI2_D3_P		110	HDMI_TX2N
21	LVDS0_D3_N		111	HDMI_TX2P
22	LVDS0_D3_P		112	ECSPI1_SCLK
23	LVDS0_D2_N		113	LVDS_DSI_DN3
24	LVDS0_D2_P		114	LVDS_DSI_DP3
25	LVDS0_D0_N		115	LVDS_DSI_DN2
26	LVDS0_D0_P		116	LVDS_DSI_DP2
27	LVDS0_D1_N		117	LVDS_DSI_CKN
28	LVDS0_D1_P		118	LVDS_DSI_CKP
29	LVDS0_CLK_N		119	LVDS_DSI_DN1
30	LVDS0_CLK_P		120	LVDS_DSI_DP1
31	UART1_TXD		121	LVDS_DSI_DN0
32	UART1_RXD		122	LVDS_DSI_DP0
33	UART3_TXD		123	V_SOM
34	UART3_RXD		124	V_SOM
35	UART4_RXD		125	V_SOM
36	UART4_TXD		126	RESERVED
37	ENET1_MDC/SAI1_RXD2		127	RESERVED
38	ENET1_MDIO/SAI1_RXD3		128	SD1_STROBE

Pad #	MCM-iMX8PV2		Pad #	MCM-iMX8PV2
39	I2C3_SCL		129	SD1_DATA0
40	I2C3_SDA		130	SD1_DATA1
41	GPIO5_21/I2C4_SDA		131	SD1_DATA2
42	PCIE_CLKREQ_B/I2C4_SCL		132	SD1_CMD
43	EARC_P_UTIL		133	SD1_DATA3
44	EARC_N_HPD		134	SD1_CLK
45	ENET1_TXC/SAI1_TXD5		135	UART2_RXD
46	ENET1_TX_CTL/SAI1_TXD4		136	VCC_RTC
47	ENET1_TD0/SAI1_TXD0		137	HDMI_DDC_SDA
48	ENET1_TD1/SAI1_TXD1		138	HDMI_DDC_SCL
49	ENET1_TD2/SAI1_TXD2		139	HDMI_CEC
50	ENET1_TD3/SAI1_TXD3		140	PWRBTN
51	ENET1_RXC/SAI1_TXC		141	USB1_TYPEC_EN_B/SD2_WP
52	ENET1_RX_CTL/SAI1_TXFS		142	SPDIF_TX
53	ENET1_RD0/SAI1_RXD4		143	SPDIF_RX
54	ENET1_RD1/SAI1_RXD5		144	SPDIF_EXT_CLK
55	ENET1_RD2/SAI1_RXD6		145	JTAG_MOD
56	ENET1_RD3/SAI1_RXD7		146	PMIC_ON_REQ
57	I2C6_SDA/SAI5_RXC		147	PMIC_STBY_REQ
58	CAN2_TX/SAI2_TXD0		148	UART2_TXD
59	ENET1_INT		149	USB1_TX_P
60	ENET1_NRST		150	USB1_TX_N
61	CAN2_RX/SAI2_MCLK		151	JTAG_TDI
62	CAN1_RX/SAI2_TXC		152	JTAG_TCK
63	CAN1_TX/SAI2_RXC		153	JTAG_TDO
64	SAI3_RXD/UART2_RTS		154	JTAG_TMS
65	SAI3_RXC/UART2_CTS		155	PCIE_TX_P
66	SAI3_RXFS		156	PCIE_TX_N
67	ENET_TXC		157	PCIE_RX_P
68	ENET_TX_CTL		158	PCIE_RX_N
69	ENET_TD0		159	PCIE_REF_CLKN
70	ENET_VIO		160	PCIE_REF_CLKP
71	ENET_TD1		161	USB2_TX_N
72	ENET_TD2		162	USB2_TX_P
73	ENET_TD3		163	USB2_DN
74	ENET_RXC		164	USB2_DP
75	ENET_RX_CTL		165	GPIO1_00
76	ENET_RD0		166	ALT_BOOT
77	ENET_RD1		167	GPIO1_10
78	SD2_RESET_B		168	SYS_RST_PMIC
79	ENET_RD2		169	USB2_RX_P
80	ENET_RD3		170	USB2_RX_N
81	ENET_MDIO		171	USB1_RX_P
82	ENET_MDC		172	USB1_RX_N
83	SAI3_TXFS		173	USB1_DP

Pad #	MCM-iMX8PV2		Pad #	MCM-iMX8PV2
84	SAI3_TXD		174	USB1_DN
85	SAI3_TXC		175	GPIO1_11
86	SAI3_MCLK		176	NC
87	ECSPI2_SCLK		177	NC
88	ECSPI2_SS0		178	QSPI_BOOT_EN_3P3
89	ECSPI2_MOSI		179	USB1_VBUS
90	ECSPI2_MISO		180	USB2_VBUS

Table 50 Ground Pads

Pad #	Pad Functions	Ref.		Pad #	Pad Functions	Ref.
G1	GND	5.1		G36	GND	5.1
G2				G37		
G3				G38		
G4				G39		
G5				G40		
G6				G41		
G7				G42		
G8				G43		
G9				G44		
G10				G45		
G11				G46		
G12				G47		
G13				G48		
G14				G49		
G15				G50		
G16				G51		
G17				G52		
G18				G53		
G19				G54		
G20				G55		
G21				G56		
G22				G57		
G23				G58		
G24				G59		
G25				G60		
G26				G61		
G27				G62		
G28				G63		
G29				G64		
G30				G65		
G31				G66		
G32				G67		
G33				G68		
G34				G69		
G35				G70		

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 51 Absolute Maximum ratings

Parameter	Min	Max	Unit
Main power supply voltage (V_SOM)	-0.3	5.5	V
Voltage on any non-power supply pin	-0.5	3.6	V
Backup battery supply voltage (VCC_RTC)	-0.3	3.8	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 52 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage (V_SOM)	3.45	3.7	5.5	V
Backup battery supply voltage (VCC_RTC)	1.5	3.0	3.6	V

7.3 ESD Performance

Table 53 ESD Performance

Interface	ESD Performance
i.MX8M Plus pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)

8 MECHANICAL SPECIFICATIONS

8.1 Mechanical Drawings

3D model and mechanical drawings in DXF format are available at

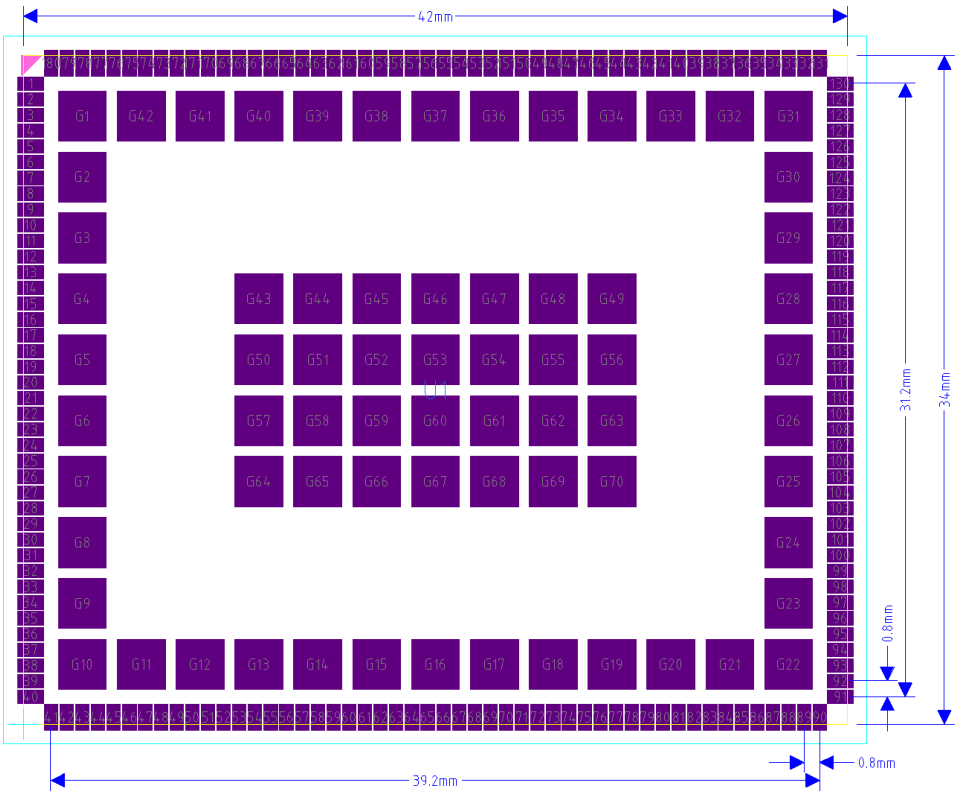
https://www.compulab.com/products/computer-on-modules/mcm-imx8pv2-nxp-i-mx-8m-plus-som-smd-system-on-module/#devres

8.2 Recommended Footprint

MCM-iMX8PV2 footprint in DXF and HKP formats is available at

https://www.compulab.com/products/computer-on-modules/mcm-imx8pv2-nxp-i-mx-8m-plus-som-smd-system-on-module/#devres

Figure 3 MCM-iMX8PV2 footprint



8.3 Heat Spreader and Cooling Solutions

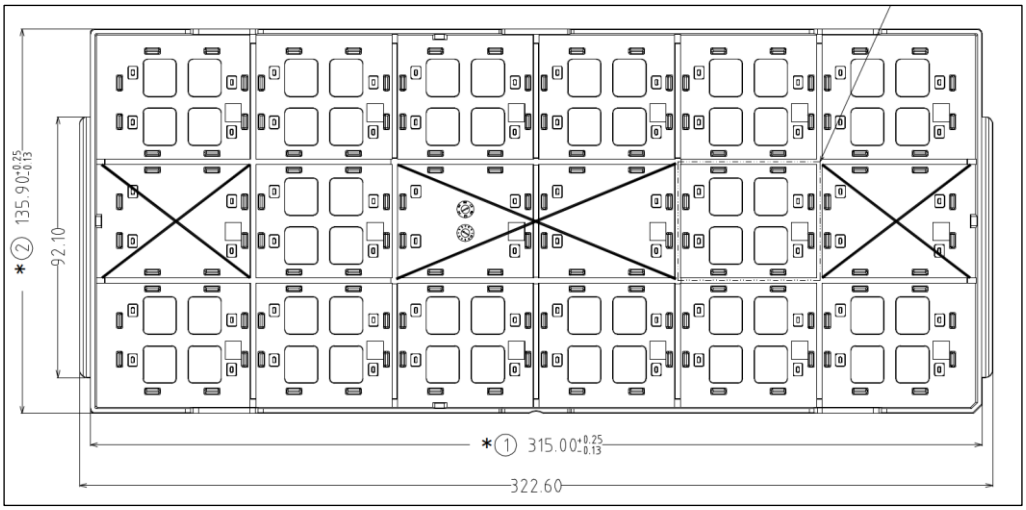
Compulab provides MCM-iMX8PV2 with an optional heat-spreader assembly. The MCM-iMX8PV2 heat-spreader has been designed to act as a thermal interface and should be used in conjunction with a heat-sink or an external cooling solution. A cooling solution must be provided to ensure that under worst-case conditions the temperature at any spot on the heat-spreader surface is maintained according to the MCM-iMX8PV2 temperature specifications. Various thermal management solutions can be used with the heat-spreader, including active and passive approaches.

9 ASSEMBLY AND STORAGE GUIDELINES

9.1 Packaging

MCM-iMX8PV2 modules are supplied in JEDEC-compliant trays. Each tray can hold 18 MCM modules.

Figure 4 MCM-iMX8PV2 tray



9.2 Storage Conditions

MCM-iMX8PV2 modules are supplied in moisture barrier bags. Before use, these must be stored at a temperature of less than 30°C, with humidity under 85% RH.

The calculated shelf-life for the dry-packed product is 12 months from the date the bag is sealed.

9.3 Baking Requirements

MCM-iMX8PV2 modules are rated MSL3. Storage and assembly processes must comply with IPC/JEDEC J-STD-033C. MCM-iMX8PV2 modules have a total thickness of < 3mm and are comparable to a die package. As such, baking instructions must comply with Table 4-1 of J-STD-033C.

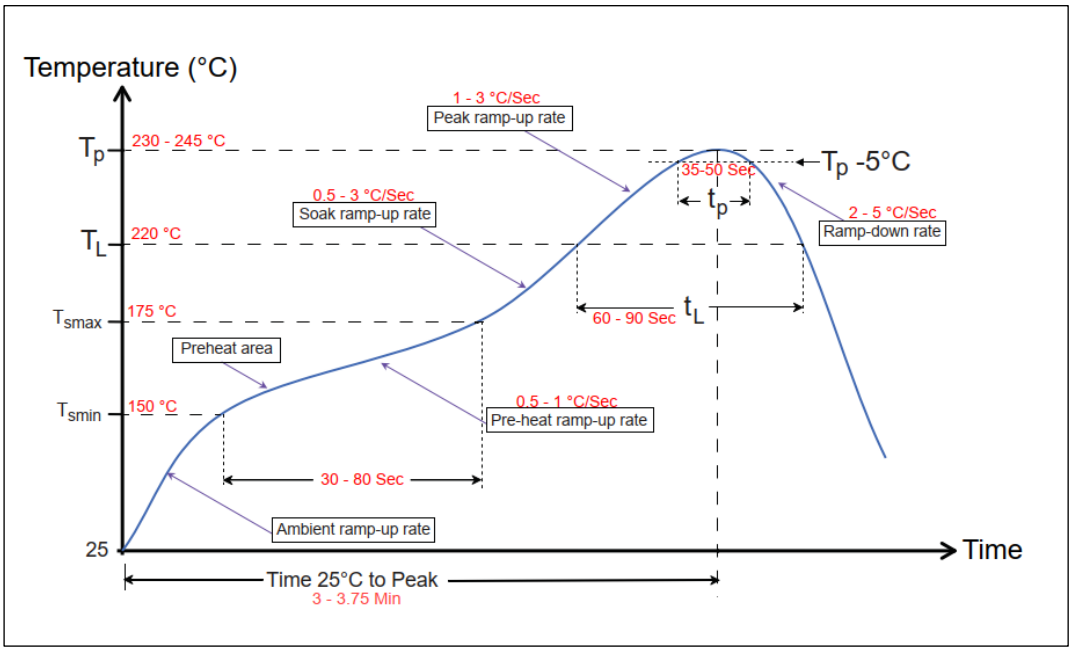
Table 54 Baking requirements - JEDEC table extract

Package Body	MSL Level	Bake @ 125C		Bake @ 90°C ≤ 5% RH		Bake @ 40°C ≤ 5% RH	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness > 2.0 mm ≤ 4.5 mm	3	48 hours	48 hours	10 days	8 days	79 days	67 days

9.4 Reflow Profile

The following profile is provided as an initial reference. The exact reflow profile should be created in accordance with the carrier-board physical characteristics and solder paste type.

Figure 5 Reference reflow profile



10 APPLICATION NOTES

10.1 Carrier Board Design Guidelines

- Ensure that all V_SOM and GND power pins are connected.
- Major power rails - V_SOM and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality because the planes provide a current return path for all interface signals.
- It is recommended to put several 10/100uF capacitors between V_SOM and GND near the SOM.
- Except for a power connection, no other connection is mandatory for MCM-iMX8PV2 operation. All power-up circuitry and all required pullups/pulldowns are available onboard MCM-iMX8PV2.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCIe, Ethernet, USB and similar high speed signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- The following interfaces should meet the differential impedance requirements with manufacturer tolerance of 10%:
  - USB2.0: DP/DM signals require 90 ohm differential impedance.
  - All single-ended signals require 50 ohm impedance.
  - PCIe TX/RX data pairs and PCIe clocks require 85 ohm differential impedance.
  - MIPI-CSI and MIPI-DSI signals require 100 ohm differential impedance.
- Refer to the SBC-MCM8PV2 carrier board reference design schematics.
- It is recommended to send the schematics of the custom carrier board to Compulab support team for review.

10.2 Carrier Board Troubleshooting

- Using an oscilloscope, check the voltage levels and quality of the V_SOM power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches.
- Using an oscilloscope, verify that the GND pins are indeed at zero voltage level and that there is no ground bouncing.
- Create a "minimum system" - only power, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
  - Devices improperly driving the local bus
  - External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
  - Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between SOM pads. Even if the signals are not used on the carrier board, shorting them can disable the module operation. An initial

check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray. Note that solder shorts are the most probable factor to prevent a module from booting.

- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from MCM-iMX8PV2, or even damage the module hardware permanently.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.